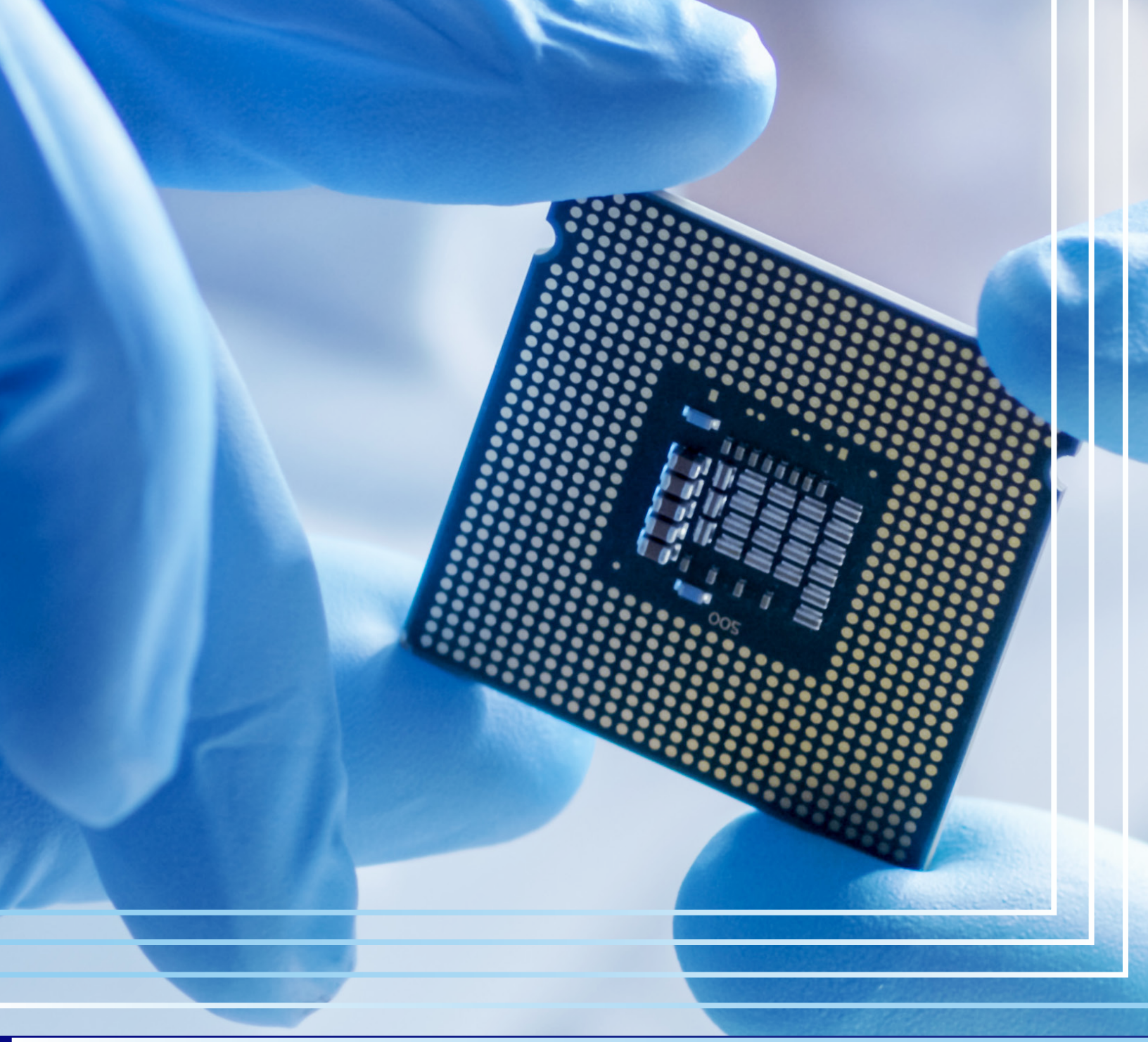

American Semiconductor Research: **Leadership Through Innovation**

SIA SEMICONDUCTOR INDUSTRY ASSOCIATION

Acknowledgements

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About the Semiconductor Industry Association (SIA)

The Semiconductor Industry Association (SIA) is the voice of the semiconductor industry, one of America's top export industries and a key driver of America's economic strength, national security, and global competitiveness. Semiconductors – the tiny chips that enable modern technologies – power incredible products and services that have transformed our lives and our economy. The semiconductor industry directly employs over a quarter of a million workers in the United States, and U.S. semiconductor company sales totaled $258 billion in 2021. SIA represents 99% of the U.S. semiconductor industry by revenue and nearly two-thirds of non-U.S. chip firms. Through this coalition, SIA seeks to strengthen leadership of semiconductor manufacturing, design, and research by working with Congress, the Administration, and key industry stakeholders around the world to encourage policies that fuel innovation, propel business, and drive international competition. Learn more at www.semiconductors.org.

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Executive Summary

From powering data centers to controlling the Mars rover Perseverance, the world demands more of its semiconductors now than it did just a few years ago. As in the past, meeting these demands – and enabling technological leadership across the U.S. economy – will require new innovations, made possible by investments in semiconductor research and development (R&D). To be commercially useful, an innovation must traverse five phases of R&D before scaling to volume production. Each successive phase is increasingly challenging: a large portfolio of initial bets is required for 1-2 innovations to reach volume production.

R&D is a critical part of a virtuous cycle of innovation that supports U.S. technology leadership. Innovations yield superior technologies and products that, when used in commercial production, provide the funds needed to make massive investments in future R&D. To develop these innovations, the U.S. semiconductor industry invested $50 billion in R&D in 2021 alone. With the passage of the 2022 CHIPS and Science act, the federal government is poised to make its single largest investment in semiconductor R&D ever. A national strategy for semiconductor R&D should target this investment toward critical gaps in the U.S. R&D ecosystem to revitalize the innovation pipeline, to align R&D with commercial priorities, and to strengthen U.S. technological competitiveness.

While the U.S. has world-class national labs, universities, and companies needed for innovations, its semiconductor R&D ecosystem faces challenges in directing investments, resourcing, facilitating collaboration, and bringing innovations to market (i.e., lab to fab gaps). If unaddressed, these challenges will limit the ecosystem's effectiveness. Meanwhile, other regions are taking steps to mitigate these challenges and to improve the effectiveness of their own R&D ecosystems through initiatives like the EU's own Chips Act and South Korea's "K-Semiconductor Belt" initiative.

The funding of the 2022 CHIPS and Science Act will amplify the scope and impact of existing U.S. semiconductor R&D organizations by establishing two new entities, the National Semiconductor Technology Center (NSTC) and the National Advanced Packaging Manufacturing Program (NAPMP).

NSTC and NAPMP provide a critical framework, focus and funding for the U.S. R&D ecosystem, ensuring technology innovations that pave the way for sustaining long-term U.S. semiconductor leadership. The NSTC and NAPMP complement the strong CHIPS Act provisions designed to increase domestic semiconductor capacity.

The NSTC and NAPMP should be closely aligned with one another, and should thoroughly include industry voices in order to most effectively promote U.S. technological competitiveness and encourage commercial buy-in. Based on our extensive consultations with industry leaders, the NSTC and NAPMP should partner widely across the semiconductor industry and bolster the U.S. R&D ecosystem's capabilities through investments in five key areas.

Five key investment areas for NSTC and NAPMP

1 Transitioning and Scaling Pathfinding Research

The NSTC and NAPMP should serve to bridge the gap between early stage R&D and at-scale production. Both should strengthen the R&D ecosystem's ability to conduct R&D and commercialize technologies that are 5 to 15 years from production, technologies for which regional leadership has yet to be determined. The NSTC and NAPMP can become hubs for aligning R&D efforts, both for industry and other agencies, allowing industry to participate in programs where it has interests, and enabling agencies to focus their own funds on their respective missions.

2&3 Research Infrastructure and Development Infrastructure

The NSTC and NAPMP should play an active role in expanding, upgrading, and providing access to institutions' technology development capabilities where they align with R&D priorities. The two initiatives must neither spread funding evenly nor concentrate investments in a single technology or location. Rather, both must balance the benefits of a highly distributed network against the benefits of scale, based on technology needs. Specifically, it is critical that the NSTC and NAPMP use existing infrastructure where possible to leverage CHIPS funding and enable faster learnings by benefiting from available resources. This is especially important for piloting and prototyping to accelerate and broaden commercialization efforts. The primary support that the NSTC and NAPMP will provide for research efforts is the establishment of transition path for promising technologies through prototyping and scale-up.

4 Collaborative Development

The NSTC and NAPMP should support full-stack innovation by convening companies to solve complex technological problems that benefit from collaboration across the full computing stack and accelerate the development of technologies, tools, and methodologies.[1] For example, creating next-generation data centers requires bringing together expertise in advanced materials, new computing architectures, packaging, software, and more. In particular, the NAPMP can convene technical experts to provide input to organizations like Institute of Electrical and Electronics Engineers (IEEE) and Joint Electron Device Engineering Council (JEDEC) when developing, for example, integration standards for heterogenous integration, chiplets, and other components of secure technologies.

5 Workforce

The NSTC and NAPMP should promote a range of programs that expand the size and skills of the U.S. semiconductor R&D pipeline and workforce to defend and strengthen the U.S. R&D ecosystem and the economic competitiveness it underpins. Without these efforts, the inadequate supply of highly skilled R&D workers – those in semiconductor design, manufacturing, and the other activities of the value chain - threatens to limit the pace of innovation.[2]

1. The 2030 Decadal Plan for Semiconductors identifies 8 high level components of the compute stack: applications, software, algorithms, architectures, circuits, devices, structures, and materials.
2. See BCGxSIA's *Strengthening the Global Semiconductor Value Chain* for additional information on the seven differentiated activities of the semiconductor value chain

Semiconductor R&D is the process by which innovative ideas are transformed into technological advancements and capability to enable the creation of more, and more advanced, semiconductors

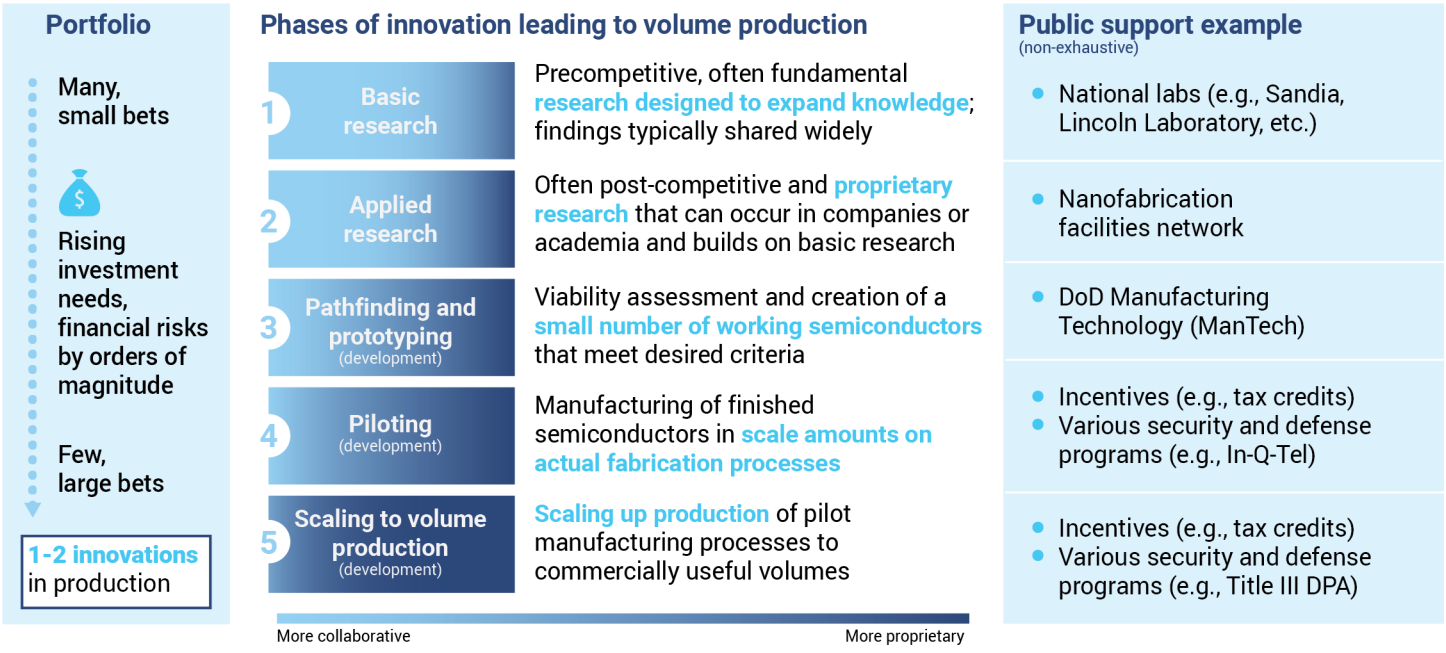
Semiconductors, or chips, are pervasive in, and increasingly critical to, the functioning of the modern world. From powering data centers analyzing historically unprecedented quantities of data, to controlling the Mars rover Perseverance in challenging environments, the world demands more from its semiconductors today than it did just a few years ago. Meeting these demands – and enabling innovation at semiconductor-dependent companies across the U.S. economy - will require sustained investments in semiconductor research and development (R&D).

R&D has been a critical element of the semiconductor industry's success since its inception. While previous SIA reports have focused on the activities that occur during semiconductor design or during semiconductor manufacturing, this report will discuss the role of semiconductor R&D and its importance in technological competitiveness.

In general, an innovation must traverse five phases of R&D to be commercially useful. These phases differ in important ways, including in the number of potential innovations in a portfolio and in the levels of ecosystem collaboration, investment needs, and technical challenges. (see Exhibit 1)

As a potential innovation goes from new idea to adoption at production scale, the level of collaboration across organizations in the ecosystem changes. Basic research

Exhibit 1:
Innovations traverse 5 phases before volume production



that expands the base of knowledge is considered "pre-competitive." Basic research typically involves collaboration among companies, governments, and other organizations in the R&D ecosystem with minimal supply chain or competition-related considerations. As a potential innovation draws closer to use in volume production, supply chain and competition-related considerations grow, and more R&D takes place within organizations rather than among them.

Not all potential innovations reach volume production. A portfolio of many potential innovations is required for a handful of innovations to successfully reach volume production. Overall investment costs and technical challenges emerge through the phases, even as the number of remaining viable potential innovations declines. Given investment needs, technical challenges, and ecosystem infrastructure limitations, many potential innovations often fail to traverse "the valley of death" of prototyping and piloting. Even when they do progress, the cost and talent constraints associated with scaling can be daunting – financial risks can be orders of magnitude larger. (see Exhibit 2)

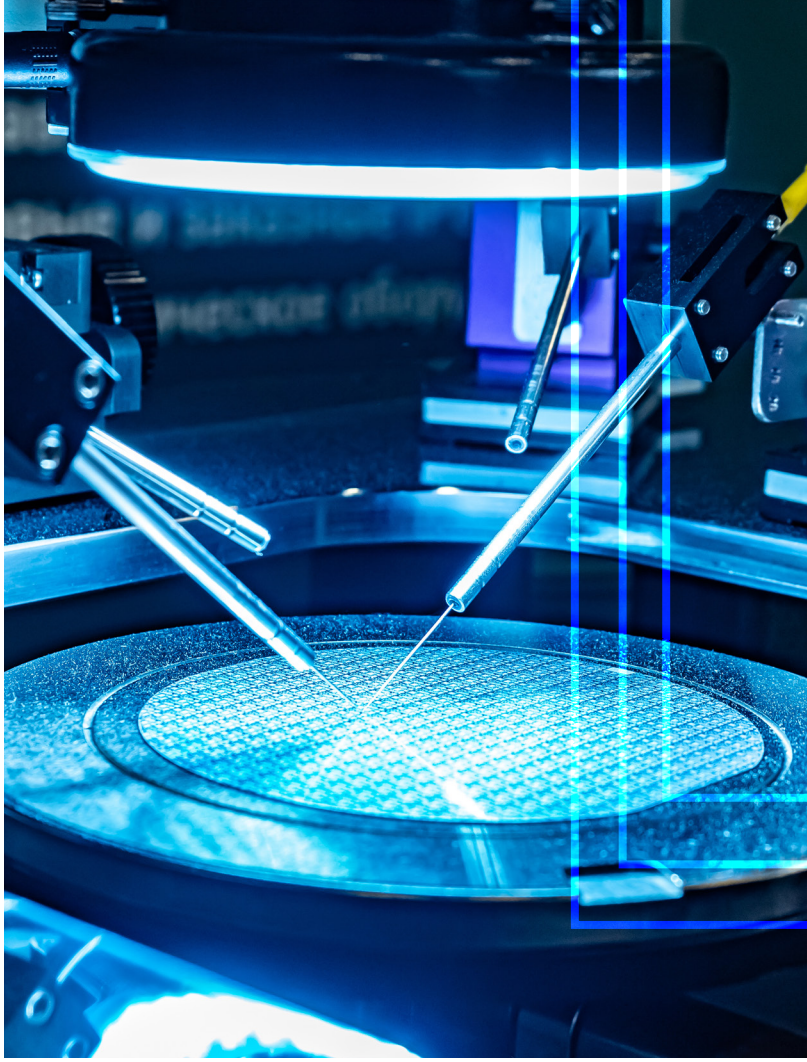
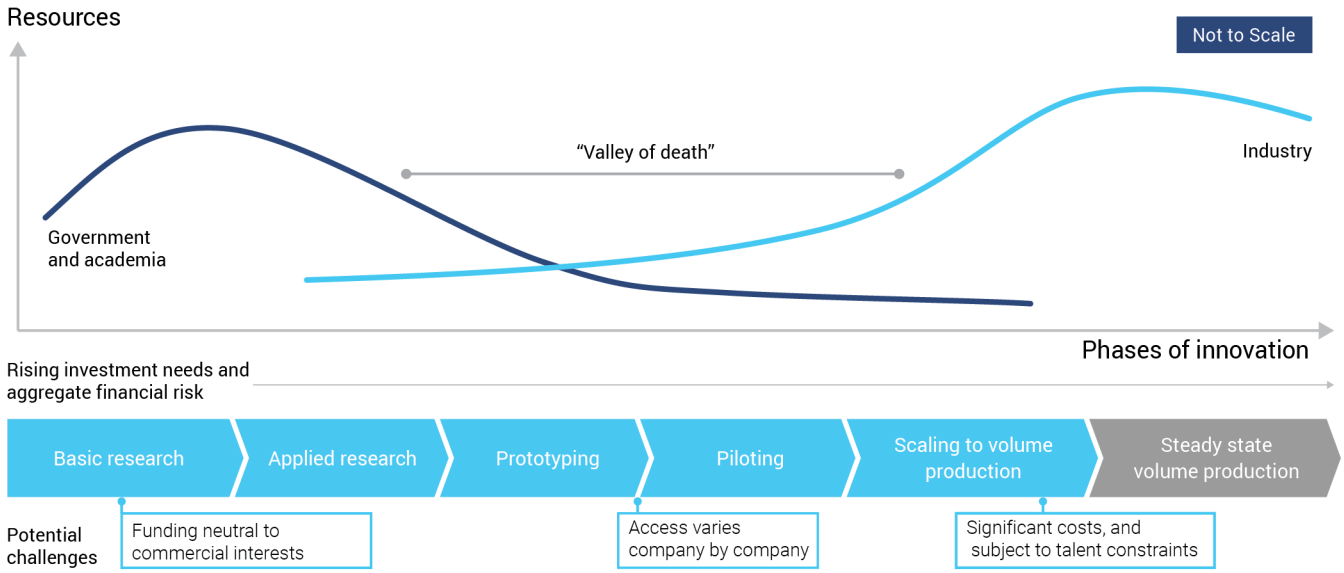


Exhibit 2:
Ecosystem gaps in phases of innovation



Note: Terminology adapted from source for clarity and consistency
Source: Government Accountability Office Nanomanufacturing (May 2014)

Semiconductor R&D is important and is part of a virtuous cycle of innovation that supports U.S. technological leadership

The ability of innovations to successfully traverse the R&D phases is critical. When incorporated at volume production, innovations yield superior technologies and products. Superior technologies and products in turn bolster U.S. market share and profit margins, and provide the funds needed to make massive investments in future R&D. (see Exhibit 3)

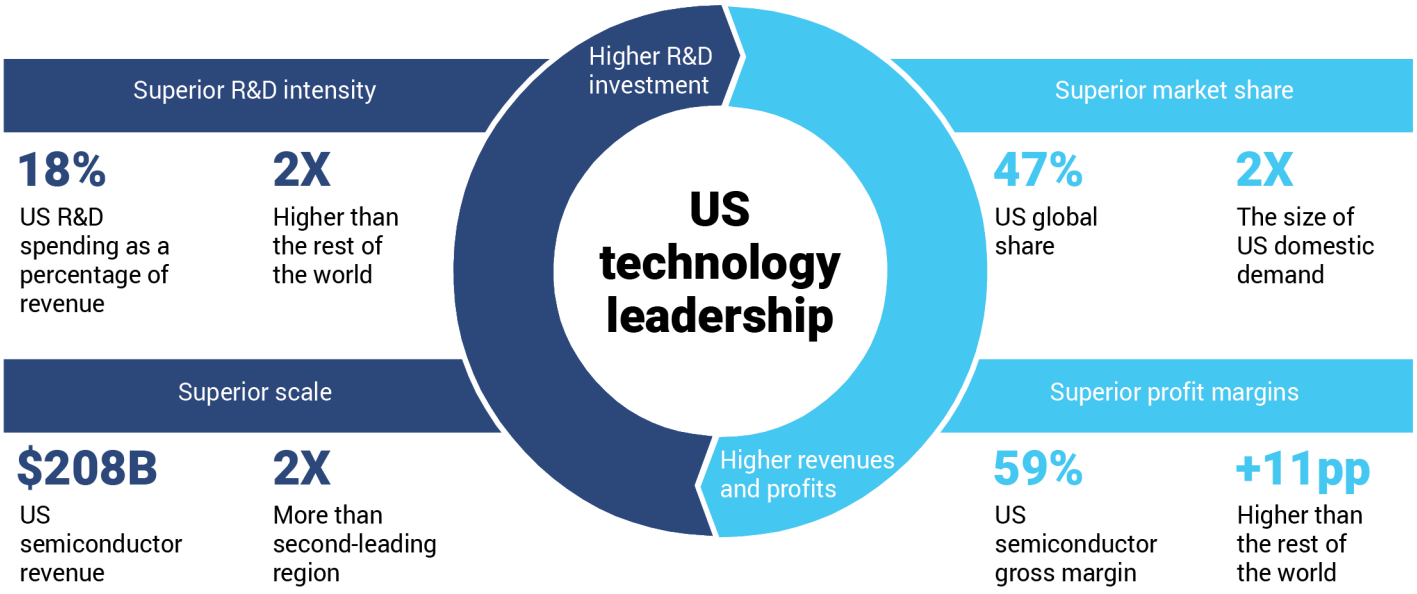
The virtuous cycle of innovation represents an opportunity and does not happen automatically. It depends on a continual pipeline of potential innovations traversing the five phases. Historically, the U.S. R&D ecosystem has supported innovations throughout this process.

For example, the U.S. military needed semiconductor materials in the 1980s with performance beyond the limits of silicon. The Office of Naval Research (ONR) and Defense Advanced Research Projects Agency (DARPA) identified and facilitated academia-industry collaboration to advance compound semiconductor materials through the phases of innovation and tailor them to industrial uses. The resulting materials, like gallium nitride, are used today in civilian and military applications and are an area of strength for U.S. industry. A wide range of companies now invest in compound semiconductor materials for use in a range of applications from electric vehicles to mobile networks to defense.

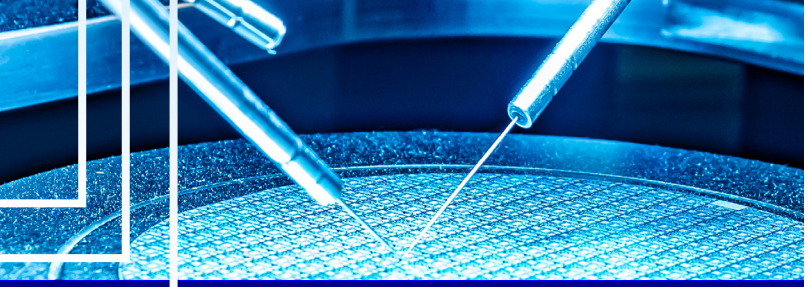
R&D is a critical competitive battleground. It is vital to long term U.S. technology leadership that the most important semiconductor innovations can be commercialized in the U.S. R&D pipelines that lack support for commercialization of innovations can wind up accelerating efforts of other competing countries and regions including adversaries.

The virtuous cycle of innovation presents a valuable opportunity, but its fulfillment is not certain. Fortunately, the coming years contain opportunities to strengthen

Exhibit 3:
R&D is part of a virtuous cycle of innovation that supports technology leadership in the US



Note: All numbers are for 2020. Revenue weighted averages of reported financial data from top companies in each region. pp = percentage points
Source: BCG analysis, using data from SIA, company reports, and BCG ValueScience Center



Spotlight: Extreme Ultraviolet Lithography

As an example of an innovation that began as R&D in the U.S. but was commercialized overseas, consider extreme ultraviolet (EUV) lithography. Lithography is a process in semiconductor manufacturing that uses light to produce extremely small patterns on materials like silicon wafers. EUV lithography is a highly advanced version of this process used for many of the most advanced chips, like those found in leading smartphones. U.S. public investment played an early and sustained role in supporting EUV lithography, while parallel investments were made in Korea and Japan.

New applications drove the need for continued transistor scaling in the late 1980s. While EUV's potential was known, many in the industry considered EUV infeasible given technical and other challenges. Nevertheless, DARPA funded the Advanced Lithography Program which conducted early research into EUV reflectometry. SEMATECH, a not-for-profit consortium that performed R&D to advance chip manufacturing, partnered across industry and academia for over 15 years to access and build out infrastructure and expertise that industry alone considered too risky. A collection of companies, including ASML, Intel, Samsung, and Taiwan Semiconductor Manufacturing Company (TSMC), invested between $10 – 17 billion to mature EUV into a commercially viable technology. ASML today is the only company with the ability to implement EUV lithography technologies in a commercially viable way. As of July 2022, only TSMC, Samsung, and Intel are using EUV to develop semiconductor process technology.

the U.S. R&D ecosystem and extend the virtuous cycle of innovation – and U.S. technological leadership - through the next generation of semiconductor technologies. Alongside the appropriation of $39 billion for semiconductor fabrication incentives, the 2022 CHIPS and Science Act provides $13 billion in funding for semiconductor R&D and the transition of technology from labs to the marketplace. This $13 billion is the focus of this report. With the enactment of the CHIPS and Science Act, Congress and the administration recognized the importance of semiconductor R&D to the United States.

Innovation along existing and new dimensions will be required for the next generation of advancements as the strategies for improving computation technologies change. Investment needs in existing dimensions like transistor scaling are rising. Alongside these, opportunities in areas like advanced packaging and heterogeneous integration are emerging. Innovations across multiple disciplines are required to create the chips that the U.S. economy will demand in the coming years.

The U.S. semiconductor industry is investing ever-increasing amounts to meet these needs, investing $50 billion in R&D in 2021 alone. Despite this, the U.S. R&D ecosystem today faces challenges in delivering the innovations needed. Important R&D enablers and infrastructure are lacking or limited in the U.S., and mechanisms are limited for collaborative development across the computing stack.

Semiconductors have driven transformative advances in every modern technology. Chips also will underpin advances in the "must-win" technologies of the future - including artificial intelligence (AI), quantum computing, and advanced wireless networks – making continued U.S. leadership in semiconductors critical to our future.[3] A national strategy for semiconductor R&D, focused on revitalizing the pipeline of innovation and aligning it with commercial priorities, will address critical gaps in the U.S. R&D ecosystem and strengthen U.S. technological competitiveness and leadership through the following decades.

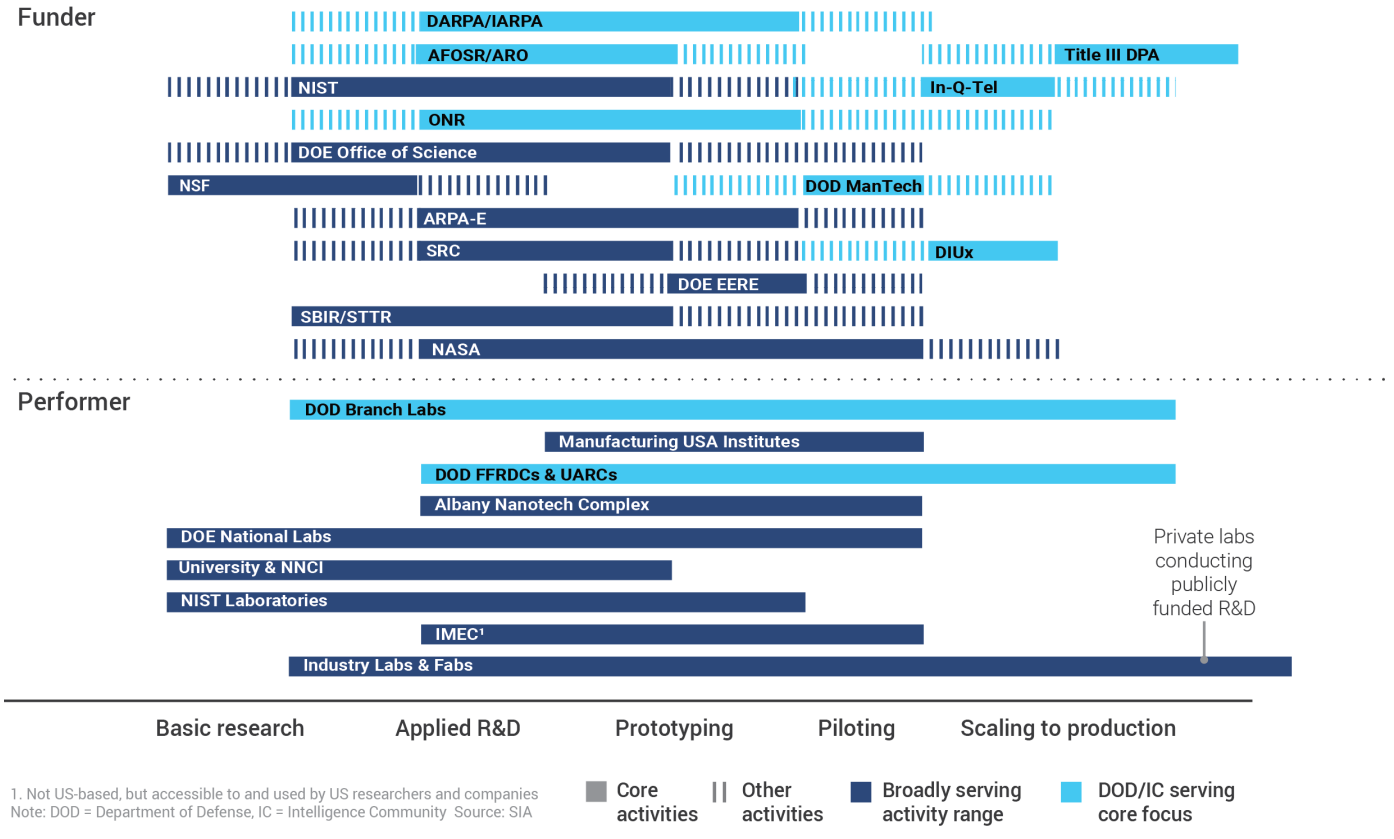
3. Semiconductors were recognized as "must-win" technologies by the U.S. Innovation and Competition Act, the National Security Commission on Artificial Intelligence, and the White House *Building Resilient Supply Chains, Revitalizing American Manufacturing, and Fostering Broad-based Growth* report.

In the U.S. R&D ecosystem, government, academia, and private industry all play a significant role in funding and performing the R&D that drives commercially useful innovation.

The semiconductor R&D ecosystem is currently composed of a broad range of institutions, including government agencies, academic institutions, private industry, and partnerships. (see Exhibit 4)

Each plays a distinct and significant role in facilitating innovation across the phases of innovation. These institutions include both funders and performers of R&D. Institutions that fund R&D may also perform R&D, and institutions that perform R&D may receive funding from a range of funders.

Exhibit 4:
Public and industry consortia R&D in the US semiconductor ecosystem



1. Not US-based, but accessible to and used by US researchers and companies
Note: DOD = Department of Defense, IC = Intelligence Community Source: SIA

Core activities | Other activities | Broadly serving activity range | DOD/IC serving core focus

Government

Government agencies (e.g., Department of Defense, Department of Energy, National Science Foundation, National Institute of Standards and Technology) are critical **funders** of R&D in the ecosystem. Such government agencies provide essential support for research that is too distant, too uncertain, or too difficult for a single firm to turn into a competitive advantage.[4]

Government-related entities (e.g., the Air Force Research Laboratory, the National Institute of Standards and Technology Material Measurement Laboratory) also perform research. Further, government also plays a significant role in shaping the infrastructure (e.g., funding university nanofabs), enablers (e.g., investing in basic research), and policies (e.g., setting permitting rules for facilities) of the R&D ecosystem. Taken together, these factors catalyze private industry investment and R&D into potential semiconductor innovations.

Academia

Academia is a key **performer** of R&D: academia performs basic research, performs applied research, and develops prototypes.[5] It also plays a significant role in training the semiconductor workforce. Academia plays a significant role in expanding the base of knowledge and disseminating findings that can be used by established companies and startups in industry.

Private industry

Private industry is both a **funder** and **performer** of R&D.[6] A wide range of companies now fund, prototype, scale, and commercialize semiconductors and related services. There are several major types of companies that conduct semiconductor R&D:

- **Integrated device manufacturers** (IDMs) are vertically integrated companies that perform design and fabrication. These companies combine the resources and expertise to bridge gaps between basic research and production, but there are only a few of these companies in the U.S. (e.g., Intel, Micron, Samsung, and Texas Instruments).[7]

- **Fabless design companies** (e.g., Qualcomm, AMD, NVIDIA, and Apple) focus on semiconductor design, the highest value-adding portion of semiconductor value chain. These companies represent approximately 55% of the private sector R&D[8] and partner with other companies for semiconductor fabrication.[9]

- **Foundries** meet the fabrication needs of both IDMs and fabless design firms. Foundries often focus exclusively on fabricating chips designed by others (e.g., TSMC, Samsung Foundry, Intel Foundry Services, and GlobalFoundries). Foundries invest in R&D related to manufacturing technologies and are responsible for a large share of advanced manufacturing.[10]

- **Semiconductor equipment and materials companies** (e.g., Applied Materials, ASML, EMD Electronics, Lam Research, Tokyo Electron) develop advanced process and inspection systems required to produce chips. Equipment and materials companies invest in R&D for new process technologies, materials and manufacturing methods that enable the semiconductor technology roadmap, and contribute significant amount to R&D investment in the semiconductor industry on par with several U.S. chip manufacturers.

Partnerships and other industry consortium

In addition, public-private partnerships (PPPs) encompass a range of organizations operated by private sector stakeholders that are publicly funded. Examples of PPPs include the federally funded research and development centers (FFRDCs) and SEMATECH.[11] PPPs can be **funders** or **performers** of R&D. Examples of PPPs include:

- **Federally Funded Research and Development Centers** (FFRDCs), which include the national labs, are public-private partnerships operated by academic institutions or private companies that are funded by and perform research for the federal government.

- **Industry consortia** of semiconductor companies and their suppliers created for various purposes. For example, the Semiconductor Research Corporation (SRC) is a consortium of semiconductor companies as well as government agencies that funds high-technology research at more than a hundred universities. Its programs span a range of applications from artificial intelligence to automotive.

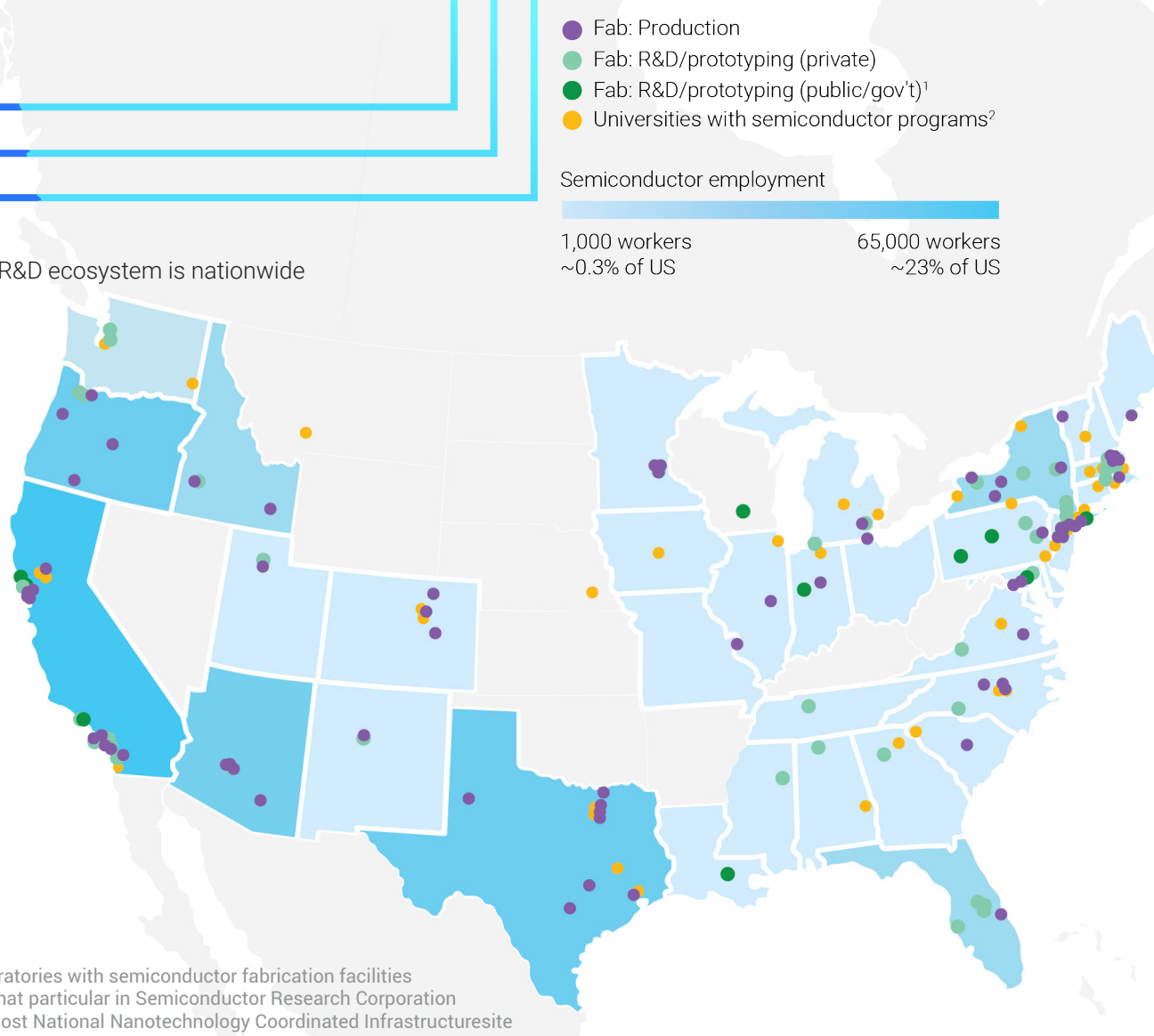
4. National Research Council. 1999. *Funding a Revolution: Government Support for Computing Research*. Washington, DC: The National Academies Press
5. National Science Board, NSF. 2020. Academic Research and Development. Science and Engineering Indicators 2020. NSB-2020-2. Alexandria, VA.
6. Varadarajan et al. "Strengthening The Global Semiconductor Supply Chain In An Uncertain Era", (BCG and SIA, April 2021).
7. MITRE Engenuity. 2021. American Innovation, American Growth: A Vision for the National Semiconductor Technology Center.
8. id. "Strengthening The Global Semiconductor Supply Chain In An Uncertain Era"
9. id. "Strengthening The Global Semiconductor Supply Chain In An Uncertain Era"
10. Foundries are responsible for a large share of advanced manufacturing and control 78% global market for 14 nanometer or below technology nodes, 100% for 5 nanometer technology nodes
11. SEMATECH received public funding from 1988-1996, then it operated without futher public sector funding

- **Non-academic research organizations** work with the U.S. R&D ecosystem on basic research. (See appendix: Non-academic research organizations)

R&D organizations across the U.S.

The organizations discussed above are major players in the U.S. R&D ecosystem. While clusters do exist in areas like Silicon Valley or North Texas, important stakeholders in the U.S. semiconductor R&D ecosystem are located across the country. (see Exhibit 5) Fabs focused on R&D or piloting can be found in at least 29 states, with additional R&D expertise at production fabs and universities with semiconductor programs.

Exhibit 5:
U.S. semiconductor R&D ecosystem is nationwide



1. Includes national laboratories with semiconductor fabrication facilities
2. Includes universities that particular in Semiconductor Research Corporation (SRC) programs or that host National Nanotechnology Coordinated Infrastructuresite
Note: No major semiconductor-related fabs, universities, or employment in Alaska
Source: SIA; BCG analysis

The U.S. R&D ecosystem faces several challenges, including those related to piloting and prototyping, that hinder the effectiveness of the ecosystem.

A well-functioning R&D ecosystem supports innovation by providing direction, resourcing, and collaboration to R&D efforts. The U.S. retains a strong portfolio of national labs, universities, and companies, but its R&D ecosystem currently faces challenges in delivering needed innovations. Examples of these challenges include:

- **Direction**

  Numerous different government agencies and departments provide public investment in semiconductor R&D. These agencies and departments have critical missions and often take steps to collaborate, but their important needs and objectives are often distinct from those of private industry. As a result, gaps may emerge in which adequate R&D investment does not reach the technical areas – for example, in ultra-low power computing dependent on collaborative innovations in materials, architectures, packaging, and software – necessary to support continued U.S. technological competitiveness and enable their adoption at production-scale.

- **Resourcing**

  Important infrastructure needed for R&D is lacking or limited domestically. For example, sub-60nm manufacturing is largely inaccessible to university researchers and startups, making it harder for U.S.-based semiconductor hardware startups to iterate on and develop their ideas in the U.S. The absence or insufficiency of R&D-related infrastructure hinders the overall ecosystem's ability to provide advancements.

- **Collaboration**

  Important opportunities for innovation exist in areas like co-optimization that require collaboration across different layers of the computing stack. Advancing R&D in any given layer of the computing stack often requires highly specialized capabilities for both individuals and organizations and the U.S. R&D ecosystem lacks mechanisms to convene capabilities across companies to address these challenges.

Other regions are taking steps to mitigate these challenges and improve the relative effectiveness of their R&D ecosystems

Regions around the world are taking steps to strengthen their semiconductor R&D ecosystems. Examples of the types of mechanisms used in other region to mitigate these challenges in their domestic R&D ecosystems include:

- **Direction:**

  Taiwan's Ministry of Science & Technology supports industry through assessment of overall semiconductor R&D and its coverage of industry needs.

- **Resourcing:**

  Japan's government will invest $6.8 billion in onshore advanced chip manufacturing, mature chip production, and R&D.

- **Collaboration:**

  South Korea will build the "K-Semiconductor Belt" to connect metro areas across the computing stack to ease collaboration and support innovation across the computing stack.

While the U.S. continues to outspend other regions in public investment in semiconductor R&D in absolute terms, other regions provide more generous support for R&D.[12] Other regions are expanding their investments in semiconductors too. Just since 2021, Japan, Singapore, South Korea, the European Union (in addition to individual EU member states like Spain) have all announced legislation to support their domestic semiconductor capabilities, including through investments in R&D. Mainland China too is investing over a hundred billion dollars to support its domestic semiconductor industry.

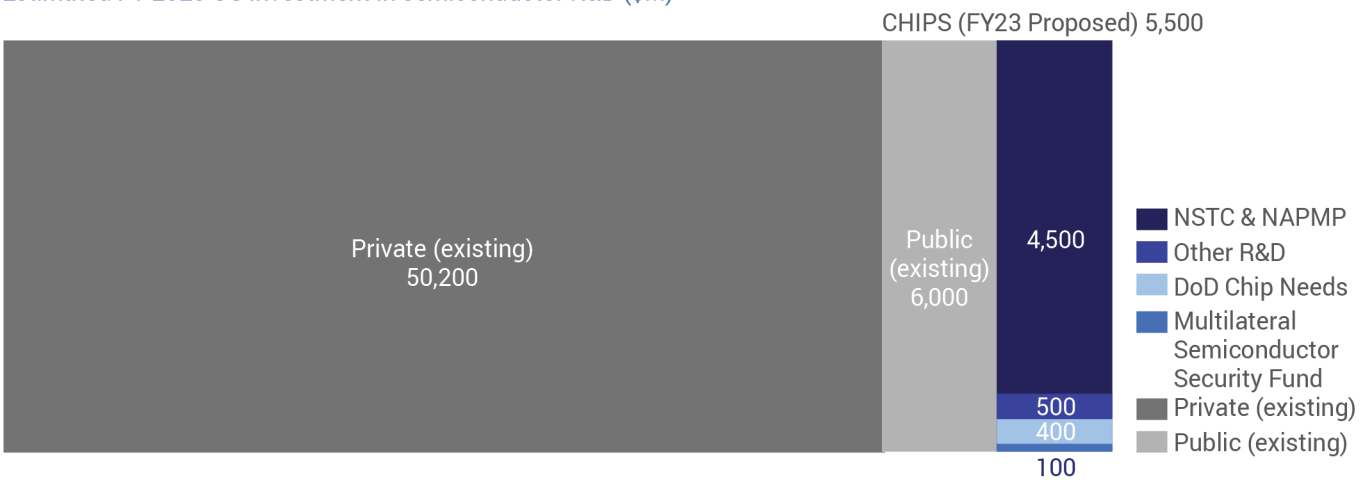
In other words, other regions are taking steps to strengthen their own R&D ecosystems and close the gap on the relative appeal of U.S.-based innovation. Recent programs in the U.S. like DARPA's Electronic Resurgence Initiative (ERI) illustrate growing recognition of the importance of publicly funded semiconductor R&D. Sustained U.S. public investment in this space through existing and new entities can mitigate challenges in the U.S. R&D ecosystem, accelerate the pace of innovation, and extend U.S. technological competitiveness.

12. See Appendix: Support for semiconductors in other regions

Entities responsible for existing public investment of semiconductor R&D will continue to play a significant role in the U.S. R&D ecosystem

Public sector and private industry entities are set to invest $60 billion in semiconductor R&D in the U.S. in 2022. Private industry provides ~$50 billion (~89%) of the total and public investment provides ~$6 billion (~11%). CHIPS and Science Act funds the CHIPS Act's semiconductor-related R&D programs at $5.5 billion for Fiscal Year 2023, to remain available until expended. (see Exhibit 6)

Exhibit 6:
The CHIPS Act's $5.5 billion in FY23 will be sizable supplement to existing annual US public investment in semiconductor R&D



Source: CHIPS and Science Act of 2022; SIA

Many existing organizations for public R&D funding play an important and distinct role in the U.S. semiconductor R&D ecosystem. (see Exhibit 7)

Exhibit 7:
Existing R&D organizations address important needs today but pursue goals distinct from industry

		For semiconductor R&D	
Department or agency	Funding ($B,FY19)	Organizations address important needs…	…but distinctions relevant to industry exist
National Science Foundation	2.7	Funds wide range of pre-competitive and basic research thoughtfully	Research areas not necessarily aligned with commercial needs and speed
Department of Energy	2.2	Manages national labs with specialized technical expertise in semiconductors	Specialized expertise often inaccessible to companies and industry
Department of Defense	1.1	Runs R&D programs related to national security and defense applications	Focus is defense needs, independent of pathway to commercial viability
National Institutes of Standards and Technology	0.03	Supports dissemination of knowledge via network of manufacturing institutes	Unable to support scaling production to commercially useful levels

Note: Funding estimates shown are unofficial and approximate.
Source: SIA Sparking Innovation (June 2020); Expert interviews

Complementing these entities, the CHIPS Act establishes important new organizations and provides an opportunity to address challenges to the U.S. R&D ecosystem

Recognizing the importance of U.S.-based semiconductor manufacturing and R&D, Congress enacted the Creating Helpful Incentives for Producing Semiconductors for America Act (CHIPS Act) in 2021 and provided funding as part of the 2022 CHIPS and Science Act. The CHIPS Act constitutes the most significant federal effort in decades to support U.S. semiconductor manufacturing and seeks to ensure that the U.S. grows both capacity to fabricate more chips in the U.S. and capability to advance chipmaking technology in the U.S.

The CHIPS and Science Act appropriates $52 billion over five years to support semiconductor manufacturing, R&D, and technology transition, with funding frontloaded to earlier years. Of these funds, $39 billion – fully 75% of the total – is directed toward public financial assistance for constructing, modernizing, or expanding facilities and equipment in the U.S. The remaining $13 billion is directed toward R&D and the transition of technologies from labs to the marketplace. (see Exhibit 8) Relative to existing efforts, the CHIPS Act constitutes a major expansion of public investment in semiconductor R&D.

Exhibit 8:
Authorized programs in CHIPS Act

Dept.	Program	Statutory objectives
White House Office	Sub-committee on microelectronics leadership	Create national strategy on microelectronics research
Commerce	Industrial Advisory Committee	Assess effectiveness of national strategy
Commerce (NIST)	Semiconductor incentives	Construct, expand, or modernize fabs located in US
Commerce (NIST)	National Semiconductor Technology Center (NSTC)	Strengthen security of supply chain and economic competitiveness; public-private partnership
Commerce (NIST)	National Advanced Packaging Mfg. Program	Strengthen domestic advanced test, assembly, packaging capabilities
Commerce (NIST)	Manufacturing USA institute	Develop and cultivate semi. manufacturing capabilities in the US
Commerce (NIST)	Microelectronics research	Accelerate R&D for metrology of next-generation microelectronics
Defense	National Network for Microelectronics Develop.	Enable lab-to-fab transition of microelectronics innovations
Defense	Defense Microelectronics	Incentivize consortia for measurably secure microelectronics
Treasury/State	Multilateral Semiconductor Security Fund	Develop and promote secure semi. supply chains with allies

Discussed in this report

Dedicated funding

No Dedicated funding

The CHIPS Act establishes two major innovative programs related to R&D:

National Semiconductor Technology Center (NSTC).
A public-private partnership to foster U.S. leadership in semiconductors by promoting advanced R&D and prototyping to strengthen U.S. technological competitiveness and supply chain security.

National Advanced Packaging Manufacturing Program (NAPMP).
A part of NIST, NAPMP is established to strengthen semiconductor advanced test, assembly, and packaging capabilities in the U.S. R&D ecosystem.

The CHIPS Act establishes certain high-level objectives, the U.S. Department of Commerce retains significant discretion in how to structure the NSTC and NAPMP. In response to its request for information, the Department has received detailed feedback from over 200 stakeholders on the incentives, infrastructure, and R&D needs to support a strong domestic semiconductor R&D ecosystem.[14]

Informed by extensive discussions with and input from SIA members, this report offers a synthesized, high-level industry perspective on how CHIPS Act R&D funding can be most effectively deployed to support U.S. technological competitiveness.

13. "History." Manufacturing USA, www.manufacturingusa.com/pages/history. Accessed 30 June 2022.
14. Request for Information (RFI) notice "Incentives, Infrastructure, and Research and Development Needs to Support a Strong Domestic Semiconductor Industry" was posted by the Department of Commerce on January 23, 2022. Responses are publicly available on Regulations.gov

Spotlight: Manufacturing USA Institutes

Manufacturing USA institute: The Manufacturing USA Institute initiative was originally established in 2014 to boost the U.S. manufacturing sector's global competitiveness and foster innovation.[13] Since inception, 16 institutes across the U.S. have been created to invigorate U.S. manufacturing, each within a specific industry sector.

Institutes are a critical resource for American innovation, supporting the initial stages of the innovation pipeline and building new and much needed communities where none exist. They serve to identify promising high-impact technologies, then manage corresponding R&D projects performed in academic and industry research labs to further advance these technologies. Upon successful completion of these projects the technologies created can transfer to development facilities in industry or otherwise for testing, piloting, and scaling to manufacturing.

The 2022 CHIPS and Science Act authorized the establishment of up to 3 Manufacturing USA Institutes to support work relating to semiconductor manufacturing including increased automation, advanced assembly and test, and workforce skills training. Funding for these institutes is included as part of the overall R&D funding within the CHIPS and Science Act.

The specific projects developed through this Manufacturing USA Institute would serve as a key pipeline for innovative technology in this sector and would be ideally transferred to either the NSTC or NAPMP for testing, piloting, and scaling. The role of this Institute and others in the technology innovation process is clarified in Exhibit 4

The NSTC and NAPMP should promote U.S. economic competitiveness through investments in several areas

Recognizing the centrality of private industry in U.S. economic and technological competitiveness, Congress authorized the NSTC as a public-private partnerships and established it through the U.S. Department of Commerce.[15] NSTC leadership should seek to include voices from academia and government, and especially industry, to promote U.S. technological and economic competitiveness most effectively.

Based on our discussions with industry leaders, the NSTC and NAPMP should bolster the U.S. R&D ecosystem's capabilities through investments in five key areas. (see Exhibit 9)

15. Sections 9906(c) and (d) of the National Defense Authorization Act of 2021 – which contains the CHIPS Act - directs that the NSTC be operated as a public private-sector consortium with participation from the private sector, the Department of Energy, and the National Science Foundation.

Exhibit 9:
Key investment areas for NSTC and NAPMP

Governance

R&D investments to be industry-led

Academia & gov't involved

Focused on all five investment areas

Investment areas	Examples (illustrative)
Transitioning & Scaling of Pathfinding Research Support pre-competitive research into technologies that are 5-15 years away from volume production	**Pre-competitive research into:** Materials (e.g., ultra wide bandgap); Beyond CMOS
Research Infrastructure Upgrade or expand access to research tools, equipment, or other necessities for ecosystem as a whole	**Upgrade and expand access to:** Adv. simulation & modeling software; Pre-mfg. validation and verification
Development Infrastructure Upgrade or expand access to existing development facilities, tools, equipment, or other necessities for whole ecosystem	**Upgrade and expand access to:** Prototyping and piloting centers; Masking infrastructure
Collaborative Development Convene companies for full stack and collaborative innovation to accelerate development of key technologies, tools, industry standards and methodologies	**Convene consortia to accelerate:** Integrated power electronics; Energy conversion and storage; Advanced packaging standards
Workforce Promote programs to increase size of US workforce in semi. R&D, support workforce readiness and skills development	**Strengthen workforce via:** Fellowships & scholarships (MA/PhD); Vocational training & trade schools

Transitioning and Scaling Pathfinding Research

U.S. semiconductor companies currently partner with several existing and well-regarded organizations like Interuniversity Microelectronics Center (imec) and the Semiconductor Research Corporation (SRC) for many pre-competitive R&D needs. To support U.S. technological and economic competitiveness most effectively, the NSTC and NAPMP should augment rather than replicate these organizations. In other words, while the NSTC and NAPMP infrastructure can support early-stage research, their primary focus should be on maturing and scaling those technologies that are ready to move beyond early-stage research. The NSTC and NAPMP should bring together research centers across government, academia, and industry to assess which technologies of commercial interest to companies in the U.S. may need but not be receiving funding for technology transition and scaling.

Consistent with the five high-level challenges discussed in the 2030 Decadal Plan for Semiconductors, the NSTC and NAPMP should strengthen the U.S. R&D ecosystem's ability to conduct and commercialize R&D technologies that are 5 to 15 years from production.[16] This future focus for technology development is important: given the extended timelines over which semiconductor R&D occurs, the investments necessary for today's major technological advancements were made many years ago. Rather than replicate capabilities currently found overseas or in domestic facilities, the NSTC and NAPMP should build and strengthen the R&D ecosystem's capabilities in emerging areas – like materials-beyond-CMOS, advanced packaging, heterogenous integration, and masking infrastructure – in which regional leadership has yet to be determined.

Although R&D funding should include an emphasis on both core semiconductor technologies and packaging technologies, there may be differences in the timelines over which breakthroughs can be realized into products in these two areas. Broadly, R&D for core semiconductor technologies should emphasize longer-term, potentially revolutionary efforts, where innovation will result from material, process flow, and tool improvements. These innovations will come from areas such as:

- Advanced architectures for logic, memory, analog
  - 3D stacked devices
  - Monolithically integrated functions
  - Memory-centric computing

- Advanced materials for beyond Complementary Metal Oxide Semiconductor (CMOS) computing and novel paradigms
  - Two dimensional materials

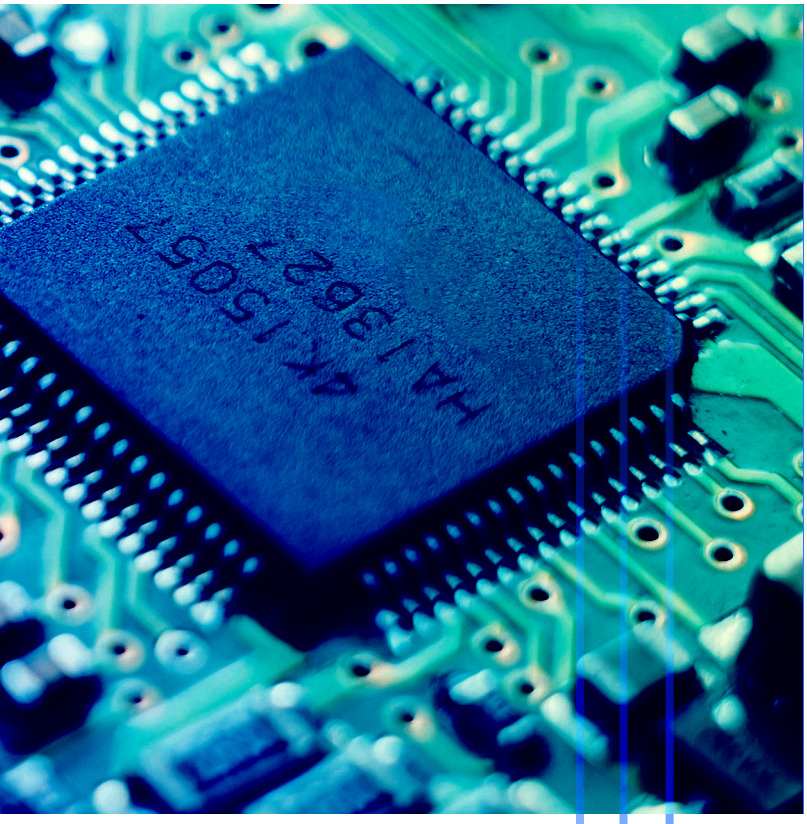
16. The 2030 Decadal Plan for Semiconductors is published by the Semiconductor Research Corporation. It identifies five seismic shifts related to 1. analog electronics, 2. new solutions in memory and storage, 3. improvements in connectivity and communication capacity, 4. breakthroughs in hardware security, and 5. improved compute energy efficiency. Additional information can be found here.

- Advanced functional materials
- Alternate paradigms such as photonic or neuromorphic
- High-voltage and -power materials
- Advanced RF materials

- General process developments
  - Advanced lithography techniques
  - Development of advanced light sources and EUV improvements
  - Improvements in metallization

- Design innovations
  - Superior domain specific accelerators across wider variety of applications
  - Mixed-signal designs, integration of intelligence and sensing capabilities
  - Design for security

- Tool improvements
  - Integration of AI into design tools, higher design abstraction
  - Superior tools for analog and RF circuits
  - Tools with enhanced capability for full-stack optimization and enablement of hardware-software codesign



- Environmental Sustainability
  - Process gases with a lower global warming potential (GWP)
  - Photolithography and other chemicals that meet functional needs with an improved environmental profile, as well as detection and treatment technologies at extremely low concentrations
  - Fab processes that satisfy demanding operational requirements while conserving natural resources (energy, water, etc.)

On the other hand, packaging efforts should include technologies that help address industry challenges in the short- and medium-term. Scaling up of new packaging methods can occur more quickly and cheaply than fundamental semiconductor material and process advances. It is not unreasonable to expect packaging breakthroughs to impact the commercial sector between 5 to 10 years after the establishment of the NSTC and NAPMP, or sooner in some rare cases. These innovations will come from areas like:

- Advanced testing and validation capabilities
  - Design-for-test and data analysis for design error reduction
  - Testing automation and integration of AI/ML tools
  - Analog, RF, and mixed signal testing

- Heterogenous integration
  - Development of industry standards for integration
  - Chiplet IP development and access
  - Integration methods for novel computing paradigms (photonic, quantum, etc.)

- Advanced packaging and high-density interconnects (<100 µm IO pitch)
  - Panel and wafer level high-bandwidth, low-latency high-density 2.5D and 3D stacking and assembly methods
  - Hybrid bonding, through-silicon-via, and advanced interposer development
  - Advanced thermal compression bonding for device lifetime improvements
  - Thermal management and crosstalk, noise, and parasitic reduction
  - Flexible, constrained form-factor packaging

- Tool Improvements
  - Package-level co-design tools
  - Superior electrical, thermal, mechanical modeling and design tools
  - Assembly and alignment automation

By investing in pathfinding researching across different investment areas and timelines, the NSTC and NAPMP can enable sustained improvements in core technologies over two decades. Although the technical areas discussed above are categorized as falling under core semiconductor or packaging technologies uniquely, there will need to be significant coordination and cross-pollination of ideas between researchers and external experts in these areas.

Prototyping and Piloting Infrastructure

The NSTC and NAPMP must go beyond only funding or coordinating existing research efforts. The two should play an active role in facilitating access to prototyping facilities or to advanced simulation and modeling software. They must also expand access to capabilities that facilitate technology transition from lab-to-fab – such as prototyping and piloting – and ensure the accessibility of these capabilities to researchers and startups. By facilitating access to these capabilities, the NSTC and NAPMP will broaden the pool of potential innovations able to traverse phases from basic research to scaling and reach commercial usefulness.

Semiconductor R&D capabilities are distributed widely – technically and geographically – across the U.S. ecosystem. To steward public investment well, the NSTC must neither spread funding evenly nor concentrate investments in a single technology or location. Under the guidance of the NSTC/NAPMP steering committees, the NSTC should expand and upgrade the distinct capabilities and infrastructure of a limited number of existing institutions.

Expanding and upgrading institutions' capabilities is important for reasons related to cost and time. Improving existing facilities (so called 'brownfield' development) improvements is cheaper and faster than building entirely new facilities ('greenfield' development). New semiconductor R&D facilities can take multiple years to build – if the NSTC attempted to create new facilities, these facilities could be industry-lagging or out of the date by the time that construction was finished.[17]

The economics of expanding and upgrading are compelling. As the NSTC evaluates which institutions' R&D infrastructure to strengthen, it must balance the benefits of a highly distributed network against the benefits of scale. Given the typically high total costs of each R&D-related facility, our analysis suggests that the NSTC should foster scale and prioritize upgrading fewer, more accessible, state-of-the-art facilities at leading universities and research centers to maximize the impact of a finite amount of public investment. However, the facilities must be upgraded with an eye towards maximizing impact relative to cost. As an illustrative example, upgrading several universities from 200mm to 300mm wafer capabilities could easily exhaust all NSTC funds while providing few truly novel capabilities.

In some cases, the NSTC/NAPMP steering committees may find it more financially prudent to leverage existing domestic industry capacity rather than upgrade lower-volume research capabilities. This could be the case for piloting infrastructure seeking to leverage 300mm wafer production capacity using industry-standard process flows, as an example. The center of gravity that the NSTC provides could open new possibilities for negotiating access to external capabilities. Examples include the coordination of multi-project wafer runs at commercial fabs, or access to commercial design tools for pre-competitive technologies.

Infrastructure for packaging R&D should include 2.5D and 3D stacking and high-density redistribution, optical packaging and test, fan-out, hybrid bonding equipment, tools for advanced interposers (silicon, glass, and high density organic), and equipment for thermocompression bonding. Equipment for high-density solder bumps, copper deposition, and fabrication of vias will be critical as well. Additionally, significant focus on advanced substrate process and flows

17. VerWey. "No Permits, No Fabs: The Importance of Regulatory Reform for Semiconductor Manufacturing", (Center for Security and Emerging Technology, October 2021).

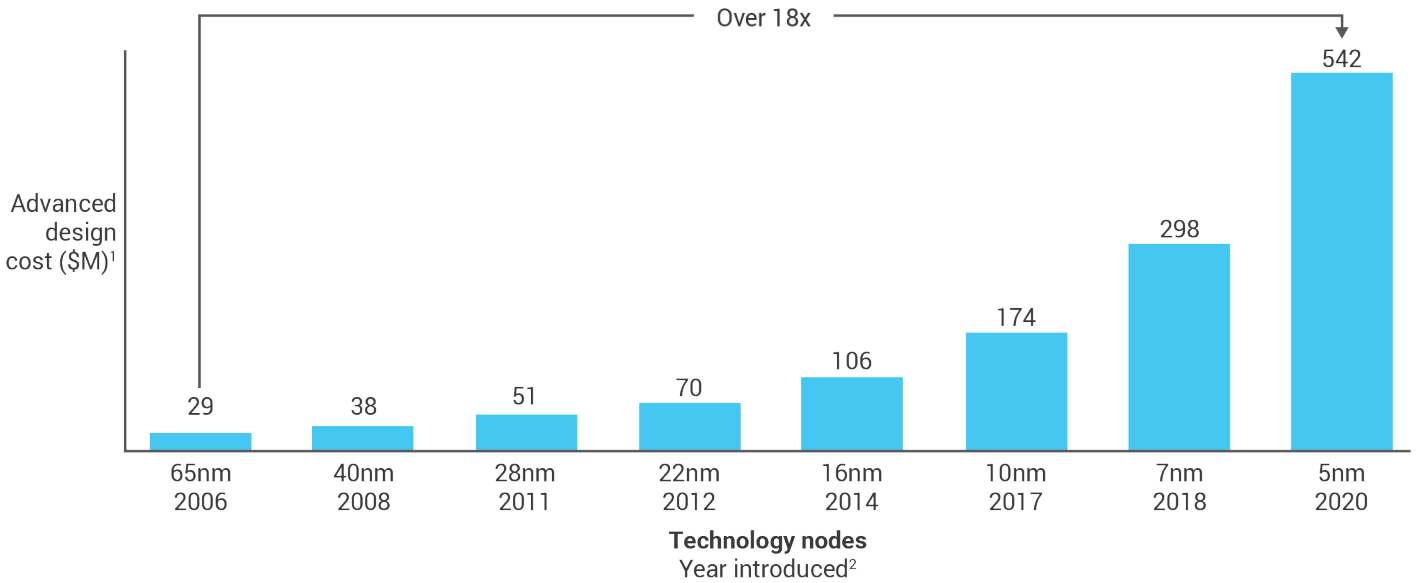
is required. A major challenge in packaging, assembly, and testing (PAT) is the economics of domestic manufacturing. While traditional PAT is labor-intensive, advanced packaging will be more skill and automation-intensive in the U.S. and its economics must reflect this to be competitive. Furthermore, new testing capabilities will be required. Negotiating access to design tools will be a significant value-add for the NAPMP, as with the NSTC.

There are many successful models employed today for semiconductor-serving organizations that the NSTC and NAPMP could look to for guidance. One example is imec, which offers many of the R&D and prototyping capabilities that are critical for the technology development pipeline. Other examples include the Manufacturing USA institutes, which create regional innovation hubs by partnering with research institutions and standing up new prototyping infrastructure, and Sandia National Laboratory's Microsystems and Engineering Sciences Applications (MESA), which provides low-volume commercial foundry services and additional design, fabrication, package, and test capabilities to government and academic researchers. The NSTC and NAPMP infrastructure can pull inspiration from these existing efforts but must go beyond the low-volume services that these existing organizations can provide. It is the ability to allow innovative materials, designs, and broad technologies at the research and prototyping levels to scale up to higher-volume production that grants the NSTC and NAPMP their differentiating value.

Collaborative Development

The engineering approaches to improving computing technology, as described by Moore's Law, are changing as development and design costs rise. (see Exhibit 10) Innovation across the full computing stack, from materials and designs to system architecture and software, is needed to unlock the next stages of semiconductor advancements. Full-stack innovation is hard: modern semiconductor companies are often highly specialized in distinct layers of the stack, and the U.S. R&D ecosystem currently lacks the mechanisms to coordinate this collaboration.

Exhibit 10:
Design costs are rising with each new technology node



1. Advanced design costs include intellectual property qualification, architecture, verification, physical, software, prototype, and validation activities 2. Year in which technology node began volume production
Source: IBS; AnySilicon; TSMC

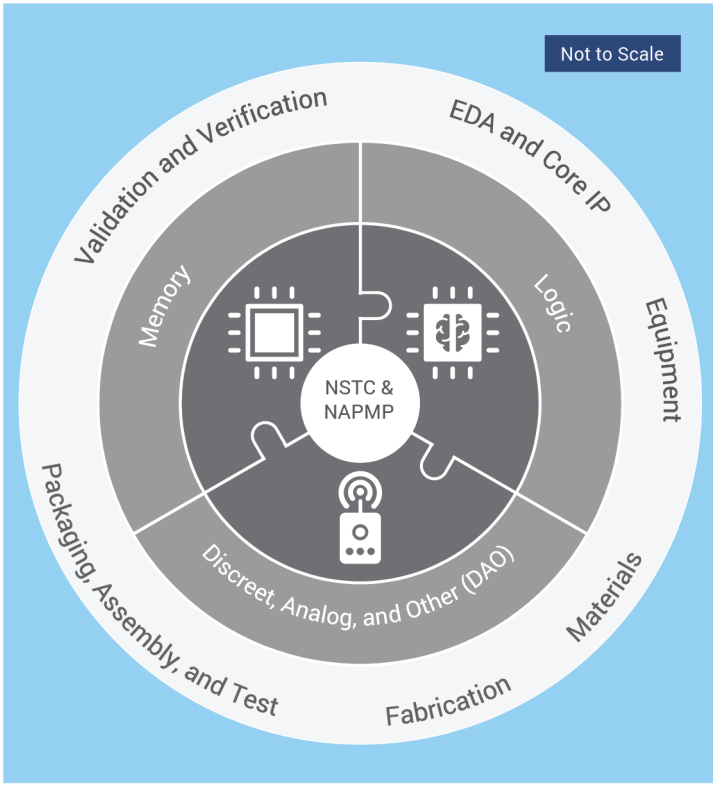
The NSTC and NAPMP should support full-stack innovation by convening companies to solve complex technology problems that require collaboration across the full computing stack and accelerate the development of technologies, tools, and methodologies. For example, the rapid growth in demand for cloud computing data centers has accentuated the need for semiconductors that deliver high compute performance with low power usage. Creating next-generation systems that meet this need requires bringing together expertise in advanced materials, new computing architectures, packaging, software, and more. The NAPMP could convene technology experts and stakeholders (including those from mission-driven governmental agencies) to provide input to groups like IEEE and JEDEC when establishing integration standards for heterogenous integration, chiplets, and other components of secure technologies. The two should own the responsibility of expanding and upgrading the U.S. R&D and prototyping ecosystem's infrastructure and capabilities to meet these ecosystem needs.[18]

Given the importance of innovations in areas like collaborative development, co-optimization, and heterogenous integration, the NSTC and NAPMP must partner widely across the industry. The two can then use their broad and representative networks across the industry to build a diversified technology and infrastructure portfolio of R&D, to facilitate more effective collaborative development, and to maintain a wide network of industry partners. (see Exhibit 11)

Workforce

The semiconductor industry is R&D-intensive and relies on highly skilled workers to conduct the R&D that leads to needed innovations. While the U.S. is home to many of the world's best researchers, a shortage of skilled talent threatens to constrain the pace of innovation (see our report on semiconductor design). At the same time, other regions are eager to attract home their nationals and provide extensive policy support to strengthen their domestic R&D ecosystems. (see Exhibit 12) Amid these competing efforts, the NSTC and NAPMP must strengthen the size and skills of the U.S. semiconductor R&D pipeline and workforce to defend the U.S. R&D ecosystem and the economic competitiveness it underpins.

Exhibit 11:
NSTC and NAPMP must partner widely across the semiconductor industry



To be successful, the NSTC and NAPMP should have **wide industry representation** to:

- Build a diversified **technology and infrastructure portfolio** for research and development
- Facilitate **collaborative development** more effectively
- Maintain a wide **network of industry partners**, including their suppliers and needs of both

Note: Graphic designed to illustrate need for NSTC to collaborate widely and is not exhaustive

18. The Universal Chiplet Interconnect Express (UCIe), an industry initiative, to create a new open standard at the package is an example of collaboration across the computing stack that can accelerate technology development.

Exhibit 12:

China, Japan, and South Korea rapidly growing R&D expenditures per researcher in the workforce

Region	GERD (% growth '00-18)	GERD/Researcher (% growth '00-18)	GERD % GDP (% growth '00-18)	Tax incentive on R&D	Public Investments
United States	$460B (52%)	$311K (2%)	2.8% (8%)	9.5%	2022: Appropriated $13B investment in semiconductor R&D
Mainland China	$431B (1067%)	$230K (335%)	2.1% (140%)	25.8%	2019: National and local government IC funds amount to $73B for manufacturing with allocations for design
Japan	$144B (30%)	$213K (24%)	3.2% (13%)	14.8%	2021: Proposed $45B investment to maintain current market share
South Korea	$86B (326%)	$211K (13%)	4.5% (113%)	4.4%[4]	2021: National Blueprint for research and production includes $1.3B in public funding
Western Europe[1]	$334B (70%)[2]	$133K (-7%)[2]	1.8% (28%)	17.6%[3]	2021: EU commits funds to double the share of the chip market by 2030
India	$52B (179%)	$153K (-5%)	0.7% (-14%)	8.2%	2021: Multi-billion-dollar investment plan for manufacturing is under development
Taiwan					2020: New subsidies of $300M to attract R&D from foreign companies over the next decade

1. Includes 33 countries classified as "Western Europe" by UNICEF
2. Average of given countries
3. Average tax subsidy for largest 20 countries
4. Tax subsidy on R&D varies by company size and industry, ranging from 2% to 50% - amount shown is based on ITIF report analysis

Source: UNSECO Institute of Statistics (UIS) Science R&D Data; ITIF report on "Enhanced Tax Incentives for R&D.."; Lit review

The NSTC and NAPMP could promote a range of programs to expand the pipeline of the U.S. semiconductor R&D workforce. According to our research, industry leaders believe that key steps for NSTC and NAPMP include:

- **Invest in U.S. STEM education.**

  Support curriculum development and standardization at the undergraduate and graduate levels to expand the pipeline of workers with prerequisite STEM skills. Provide opportunities for students at the K-12 level to engage with the industry to gain an awareness of and fascination with semiconductor technologies. NSTC and NAPMP centers could collaborate with or help establish engineering summer camps at US universities to provide exposure to semiconductor R&D. Working with partner institutions and companies to provide scholarships and research fellowships can help increase the number of students pursuing 4+ year degrees within the field.

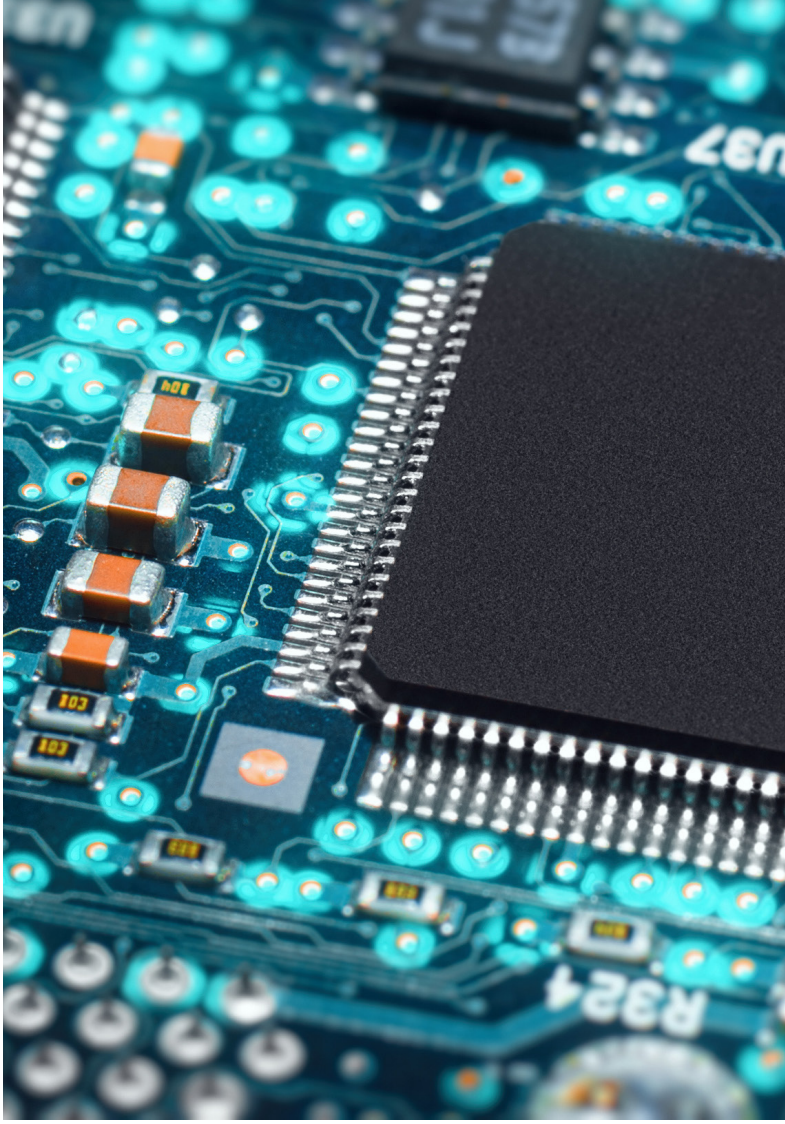
- **Attract STEM workers to the industry.**

  Educate and train students about career opportunities in the semiconductor industry through apprenticeships, internships, and mentorship programs. Work with community and technical colleges to develop programs to bring more technicians and tradespeople to the field and to raise awareness of semiconductor career pathways. Partner with retraining and cross-training programs for workers with existing foundational STEM skills, such as veteran employment organizations.

- **Promote flexible work authorization.**

  Promote flexible work authorization – like optional practical training - that enable foreign nationals to work in the U.S. or hold temporary employment directly related to their major area of study if they graduate from U.S. universities with skills critical to industry. This could happen pre-completion or post-completion of the relevant degree.

In addition, the NSTC and NAPMP must strengthen the skills of the workforce. According to our research, industry leaders believe that key steps for NSTC and NAPMP should include:



- **Invest in worker retraining and upskilling.**

  As the industry explores new dimensions of innovation, these programs can ensure the U.S. R&D ecosystem workforce is well-equipped to drive future advances.

- **Accelerate new employee readiness.**

  Given the specialized skills needed for semiconductor R&D, new employees need time before they effectively engage in important R&D. The NSTC and NAPMP could establish prefab programs to enable a worker to contribute more quickly to R&D.

The pipeline of highly skilled R&D workers currently threatens to limit the pace of innovation. By expanding the supply of these workers and upgrading their skills, the NSTC and NAPMP can strengthen the overall U.S. R&D ecosystem.

The U.S. can employ a range of best practices to ensure the success of this public investment

The CHIPS Act constitutes a major expansion in U.S. public investment in semiconductor R&D. The U.S. can take several actions to ensure this investment complements existing public investment and revitalizes the virtuous cycle of innovation in the U.S. to strengthen the R&D ecosystem.

Focus on impact:

Public investment in R&D should be aligned with identifiable objectives, including a focus on impactful new technologies and on potential commercial viability. Investment should help commercialize innovative ideas and flexibly address barriers to fixing the innovation pipeline for promising technologies.

Foster scale:

The U.S. R&D ecosystem will be better served by fewer, more accessible, and best-in-class clusters – including both physical infrastructure and workforce expertise - rather than many clusters less well-suited to industry R&D needs. Given costs of maintaining a large network of potentially antiquated facilities, fostering scale allows a given amount of public investment to be spent in a more impactful manner.

Look ahead:

From both a technical and financial perspective, public investment should support the U.S. R&D ecosystem in meeting needs that are 5 to 15 years into the future. The infrastructure and enablers necessary for the next 3-5 years of technical advancements have already largely been built. Given that research needs in this industry can range from multi-year to multi-decade, financial investments must be predictable over extended periods of time.

Collaborate:

The U.S. semiconductor R&D ecosystem contains and partners with many existing and effective organizations and programs. Where possible, public investment should augment and coordinate with, rather than replicate, these organizations and programs.

Conclusion

By incorporating the investments discussed here, the U.S. R&D ecosystem in 2030 should be characterized by a larger pipeline of new semiconductor products, tools, and processes, a bigger and more skilled workforce engaged in semiconductor R&D, and an accelerated timeline from basic research to commercialization.

Since its inception, the U.S. R&D ecosystem has enabled a virtuous cycle of innovation that has contributed to U.S. technology leadership. The ecosystem remains strong, with world-class national labs and universities, along with companies that have invested an unprecedented $50 billion in semiconductor R&D in 2021 alone. The funding from the 2022 CHIPS and Science Act and subsequent establishment of industry-led entities in the NSTC and NAPMP will provide a once-in-a-generation opportunity to revitalize the pipeline of innovation and will extend U.S. technological competitiveness through the following decades.

Appendix: Non-academic research organizations

Private industry also works with non-academic research organizations in the U.S. and in other regions for basic research. This includes organizations like the Semiconductor Research Corporation (SRC), the Interuniversity Microelectronics Centre (imec), and CEA-Leti. While U.S. companies and researchers are not restricted to working with U.S.-based research organizations, the non-academic research organizations in Europe and Asia are typically larger and better resourced than their U.S. peers. (see Exhibit 13)

Exhibit 13:

Non-academic research organizations in Europe and Asia are larger and better resourced than US-based organizations

	US	Europe			Asia	
	SRC Semiconductor Research Corporation	imec	CEA Leti	Fraunhofer	工業技術研究院 Industrial Technology Research Institute	A*STAR Agency for Science, Technology and Research
Headquarters[1]	United States	Belgium	France	Germany	Taiwan	Singapore
Year founded	1982	1984	1967	1949	1973	1991
Entity Type	Non-profit	Non-profit Govt. Funded	Non-profit Govt. Funded	Non-profit Govt. Funded	Non-profit Govt. Funded	Govt. owned
Number of partners	125+	600+	300+	75	143	20
Number of employees	~10[2]	4,000	1,500	30,000	6,000	NA
Revenue	$90M	$741M	$330M[3]	$3,096M	NA[4]	NA
Regions of operation	1[2]	7	3	9	5	1
Number of patents	700+	1,600+	3,100+	6,800+	17,000+	350+
Cleanroom facilities	None	12,000 sq. meters	8,000 sq. meters	5,500+ sq. meters	NA	3,000 sq. meters

1. First country listed is company headquarters
2. In addition to its employees, SRC funds approximately 100 professors, 1400 graduate students, and 800 researchers at member companies across ~10 regions around the world
3. Refers to annual research funding
4. 50% of ITRI funding comes from the government.

Source: Companies websites, annual reports, BCG analysis

Appendix: Support for semiconductors in other regions

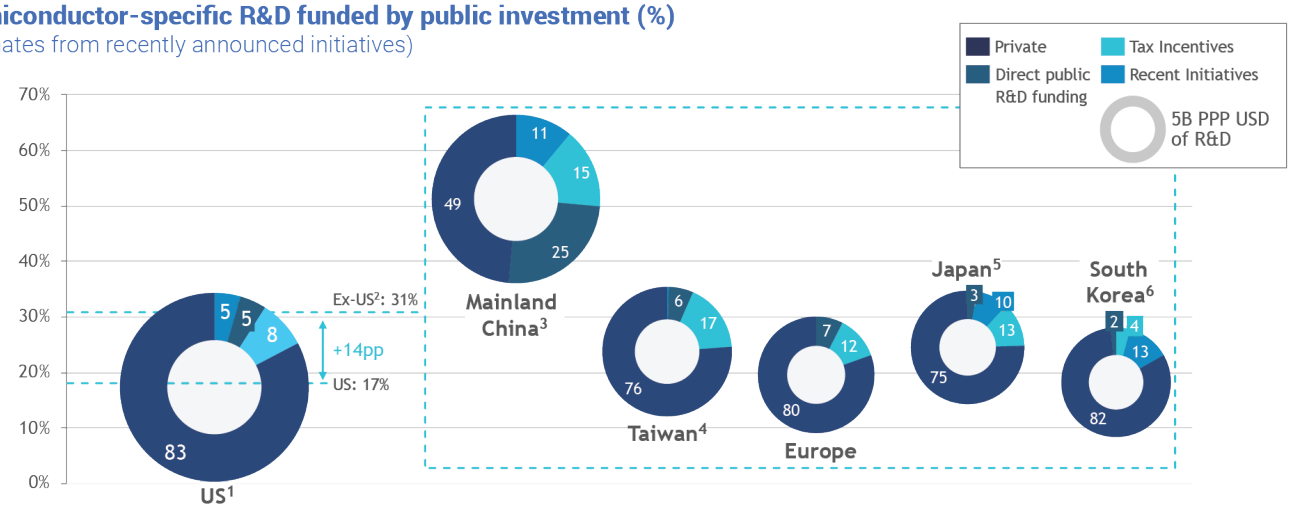
While the U.S. continues to outspend other regions in public investment in semiconductor R&D in absolute terms, other regions provide more generous support for R&D.

The overall share of semiconductor-specific R&D funded by public investment in the U.S. is 23.3%. By comparison, the share is 35.7% across mainland China, the European Union, Taiwan, Japan, and South Korea. (see Exhibit 14)

Exhibit 14:

Share of semiconductor-specific R&D funded by public investment varies by region

Share of semiconductor-specific R&D funded by public investment (%)
(includes estimates from recently announced initiatives)



1. Includes semiconductor-specific R&D funding over five years from the CHIPS and Science Act.
2. Includes mainland China, Europe, Taiwan, Japan, and South Korea.
3. Includes elimination of 25% corporate income tax for semiconductor design.
4. Includes NT$10B over 7 years for foreign companies to establish R&D centers.
5. Includes recent initiatives such as the Post 5G fund and Green Innovation Fund.
6. Includes recent initiatives such as K-semiconductor belt strategy and AI R&D programs.

Note: Percentages represent share of total semiconductor-specific R&D funded by public investment
Sources: OECD national accounts data and ITIF; Government websites; SIA; BCG analysis.

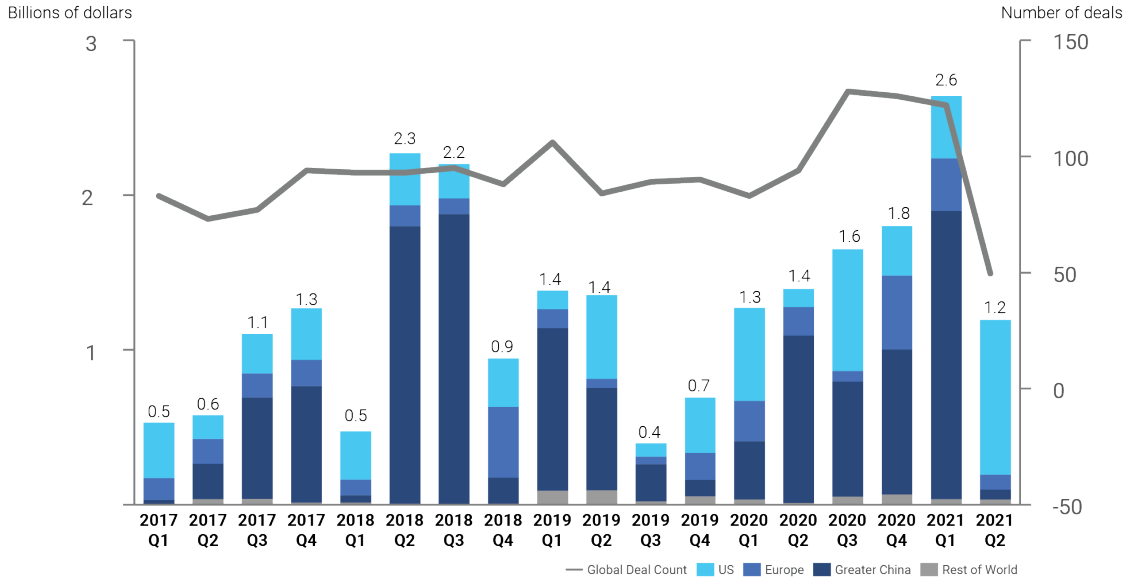
Appendix: Venture capital funding for semiconductor startups

Amid supply chain bottlenecks and high demand for chips, semiconductor startups – in China and the U.S. – have raised significant amounts of venture capital funding in recent years. Fueled in part by strong expected demand for artificial intelligence and machine learning chips, global venture capital investment set a quarterly record for deal value at $2.64 billion during the first three months 2021. 70% of these funds were raised by Chinese semiconductor startups, with the U.S. raising 15%. U.S. venture capital funding for semiconductor startups has reached a 20-year high. (see Exhibit 15) [19]

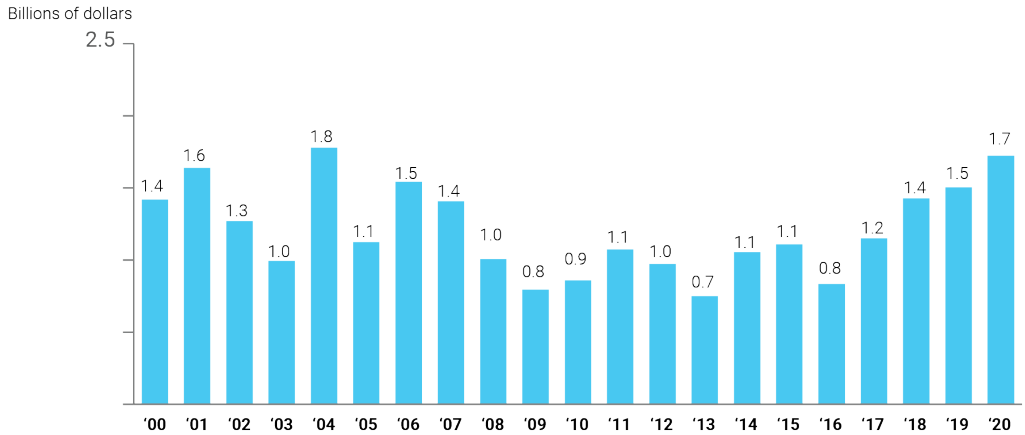
Exhibit 15:

Venture capital funding raised by semiconductor startups is at a multi-year high globally and in the US

Globally, China and the US lead in semiconductor venture capital funds and deal count



Within the US, venture capital funding for semiconductor companies at ~20 year highs



Note: Greater China includes Mainland China and Taiwan
Source: PitchBook

19. Lee, Jane Lanhee. "U.S. Chip Startups, Long Shunned in Favor of Internet Bets, Stir Excitement Again." U.S., 5 May 2021, www.reuters.com/article/venture-capital-semiconductors-funding-idINKBN2CM10S. Thorne, James. "It's U.S. vs. China in Race to Build Chip Technology of Tomorrow." PitchBook, 4 May 2021, pitchbook.com/news/articles/U.S.-China-semiconductor-chipmakers-venture-capital.