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Łukasiewicz Fuzzy Logic Networks and Their Ultra Low Power Hardware Implementation

Rafał Długosz[1,*], Witold Pedrycz[2]

1- Swiss Federal Institute of Technology in Lausanne, Institute of Microtechnology,
Rue A.-L. Breguet 2, CH-2000, Neuchâtel, Switzerland,
[*]fellow of the Marie Curie OIF fellowship
2- University of Alberta, Department of Electrical and Computer Engineering
ECERF Building, Edmonton, T6G 2V4, Canada

Abstract. In this paper, we propose a new category of current-mode Łukasiewicz OR and AND logic neurons and logic networks and show their ultra low power realization. The introduced circuits can operate with very low input signals that set up the operating point of transistors in the subthreshold region. In this region, the mismatch between transistors has much stronger impact on the current mirror gain than in the strong inversion region. The proposed solution minimizes this problem by reducing the number of current mirrors between the input and output of the neuron to only one.

1 Introduction

Łukasiewicz logic connectives are one of the possible realizations of logic operators for fuzzy sets [1]. They are interesting examples of a broad category of logic connectives known as t-norms and t-conorms. More formally, the Łukasiewcz *and* operator is described as follows:

$$atb = \max(0, a + b - 1) \tag{1}$$

while the *or* operator is governed by the following expression

$$asb = \min(1, a + b) \tag{2}$$

where the (logic) truth values *a* and *b* assume values in the unit interval.

These logic connectives can be put together in the construction of *logic* neurons that are viewed as generic processing units encountered in neurocomputing. Logic neurons [2] offer functionality which relies both on neurocomputing and fuzzy logic. The logic neurons come with well-defined semantics, which is drawn from the nature of the underlying logic processing inherent to fuzzy computing. We encounter two fundamental categories of fuzzy neurons.

OR neuron: this neuron realizes an *and* logic aggregation of inputs $\mathbf{x} = [x_1\ x_2 \ldots x_n]$ with the corresponding connections (weights) $\mathbf{w} = [w_1\ w_2 \ldots\ w_n]$ and then summarizes the partial results in an *or*-wise manner (hence the name of the neuron). The concise notation underlines this flow of computing, $y = OR(\mathbf{x}\ ;\ \mathbf{w})$ while the realization of the

logic operations gives rise to the expression (commonly referred to as an s-t combination or s-t aggregation)

$$y_{OR} = \sum_{i=1}^{n} (x_i t w_i) \tag{3}$$

Here "t" denotes a certain t-norm whereas "s" refers to some t-conorm. Bearing in mind the interpretation of the logic connectives, the OR neuron realizes the following logic expression being viewed as an underlying logic description of the processing of the inputs

$$y_{OR} = (x_1 \textit{ and } w_1) \textit{ or } (x_2 \textit{ and } w_2) \textit{ or } \ldots \textit{ or } (x_n \textit{ and } w_n) \tag{4}$$

Apparently the inputs are logically "weighted" by the values of the connections (w_i) before producing the final result. In other words we can treat "y" as a truth value of the above statement where the truth values of the inputs are affected by the corresponding weights. Noticeably, lower values of w_i discount the impact of the corresponding inputs; higher values of the connections (especially those being positioned close to 1) do not affect the original truth values of the inputs. In limit, if all connections w_i, i =1, 2,…,n are set to 1 then the neuron produces a plain *or*-combination of its inputs:

$$y_{OR} = x_1 \textit{ or } x_2 \textit{ or } \ldots \textit{ or } x_n \tag{5}$$

The values of the connections set to zero eliminate the corresponding inputs. Computationally, the OR neuron exhibits nonlinear characteristics (that is inherently implied by the use of the t- and t-conorms.

AND neuron: the neurons in the category, denoted by y = AND(**x**; **w**) with **x** and **w** being defined as in case of the OR neuron, are governed by the expression

$$y_{AND} = \prod_{i=1}^{n} (x_i s w_i) \tag{6}$$

In comparison with the previous category of the neurons, the *or* and *and* connectives are used in a reversed order: first the inputs are combined with the use of the t-conorm and the partial results produced in this way are aggregated *and*-wise. Higher values of the connections reduce impact of the corresponding inputs. In limit w_i =1 eliminates the relevance of x_i. With all w_i set to 0, the output of the AND neuron is just an *and* aggregation of the inputs

$$y_{AND} = x_1 \textit{ and } x_2 \textit{ and } \ldots \textit{ and } x_n \tag{7}$$

2 Implementation of the OR and the AND neurons using typical CMOS fuzzy operators

Basic fuzzy logic operators together with their CMOS hardware implementation have been described in [3]. To realize these operators the current-mode technique is the

most suitable as it allows for an easy realization of summation and subtraction operations. The logic *or* and the *and* operators are also referred to as the bounded sum and the bounded product, respectively [3]. Using the approach presented in [3] both operators can be implemented using circuits shown in Figure 1. This figure presents a simplified diagram of the Łukasiewicz network that consists of two layers of neurons. In this case, the network comes in the AND-OR configuration, although the dual configuration, that is OR-AND, arises as another alternative topology.

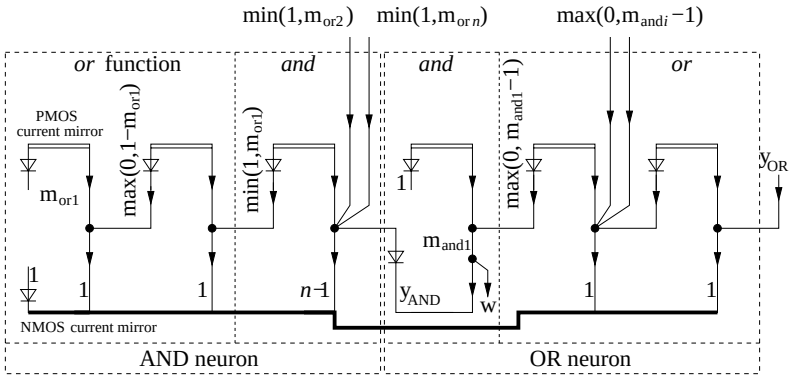

Fig. 1: Implementation of an example AND-OR Łukasiewicz network

As mentioned above, the current-mode technique offers a very effective platform for the implementation of the logic operators, however it is a source of limited accuracy of these circuits. One of the main problems encountered in this realization is a mismatch between transistors present in the current mirrors [4]. Usually, the threshold voltage mismatch, ΔV_{th}, is assumed to be the main reason causing mismatch between the transistors working in a current mirror. Assuming that both transistors have equal dimensions then in the weak inversion region the mirror's gain that results from ΔV_{th} can be calculated as follows [5]:

$$G = I_2 / I_1 = \exp\left(-\Delta V_{th} / V_T\right) \tag{8}$$

where V_{T} is the thermal voltage(about 26mV in the room temperature of 300 K). The influence of the transistor dimensions on the mismatch effect for different technologies has been reported and studied in many papers. For instance, in the CMOS 0.18μm process, the standard deviation of the V_{th} mismatch varies between 0.7 and 2.7 [mV] given that the transistor gate's area ($W \cdot L$) varies in the range between 75 and 5 μm^2 [6]. In the weak inversion region, this effect introduces to the current mirror a gain error of 2.8%; however this error could as high as 12 %. In the strong inversion region, the influence of the mismatch on the gain is about 6 – 8 times smaller, but it is still important in case of circuits with large number of intermediate current mirrors. In the circuit shown in Figure 1 the number of current mirrors between the input and the output equals to 6. For small transistors working in the strong inversion regime the error of 6-10 % is realistic, while in the subthreshold region this error could be as high as 40 %.

3 The proposed realization of the Łukasiewicz OR and AND logic neurons

To overcome the serious problem described above, we consider the realization presented in Figure 2. The circuits take advantage of the current mode, but signal paths are controlled by current-mode comparators, realized using NOT gates, and switches.

The topology of the circuit is selected in a way it minimizes the number of the intermediate current mirrors so that it limits an overall error. In the proposed solution the input signals are directly transferred to comparators as well as to other branches, including the output branch, using the same multi-output current mirror. For this reason, the mismatch error in each branch is always related to the same input transistor and thus does not accumulate over successive processing steps. For sufficiently large transistors this error does not exceed 2%.

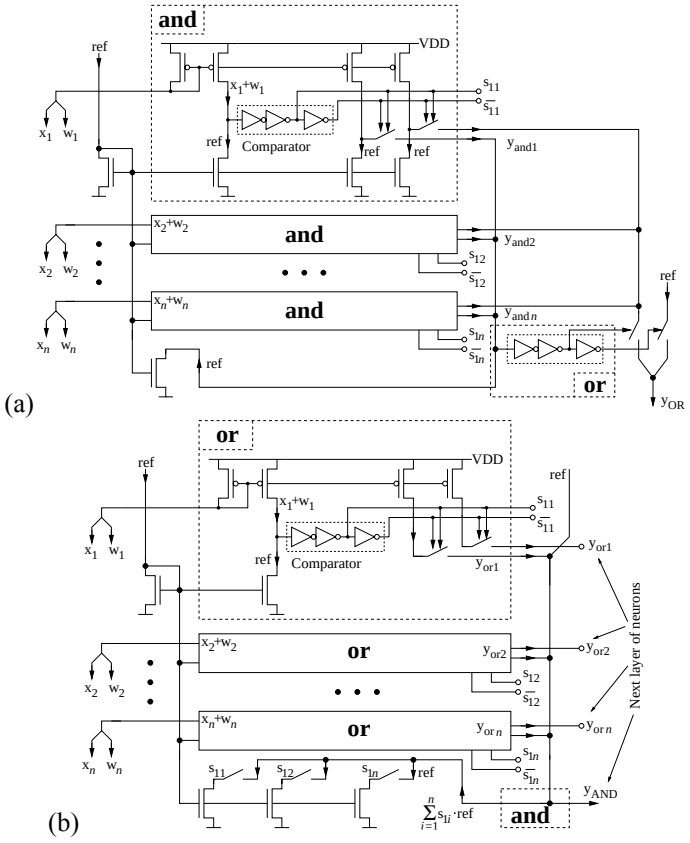

Fig. 2: The proposed Łukasiewicz neurons: (a) OR and (b) AND.

Some simulation results for the logic neurons implemented in this way are shown in Figure 3 and 4, respectively. In the completed simulations both neurons have 4 inputs (x) and 4 weights (w). For the ease of visualization, the values of x and w are kept the

same. The upper plot in both figures presents the input and the output signals. The second plot in Figure 3 illustrates operation of the comparator. A very important aspect here concerns a precision of the designed circuits, which has been evaluated by comparing the simulated signals showing at the outputs and the values obtained from (4) and (6) for given inputs. The third plot in Figure 3 presents the percentage error for the OR neuron. The error is the highest for small signals. It is also quite high in periods, in which comparators have to change the state which introduces some delay. For the full scale input signals the error is well below 0.5%.

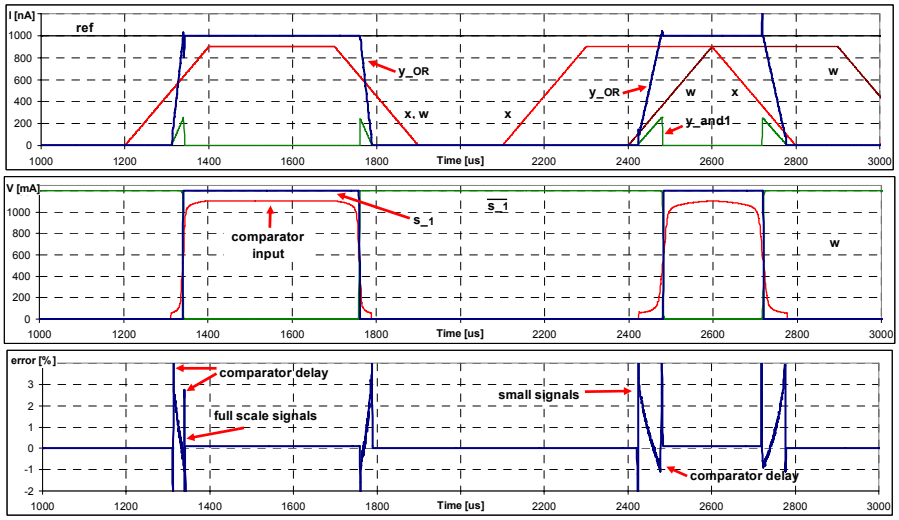

Fig. 3: Simulation results for OR neuron: (top) input and output signals (middle) operation of the comparator (bottom) error between ideal and simulated cases

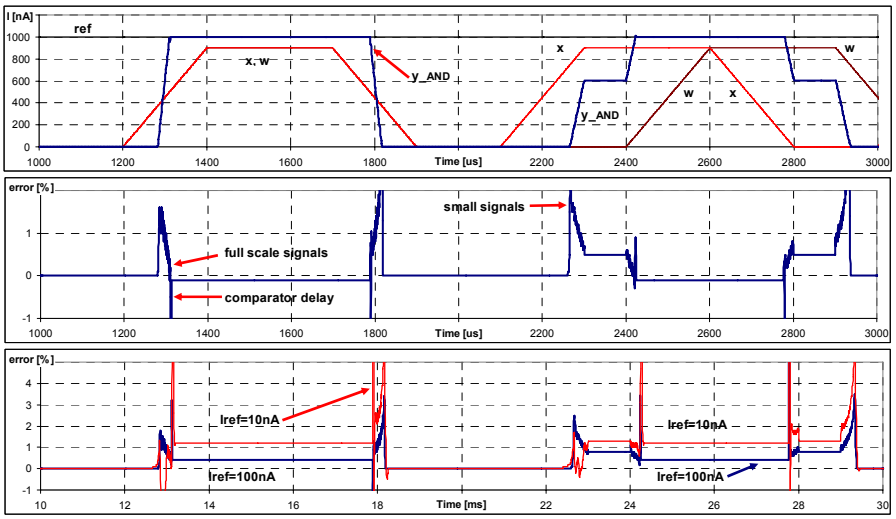

Fig. 4: Simulation results forthe AND neuron: (top) input and output signals (middle) resultant error (I_{ref}=1000 nA) (bottom) errors for I_{ref}=100 nA and 10 nA

The similar results, Figure 4, have been obtained for the AND neurons. In this case the error calculated in relation to the full scale signal is at the level of 0.25%. The third plot presents the error in case of reduced values of the input signals, namely for I_{ref} = 100 nA and 10 nA. We note that although the error increases for smaller signals, it happens relatively slowly.

One of the key objectives is to reduce power dissipation of electronic circuits to enable their effective usage in ultra low power portable devices [7]. The ability of the circuits to work with signals which vary in a large range of values is one of the paramount features of our design. In this type of circuits the power dissipation almost linearly depends on the values of the input signals. For the input signals varying in the range up to 1 μA the average power dissipation equals to c.a. 10 μW, while for the range of 10 nA the power dissipation becomes reduced to 95 nW only.

The results presented in this study are reported for the CMOS 0.18μm process and the supply voltage of 1.2 V. One could note that these circuits operate properly between 1.8 and 0.9V of the supply. In newer CMOS technologies, the supply voltage could be further reduced that facilitating further reduction of power dissipation.

4 Conclusions

In this study, we have proposed the new ultra low power circuit realization of *or* and the *and* Lukasiewicz operators used as logic connectives in OR and AND neurons. In the proposed circuits the error reduction for small signals is achieved by eliminating a chain of current mirrors between the input and the output of the neurons. The simulation results show that the circuits can operate with currents that are at the level of single nAmps, which is an attractive feature especially for very low power portable devices.

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