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FPGA implementation of an integrate-and-fire LEGION model for image segmentation

Bernard Girau and Cesar Torres-Huitzil

1- LORIA INRIA-Lorraine / University Nancy 2 - Cortex team
campus scientifique B.P. 239 54506 Vandoeuvre-les-Nancy - France

2- INAOEP - Computer science department
Luis Enrique Erro #1, Tonantzintla - Puebla - Mexico

Abstract. Despite several previous studies, little progress has been made in building successful neural systems for image segmentation in digital hardware. Spiking neural networks offer an opportunity to develop models of visual perception without any complex structure based on multiple neural maps. Such models use elementary asynchronous computations that have motivated several implementations on analog devices, whereas digital implementations appear as quite unable to handle large spiking neural networks, for lack of density. In this work, we consider a model of integrate-and-fire neurons organized according to the standard LEGION architecture to segment grey-level images. Taking advantage of the local and distributed structure of the model, a massively distributed implementation on FPGA using pipelined serial computations is developed. Results show that digital and flexible solutions may efficiently handle large networks of spiking neurons.

1 Introduction

Biological arguments indicate that some vision tasks, as well as most olfactory tasks, cannot be satisfactorily performed by standard neural models that use an analog computation mode, where values stand for mean firing rates of natural spiking neurons [1, 2, 3, 4]. Temporal coding has to be fully exploited, for example through the notion of neuron synchronization [5, 6]. Among several works carried out by our team so as to develop a fully neural system for autonomous robotics, we have studied the use of standard spiking models for a rough real-time analysis of the robot visual environment. In order to study the possibilities of embedded real-time implementations, we have first chosen to implement a well-known though criticized spiking model for image segmentation on FPGAs: the integrate-and-fire LEGION model [7], since this model is able to segment grey-level images, and its underlying 2D structure fits the topological constraints of FPGA implementations. Our work mostly focuses on low-area solutions, based on the use of a standard serial arithmetic within pipelined loops. As a result, a fully parallel implementation of the LEGION network has been mapped onto a Xilinx VIRTEX FPGA device, large enough to handle our low-resolution robot image sequences. Steady communication channels, synapses, have been preferred to event-driven systems so that our implementation is fully distributed. The LEGION model is described in section 2. The global architecture of the hardware implementation of the spiking neural model is detailed in section 3, before implementation results are given in section 4.

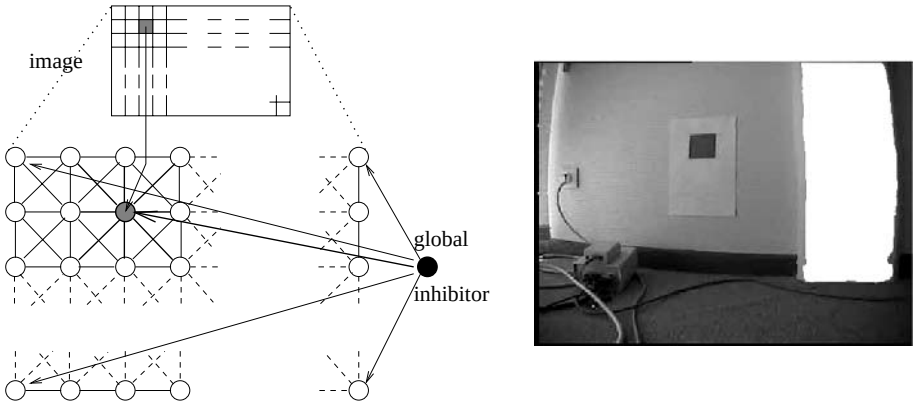

Fig. 1: LEGION network : a) 2D architecture - b) image segmentation

2 LEGION Model Description

2.1 Principle

Oscillations of neurons in the cortex are now considered as a important mechanism that is involved in several cognitive functions of the brain. Our research team is more particularly interested in the role that this mechanism plays in perceptive tasks such as vision and olfaction [2].

Several studies have shown that oscillations of neurons take part in several perceptive functions of the cortex. These oscillations are used in visual perception to segment features in a visual scene [8]. Neurons in cortical areas such as primary visual area V1 are known to "see" only a small localized part of the visual field (such areas are retinotopically organized). And yet synchronized behaviors have been detected for groups of neurons which visual fields are strictly separated. These neurons bind together thanks to the synchronization of their firing activities.

The LEGION network (Local Excitatory Global Inhibitory Oscillator Network) has been proposed in [9] based on biological considerations. This simple model consists of a 2D grid of oscillators (see figure 1-a) that receive visual stimuli. Neighboring oscillators are coupled by excitatory connections, and a global inhibitor gets active when any oscillator jumps up.

The original LEGION model uses relaxation oscillators [9]. In order to segment images, the LEGION model groups oscillators that receive their input from similar features in an image. Oscillators group together by synchronization of their phase thanks to excitatory connections, and they get desynchronized from other groups of oscillators by means of global inhibition (see figure 1-b: in this image taken by our robot camera, pixels in white correspond to a group of simultaneously firing neurons, thus segmenting a distinct part of the wall).

2.2 Integrate-and-fire LEGION

After having been applied to binary image segmentation, and then to grey-level image segmentation [10], the LEGION architecture has been chosen in [7] as an interesting model to study synchronization and desynchronization of integrate-and-fire oscillators (or spiking neurons). Beside the interest of this approach so as to study the complex properties of assemblies of such oscillators, it provides us with a model that keeps synchronization properties while being suited for digital VLSI implementation. The dynamics of a LEGION network of integrate-and-fire oscillators is defined according to the following equation:

$$\frac{dx_i}{dt} = -x_i + I_i + \sum_{j \in N(i)} \frac{\alpha_{ij}}{Z_i} P_j - G$$

where the sum is over the oscillators in a neighborhood, $N(i)$, around oscillator i, x_i is the potential of oscillator i, Z_i is the number of nearest neighbors that oscillator i has (to take into account boundaries problems). α_{ij} is the coupling strength. P_j is a neighbor oscillator that fires at a given time producing an excitation pulse to oscillator i. G is an instantaneous inhibitory pulse to the entire network when any oscillator in the network fires. When $x_i = 1$ the oscillator is said to fire; its potential is instantly reset to 0, and it sends excitation to its neighbors.

The parameter, I_i is the external stimulus given to oscillator i and when applied to image segmentation it depends on the input image. In order to segment grey level images, the parameter I_i is computed as follows [10]. Let p_i be the intensity of pixel i. If $|p_i - p_j|$ is less that a given threshold, then the two pixels are said to satisfy the pixel difference test. Two oscillators have a nonzero coupling strength only if they are neighbors and if their pixels satisfy the pixel difference test. The weights of the connection strengths α_{ij} are determined by the number of neighboring pixels of i that pass the pixel difference test. If half of the pixels in $N(i)$ satisfy the pixel difference test, then I_i is set to a value I_L greater than 1. If no neighboring pixel satisfies the pixel difference test then I_i is set to zero. Otherwise, I_i is given a stimulus I_N, which is less than but near 1.

It has been demonstrated that integrate-and-fire LEGION maintains its segmentation capabilities since their synchronizing properties are similar to relaxation oscillators [7]. Due to the oscillatory characteristic in LEGION, a large amount of differential equations need to be solved, which induces a high computational load and power consuming task in conventional processors. The use of integrate-and-fire oscillators are attractive for digital VLSI implementation for perceptual organization in embedded systems.

3 LEGION Hardware Implementation

3.1 Field Programmable Gate Arrays for Neural Computations

The very fine-grain parallelism of neural networks uses many information exchanges, thus it better fits hardware implementations than conventional processors [11]. Configurable hardware devices such as FPGAs (Field Programmable Gate Arrays) offer a

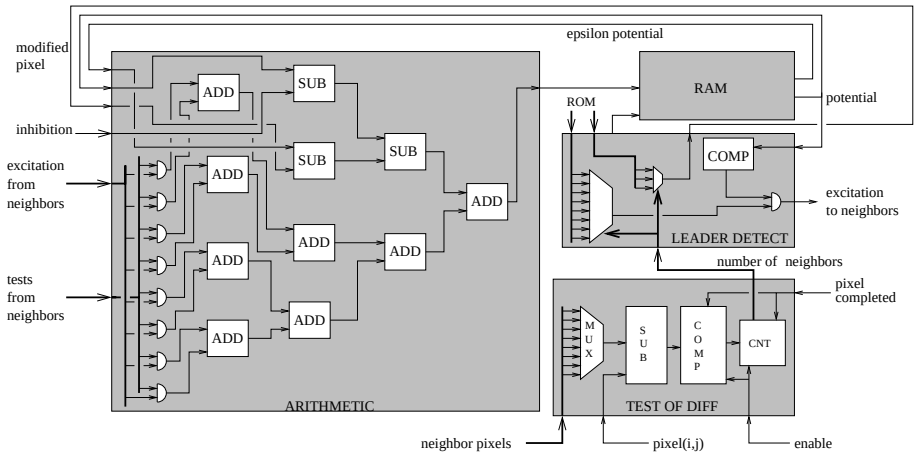

Fig. 2: Architecture of a single neuron

cheap compromise between the hardware efficiency of digital ASICs and the flexibility of a simple software-like handling.

Most work on digital neural network implementations uses digital words to implement classical neural models where all interactions are represented by the mean firing rate of the neurons. On the other hand, recent research on neuroscience has developed spiking neural models that are much closely coupled with action potential or spikes communication and even more tightly related to the brain abilities than classical neural models. Spiking neural networks appear as well suited to be implemented in digital logic, as spikes are inherently binary [12]. Nevertheless, digital implementations of large spiking networks are a real challenge, that must be adressed by means of specific low-area technological choices.

3.2 General architecture

Due to the high computational requirements of LEGION, the highly dense interconnectivity and the area greedy operators, a serial hardware implementation on massively fine grain parallel structures was chosen. Analysis and experimental results were carried out to determine the best wordlength in terms of performance and cost. For the FPGA LEGION implementation, serial arithmetic with a 12-bit fixed point representation was chosen in order to favor a high density of neurons per silicon area while preserving accuracy and performance of the model. The pixels of the input image were coded in 8 bits for gray level image.

The general architecture for the LEGION neuron model is shown in the simplified block diagram of figure 2. All neurons used in the network are architecturally identical although they may be functionally different on the image boundaries. The proposed hardware neuron model consists of four main modules: a test of difference, arithmetic, a RAM and a leader detector module. The key idea for the conception of the proposed

neuron architecture relies on the association of basic operators to specific arithmetical computations of equation 3, the use of some previously stored constants to avoid hardware complexity of nonlinear operators and in the transformation of the differential equation into an equation of differences using Euler's method.

Pixel Difference Test Module: The difference test module determines the number of neighbors that fulfill the requirements of difference test. It is essentially constituted by a multiplexer, a subtractor, a counter and a comparator optimized for serial arithmetic.

The difference test is applied between the pixels of two neighbor neurons, the central pixel and the current pixel selected by the multiplexer. The absolute difference of these values is compared to a constant threshold, 16 for the current implementation (any other power of 2 value would lead to a similar architecture). If the absolute difference is below the threshold, then pixels satisfy the test of difference. The module operates sequentially with all its neighbors and then it sends the number of neighbors that satisfy the test to the leader module for further utilization.

Arithmetic Module: This module performs the arithmetical operations that define the dynamics of the neuron model, as stated in equation 3. The module is composed of a tree of serial adders and subtractors, and AND gates. The arithmetic module receives excitation signals from its neighbors, the global inhibition, and the previous internal potential stored in the RAM module. An integration step $\epsilon = \frac{1}{4}$ is used to solve the difference equation through the Euler's method. To avoid multipliers, the potential and ϵ times the potential are simultaneously provided by the RAM module using an appropriated addressing scheme.

RAM Module: This module is basically constituted by a 16x1 dual port memory RAM that stores the neuron internal potential produced by the arithmetic module on each clock cycle as shown in figure 5(a). The two bus addresses are driven by two global counters, delayed 4 clock cycles one of each other, to provide the current neuron potential and the potential scaled with the integration step ϵ.

Leader Detector and Excitation Module: The leader detector module determines the modified value of a pixel associated to an oscillator, and generates the excitation potential contribution at a given time, and the excitation spike. Three possible values for the modified pixel may be assigned (see section 2.2): $I_L = 1.25$, $I_N = 0.95$, and 0. Also, the excitation potential contribution depends on the number of neighbors satisfying the difference test. The module computes this strength, selecting values previously stored in an internal memory in order to avoid multipliers and divisions. The module generates an excitation pulse if the internal potential is greater than the unit.

4 FPGA Implementation Results

The proposed neuron hardware model and the LEGION oscillator network have been successfully modeled in VHDL and implemented in a FPGA device. The VHDL model

of LEGION network is configurable and can be built up for different gray level image sizes. The synthesis results for the neuron hardware model and a 16x16 configuration of LEGION network targeted to a Xilinx Virtex XC2V1500FF896-4 device are: 7678/7680 (99%) used slices, 12295/15360 (83%) used LUTs, and 5512/15360 (35%) used flip-flops. The estimated maximum clock frequency is 50 MHz.

The massively parallel and pipelined implementation appears as highly attractive for FPGA implementation. It is particularly efficient from the device utilization point of view. A testbench was developed to provide stimulus to the architecture from a previously captured image. The produced results were compared to the software implementation of LEGION providing satisfactory results in the tests performed by the hardware model (functional and timing simulations).

5 Conclusion

This paper presents a massively distributed digital implementation of a spiking neural network for image segmentation based on the time oscillatory correlation theory. The results show that efficient implementations of large neural networks can be achieved through the use of specialized datapaths with serial arithmetic.

Our implementation allows to handle image segmentation with low area cost in most up to date FPGA technology. The modularity, scalability and high efficient implementation would be beneficial in an embedded system environment for visual perception. The implementation presented in this paper brings new perspectives in the digital hardware implementation of spiking neural models and goes forward in the analysis and design of digital VLSI neuromorphic circuits.

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