A COMPACT 30GIPS REAL-TIME VISION SYSTEM RVS-2

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ABSTRACT

This paper describes the Real-Time Vision System (RVS-2) which shows quite high performance for low-level image processing while it is implemented in compact size. The RVS-2 consists of a IMAP board, a video board and a host workstation and the IMAP board consists of eight highly integrated IMAP LSIs and a dedicated control LSI(RVSC). The IMAP chip integrates 2Mbytes image memory and 64 processor elements which operate in SIMD manner. The RVSC chip has functions to carry out global data operations efficiently without any interactions with the host workstation, as well as the functions for providing a instruction stream to IMAP chips. The peak performance of RVS-2 is 30GIPS and most of basic image processing are carried out within about 0.1 to 0.7ms, which is about 50 to 300 times faster than the video frame rate.

1. INTRODUCTION

Vision systems have been getting more and more important as needs are increasing for real-time applications such as vision-based computer interfaces or surveillance systems. It is desired that the processing system should have very high performance for low-level image processing in order to obtain reliable and stable results. It is also required that the system should be implemented in compact size so as to be used in many environments and to expand application fields. Many image processing algorithms can be executed efficiently by parallel computation on SIMD(Single Instruction stream Multiple Data stream) architecture[1][2]. One of its problems is the data transfer bandwidth between processors and a image memory. SIMD processors require a large amount of image data at a time, and this makes the total system complex and large. In order to resolve this problem and meet the two requirements mentioned above, the authors have previously proposed Integrated Memory Array Processor (IMAP) architecture and a Real-Time Vision System (RVS-1) using prototype IMAP LSIs[3][4], where a one-dimensional processor array is embedded in a video RAM so that data transfer bottleneck between the image memory and the processor array is avoided. While the RVS-1 has proved that the IMAP architecture shows good processing performance for data parallel algorithms, it is desired to be improved in size as well as in global data processing performance.

This paper describes a highly integrated IMAP LSI in section 2 and a compact real-time vision system RVS-2 in section 3. The performance of image processing is also discussed in section 4.

2. A HIGHLY INTEGRATED IMAP LSI

The authors have developed a highly integrated IMAP LSI, which consists of 2Mbit image memory and a one-dimensional array of 64 processing elements (PE) as shown in Fig.1[5]. IMAP memory part can be accessed from outside of the chip via a random access port and two serial access ports, just like a VRAM. Video images are to be input and output via the serial access ports. PE array applies image processing operations to images stored in IMAP memory. All PEs execute a single instruction stream, which is given from outside, in SIMD manner.

Figure 2 shows one PE configuration. A 4K bytes column of image memory is assigned to each PE. Each processing element has an 8 bit architecture, and it consists of ALU/Shifter, 12 general registers, a memory data register, an address register and a mask register. The content in a mask register enables to change the operations based on a condition locally calculated by each PE in SIMD execution.

Since a row of image data can be transferred at once

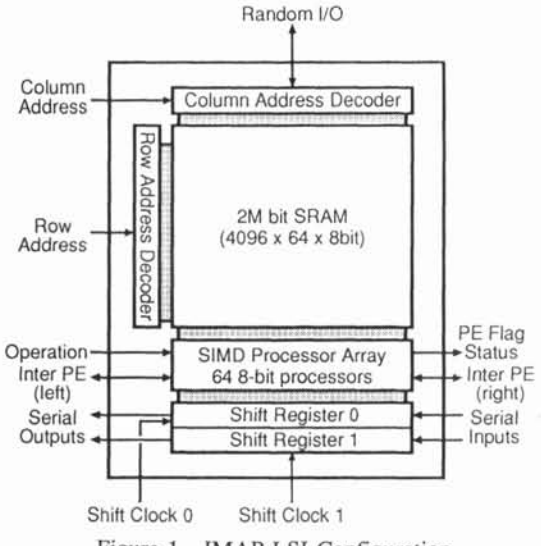

Figure 1 IMAP LSI Configuration

between the data registers and the image memory, very wide bandwidth required for high-speed low-level image processing is obtained. The address register is used to make an indexed addressing access. The 4k byte memory assigned to each PE is divided logically into 16 of 256byte-block, and an indirect access, in which each PE can access different memory locations, can be carried out within each blocks. Provided with the memory data register and the address register, the memory read/write operation and computation by ALU/Shifter can be executed simultaneously.

Figure 3 shows chip layout for the IMAP LSI. Specifications for the IMAP LSI is shown in Table 1. Eleven million transistors are integrated in 15.1mm by 15.6mm die size. The peak performance is 3.84GIPS at 40MHz operation clock.

3. REAL-TIME VISION SYSTEM RVS-2

IMAP architecture adopts one dimensional PE array so as to allow us to build a large size of IMAP system easily. By using eight IMAP LSIs, the authors have developed Real-Time Vision System RVS-2, which has

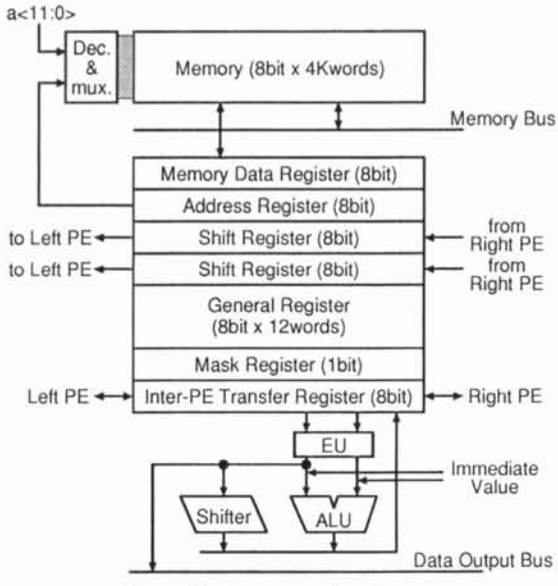

Figure 2 Processor Configuration

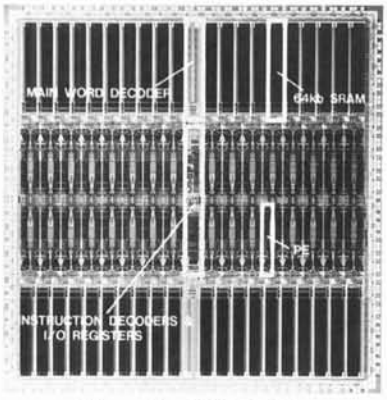

Figure 3 IMAP LSI

512 PEs and 2M bytes on-chip image memory. Figure 4 shows the configuration of RVS-2. RVS-2 consists of a IMAP board, a video board and a host workstation board, and they are connected via VME bus. Color images are directly transferred among the video board and IMAP image memory via the two shift registers, where one of them is used for the intensity component and the other is used for the color component.

The execution of IMAP program should be synchronized to image input timing. Six kinds of interrupt signals are sent from the video board to the controller on the IMAP board, i.e., a) odd/even first-line interrupt, b) odd/even line interrupt, c) odd/even frame interrupt. The controller invokes an appropriate program which copies input image or output image between the shift registers and the image memory, or a program which carries out main processing tasks, according to the kind of interrupt signals. The program to be activated is fully programmable for users.

Figure 5 shows the configuration of the IMAP board and an external view of the IMAP board is shown in Figure 6. The IMAP board consists of eight IMAP LSIs, controller LSI (RVSC), a program memory, a data memory and VME-bus interface. The eight IMAP chips are connected in serial on the daughter-board, and other chips are on the main-board.

The main function of the RVSC is sequencing program execution of IMAP chips. Receiving video interrupt signals, RVSC activates a specified program and generates an instruction stream to the IMAP chips which is stored in the program memory. The program code also includes instruction fields for the RVSC. The flag status of the IMAP chips can be referred by the RVSC. RVSC uses them to change the program sequence such as a conditional branch or a conditional subroutine call. RVSC has also a communication mechanism with the host workstation by using interrupts. When host workstation writes to the interrupt register, RVSC treats it as a interrupt signal and invoke a specified program. RVSC also has an instruction to generate a interrupt signal to the host workstation (VME bus). The interrupt mechanism of RVSC enables to change a program sequence dynamically according to the results by IMAP or host workstation computation, and makes it easy to do

Table 1 IMAP LSI Specifications

Process Technology	$0.55\mu m$ BiCMOS, double-layer metal
Chip Size	15.1mm × 15.6mm
Number of Transistors	11 million
Clock Rate	Processor: 40MHz, Memory: 80MHz
Package	208 pin PGA
Power Supply	3.3V
Maximum Power Dissipation	4.0W
Average Power Dissipation	~2.0W
Peak Performance	3.84GIPS (8 bit)

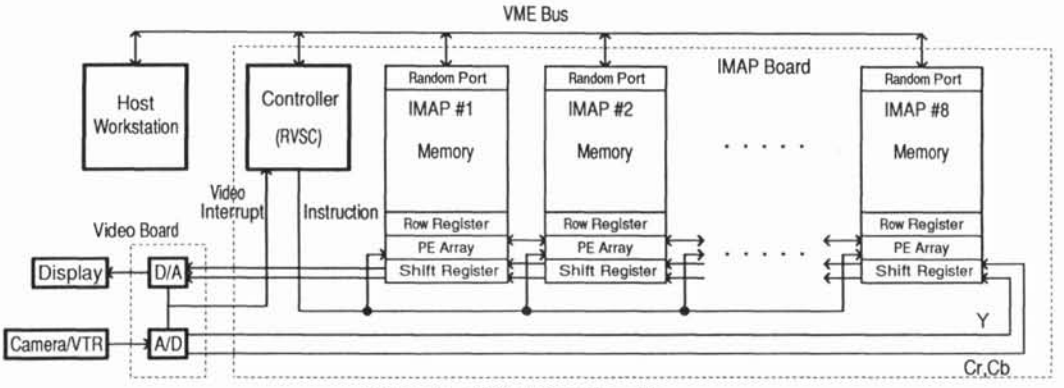

Figure 4 RVS-2 Configuration

an asynchronous and parallel programming among IMAP and host workstation.

The second function of the RVSC is arbitrating the memory access conflicts from the host workstation, PE array of IMAP and RVSC itself. The image memory and the data memory can be accessed from the system bus asynchronously to the internal PE operations or to the RVSC operations. In case of the image memory access from the system bus conflicts with that from internal PEs or RVSC, or in case of the data memory access from the system bus conflicts with that from RVSC, RVSC arbitrates them so as to make the overhead minimum.

The third function of the RVSC is processing of the global data over the PEs. In order to make the entire image processing fast, not only the performance of pixel or local operations by every PEs, but also the performance of the global data operation should be efficient, such as position detection by using location of PEs which detect specific features or integrating the results of PEs in order to feedback processing parameters. RVSC has following functions to meet this requirements.

1) Its own 16bit processor and external data memory,
2) Selective access to the status or register data from an arbitrary PE of the IMAP chips,
3) Data broadcasting to IMAP chips.

The selective access function is mentioned in detail here. Since IMAP has instructions to output register data in a PE specified by a PE number or the activeness of the mask register, RVSC can access register data on any specific PE. Furthermore, a unique operation is supported to make it efficient to read data sequentially from plural PEs detecting specific conditions, which is similar mechanism to content addressable memory (CAM). First, each PE satisfying conditions sets the mask register, and then reset the mask register except at a PE at the left-most or right-most within each chip. The IMAP chips also output a presence of active mask registers. Next, RVSC selects the global left-most or right-most PE according to the presence bit outputs from all IMAP chips, and read data of the detected PE if necessary. After resetting the mask register of the PE which is read by RVSC, the same procedure is repeated until no mask register is active. By this procedure, RVSC can efficiently gather data sparsely dispersed over the PEs, and calculate the size of a segmented area obtained by PE processing, because the number of execution steps is constant, while it would be proportional to the size of the segmented area if without this mechanism. By using the selective access mechanism and the RVSC processor mentioned above, RVSC can execute global operations efficiently without any interactions with the host workstation.

Figure 7 shows an system external view of the RVS-2. RVS-2 cabinet is at the left side of the large display for the host workstation. Two small displays are for the video input/output monitoring. Peak performance of RVS-2 is 30GIPS, including the memory access operation which is carried out in parallel to the ALU operation.

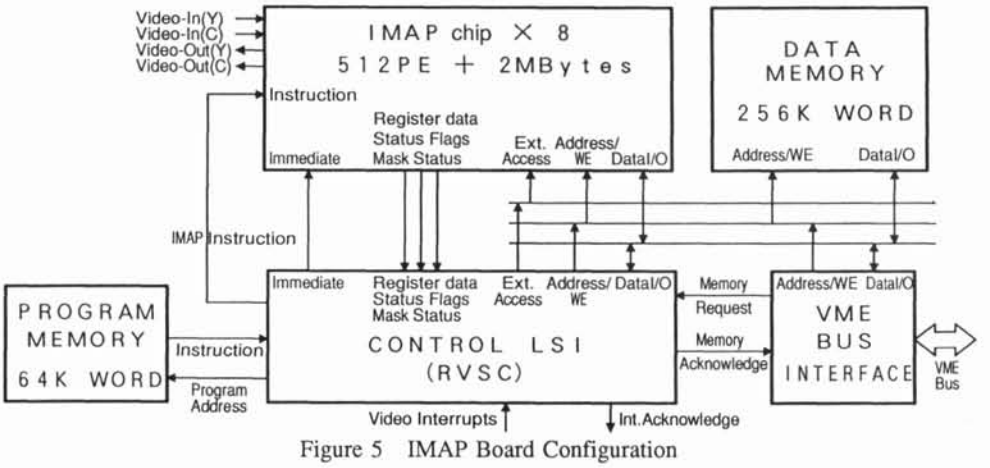

Figure 5 IMAP Board Configuration

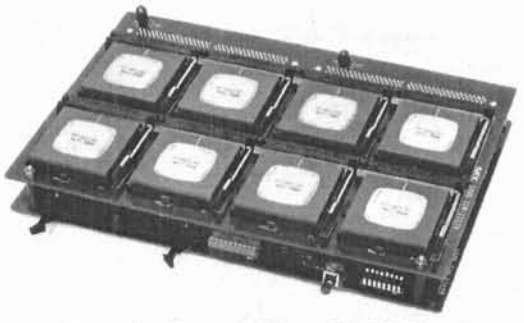

Figure 6 External View of IMAP Board

4. IMAGE PROCESSING PERFORMANCE

Table 2 shows examples of basic image processing performances. All algorithms except hough transform are applied to 512 by 512 pixel, 8bit images. The performance of hough transform is the case when 1% pixels of a image, i.e. about 2.5k pixels, are processed. The transfer rate column shows the data transfer rate in Gbytes per second between the image memory and the PE array during the execution.

The image subtraction, background detection and moving area detection are examples of operations using two images. RVS-2 can carry out these memory-access intensive processing rapidly without suffering from memory access bottleneck. Data transfer rate attains to 4 to 8 Gbytes per second in these operations.

Histogram calculation and Hough transform are examples of another memory-access intensive operations, where the memory address to be accessed depends on the input image and is not able to be scheduled in advance. Since each PE of RVS-2 has indirect memory access, this operation is carried out efficiently at each PE in parallel. Seventeen percent of the total instructions are indirect memory access in hough transform, for example.

Filtering operations are often used in low-level image operations, and they are carried out in about 0.4 to 0.7ms. Since most of basic low-level image processing are carried out in 0.1 to 0.7ms, and they are 50 to 300 times faster than the video frame rate, RVS-2 can carry out in real-time much more complex processing where tens of basic image processing are combined.

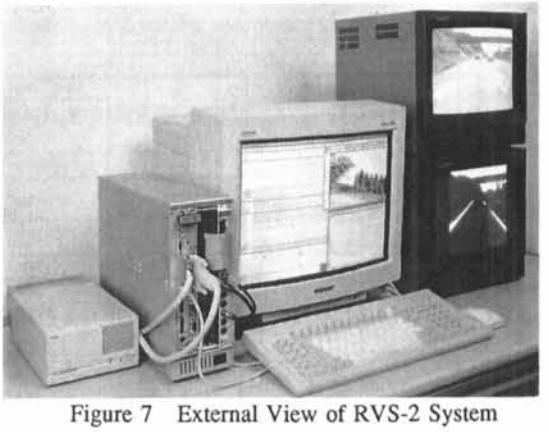

Figure 7 External View of RVS-2 System

CONCLUSION

A highly integrated IMAP LSI, a one-board type Real-Time Vision System RVS-2 and its performance have been presented. The RVS-2 has shown high performance for low-level image processing which is 50 to 300 times faster speed than the video frame rate. This high performance and compactness must make the real-time image processing practical and it will help to extend the application fields.

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Table 2 Examples of Image Processing Performances

Algorithm	Execution Time (ms)	Ratio to Video Rate	Transfer Rate(GB/s)
Intensity Projection	0.064	516	4.0
Image Subtraction	0.10	320	7.7
Background Detection	0.18	184	4.3
Moving Area Detection	0.33	100	3.1
3x3 Averaging Filter	0.42	78	1.2
3x3 Laplacian Filter	0.42	78	1.2
3x3 Range Filter	0.66	50	0.79
Sharpening	0.41	81	1.3
Histogram	0.73	45	3.9
Hough Transform	2.0	16	3.2