Editorial
Real-Time Implementation of VVC Standard for Consumer Electronic Devices

I. Summary of the Special Section

WE ARE pleased to present this Special Issue on this timely and important topic. The next generation ISO/IEC MPEG and ITU-T VCEG video coding standard called versatile video coding (VVC) was released in July 2020 [1], [2]. VVC includes some coding tools enabling an important coding gains estimated to 35% of bit-rate reductions for the same quality in terms of peak signal to noise ration (PSNR) compared with high efficiency video coding (HEVC) in random access (RA) coding configurations. For all intra (AI) configuration the improvement is a bit lower and estimated in a 25%. Moreover, subjective comparison recently conducted between HEVC and the VVC reference software, has shown that this gain is even higher reaching up to 50% of bit-rate reduction for the same perceived quality [3], [4]. Unfortunately the coding gain is associated to an increase in the algorithm complexity at both encoder and decoder sides. The VVC encoder is estimated to be 8× more complex than HEVC in RA configuration and 25×. The complexity of the VVC decoder is doubled compared to HEVC. Therefore, complexity reduction and optimization of VVC is critical to design of software and hardware real time VVC codecs for successful deployment on video consumer devices including among others TVs, mobile phones and tablets.

To enable real time implementations of the VVC codec in consumer electronic products, significant efforts should be dedicated to reach real time performance at high resolution videos (4K and 8K) or with applications with very limited resources (memory/battery). This special issue addresses real time software and hardware implementations of the VVC encoder and decoder on consumer electronic devices. Topics of interest in this special section include (but are not limited to): 1) Real time software implementations of VVC codec for consumer electronic devices. 2) Hardware implementations of VVC codec on FPGA and ASIC devices. 3) Real time Implementations of VVC quality enhancement and super resolution algorithms. 4) Machine learning based complexity reduction of the VVC encoder. 5) Low level optimizations (SIMD) and high level parallelism for VVC codecs on mobile devices. 6) Energy estimation models of VVC codecs on mobile platforms. 7) VVC-based live video broadcast and streaming OTT, DASH, CMAF. 8) VVC coding tools complexity and coding performance analysis.

The papers accepted for publication in this special issue are briefly described, for more details, the reader may refer to the corresponding paper [5]–[9]. These papers address different aspects to design real time VVC encoders and decoders from tools optimizations [5], [6] for software and hardware VVC decoders, complexity reduction of VVC encoder [7], [9] to the design of real time software VVC encoders [8].

VVC has introduced two transforms, the multiple transform selection (MTS) as the primary transform and the low frequency non-separable transform (LFNST) as the secondary one. At the encoder side, MTS selects horizontal and vertical transforms among three trigonometrical transforms (discrete cosine transform (DCT) type II, discrete sine transform (DST) type VII and DCT type VIII). Unfortunately, the DST-VII does not have efficient fast algorithmic implementation. This lack of optimized implementations decrease the performance of both, encoder and decoder.

Additionally in terms of resources needed for the implementations, the use of the three transforms MTS increases the memory usage because it is needed to store more coefficients. Authors in [5] proposed an efficient approximation of the DST-VII based on the DCT-II and adjustment stage. This approximation has been solved as an integer optimization problem. The target of this approximation is to minimize the error and the orthogonality of the approximated DST-VII transform with constraints of the adjustment stage. The sparse nonlinear optimizer (SNOPT) solver with an additional relaxation constraint is used to solve the problem and find the best sparse adjustment band matrices for different transform sizes. The DCT-VIII is calculated from the approximate DST-VII with additional processing operations involving only data reordering and sign changes. This approximation provides a reduction in memory usage and arithmetic operations. This approach has not impact in the video codec performance compared with the VVC reference software. These approximations make this implementation suitable for energy-efficient VVC encoders and decoders deployed on consumer electronic applications.

Adaptive loop filter (ALF) is another in-loop filter tool introduced in VVC that increases both the codec complexity and the memory usage. Authors [6] in tackled these concerns regarding the design of an efficient hardware implementation

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of this filter. The percentage of computational load of the ALF filter over the global codec is very high so the optimization of this tool is mandatory to achieve real-time performance. This paper proposes an efficient hardware implementation of the ALF filter for a VVC. The optimization is based on a novel scanning order between Luma and Chroma components that reduces significantly the ALF memory used. The proposed design reduces the area and allows the use of an unified hardware for the ALF tool. The proposed architecture uses 26 multipliers with a fixed throughput of 2 pixels/cycle and fixed latency. This design operates at 600 MHz frequency enabling to decode on ASIC platform a 4K video at 30 fps using 4:2:2 chroma format.

Complexity reduction of an intra VVC encoder is tackled in [7]. This paper thoroughly analyzes the performance and complexity of all intra coding tools in VVC and identify the most intensive computational modules. The complexity reduction proposed in based on downsampling and upsampling the video frames. The downsampling reduces the resolution of an original video in both directions. Later, neural network used in super-resolution applications is used to increase the resolution of the reconstructed frames. The obtained results demonstrate a high reduction in the encoder complexity with an acceptable video quality.

Wieckowski *et al.* in [8] analyzed the encoding complexity increase of VVC over HEVC. Implementation-based aspects are applied including among other low-level software optimizations. A new algorithm is proposed to limit the encoder search space and some empirical measures are conducted in order to demonstrate the interest of the proposal. Based on this measure, authors compare the search space of HEVC test model (HM) and VVC test model (VTM), but also of the open encoder implementation called *VVenC*. The research demonstrate the interest to reduce the search space and its impact on compression performance. The results demonstrate that the search space proposed in VTM can be limited including early termination strategies or disabling some coding tools.

Viitanen *et al.* in [9] adapted a HEVC intra encoder development previously to generate a new VVC encoder for intra sequences. The VVC-compliant encoder includes some of the encoding modes defined in the new standard not available in HEVC. This approach allow to use an optimized open encoder before starting the development from scratch. Several sequences has been encoded and the performance of the HEVC encoder has been compared with the VVC encoder. The impact of each added coding tool is independently evaluated in relation to the VVC baseline implementation. Finally, the proposed solution is compared with other previously published implementations.

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REFERENCES

[1] B. Bross *et al.*, "Overview of the versatile video coding (VVC) standard and its applications," *IEEE Trans. Circuits Syst. Video Technol.*, vol. 31, no. 10, pp. 3736–3764, Oct. 2021.

[2] W. Hamidouche *et al.*, "Versatile video coding standard: A review from coding tools to consumers deployment," 2021, *arXiv:2106.14245*.

[3] C. Bonnineau, W. Hamidouche, J. Fournier, N. Sidaty, J.-F. Travers, and O. Déforges, "Perceptual quality assessment of HEVC and VVC standards for 8K video," *IEEE Trans. Broadcast.*, vol. 68, no. 1, pp. 246–253, Mar. 2022.

[4] N. Sidaty, W. Hamidouche, O. Déforges, P. Philippe, and J. Fournier, "Compression performance of the versatile video coding: HD and UHD visual quality monitoring," in *Proc. Pict. Coding Symp. (PCS)*, 2019, pp. 1–5.

[5] W. Hamidouche, P. Philippe, S. A. Fezza, M. Haddou, F. Pescador, and D. Menard, "Hardware-friendly multiple transform selection module for the VVC standard," *IEEE Trans. Consum. Electron.*, early access, Mar. 30, 2022, doi: 10.1109/TCE.2022.3163345.

[6] I. Farhat, W. Hamidouche, A. Grill, D. Ménard, and O. Déforges, "Adaptive loop filter hardware design for 4K ASIC VVC decoders," *IEEE Trans. Consum. Electron.*, early access, Jan. 25, 2022, doi: 10.1109/TCE.2022.3146272.

[7] K. Choi, T. V. Le, Y. Choi, and J. Y. Lee, "Low-complexity intra coding in versatile video coding," *IEEE Trans. Consum. Electron.*, early access, Jan. 24, 2022, doi: 10.1109/TCE.2022.3145397.

[8] A. Wieckowski, J. Brandenburg, B. Bross, and D. Marpe, "VVC search space analysis including an open, optimized implementation," *IEEE Trans. Consum. Electron.*, early access, Feb. 3, 2022, doi: 10.1109/TCE.2022.3148813.

[9] M. Viitanen, J. Sainio, A. Mercat, A. Lemmetti, and J. Vanne, "From HEVC to VVC: The first development steps of a practical intra video encoder," *IEEE Trans. Consum. Electron.*, early access, Jan. 24, 2022, doi: 10.1109/TCE.2022.3146016.

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