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Designs of Two Quadruple-Node-Upset Self-Recoverable Latches for Highly Robust Computing in Harsh Radiation Environments

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This article proposes two quadruple node upset (QNU) recoverable latches, namely *QNU-recoverable and high-impedance-state (HIS)-insensitive latch* (QRHIL) and QRHIL-LC (low-cost version of the QRHIL), for highly robust computing in harsh radiation environments. First, the QRHIL that mainly consists of a 5×5 looped C-element matrix is proposed. Then, to reduce overhead, the QRHIL-LC that mainly uses 24 interlocking C-elements is proposed. Both latches can self-recover from any QNU, while the QRHIL-LC has a low cost compared to the QRHIL. Simulation waveforms show the QNU-recoverability of the proposed QRHIL and QRHIL-LC latches. Moreover, compared with the QRHIL latch, the QRHIL-LC can approximately save power dissipation by 16% and silicon area by 5%.

I. INTRODUCTION

With the continuous scaling of nano-scale CMOS, transistor sizes become smaller and smaller, making the critical charge of circuit nodes smaller and smaller so that the nodes become severely susceptive to soft errors, such as *single node upsets* (*SNUs*) and *multiple node upsets* [1]. When a particle such as neutron and proton with sufficient energy hits the sensitive area of a CMOS transistor [2], [3], an SNU can be detected at the drain of the impacted transistor. What's more, the aggressive reduction of transistor sizes can help the hit of a radiative particle to cause multiple-node charge collection to affect two, three, or even four closer nodes, leading to a *double node upset* (*DNU*), a *triple node upset* (*TNU*), or a *quadruple node upset* (*QNU*), respectively [4], [5], [6]. SNUs, DNUs, TNUs as well as QNUs are major examples of soft errors.

Yan et al. [4] indicate that to accurately calculate the QNU occurrence probability is very difficult since six or more types of parameters need to be provided. Thus, we qualitatively introduce the requirement of designs with QNU-recoverability. Because of charge-sharing, a QNU can be induced by the hit of a single high-energy radiative particle in harsh radiation environments [4]. The detailed reason is that, if an advanced circuit is greatly integrated and fabricated with an extremely small technology node like 7 nm, more transistors and nodes would be much closer, so that the probability of an event like that will severely increase.

To protect against soft errors for storage elements, researchers in recent years have proposed many designs of SRAM cells [7], [8], *flip-flops* [1], [9], [10], [11] as well as latches [4], [5], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31]. Clearly, among the existing latch circuits, there are some SNU-mitigated ones [12], [13], [14], there are some both SNU- and DNU-mitigated ones [15], [16], [17], [18], [19], [25], [26], [27], [28], [29], and there are also some SNU, DNU, and TNU simultaneously mitigated ones [20], [21], [22], [23], [24]. As far as we know, there are only a few latches that are hardened against SNUs, DNUs, TNUs, and QNUs, simultaneously [4], [5], [24], [30], [31]. However, these latches cannot self-recover from QNUs or suffer from large overhead in terms of power, delay, and/or area. In other words, these latch designs can provide correct output values when they suffer from a QNU, but many

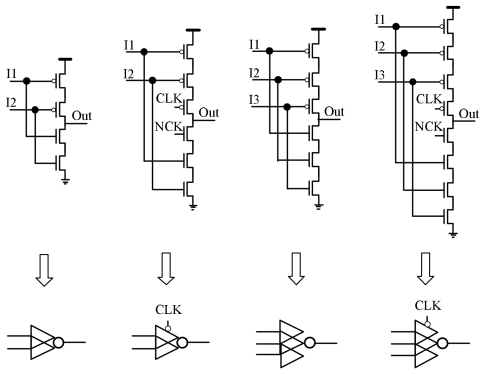

Fig. 1. C-element structures. (a) Two-input C-element. (b) Clock-gating based two-input C-element. (c) Three-input C-element. (d) Clock-gating based three-input C-element.

nodes in these designs even cannot recover from a DNU. Hence, node upsets can be accumulated especially over a long period of time in hold/standby mode. Note that, among the SNU-mitigated latch designs, only the designs in [12], [13], [14] can provide recovery from any SNU. Among the DNU-mitigated latch designs, only the designs in [18], [19], [26], [28], [29] can provide recovery from any DNU. Among the TNU-mitigated latch designs, only the *triple-node-upset self-recoverable latch* (*TNURL*) [23] and *input-split-C-element-based TNU-resilient latch* (*ISC-TRL*) [24] can provide recovery from any TNU. Among the QNU-mitigated latch designs, although the *input-split-C-element-based QNU-resilient latch* (*ISC-QRL*) [24] is tried to recover from any QNU, we found some counter examples so that the ISC-QRL cannot provide complete QNU self-recoverability. Therefore, as far as we know, no latch circuit can provide complete QNU-recovery except the latch proposed in the preliminary conference version of this article [30]. However, the solution in [30] consumes a large overhead especially in terms of area and power. This motivates us to propose a QNU-recoverable latch that has a low cost.

The rest of the article is introduced as follows. Section II introduces existing latches. Sections III and IV describe the structure, operations, and simulations for the proposed latches, respectively. Section V presents extensive comparison results of alternative latches, finally, Section VI concludes the article.

II. EXISTING LATCHES

C-elements (*CEs*) are extensively employed as important components for radiation-hardened latch designs. Fig. 1 presents the structures of some CEs, such as the two-input and three-input ones as well as the *clock-gating* (*CG*) based two-input and three-input ones so that a four-input one can be easily constructed. A CE has the same functioning as a traditional inverter when its inputs receive the same value state; its output can temporally keep its original value due to capacitances when its input value states change to be different. Note that a CG-based CE is controllable through the *system clock* (*CLK*) as well as the *negative system clock* (*NCK*), simultaneously.

Fig. 2 presents the structures of existing hardened latch designs, such as *highly robust and low cost* (*HRLC*) [12], *dual interlocked storage cell* (*DICE*) [13], *self-healing, high performance and low-cost radiation hardened* (*SHLR*) [14], *high performance, low-cost, DNU tolerant latch-enhanced version* (*HLDTL-EV*) [15], *dual input inverter radiation tolerant* (*DIRT*) [16], *radiation hardened* (*RH*) [17], *DNU resilient latch* (*DNURL*) [18], *double node upset self-healing* (*DNUSH*) [19], *low cost and TNU tolerant* (*LCTNUT*) [20], *TNU-hardened latch* (*TNUHL*) [21], TNURL latch [23], and *QNU-tolerant latch (QNUTL)* [4]. Note that, the switches in Fig. 2 represent the *transmission gates* (*TGs*). For example, each TG marked with NCK indicates that the gate terminal of the pMOS transistor is connected with NCK and the gate terminal of the nMOS transistor is connected with CLK. This feature applies to all latch designs in this article.

As shown in Fig. 2(a), the HRLC latch mainly comprises two parts. The upper part is comprised of four circularly linked modified inverters (the input and output are coupled), and the lower part is comprised of a Schmitt-trigger marked with S, two inverters as well as a two-input CE, making the HRLC latch SNU-recoverable. As shown in Fig. 2(b), the DICE latch mainly comprises four interlocked input-split inverters. The DICE latch can provide recovery from any possible SNU. As shown in Fig. 2(c), the SHLR latch mainly comprises two CG-based two-input CEs and three input-split inverters to form interlocked feedback loops so that it can provide complete SNU-recoverability. However, these latches cannot tolerate DNUs, since each of these latches has at least a node pair that cannot provide tolerance against a DNU.

As shown in Fig. 2(d), the HLDTL-EV latch mainly comprises an *SNU resilient cell* (*SRC*) and an additional part at the bottom. The SRC comprises two inverters and three 2-input CEs to provide complete SNU tolerance as well as partial DNU tolerance. The additional part can provide extra DNU tolerance that cannot be achieved by the SRC. The latch can tolerate any DNU. As shown in Fig. 2(e), the DIRT latch mainly comprises two levels of input-split inverters. In each level, there are six input-split inverters. The latch can provide DNU tolerance. As shown in Fig. 2(f), the RH latch mainly comprises an extended DICE and a CG-based CE. The extended DICE cell can reduce sensitive nodes and transistors so as to ignore insensitive DNUs. The latch can tolerate any DNU. As shown in Fig. 2(g), the DNURL latch mainly comprises three interlocked SRCs so as to provide complete DNU recoverability. As shown in Fig. 2(h), the DNUSH latch comprises two symmetrical parts (top and bottom) to provide complete DNU recoverability. Indeed, the HLDTL-EV, DIRT, RH, DNURL, and DNUSH latches are effectively DNU hardened. However, they cannot completely tolerate TNUs and cannot completely self-recover from TNUs, since at least one list of three nodes cannot tolerate a TNU for any of them.

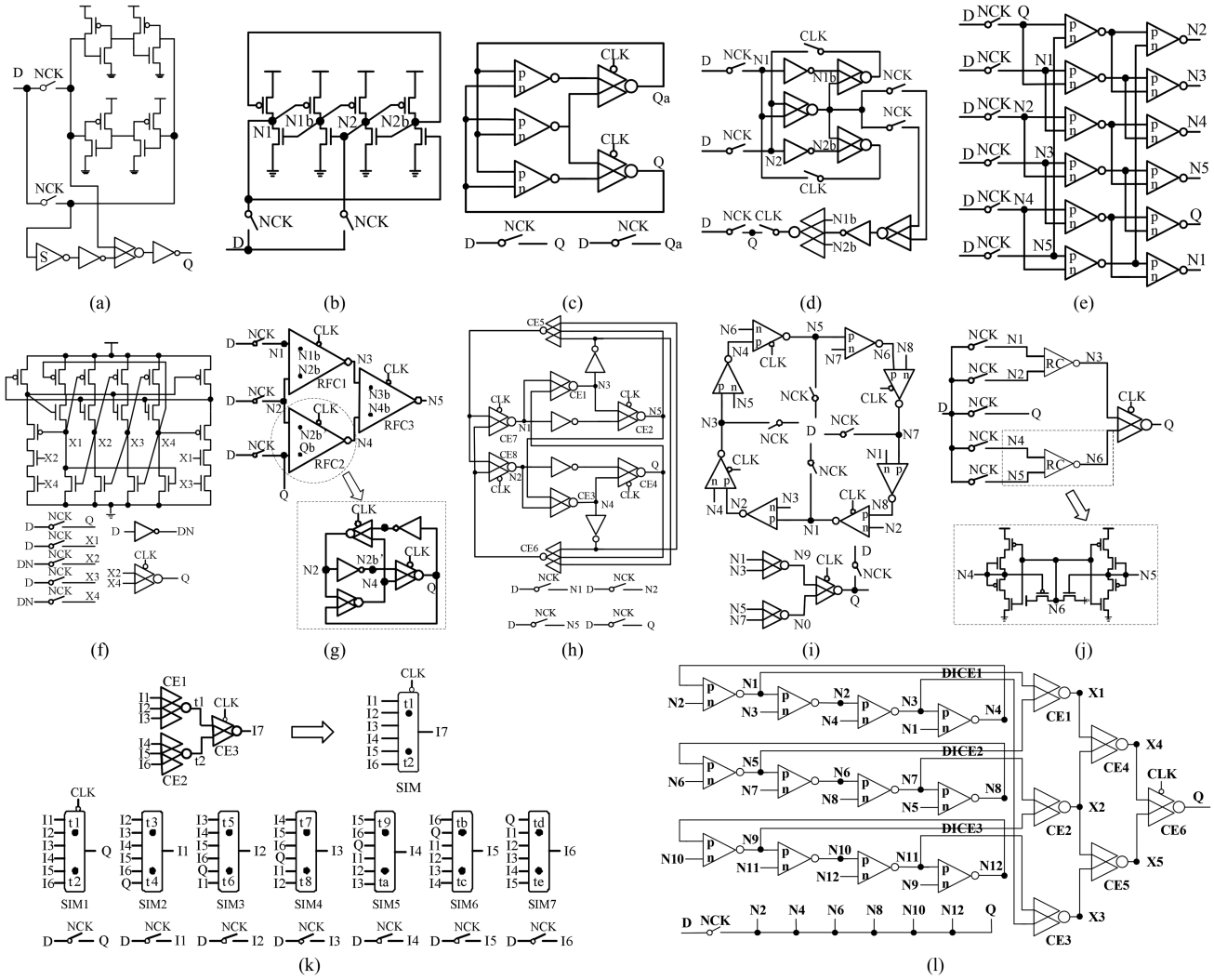

Fig. 2. Schematics of existing hardened latches. (a) HRLC [12]. (b) DICE [13]. (c) SHLR [14]. (d) HLDTL-EV [15]. (e) DIRT [16]. (f) RH [17]. (g) DNURL [18]. (h) DNUSH [19]. (i) LCTNUT [20]. (j) TNUHL [21]. (k) TNURL [23]. (l) QNUTL [4].

As shown in Fig. 2(i), the LCTNUT latch mainly comprises a *storage module* (*SM*) and a dual-level *soft-error-interceptive module* (*SIM*). The LCTNUT latch can provide complete TNU tolerance due to error-interception of the SIM. As shown in Fig. 2(j), the TNUHL latch mainly comprises two *restorer circuit* (*RC*) cells and a CG-based two-input CE so as to provide TNU tolerance. However, according to our simulations, we found that the TNUHL latch cannot provide complete DNU/TNU tolerance. As shown in Fig. 2(k), the TNURL latch mainly comprises seven SIMs to provide TNU recoverability. However, these latches cannot provide QNU tolerance, since at least one list of four nodes cannot tolerate a QNU for any of them. As shown in Fig. 2(l), the QNUTL latch mainly comprises three DICEs and a triple-level SIM. The QNUTL latch can provide QNU tolerance but cannot provide complete QNU recoverability. Note that a latch is *high-impedance-state* (*HIS*)-insensitive if it can recover from node upsets because the inputs of any CE in the latch cannot keep different values for a long period of time.

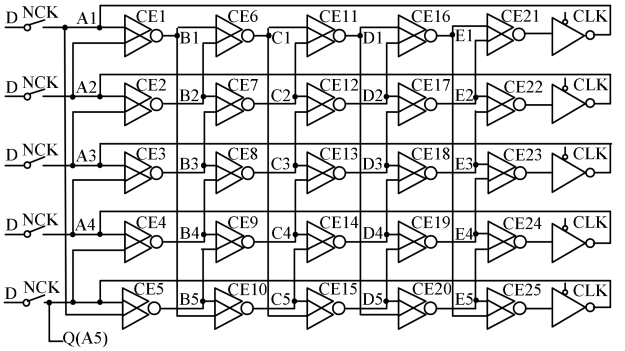

Fig. 3. Schematic of the proposed QRHIL latch.

III. PROPOSED QRHIL LATCH DESIGN

A. Structure and Working Flow

Fig. 3 shows the proposed *QNU-recoverable and HIS-insensitive latch* (*QRHIL*). The latch comprises five TGs marked with NCK, a CE matrix constructed from 25

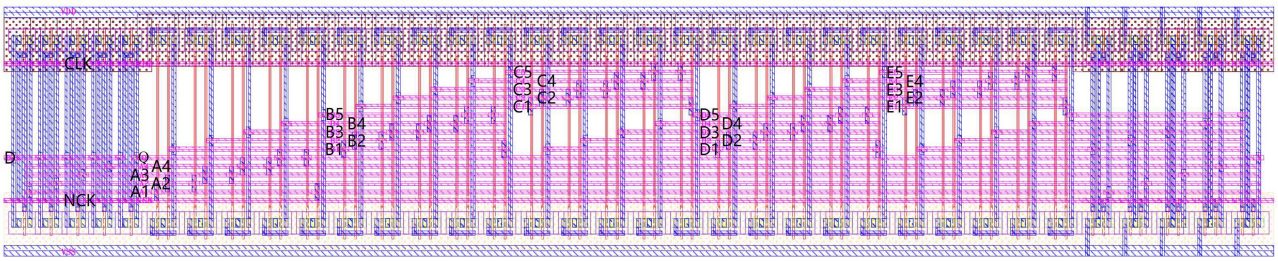

Fig. 4. Layout of the proposed QRHIL latch.

interlocked CEs that are CE1–CE25, as well as five CG-based inverters in the last column. As presented in Fig. 3, the CE matrix comprises five columns and each column comprises five CEs. In the latch, the CEs' outputs in every column feed the CEs' inputs in the subsequent column. For every CE, the output feeds the single inputs of the next-column two CEs. In the latch, signals D and Q (A5) denote the input and output, respectively. Note that the latch is recoverable from node-upsets so that it is insensitive to the HIS. Fig. 4 shows the layout of the proposed QRHIL latch.

When CLK and NCK have the values "1" and "0," respectively, the latch is operated in transparent mode so that the TGs are ON. Hence, the value of D can propagate from A1 to A5 through TGs. Subsequently, the value of A1–A5 can propagate from B1 to B5 through CE1 to CE5, respectively. In this manner, all CEs' outputs can be pre-charged by D. However, the output values of CE21–CE25 cannot propagate from A1 to A5 since the CG-controlled transistors in these inverters can block the value transmission in this operation mode; hence, the value of Q can be determined by D only through a TG so that the current competition at Q can be avoided, reducing power and D to Q delay. Therefore, the proposed latch can operate properly since all node values can be correctly initialized.

The current competition issue is explained here. We can assume that the inverters in Fig. 3 are not based on CG, i.e., there are no clock-controlled transistors in the inverters. Then, if the latch is initialized, each node has a correct value and many feedback loops can be constructed in the latch. In transparent mode, all switches are ON. If a new D-value arrives, this new value will compete with the old value in the latch. For example, the right-bottom inverter in Fig. 3 is outputting an old Q(A5) value, but a new D-value passes through the left-bottom switch, so that Q(A5) suffers from the current competition. However, Fig. 3 has no current competition problem, because the CG-based inverters cannot output a value in transparent mode.

When CLK and NCK have the values "0" and "1," respectively, the latch is operated in hold mode so that the TGs are OFF. Meanwhile, the CLK and NCK signals turn ON the transistors in the inverters; thus, CE25's output can drive Q through the right-bottom CG-based inverter in Fig. 3. With 25 interlocked CEs, the latch can store values through many constructed feedback loops. In hold mode, the SNU, DNU, TNU, and QNU self-recoverability is introduced. Note that, if an inverter's input has a flipped value, the value can propagate to its output; hence, the inverter's input and output have the same upset sensitivity. Thus, we do not need to consider the outputs of inverters for the fault-tolerance discussion. This means that only 25 nodes for the latch need to be considered.

First, we discuss the QNU self-recoverability of the proposed latch. Because the proposed latch is symmetrically constructed, only five cases, i.e., case 1–case 5, need to be considered.

Case 1: Quadruple nodes in the same row of the CE matrix are impacted by a QNU. Since the latch is symmetrically constructed, we can only select <A1,B1,C1,D1> as the QNU node list for illustration. For the case where <A1,B1,C1,D1> suffers from a QNU, A1–D1 can be upset temporally. Because D1 is the impacted single input of both CE16 and CE20 but the other single inputs of both CE16 and CE20 are not affected, the outputs of both CE16 and CE20 still have correct values. Simultaneously, D2–D4 are not affected; hence, the outputs of CE17–CE19 are still correct. Thus, CE21–CE25's inputs remain correct. Then, CE21–CE25's correct outputs feed A1–A5 through the inverters so that the latch can recover from errors. Therefore, the latch can provide self-recoverability from QNUs in Case 1.

Case 2: Triple nodes in the same row as well as one node in another row of the CE matrix are impacted by a QNU. The worst case is considered, which means that one CE's inputs are both impacted. Because the latch is symmetrically constructed, the representative node lists only include <A1,B1,C1,A2>, <A1,B1,C1,A5>, <A1,B1,C1,B2>, <A1,B1,C1,B5>, <A1,B1,C1,C2> as well as <A1,B1,C1,C5>.

For the case where <A1,B1,C1,A2> suffers from a QNU, the directly impacted nodes can be upset temporally. Clearly, the upset A1 and A2 can upset B1 through CE1, but the upset A2 cannot upset the other nodes because CE2 can intercept the error at A2 so that this case equals to the case that a TNU occurs at <A1,B1,C1>. Moreover, as in Case 1, <A1,B1,C1,D1> can provide QNU recovery so that <A1,B1,C1> can provide TNU recovery. Thus, <A1,B1,C1,A2> can provide QNU recovery. In the same manner, node lists <A1,B1,C1,B2> and <A1,B1,C1,C2> can also provide recovery from QNUs.

For the case where <A1,B1,C1,A5> suffers from a QNU, the directly impacted nodes can be temporally upset. Because CE5's inputs are upset temporally, CE5 can output

an error at B5. At this time, CE10 can output an error at C5 because the CE's inputs (B1 and B5) are temporally upset. Then, CE15 can output an error at D5 because the CE's inputs (C1 and C5) are temporally upset. Because A5, B5, C1, and C5 are the temporally upset single inputs of CE4, CE9, CE11, and CE14, respectively, and D5 is the temporally upset single input of both CE19 and CE20, all of these CEs' outputs still have correct values (the single-input-impacted or non-impacted CEs can block errors). Hence, CE21–CE25's inputs still have correct values. Thus, CE21–CE25's correct outputs can remove all errors in the latch. In the similar way, <A1,B1,C1,B5> as well as <A1,B1,C1,C5> can also provide QNU recovery. Therefore, the latch can provide recoverability from QNUs in Case 2.

Case 3: Double nodes in the same row as well as double nodes in another row of the CE matrix are impacted by a QNU. The worst case is considered, which means that all inputs of two CEs are affected. Because the latch is symmetrically constructed, the representative node lists only include <A1,B1,A2,B2> as well as <A1,B1,A5,B5>.

For the case where <A1,B1,A2,B2> suffers from a QNU, the directly impacted nodes can be temporally upset. Clearly, the upset B1 and B2 can upset C1 through CE6, but the upset B2 cannot upset the other single nodes because CE7 can intercept the error at B2 so that this QNU node list is similar to the TNU node list <A1,B1,C1> that is mentioned in Case 2. Thus, node list <A1,B1,A2,B2> can provide recoverability from the QNU.

For the case where <A1,B1,A5,B5> suffers from a QNU, the directly impacted nodes can be temporally upset. Clearly, B1 is the temporally upset single input of both CE6 and CE10 and B5 is the temporally upset single input of both CE9 and CE10, but B2–B4 are not affected so that CE6–CE9's outputs still have correct values. Note that CE10's inputs are affected and thus CE10 cannot provide a correct value at its output. Nevertheless, both CE14 and CE15 can block the error at C5. Clearly, the errors can be intercepted by CEs. Hence, the inputs and outputs of CE21–CE25 still have correct values. Thus, CE21–CE25 can remove all errors. This means that all key node lists in this case can recover from QNUs. Therefore, the latch can provide recoverability from QNUs in Case 3.

Case 4: Double nodes in the same row as well as one node in each of the other two rows of the CE matrix are impacted by a QNU. The worst case is considered, which means that all inputs of two CEs are affected. Because the latch is symmetrically constructed, the representative node lists only include <A1,B1,A2,A3>, <A1,B1,A2,A5>, <A1,B1,B2,B3>, <A1,B1,B2,B5>, <A1,B1,A2,B5> as well as <A1,B1,A5,B2>.

For the case where <A1,B1,A2,A3> suffers from a QNU, the directly impacted nodes can be temporally upset. Clearly, because all inputs of both CE1 and CE2 are temporally upset, both B1 and B2 are upset temporally. Hence, C1 is temporally upset. Clearly, A1, A3, B1, and B2 are the temporally upset single inputs of CE5, CE3, CE10, and CE7, respectively, and C1 is the temporally upset single input of both CE11 and CE15, and simultaneously each of the mentioned CEs also has a correct input so that all of these CEs' outputs are still correct. This means that the CEs can block errors in the latch. Hence, the inputs and outputs of CE21 to CE25 still have correct values. Thus, CE21–CE25 can remove all errors. In the similar way, node list <A1,B1,B2,B3> can also provide recoverability from a QNU. Moreover, for any other QNU node list in this case, we can investigate that there exists at least one column of CEs whose outputs still have correct values so that the column of CEs can remove all errors in the latch. Therefore, the proposed latch can provide recoverability from QNUs in Case 4.

Case 5: Quadruple nodes in the same column of the CE matrix are impacted by a QNU. The worst case is considered, which means that all inputs of three CEs are affected. Because the latch is symmetrically constructed, the representative node list only includes <A1,A2,A3,A4>.

For the case where <A1,A2,A3,A4> suffers from a QNU, the directly impacted nodes can be temporally upset. Clearly, all inputs of CE1–CE3 are temporally upset so that all these CEs' output have wrong values. Clearly, B1–B3 are also upset temporally so that all inputs of both CE6 and CE7 are upset temporally. Hence, both C1 and C2 are also upset temporally so that D1 is also upset temporally. Nevertheless, the errors can be blocked by CEs so that they cannot pass from E1 to E5. Hence, CE21 to CE25's inputs remain correct. Thus, CE21–CE25 can remove all errors. Therefore, the latch can provide recoverability from QNUs in Case 5.

From the above discussions we can draw a conclusion that our proposed QRHIL latch can provide recovery from any QNU. Obviously, our proposed QRHIL latch can also recover from any possible SNU, DNU, as well as TNU. Note that, the QRHIL can be generalized to recover from SNUs, DNUs, TNUs, QNUs, and N node upsets. For the left-bottom or left-top 2×2 CEs of QRHIL, we can feed the outputs of the output-level CEs back to the inputs of the input-level CEs to implement SNU recovery. For the left-bottom or left-top 3×3 CEs of QRHIL, we can feed the outputs of the output-level CEs back to the inputs of the input-level CEs to implement DNU recovery. For the left-bottom or left-top 4×4 CEs of QRHIL, we can feed the outputs of the output-level CEs back to the inputs of the input-level CEs to implement TNU recovery. In this way, we can use (N+1)×(N+1) CEs to implement N node upset recovery. Note that, if N is even, an inverter needs to be added to the output of each output-level CE to ensure correct logic.

B. Simulations

The proposed latch design was implemented in 22 nm CMOS technology from GlobalFoundries. The Synopsys HSPICE tool was used to perform all simulations. The pMOS transistors had the W/L ratio of 90 nm/22 nm and the nMOS transistors had the W/L ratio of 45 nm/22 nm. The 0.8 V supply voltage and room temperature were used. Note that, a flexible fault-injection current-source model

TABLE I
Statistic Results for the Complete Key SNU, DNU, and TNU Injections of the QRHIL Latch According to Fig. 6

Time (ns)	SNUs/DNUs /TNUs	State	Time (ns)	SNUs/DNUs /TNUs	State	Time (ns)	SNUs/DNUs /TNUs	State	Time (ns)	SNUs/DNUs /TNUs	State
0.1	A1	Q = 0	10.3	A1, A3	Q = 1	20.5	A1, E4	Q = 0	30.7	A1, B1, Q	Q = 1
0.3	B1	Q = 0	10.5	A1, A4	Q = 1	20.7	A1, E5	Q = 0	32.1	A1, B1, B2	Q = 0
0.5	C1	Q = 0	10.7	A2, A4	Q = 1	22.1	A1, E3	Q = 1	32.3	A1, B1, B5	Q = 0
0.7	D1	Q = 0	12.1	A2, Q	Q = 0	22.3	A1, D4	Q = 1	32.5	A1, C1, A2	Q = 0
2.1	A1	Q = 1	12.3	A3, Q	Q = 0	22.5	A1, E4	Q = 1	32.7	A1, C1, Q	Q = 0
2.3	B1	Q = 1	12.5	A1, B2	Q = 0	22.7	A1, E5	Q = 1	34.1	A1, B1, B2	Q = 1
2.5	C1	Q = 1	12.7	A1, C2	Q = 0	24.1	A1, B1, C1	Q = 0	34.3	A1, B1, B5	Q = 1
2.7	D1	Q = 1	14.1	A2, Q	Q = 1	24.3	A1, B1, D1	Q = 0	34.5	A1, C1, A2	Q = 1
4.1	E1	Q = 0	14.3	A3, Q	Q = 1	24.5	A1, C1, E1	Q = 0	34.7	A1, C1, Q	Q = 1
4.3	A1, B1	Q = 0	14.5	A1, B2	Q = 1	24.7	A1, A2, A3	Q = 0	36.1	A1, C1, C2	Q = 0
4.5	A1, C1	Q = 0	14.7	A1, C2	Q = 1	26.1	A1, B1, C1	Q = 1	36.3	A1, C1, C5	Q = 0
4.7	A1, D1	Q = 0	16.1	A1, D2	Q = 0	26.3	A1, B1, D1	Q = 1	36.5	A1, D1, A2	Q = 0
6.1	E1	Q = 1	16.3	A1, E2	Q = 0	26.5	A1, C1, E1	Q = 1	36.7	A1, D1, Q	Q = 0
6.3	A1, B1	Q = 1	16.5	A1, C3	Q = 0	26.7	A1, A2, A3	Q = 1	38.1	A1, C1, C2	Q = 1
6.5	A1, C1	Q = 1	16.7	A1, D3	Q = 0	28.1	A1, A2, A4	Q = 0	38.3	A1, C1, C5	Q = 1
6.7	A1, D1	Q = 1	18.1	A1, D2	Q = 1	28.3	A1, A3, Q	Q = 0	38.5	A1, D1, A2	Q = 1
8.1	A1, A2	Q = 0	18.3	A1, E2	Q = 1	28.5	A1, B1, A2	Q = 0	38.7	A1, D1, Q	Q = 1
8.3	A1, A3	Q = 0	18.5	A1, C3	Q = 1	28.7	A1, B1, Q	Q = 0	40.1	A1, D1, D2	Q = 0
8.5	A1, A4	Q = 0	18.7	A1, D3	Q = 1	30.1	A1, A2, A4	Q = 1	40.3	A1, D1, D5	Q = 0
8.7	A2, A4	Q = 0	20.1	A1, E3	Q = 0	30.3	A1, A3, Q	Q = 1	42.1	A1, D1, D2	Q = 1
10.1	A1, A2	Q = 1	20.3	A1, D4	Q = 0	30.5	A1, B1, A2	Q = 1	42.3	A1, D1, D5	Q = 1

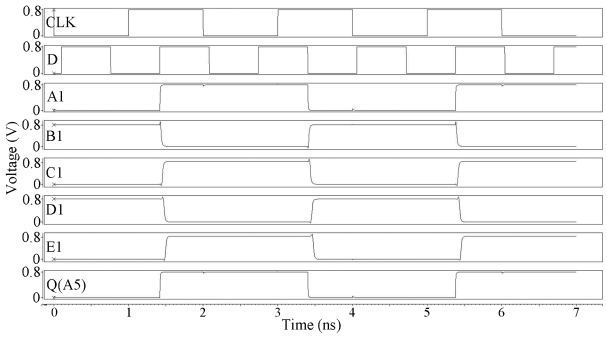

Fig. 5. Error-free operation simulations of the proposed QRHIL latch.

with parameters was also used as in [4], [5], [18], [20], [23] to perform all node-upset injections and the red lighting marks that will be introduced below just denote the injected node-upsets in this article.

Fig. 5 shows the error-free operation simulations of the proposed QRHIL latch. It can be seen that the simulation waveforms demonstrate that the error-free operations of the QRHIL latch in both transparent and hold modes are similar to those of a traditional D-latch, respectively, which validates the correct behavior of the proposed QRHIL latch.

Node-upset injections for the QRHIL latch are discussed here. Firstly, SNUs are considered. Because the latch is symmetrically constructed, only five representative single nodes A1, B1, C1, D1, and E1 suffering from SNUs need to be considered. As presented in Fig. 6 and Table I, when Q's state is 0 and at 0.1, 0.3, 0.5, 0.7, and 4.1 ns, an SNU was, respectively, injected on single nodes A1, B1, C1, D1, and E1. Meanwhile, for the above nodes' reverse states, SNU simulations were also done. We can see that these injected SNUs can be removed by the latch (i.e., the latch can self-recover from SNUs).

Secondly, DNU injections are discussed. Because the latch is symmetrically constructed, the representative DNU node pairs include <A1,B1>, <A1,C1>, <A1,D1>, <A1,A2>, <A1,A3>, <A1,A4>, <A2,A4>, <A2,A5>, <A3,A5>, <A1,B2>, <A1,C2>, <A1,D2>, <A1,E2>, <A1,C3>, <A1,D3>, <A1,E3>, <A1,D4>, <A1,E4>, and <A1,E5>. As shown in Fig. 6 and Table I, when Q's state is 0 and at 4.3, 4.5, 4.7, 8.1, 8.3, 8.5, 8.7, 12.1, 12.3, 12.5, 12.7, 16.1, 16.3, 16.5, 16.7, 20.1, 20.3, 20.5, and 20.7 ns, a DNU was respectively injected to these node-pairs. Meanwhile, for all the above node pairs' reverse states, DNU simulations were also done. We can see that these DNUs can be removed by the latch (i.e., the latch can self-recover from DNUs).

Thirdly, TNUs are considered. Because the proposed latch is symmetrically created, the representative TNU node lists include <A1,B1,C1>, <A1,B1,D1>, <A1,C1,E1>, <A1,A2,A3>, <A1,A2,A4>, <A1,A3,A5>, <A1,B1, A2>, <A1,B1,A5>, <A1,B1,B2>, <A1,B1,B5>, <A1,C1,A2>, <A1,C1,A5>, <A1,C1,C2>, <A1,C1, C5>, <A1,D1,A2>, <A1,D1,A5>, <A1,D1,D2>, and <A1,D1,D5>. As shown in Fig. 6 and Table I, when Q's state is 0 and at 24.1, 24.3, 24.5, 24.7, 28.1, 28.3, 28.5, 28.7, 32.1, 32.3, 32.5, 32.7, 36.1, 36.3, 36.5, 36.7, 40.1, and 40.3 ns, a TNU was respectively injected to these TNU node lists. Meanwhile, for all the above node lists' reverse states, all TNU simulations were also done. We can see that these injected TNUs can be removed by the latch (i.e., the latch can self-recover from TNUs).

Fig. 7 presents the key QNU injection simulations of the proposed QRHIL latch. Since the latch is symmetrically created, the representative QNU node lists only include <A1,B1,C1,D1>, <A1,B1,C1,A2>, <A1,B1,C1,A5>, <A1,B1,C1,B2>, <A1,B1,C1,B5>, <A1,B1,C1,C2>, <A1,B1,C1,C5>, <A1,B1,A2,B2>, <A1,B1,A5,B5>,

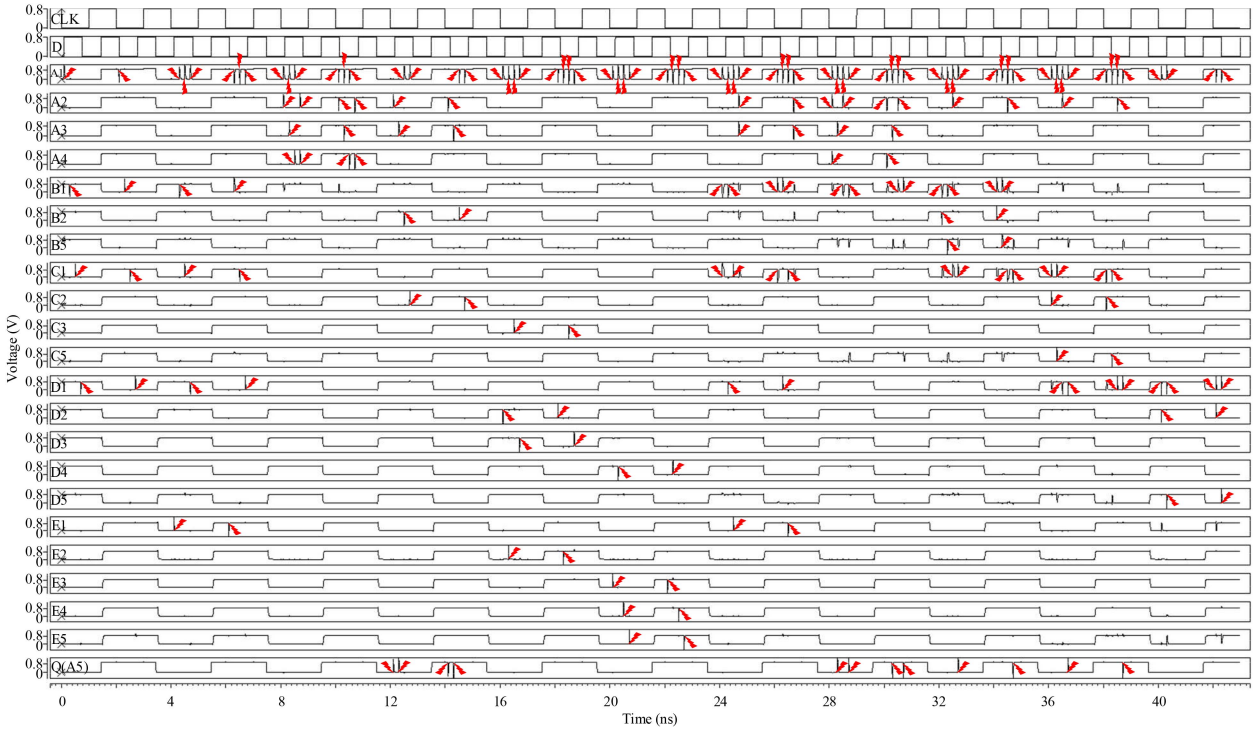

Fig. 6. Key SNU, DNU, and TNU injection simulations of the proposed QRHIL latch.

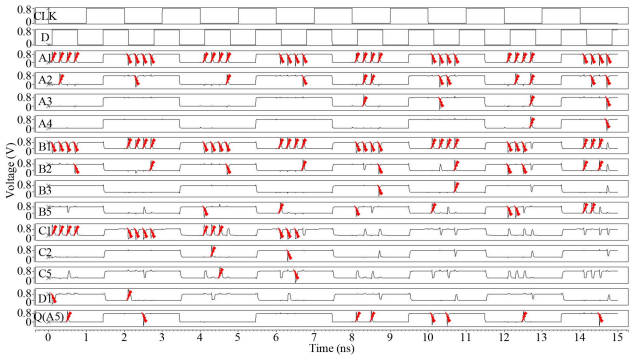

Fig. 7. Key QNU injection simulations of the QRHIL latch.

TABLE II
Statistic Results of Key QNU Injection Simulations for the QRHIL Latch Design According to Fig. 7

Time (ns)	QNUs	State	Time (ns)	QNUs	State
0.1	A1, B1, C1, D1	0	8.1	A1, B1, Q, B5	0
0.3	A1, B1, C1, A2	0	8.3	A1, B1, A2, A3	0
0.5	A1, B1, C1, Q	0	8.5	A1, B1, A2, Q	0
0.7	A1, B1, C1, B	0	8.7	A1, B1, B2, B3	0
2.1	A1, B1, C1, D1	1	10.1	A1, B1, Q, B5	1
2.3	A1, B1, C1, A2	1	10.3	A1, B1, A2, A3	1
2.5	A1, B1, C1, Q	1	10.5	A1, B1, A2, Q	1
2.7	A1, B1, C1, B2	1	10.7	A1, B1, B2, B3	1
4.1	A1, B1, C1, B5	0	12.1	A1, B1, B2, B5	0
4.3	A1, B1, C1, C2	0	12.3	A1, B1, A2, B5	0
4.5	A1, B1, C1, C5	0	12.5	A1, B1, Q, B2	0
4.7	A1, B1, A2, B2	0	12.7	A1, A2, A3, A4	0
6.1	A1, B1, C1, B5	1	14.1	A1, B1, B2, B5	1
6.3	A1, B1, C1, C2	1	14.3	A1, B1, A2, B5	1
6.5	A1, B1, C1, C5	1	14.5	A1, B1, Q, B2	1
6.7	A1, B1, A2, B2	1	14.7	A1, A2, A3, A4	1

<A1,B1,A2,A3>, <A1,B1,A2,A5>, <A1,B1,B2,B3>, <A1,B1,B2,B5>, <A1,B1,A2,B5>, <A1,B1,A5,B2> as well as <A1,A2,A3,A4>. In Fig. 7 and Table II, when Q's state is 0 and at 0.1, 0.3, 0.5, 0.7, 4.1, 4.3, 4.5, 4.7, 8.1, 8.3, 8.5, 8.7, 12.1, 12.3, 12.5 as well as 12.7 ns, a QNU was respectively injected to these QNU node lists. Meanwhile, for the above node lists' reverse states, all QNU simulations were also done. We can see that these injected QNUs can be removed by the latch (i.e., the latch can provide recovery from QNUs).

From the above discussions, we can draw a conclusion that the proposed QRHIL latch can provide complete recoverability from SNUs, DNUs, TNUs, as well as QNUs so that the latch can be used for reliable storage/computing especially in environments with harsh radiation.

IV. PROPOSED QRHIL-LC LATCH DESIGN

A. Structure and Working Flow

Fig. 8 shows the structure of the low-cost version of the QRHIL (QRHIL-LC). It comprises five TGs and twenty-four interlocked 2-input CEs that are CE1–CE24. Note that CE1, CE3, CE9, and CE17 are two-input CEs with CG. As shown in Fig. 8, the 24 CEs are divided into 3 levels: the outer level (i.e., CE1–CE8), the middle level (i.e., CE9–CE16), and the inner level (i.e., CE17–CE24). Note that N1 is the output of CE1, and similarly, Ni is the output of CEi ($1 \leq i \leq 24$). For each CE in the outer level, its output is fed to the single input of the CE in the same level and the

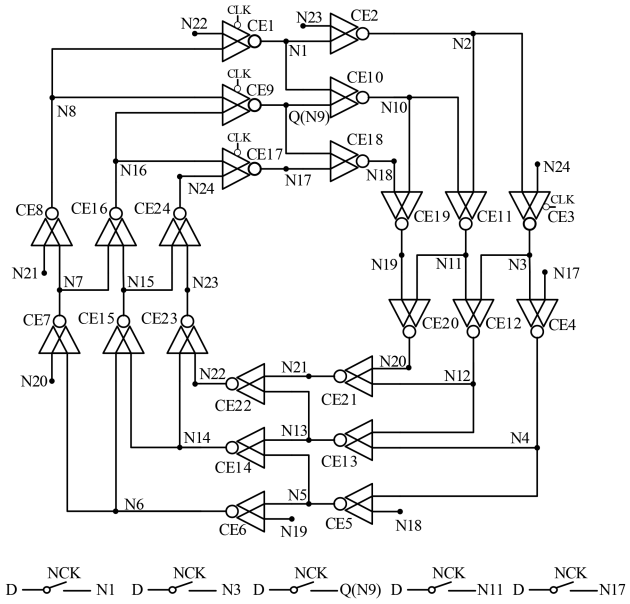

Fig. 8. Structure of the proposed QRHIL-LC latch.

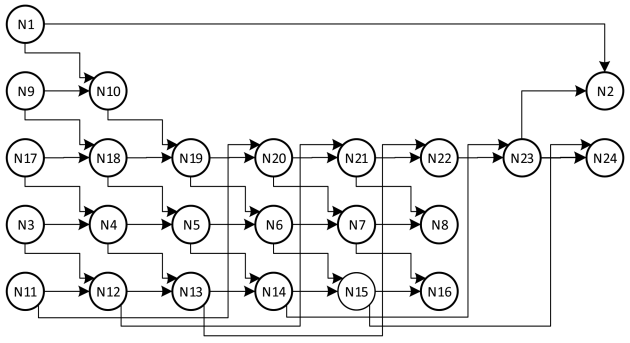

Fig. 9. Topology of CE-outputs of the proposed QRHIL-LC latch.

single input of the CE in the middle level. For each CE in the middle level, its output is fed to the single input of the CE in the same level and the single input of the CE in the inner level. For each CE in the inner level, its output is fed to the single input of the CE in the same level and the single input of the CE in the outer level. For the QRHIL-LC latch, D and Q (N9) are the input and output, respectively.

When CLK and NCK have the values "1" and "0," respectively, the latch is operated in transparent mode so that the pMOS/nMOS transistors in the switches with input D are ON. Hence, N1, N3, N9 (Q), N11, and N17 can be initialized by D. It can be seen from Figs. 8 and 9 that N1 and N9 feed N10 (through CE10) and thus the value of N10 can be determined. Similarly, the values of N4, N2, and N18 can be determined. Then, all of the other nodes can be subsequently determined (see Fig. 9). Note that, CE9 uses CG to reduce current competition at node Q (N9) to decrease power as well as D to Q delay. Therefore, the proposed latch's normal operations are correct in this mode since its initialization can be correctly finished (and the value of D can pass to Q).

When CLK and NCK have the values "0" and "1," respectively, the latch is operated in hold mode so that the pMOS/nMOS transistors in the switches with input D are OFF. Since each level feeds itself and another level, many feedback loops (e.g., the outer, middle, and inner feedback loops) can be effectively created to retain values. Thus, the proposed latch's normal operations are correct in transparent mode since the latch can keep values correctly and the kept values can output through Q. Fig. 10 shows the layout of the QRHIL-LC latch.

In the following, the QNU self-recoverability of the QRHIL-LC latch is discussed. Clearly, only four cases, i.e., case 1–case 4 in the following, need to be considered.

Case 1: A QNU affects quadruple nodes at the same level. Considering the worst case, four adjacent CEs are impacted at the same time. Because of the looped structure of the latch, the representative node list only includes <N1,N2,N3,N4>.

For the case where <N1,N2,N3,N4> is impacted by a QNU, all directly impacted nodes are temporally upset. Indeed, for CE2–CE4, their single input and output are simultaneously impacted by the QNU, so that their single input needs to be recovered; otherwise, the output cannot recover. This means that N1 needs to be first recovered. Since N9–N12 are respectively the correct single inputs of CE10–CE13 whose outputs are not impacted, the error at N1– N4 cannot propagate to the outputs of CE10–CE13 (i.e., the CEs can block the single errors at their single inputs), respectively. Meanwhile, N18 is the correct single input of CE5 so that the error at N4 cannot propagate to the output of CE5. Therefore, the QNU is blocked by CEs so that the other nodes, such as N8, N17, N22, N23, and N24, are still correct. Moreover, since all inputs of CE1 (i.e., N8 and N22) are correct, N1 can recover through CE1. Subsequently, N2 can be recovered by the recovered N1 along with the correct N23 through CE2. Similarly, N3 and N4 can subsequently recover through CE3 and CE4. In other words, <N1,N2,N3,N4> can provide QNU recovery. Therefore, the latch can provide QNU recovery in Case 1.

Case 2: A QNU impacts three nodes in the same level and one node in another level. Considering the worst case, both the single input and the output of two CEs and all inputs of at least one CE are impacted at the same time. Because of the looped structure of the latch, the representative node lists only include <N1,N2,N3,N9>, <N1,N2,N3,N23>, <N9,N10,N11,N1>, <N9,N10,N11,N17>, <N17,N18, N19,N9> as well as <N17,N18,N19,N3> (note that N17 and N3 are the inputs of CE4 in the outer level).

For the case where <N1,N2,N3,N9> is impacted by a QNU, all directly impacted nodes are temporally upset. Since all inputs of CE10 are temporally flipped, the error can propagate to N10 through CE10. Then, the temporally upset N2 and N10 can propagate the error to N11 through CE11. Similarly, the error can propagate to N12 through CE12. However, since N17 is the correct single input of CE18, the error at N9 cannot propagate to N18 through CE18. Similarly, the error at N3, N10, and N11 cannot propagate to N4, N19, and N20 through CE4, CE19, and CE20, respectively, and the error at N12 cannot propagate to N13 and N21 through CE13 and CE21, respectively. Therefore, the QNU is blocked by CEs so that the other

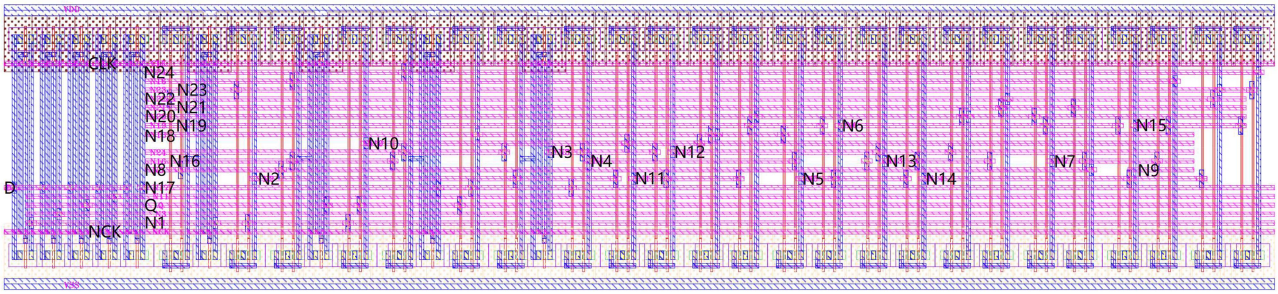

Fig. 10. Layout of the proposed QRHIL-LC latch.

nodes, such as N8, N16, N22, N23, and N24, are still correct. Since all inputs of CE1 and CE9 are correct, N1 and N9 can recover through CE1 and CE9, respectively. Subsequently, N2 can be recovered by the recovered N1 along with the correct N23 through CE2, and N10 can be recovered by the recovered N1 and N9 through CE10. Similarly, N3, N11, and N12 can subsequently recover through CE3, CE11, and CE12, respectively. Therefore, <N1,N2,N3,N9> can provide QNU recovery. In the similar way, node lists <N9,N10,N11,N17> and <N17,N18,N19,N3> can also self-recover from QNUs.

For the case where <N1,N2,N3,N23> is impacted by a QNU, all directly impacted nodes are temporally upset. Since only all inputs of CE2 are flipped and N2 is already flipped, the error cannot propagate to the other nodes. Therefore, the QNU is blocked by CEs so that, the other nodes, such as N8, N14, N22, N23, and N24, are still correct. Because all inputs of CE1 and CE23 are correct, N1 and N23 can recover through CE1 and CE23, respectively. Subsequently, the recovered N1 and N23 can recover N2 through CE2. Then, the recovered N2 along with the correct N24 can recover N3 through CE3. Therefore, <N1,N2,N3,N23> can provide QNU recovery. In the same way, <N9,N10,N11,N1> as well as <N17,N18,N19,N9> can also self-recover from QNUs. Therefore, the latch can provide recovery from QNUs in Case 2.

Case 3: A QNU affects two nodes in the same level and affects two nodes in another level. We also consider the worst case, i.e., two CEs' all inputs are affected at the same time. Because of the looped structure of the proposed latch, the representative node lists only include <N1,N9,N2,N10>, <N1,N23,N2,N24>, and <N9,N17,N10,N18>.

For the case where <N1,N9,N2,N10> is affected by a QNU, all directly impacted nodes are temporally upset. Because all inputs of CE11 are temporally flipped, the error can propagate to N11 through CE11. However, since N3 and N19 are the correct single inputs of CE12 and CE20, respectively, the error at N11 cannot propagate to N12 and N20 through CE12 and CE20, respectively. In a similar manner, the error cannot propagate to the other nodes. Therefore, the QNU is blocked by CEs so that, the other nodes, such as N8, N16, N22, and N23, still have correct values. These correct nodes can recover the flipped nodes through CEs. Therefore, <N1,N9,N2,N10> can provide QNU recovery. Similarly, <N1,N23,N2,N24> and <N9,N17,N10,N18> can also recover from QNUs. Therefore, the latch can provide recovery from QNUs in Case 3.

Case 4: A QNU affects two nodes in the same level and also impacts one node in each of the other two levels. We also consider the worst case, i.e., three CEs' all inputs are affected at the same time. Because of the looped structure of the proposed latch, the representative node list is <N1,N9,N17,N23> only.

For the case where <N1,N9,N17,N23> is impacted by a QNU, all directly impacted nodes are temporally upset. Because all inputs of CE2, CE10, and CE18 are temporally flipped, the error can propagate to N2, N10, and N18 through CE2, CE10, and CE18, respectively. Subsequently, the flipped N2 and N10 can propagate the error to N11 through CE11 and the flipped N10 and N18 can propagate the error to N19 through CE19. Then, the flipped N11 and N19 can propagate the error to N20 through CE20. However, the error cannot propagate further to other nodes due to CEs' error interception. Hence, the inputs of CE1, CE9, CE17, and CE23 still have correct values. Therefore, all affected nodes can recover through CE1, CE9, CE17, and CE23, respectively. Therefore, <N1,N9,N17,N23> can recover from the QNU. In other words, the proposed latch can provide recovery from QNUs in Case 4.

From the above discussions, we can draw a conclusion that the proposed novel QRHIL-LC latch is completely recoverable from QNUs. Therefore, the QRHIL-LC latch is also completely recoverable from SNUs, DNUs, as well as TNUs. Note that, the QRHIL-LC can be generalized to recover from DNUs, TNUs, QNUs, and N node upsets but N should be less than 8. For the internal eight CEs (one large loop), a latch can be constructed to recover from DNUs. For the internal 2×8 CEs (two large loops), a latch can be constructed to recover from TNUs. For the internal 3×8 CEs (three large loops), a latch (i.e., QRHIL-LC) can be constructed to recover from QNUs. In this way, we can use (N-1)×8 CEs to implement N node upset recovery but N should be less than 8. This is because, once eight nodes, e.g., 8 nodes in a large loop, are simultaneously impacted, one input and the output of each CE are impacted so that each CE in the loop cannot output a correct value (a CE can output a correct value only if its inputs are all correct).

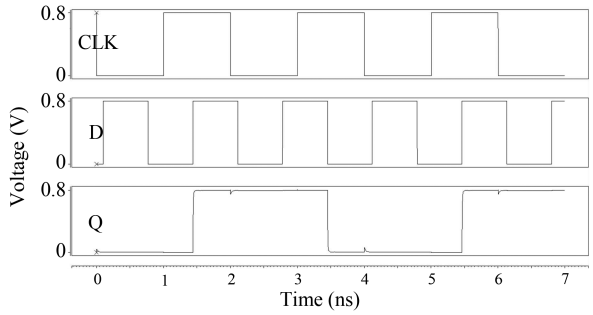

Fig. 11. Error-free operation simulations of the QRHIL-LC latch.

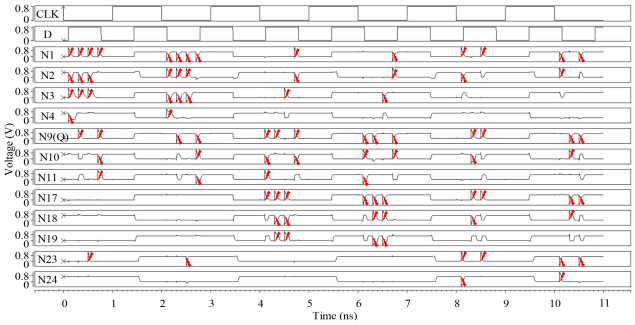

Fig. 12. Key QNU injection simulations of the proposed QRHIL-LC latch.

B. Simulations

Similarly, the QRHIL-LC latch was also implemented in 22 nm CMOS technology from GlobalFoundries and all simulations were also performed using the Synopsys HSPICE tool. The parameters are the same as those of the QRHIL latch discussed in Section III-B. Fig. 11 shows the error-free operation simulations of the QRHIL-LC latch. The simulations demonstrate that the error-free operations of the QRHIL-LC latch in both transparent and hold modes are similar to those of a traditional D-latch, which validates the correct behavior of the proposed QRHIL-LC latch.

Fig. 12 shows the QNU injection simulations of the proposed QRHIL-LC latch. Based on the previous QNU discussions, key node lists <N1,N2,N3,N4>, <N1,N2,N3, N9>, <N1,N2,N3,N23>, <N9,N10,N11,N1>, <N9,N10, N11,N17>, <N17,N18,N19,N9>, <N17,N18,N19,N3>, <N1,N9,N2,N10>, <N1,N23,N2,N24>, <N9,N17,N10, N18>, <N1,N9,N17,N23> were selected for QNU injections, respectively. As shown in Fig. 12 and Table III, when Q's state is 0 and at 0.1, 0.3, 0.5, 0.7, 4.1, 4.3, 4.5, 4.7, 8.1, 8.3, and 8.5 ns, a QNU was respectively injected to these QNU node lists. Meanwhile, for the above node lists' reverse states, all QNU simulations were also done. We can see that these injected QNUs can be removed by the latch (i.e., the latch can provide recovery from QNUs).

From the above discussions, we can draw a conclusion that the proposed QRHIL-LC latch can provide complete recoverability from SNUs, DNUs, TNUs, as well as QNUs so that the latch can be used for reliable storage/computing in environments with harsh radiation.

TABLE III
Statistic Results for the Complete Key QNU Injections of the QRHIL-LC Latch According to Fig. 12

Time (ns)	QNUs	State	Time (ns)	QNUs	State
0.1	N1, N2, N3, N4	0	4.7	N1, N9, N2, N10	0
0.3	N1, N2, N3, N9	0	6.1	N9, N10, N11, N17	1
0.5	N1, N2, N3, N23	0	6.3	N17, N18, N19, N9	1
0.7	N9, N10, N11, N1	0	6.5	N17, N18, N19, N3	1
2.1	N1, N2, N3, N4	1	6.7	N1, N9, N2, N10	1
2.3	N1, N2, N3, N9	1	8.1	N1, N23, N2, N24	0
2.5	N1, N2, N3, N23	1	8.3	N9, N17, N10, N18	0
2.7	N9, N10, N11, N1	1	8.5	N1, N9, N17, N23	0
4.1	N9, N10, N11, N17	0	10.1	N1, N23, N2, N24	1
4.3	N17, N18, N19, N9	0	10.3	N9, N17, N10, N18	1
4.5	N17, N18, N19, N3	0	10.5	N1, N9, N17, N23	1

V. COMPARISONS

A. Reliability and Cost of Latches

To make a fair comparison, the reviewed SNU, DNU, TNU, and/or QNU mitigated latches listed in the Section II were also implemented under the same conditions/parameters as our proposed QRHIL and QRHIL-LC latches (i.e., for transistor W/L sizes, the pMOS had the ratio of 90 nm/22 nm and the nMOS had the ratio of 45 nm/22 nm; for other parameters, 0.8 V supply voltage and room temperature were used).

Reliability comparison results are presented in Table IV. It can be seen that both the proposed QRHIL and QRHIL-LC latches have nine "$\surd$" marks. The proposed QRHIL and QRHIL-LC latches can provide QNU tolerance and QNU recoverability but the other latches cannot simultaneously provide. Note that a QNU-recoverable latch is HIS-insensitive because the inputs of a CE cannot keep different values for a long period of time. Moreover, the last column of Table IV shows the comparisons of the critical charge (Q_{crit}) of these latches. We measured the critical charge of latches using the approach described in [32]. It can be seen from Table IV that the critical charge of our proposed two latches is not small.

Fig. 13 shows comparisons of overhead for these hardened latches, in terms of transmission delay, power consumption, silicon area, and delay-power-area product (DPAP). In Fig. 13, "Delay" denotes the transmission delay from D to Q (i.e., the average of rise and fall delays from D to Q), "Power" denotes the average power consumption (dynamic and static), "Area" denotes the silicon area calculated based on the layout of each latch, and DPAP is calculated through multiplying the delay, power, and area to evaluate the overall overhead of all latches.

(Delay Comparison) Delay overhead comparison results are shown in Fig. 13(a). It can be seen that the proposed two latches as well as existing latches, such as HLDTL-EV, RH, LCTNUT, TNUHL, and QNUTL, have a small D-Q delay. This is mainly because a high-speed path is embedded from D to Q for each of them. Note that, the proposed latches consume moderate delay to completely provide the QNU recovery.

(Power Comparison) In terms of power, it can be seen from Fig. 13(b) that the TNUHL latch has lower power

TABLE IV
Reliability Comparison Results Among the Hardened Latches

Latch	Ref.	SNU Tolerant	SNU Recoverable	DNU Tolerant	DNU Recoverable	TNU Tolerant	TNU Recoverable	QNU Tolerant	QNU Recoverable	HIS Insensitive	Q_{cirt} (fC)
HRLC	[12]	√	√	×	×	×	×	×	×	√	3.77
DICE	[13]	√	√	×	×	×	×	×	×	√	5.00
SHLR	[14]	√	√	×	×	×	×	×	×	√	4.45
HLDTL-EV	[15]	√	×	√	×	×	×	×	×	×	2.01
DIRT	[16]	√	√	√	×	×	×	×	×	√	4.90
RH	[17]	√	√	√	×	×	×	×	×	×	2.74
DNURL	[18]	√	√	√	√	×	×	×	×	√	4.65
DNUSH	[19]	√	√	√	√	×	×	×	×	√	4.37
LCTNUT	[20]	√	√	√	×	√	×	×	×	×	3.37
TNUHL	[21]	√	×	×	×	×	×	×	×	×	2.52
TNURL	[23]	√	√	√	√	√	√	×	×	√	3.74
ISC-TRL	[24]	√	√	√	√	√	√	×	×	√	4.68
ISC-QRL	[24]	√	√	√	√	√	√	×	×	√	4.39
QNUTL	[4]	√	√	√	×	√	×	√	×	×	3.40
QRHIL	(Proposed)	√	√	√	√	√	√	√	√	√	4.06
QRHIL-LC	(Proposed)	√	√	√	√	√	√	√	√	√	4.53

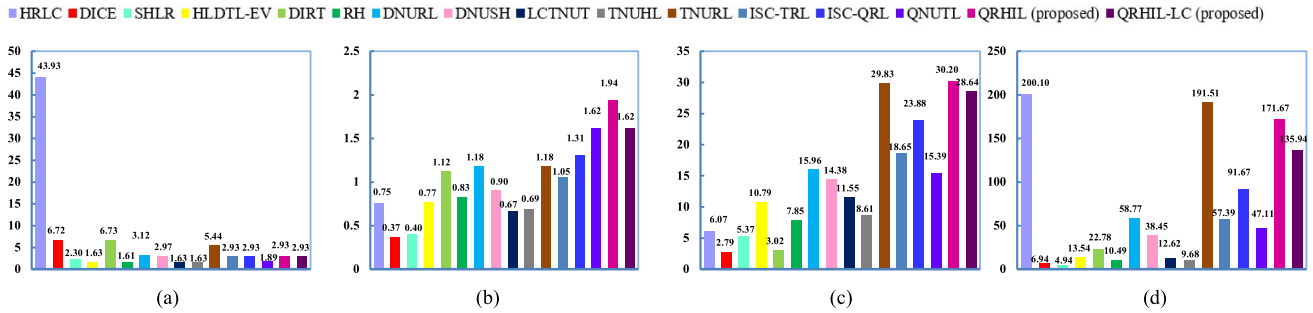

Fig. 13. Overhead comparison results among these hardened latches. (a) Delay (ps). (b) Power (μW). (c) Area (μm^2). (d) DPAP $\times 10^{-2}$.

TABLE V
Calculation Result of Each Slope for Fig. 14

Curve	Slope	Curve	Slope
<0.75, 0.80>	0.26	<1.00, 1.05>	0.62
<0.80, 0.85>	0.28	<1.05, 1.10>	0.76
<0.85, 0.90>	0.35	<1.10, 1.15>	0.91
<0.90, 0.95>	0.42	<1.15, 1.20>	1.08
<0.95, 1.00>	0.51	<1.20, 1.25>	1.27

*The average slope is 0.65.

dissipation because of the smaller area although there is some current competition at inputs of RC circuits. Note that, if a latch has a large silicon area and/or it does not employ the CG approach, its power consumption is large. In order to provide complete QNU recoverability, the two proposed latches use redundant silicon area so that their power dissipation is not small.

(Area Comparison) In terms of area, we can see from Fig. 13(c) that the proposed two latches and the TNURL latch require more area. This is mainly because they employ extra transistors to ensure enhanced reliability. Therefore, our proposed QRHIL and QRHIL-LC latches are completely QNU-recoverable but at the cost of moderate silicon area.

(DPAP Comparison) In terms of DPAP, we can see from Fig. 13(d) that the proposed two latches, HRLC and TNURL, have a higher DPAP because their delay, power, and/or area are large. However, compared to the TNURL latch that is not QNU-tolerant and not QNU-recoverable, our proposed QRHIL latch has a moderate DPAP mainly because its delay is smaller; the proposed QRHIL-LC latch has a smaller DPAP since its delay, area, and power are small compared to the QRHIL latch.

B. Process Voltage and Temperature Variation Effects

Latches, particularly implemented in nanoscale CMOS, are susceptible to *process, supply voltage, and temperature* (*PVT*) variations. Therefore, we evaluate the PVT variation effects on latches using the approach as in [33]. According to [33], when assessing PVT variation effects on a latch, only one parameter is adjusted at a time, and the other parameters remain unchanged. For instance, when investigating the impact of supply voltage variations on a latch, we need to alter only the supply voltage and maintain all other parameters constant.

TABLE VI
Sensitivity of Delay or Power of the Alternative Hardened Latches to PVT Variations

Latch	Supply voltage vs. Delay	Supply voltage vs. Power	Temperature vs. Delay	10^{-2} × Temperature vs. Power	Threshold-voltage increment vs. Delay	10^{-2} × Threshold-voltage increment vs. Power	LEEF vs. Delay	10^{-2} × LEEF vs. Power
HRLC	3.11	2.62	8.64	5.75	4.47	4.00	18.97	4.80
DICE	0.48	1.61	1.01	3.25	0.65	2.20	6.09	2.90
SHLR	0.12	1.36	0.43	3.25	0.13	2.10	0.68	2.20
HLDTL-EV	0.08	1.38	0.25	3.50	0.09	2.40	0.39	2.60
DIRT	0.48	4.82	1.01	9.50	0.65	6.70	6.09	8.30
RH	0.08	1.45	0.26	4.13	0.09	3.30	0.39	3.20
DNURL	0.15	2.58	0.51	7.13	0.16	4.60	0.83	4.80
DNUSH	0.14	1.77	0.48	4.63	0.16	3.30	0.83	3.40
LCTNUT	0.08	1.94	0.26	5.00	0.09	3.40	0.39	3.60
TNUHL	0.09	3.72	0.25	7.13	0.09	5.40	0.39	5.70
TNURL	0.26	0.66	0.88	4.88	0.29	1.30	1.67	2.30
ISC-TRL	0.14	0.45	0.47	1.50	0.15	1.40	0.81	1.40
ISC-QRL	0.14	0.56	0.47	1.75	0.15	1.70	0.81	1.90
QNUTL	0.09	5.00	0.32	9.88	0.09	7.10	0.48	9.60
QRHIL	0.14	0.81	0.47	3.00	0.15	2.00	0.81	2.30
QRHIL-LC	0.14	0.65	0.47	2.00	0.15	1.90	0.81	2.00

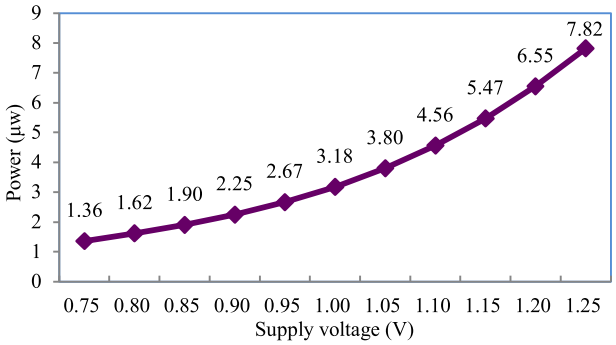

Fig. 14. Impact of supply voltage variations on power for QRHIL-LC.

Fig. 14 shows the impact of supply voltage variations on power for the QRHIL-LC latch. There are 11 samples for supply voltage variations from 0.75 to 1.25 V with increment step 0.05 V. These samples just form ten curve segments, i.e., <0.75, 0.80>, <0.80, 0.85>, <0.85, 0.90>, <0.90, 0.95>, <0.95, 1.00>, <1.00, 1.05>, <1.05, 1.10>, <1.10, 1.15>, <1.15, 1.20> and <1.20, 1.25>. The slope of each curve segment can be calculated. For example, the slope of <0.75, 0.80> is equal to that of the power measured at 0.80 V minus the power measured at 0.75 V. Then, based on the absolute values of the slopes of ten curve segments, the *average slope* (*AS*) of the entire curve (i.e., <0.75, 1.25>) can be obtained. Table V shows the calculation result of each slope and the AS. Clearly, the AS can represent the power sensitivity of the QRHIL-LC latch to supply voltage variations. The AS can be used to assess the sensitivity of each latch to PVT variations. We assume that D_1, D_2, D_3, …, D_i are samples of delay or power of a latch, where i is the sample count. Then, the AS (sensitivity) can be calculated as

$$\mathrm{AS} = \frac{1}{i-1}\sum_{k=2}^{i} |D_k - D_{k-1}| \,. \qquad (1)$$

As shown in Table VI, we calculated the AS (sensitivity) of delay or power of each latch to PVT variations with (1). In Table VI, "Supply voltage vs. Delay," "Temperature vs. Delay," "Threshold-voltage increment vs. Delay," and "L_{EEF} vs. Delay" denote the sensitivity of delay of each latch to supply voltage, temperature, threshold-voltage, and *effective channel length* (L_{EEF}) variations, respectively, so that we can know the meaning of "Supply voltage vs. Power," "Temperature vs. Power," "Threshold-voltage increment vs. Power," and "L_{EEF} vs. Power." Note that the supply voltage was ranged from 0.75 to 1.25 V, increasing 0.05 V at each step; the temperature was ranged from -20 to 120 °C, increasing 20 °C at each step; the threshold-voltage increment was ranged from 0 to 0.1 V, increasing 0.01 V at each step; the L_{EEF} was ranged from 22 to 32 nm, increasing 1 nm at each step.

It can be seen from Table VI that, compared to the QNU-tolerant QNUTL latch, the delay of the proposed two latches is more sensitive to PVT variations; however, compared to the first HRLC latch, the delay of the proposed two latches is less sensitive to PVT variations. Moreover, compared to the QNU-tolerant QNUTL latch, the power of the proposed two latches is less sensitive to PVT variations; however, compared to the first HRLC latch, the power of the proposed two latches is still less sensitive to PVT variations. In summary, the proposed latches are moderately sensitive to PVT variations.

VI. CONCLUSION AND FURTHER WORK

Technology scaling of CMOS increases the sensitivity of integrated circuits to soft errors. In this article, a completely QNU-recoverable latch (namely QRHIL) has been proposed. To ensure a smaller D to Q delay, a high-speed path has been embedded between D and Q. Moreover, to reduce overhead, this article has further presented the low-cost

version of QRHIL (namely QRHIL-LC). Simulation results have demonstrated the QNU-recoverability of the QRHIL as well as QRHIL-LC latches. The proposed QRHIL and QRHIL-LC can be used for reliable storage/computing in environments with harsh radiation as well as safety-critical applications where high reliability is required.

Readers may aware that the setup time of the proposed latches is large since the data will have to propagate through many CEs before a stable signal is attained. In our further work, we would like to try to propose high-reliability latches with low cost and analyze the results. Moreover, the soft-error rate of latches will also be calculated with failure-in-time metric.

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