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Digital Adaptive Calibration of Multi-Step Analog to Digital Converters

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This paper reports a novel approach for calibration of multi-step A/D converters based on the steepest-descent estimation method. The calibration procedure is enhanced with dedicated embedded sensors, which register on-chip process parameter and temperature variations. Additionally, to guide the verification process with the information obtained through process monitoring, two efficient algorithms based on an expectation-maximization method and adjusted support vector machine classifier, respectively, are proposed. The algorithms are evaluated on a prototype 12 bits A/D converter fabricated in standard single poly, six metal 90 nm CMOS.

Keywords: Analog to Digital Converter, Calibration, Process Variation Monitoring, Diagnosis, Debugging.

1. INTRODUCTION

The static parameters of a multi-step analog to digital (A/D) converter are determined by analog errors in various A/D converter components. Therefore, a major challenge in A/D converter debugging and calibration is to estimate the contribution of those individual errors to the overall A/D converter linearity parameters. The observation of important design and technology parameters, such as temperature, threshold voltage, etc., is enhanced with dedicated sensors embedded within the functional cores.[1] The steps causing discontinuities in the A/D converter's stage transfer functions can be analyzed, minimized or corrected with a wide variety of calibration techniques.[2–7] The mismatch and error attached to each step can either be averaged out, or their magnitude can be measured and corrected. In general, most of the debugging and calibration methods require that a reference signal is available in the digital domain, this being the signal that the actual stage output of the A/D converter is compared with. This reference signal is in the ideal case a perfect, infinite resolution, sampled version of the signal applied to the A/D converter under test. Nevertheless, in a practical situation, the reference signal must be estimated in some way. This can be accomplished by incorporating auxiliary devices such as a reference A/D converter, sampling the same signal as the A/D converter under test,[8] or a D/A converter feeding a digitally generated signal to the A/D converter under test.[9]

In this paper, such an A/D converter is augmented with dedicated sensors embedded within the converter to supplement the circuit calibration and to guide the verification process with the information obtained through the monitoring process.[10] Furthermore, the design-for-test (DfT) capabilities permit a multi-step A/D converter re-configuration in such a way that all sub-blocks are tested for their full input range allowing full functional observability and controllability. Additionally, in the proposed method the overlap between the conversion ranges of two stages is considered to avoid conflicting operational situations that can either mask faults or give an incorrect interpretation.

This paper is organized as follows: Section 2 focuses on the multi-step A/D converter architecture and the concept of debugging and calibration enhanced by process variation monitoring. In Section 3, design considerations for each stage of dual-residue multi-step A/D converter and calibration algorithm are highlighted. Section 4 discusses the algorithms for verification process guidance, namely, the expectation-maximization and the support vector machine. In Section 5 experimental results obtained on a prototype multi-step A/D converter fabricated in standard 90 nm CMOS are presented. Finally, Section 6 provides a summary and the main conclusions.

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2. CONCEPT OF PROCESS VARIATION MONITORING ENHANCED CALIBRATION

Even though extensive research[11–14] has been done to estimate the various errors in different A/D converter architectures, the use of DfT and dedicated sensors for the analysis of multi-step A/D converters to update parameter estimates has been negligible. The influence of the architecture on A/D converter modeling is investigated in Ref. [11]. In Ref. [12] with the use of some additional sensor circuitry, pipeline A/D converters are evaluated in terms of their response to substrate noises globally existing in a chip. In Ref. [13], the differential nonlinearity test data is employed for fault location and identification of the analog components in the flash A/D converter, and in Ref. [14] it is shown how a given calibration data set may be used to extract estimates of a specific error performance. Functional faults in each of the analog components in a multi-step A/D converter affect the transfer function differently,[12] and analyzing this property forms the basis of our approach. The A/D converter characteristics may also change while it is used, e.g., due to temperature change and component aging. This means that the A/D converter has to be reevaluated at regular intervals through temperature sensors to examine its performance. Each stage of the A/D converter under test is evaluated experimentally, i.e., a signal is fed to the input of each stage of the A/D converter and the transfer characteristics of each stage of the A/D converter is determined from the outcome.

2.1. A/D Converter Architecture

The multi-step architecture (Fig. 1) allows the design of a high-speed, power efficient converter with a reasonable amount of hardware. The differential input signal is sampled with three-time interleaved sample-and-hold (S/H), which eliminates the need for re-sampling of the signal after each quantization stage. The resulting sampled signal is then further processed in three steps, namely, the coarse (4 bit), the mid (4 bit) and the fine (6 bit) steps. The acquired signal from the coarse quantization is stored in a latch and is also applied to a switch unit to select the references for the mid quantization in the next clock phase. The selected reference signals are combined with the held input signals from the S/H in two mid residue amplifiers. Similarly, the outputs of both coarse and mid A/D converters are combined together in order to select proper references for the fine quantization. Correspondingly, these references are combined with the sampled input signal in two fine residue amplifiers, before they are processed in a fine stage.

Typically, the full range of the mid quantization resistance ladder is longer than one step in the coarse quantization ladder. With this over-range compensation in the mid ladder (e.g., similar principle is applicable to the fine ladder as well) the static errors can be corrected since the signal still lies in the range of the mid ladder. This means that the output of the A/D converter is redundant and it is not possible, from the digital output, to find the values from each sub-ranging step without employing dedicated DfT.[15] To set the inputs of the individual A/D converter stages at the wanted values, a scan-chain is available in the switch-matrix circuit. For mid-range A/D converter measurements, the coarse A/D converter values are prearranged since they determine mid-range A/D converter references. Similarly to evaluate the fine A/D converter both the coarse and mid A/D converter decisions are set to predetermined value. The response of each of the individual

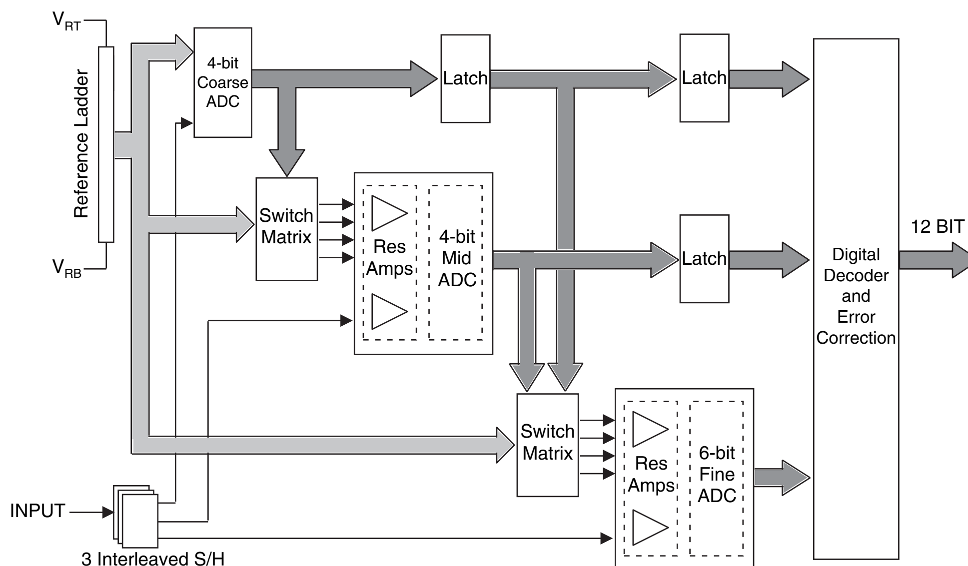

Fig. 1. Block diagram of the 12-bit multi-step A/D converter.

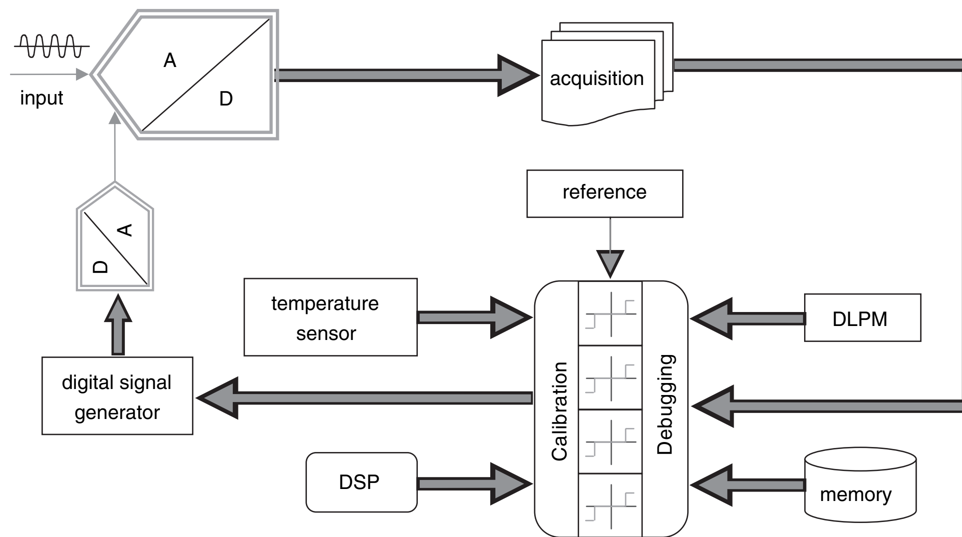

Fig. 2. Conceptual view of the debugging and calibration loop.

A/D converter stages is subsequently routed to the test bus. The sub-D/A converter (implemented as a combination of the reference ladder and the switch matrix) settings are controlled by a serial shift of data through a scan chain that connects all sub-D/A converter registers. To capture the current settings of the sub-D/A converter, it is possible to freeze the contents of the sub-D/A converter registers in normal mode and shift out the data via the scan-chain. A test control bit per sub-D/A converter is available to adjust (increase) the reference current to obtain an optimal fit of sub-D/A converter output range to the A/D converter input range.

2.2. Process Variation Monitoring Based Calibration

The overall multi-step A/D converter consists primarily of non-critical low-power components, such as low-resolution quantizers, switches and open-loop amplifiers for increased power efficiency. Although a multi-step A/D converter makes use of a considerable amount of digital logic, most of its signal-processing functions are executed in the analog domain. Consequently, the conversion process is susceptible to analog circuit and device impairments. The primary static error sources present in each stage of a multi-step A/D converter are systematic decision stage offset errors λ, stage gain errors η, and errors in the internal reference voltages γ. To facilitate the measurement of these fluctuations, an evaluation strategy as depicted in Figure 2 is proposed. The algorithm inputs are the outputs of each stage of the multi-step A/D converter, and outputs of die-level process monitor (DLPM) circuits and temperature sensors. The desired output is collected from the back-end A/D converter and subtracted from the corresponding nominal value. The algorithm gives the required information to the digital pattern generator, whose outputs steer the calibration D/A converter, thereby closing the calibration loop. The temperature sensor based on Ref. [16] registers any on-chip temperature changes, and, if required, updates the estimation algorithm.

The DLPM measurements are directly related to asymmetries between the branches composing the circuit; for all primary error sources, we derive separate DLPMs by extracting (replicating) the targeted error contributor of each stage (e.g., λ, η, and γ). The primary reason for replicating the error contributors is to avoid large added loading of the test scheme on the circuits in sensitive analog signal paths. Additionally, by separating DLPMs from the signal path, the monitors can be designed to maximize the sensitivity of the circuit to the target parameter to be measured. A discrimination window for various die-level process monitors is defined according to the rules of the multi-step A/D converter error model.[11]

3. DESIGN OF MULTI-STEP A/D CONVERTER

3.1. Time-Interleaved Sample-and-Hold

The sampling rate of a system is further increased by a using time-interleaved technique,[17] where a higher sampling rate is obtained by running the system in parallel, although at different clock phases. However, in the front-end S/H (Fig. 3), where the clock is used to sample a continuous time signal, any deviation of the sampling moment from its ideal value results in an error voltage in the sampled signal equal to the signal change between these two moments. The clock skew between the sampling clocks of distributed S/H circuits can be calibrated by measuring its value and controlling tunable delays of a DLL.[18] Nevertheless, in general, calibration of the skew between S/H circuits has two significant drawbacks. First, skew measurement is complex and second, the tuning of the delays requires high accuracy from the calibration

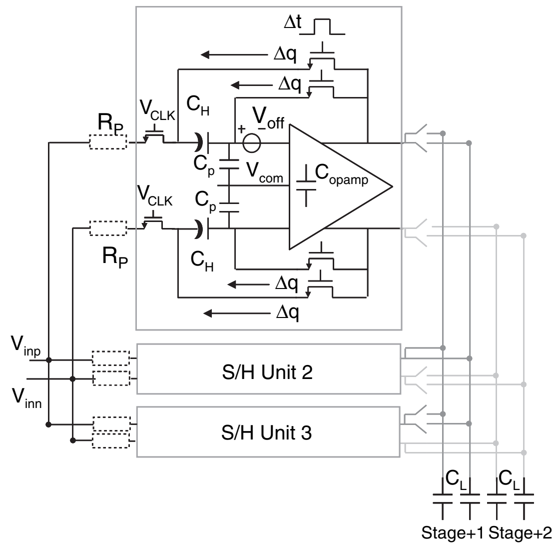

Fig. 3. Sources of errors in the three times interleaved sample-and-hold; Δq, Δt, C_p, R_p, V_{off}, C_H, C_L designate charge injection errors, timing errors, parasitic capacitance, parasitic resistance, offset voltage, hold capacitance and load capacitance, respectively.

hardware and algorithm. Alternatively, timing alignment within the required accuracy can be obtained by using a master clock[19] to synchronize the different sampling instants and by careful design while matching the channels clock and input signals lines.[20] In this design, a similar approach is followed: besides the extensive shielding and matching of the clock lines, the delays of any active buffers within the clock distribution network are kept to the minimum.

Besides timing mismatch, time-interleaved S/H suffers from offset, gain and bandwidth mismatch. One limitation of the offset cancelling method[21] from a systems point of view is the fact that the static offset has to be measured before the calibration. The gain mismatch can be calibrated digitally by measuring the reference levels and storing them in a memory. The ideal output code can be recovered using these measured reference levels.[22] In our implementation the resulting *dc* offset is mainly cancelled with design percussions, such as differential signal path, bottom plate sampling, small feedback switches, opamp high common-mode rejection ratio and by using the closed loop sampling architecture such that consequent offset mismatch is sufficiently low for the required resolution. By dimensioning the open loop *dc*-gain of the operational amplifiers large enough, the effect of gain mismatch is suppressed below the quantization noise level. With careful sizing and layout, capacitor matching sufficient for twelve bit resolution is achieved. By increasing the bandwidth, the impact of the bandwidth mismatch at the signal frequency becomes lower. For this reason, the bandwidth of each sample-and-hold unit has been chosen larger than what is required when just looking at signal attenuation.

3.2. Stage Design

To maximize the settling time of the sub-D/A converter output, i.e., to achieve a high conversion speed, the coarse and mid A/D converter should be able to provide its output to the sub-D/A converter as soon as possible after the S/H circuit samples the input and enters the hold mode. Therefore, the coarse and mid A/D converter are of parallel, flash type[23] as it provides the highest throughput rate. It should be noted that insufficient settling in coarse and mid A/D converter or mismatch in coarse and mid comparators is directly translated into a quantization error and appears as a shift in the location of the quantization step causing missing codes. To cope with these errors, we have applied over-range and digital correction[24] technique. On a circuit level, dynamic comparators are used to eliminate static power consumption. The low comparator offset is achieved as a result of signal amplification in the preamplifier circuits, the large transresistance of the current-to-voltage conversion, the two-phase clocking scheme,[25] which reduces the number of devices that contribute to the offset, and finally the choice of appropriate transconductance ratios. As a result of the absence of offset compensation, the clock frequency is high.

To reduce power consumption of the 6-bit fine A/D converter, the folding and interpolation technique[26] is applied. In order to increase the intrinsic resolution, more zero-crossings (e.g., necessary for the digital output code transitions) have to be created across the input range. This can be achieved by increasing the number of folding amplifiers at the input or by increasing the interpolation factor. However, these approaches result in increased power consumption, and degraded speed performance. Alternatively, the number of foldings in each folding signal before interpolation can be increased. Conversely, the transconductance curves of the differential pairs starts overlapping; deteriorating the gain of the folding amplifier. In this design, to alleviate the problem of overlapping transconductance curves, folding is conducted at a lower frequency in each stage.[27]

The sub-D/A conversion is based on resistor-ladder architecture since it is relatively simple and inherently monotonic as long as the switching elements are designed correctly. Additionally, the DNL of resistor-ladder is relatively low compared to other architectures. Switches in switch matrix are simple CMOS switches designed to have low enough on-resistance to provide sufficient bandwidth for twelve bit settling of the reference signals on the residue amplifiers.

3.3. Inter-Stage Design

To build multi-step A/D converter with a large tolerance to component non-idealities, redundancy is introduced by making the sum of the individual stage resolutions greater than the total resolution. The conversion accuracy thus

solely relies on the precision of the residue signals; the conversion speed, on the other hand, is largely determined by the settling speed of the residue amplifier. When the redundancy is eliminated by a digital-correction algorithm, it can be used to eliminate the effects of inter-stage offset on the overall linearity. However, a gain error in the residue amplifier is still critical. The accumulative inter-stage gain relaxes the impact of circuit non-idealities, such as noise, nonlinearity, and offset, of later stages on the overall conversion accuracy. Consider a classical single-residue processing in multi-step A/D converter illustrated in Figure 4(a). A gain error in the residue amplifier scales the total range of residue signal and causes an error in the analog input to the next stage when applied to any nonzero residue, resulting in residue signal not fitting in the fine A/D converter range. If the error in the analog input to the fine ADC stage is more than one part in 2^r (where r is the resolution remaining after the residue amplifier gain error), it will result in a conversion error, which can lead to non-monotonicity or missing codes, that is not removed by digital correction. In our design, the implemented dual-residue signal processing[28] as illustrated in Figure 4(b) spreads the errors of the residue amplifiers over the whole mid and fine range, which results in an improved linearity. According to quantization decision of the previous stage, a first and a second residue amplifier pass the difference between the analog signal and the closest and the second closest quantization level, respectively. By passing both residues to subsequent stages, information is propagated about the exact size of the quantization step, as the sum of the two residues is equal to the difference between the two quantization levels. The absolute gain of the two residue amplifiers is therefore not important, providing that both residue amplifiers match and have sufficient signal amplitude to overcome finite comparator resolution.

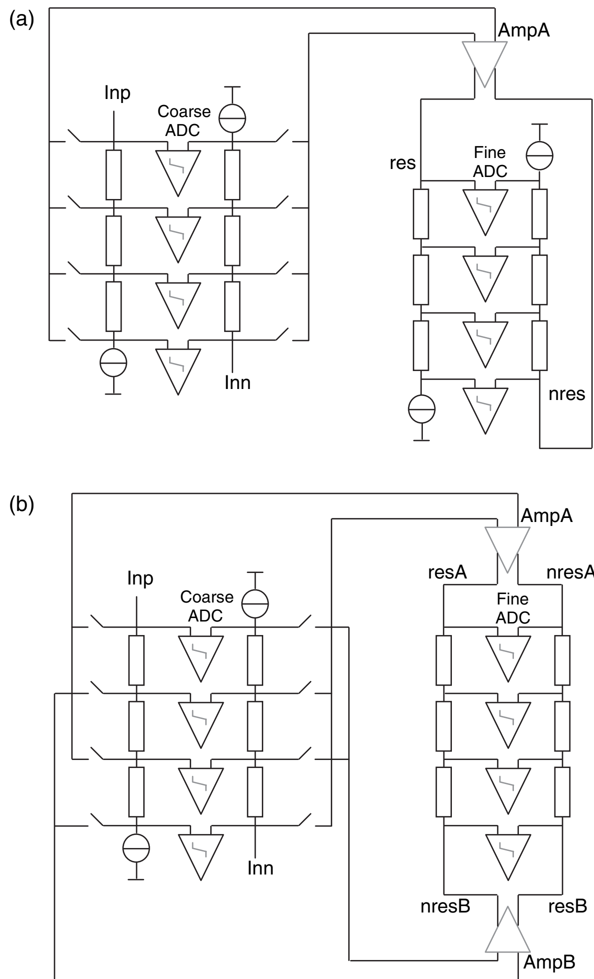

Fig. 4. (a) Single-residue, (b) Dual-residue processing.

3.4. Multi-Stage Circuit Calibration Algorithm

The gain (and nonlinearity) errors in the coarse and mid A/D converter provoke over-range problems and code level shifting. Consequently, the approaches to apply digital correction are based on either increasing the input range of the next stage and using extra comparators, or on using the partial codes in the next stages to correct the code of the present stage. The effect of introducing a over-range and digital correction[24] technique on the coarse A/D converter offset is studied by examining the plots shown in Figures 4(a)–(b). When the coarse A/D converter has some nonlinearity, even with an ideal D/A converter, as shown in Figure 5(a), results in two of the coarse A/D converter decision levels being shifted, one by $-1^{1/2}$ LSB ($n+1$ error) and the other by $+2$ LSB ($n+2$ error). If the conversion range of the second stage is increased to handle the larger residues, it can be encoded and the errors corrected (Fig. 5(b)). The effect of an offset error in a comparator on a stage transfer function is shown in Figure 5(c). The dotted line represents an ideal transfer function, and the solid line shows a transfer function with an offset voltage in a comparator. In a multi-step A/D converter, an error in the gain stage (Fig. 5(d)) causes a non-linearity in the input to output transfer characteristic. The influence of the finite gain-bandwidth product of each stage on the total A/D converter resolution is illustrated in Figure 5(e).

The references of the sub-D/A converter and the subtraction of the input signal and the sub-D/A converter output determine the achievable accuracy of the total A/D converter. The residue signal V_{res} is incorrect exactly by the amount of the sub-D/A converter nonlinearity caused by errors in the internal reference voltages γ

$$V_{res} = \eta V_{in} - (s-1)\gamma V_{ref} - \lambda V_{offset} \tag{1}$$

where s is the observed stage and V_{in}, V_{ref} and V_{offset} are input, reference and offset voltage, respectivly. To obtain a digital representation of (1) each term is divided with V_{ref}

$$D_{out} = \eta D_{in} - (s-1)\gamma - \lambda D_{os} \tag{2}$$

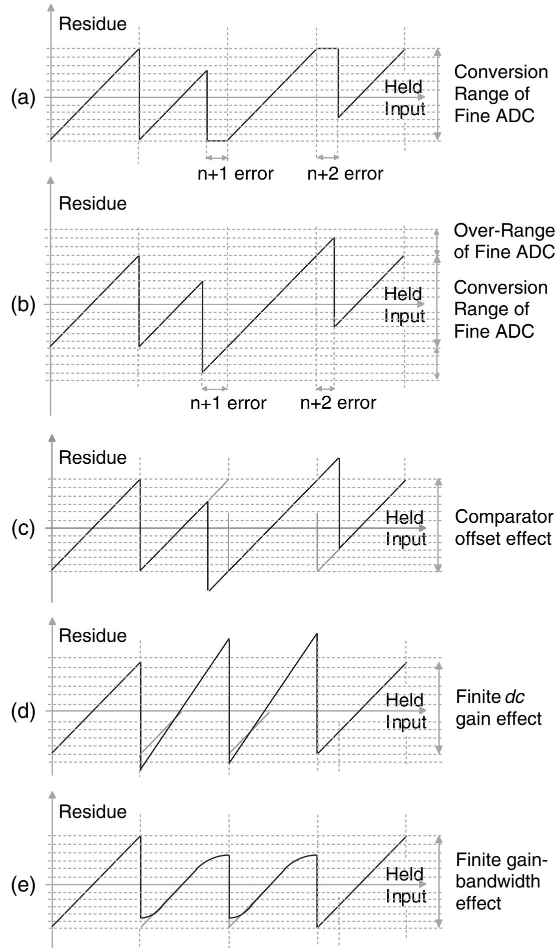

Fig. 5. (a) Residue versus input with coarse A/D converter offset, (b) Residue versus input with coarse A/D converter offset errors when over-range is applied, (c) Effect of comparator offset, (d) Finite dc gain effect on transfer function, and (e) Finite gain-bandwidth effect on transfer function.

where $D_{\text{in}} = V_{\text{in}}/V_{\text{ref}}$, $D_{\text{out}} = V_{\text{res}}/V_{\text{ref}}$, and $D_{\text{os}} = V_{\text{offset, i}}/V_{\text{ref}}$. By denoting the kth stage input, output and offset voltage as $D_{\text{in, k}} = V_{\text{in, k}}/V_{\text{ref}}$, $D_{\text{out}} = V_{\text{res, k}}/V_{\text{ref}}$, and $D_{\text{os}} = V_{\text{offset, k}}/V_{\text{ref}}$, respectively, a recursive relationship when (2) is applied to each stage in sequence becomes

$$\begin{aligned} D_{\text{out}} = D_{\text{out,3}} &= \{[\ldots]\eta_2 - (D_2 - 1)\gamma_2 - \lambda_2 D_{\text{os,2}}\}\eta_3 \\ &- (D_3 - 1)\gamma_3 - \lambda_3 D_{\text{os,3}} = D_{\text{in,N}}\eta_{\text{N}} \ldots \eta_1 \\ &- (D_3 - 1)\gamma_3 - \lambda_3 D_{\text{os,3}} \end{aligned} \tag{3}$$

Such a model is useful to generate an efficient adaptive filtering algorithm using a look-up table for error estimation and fault isolation. In this paper, proposed calibration algorithm based on the steepest-descent method (SDM)[29] involves the creation of an estimation error e, by comparing the estimated output $D'_{\text{out}}(t)$ to a desired response $D_{\text{out}}(t)$. Statistical data extracted through the DLPM measurements provide the SDM estimates $(W')^{\text{T}} = [\eta', \gamma', \lambda']$ with an initial value. In the SDM algorithm (Fig. 6), by setting the different input values D_{in} for each stage at iteration time t, the unknown filter output $D_{\text{out}}(t)$ becomes

$$D_{\text{out}}(t) = D_{\text{in}}(t) \times W \tag{4}$$

The desired output $D_{\text{out}}(t)$ is collected from the back-end A/D converter and subtracted from the corresponding nominal value. This desired response is then supplied to the filter for processing. Based on the predefined inputs and current error estimates, the SDM algorithm involves the creation of an estimation error e, by comparing the estimated output $D'_{\text{out}}(t)$ to a desired response $D_{\text{out}}(t)$. The automatic adjustment of the input weights $(W')^T = [\eta', \gamma', \lambda']$ is performed in accordance with the estimation error e

$$W'(t+1) = W'(t) - \mu \times D_{in}(t) \times e(t) \tag{5}$$

where the scaling factor used to update $W'(t+1)$ is the step-size parameter, denoted by μ. $D_{\text{out}}(t)$ and $D_{\text{in}}(t)$ are matrices with 2^{n-1} rows and three columns, where n is the resolution of the stage. The step size, μ, decreases in each iteration until the input weights decrease, i.e., until $W'(t+1) < W'(t)$. The estimation error, e, is the difference between the desired response and the actual steepest-descent filter output

$$e(t) = D'_{\text{out}}(t) - D_{\text{out}}(t) \tag{6}$$

based on the current estimate of the weight vector, W'

$$D'_{\text{out}}(t) = D_{in}(t) \times W'(t) \tag{7}$$

At each iteration, the algorithm requires knowledge of the most recent values, $D_{\text{in}}(t)$, $D_{\text{out}}(t)$ and $W'(t)$. During the course of adaptation, the algorithm recurs numerous times to effectively average the estimate and to find the best estimate of weight W.

The temporary residue voltage in input D_{in} needs to be updated after each iteration time to improve the accuracy, which can be done by using the current error estimate W'. As temperature can vary significantly from one die area to another, these fluctuations in the die temperature influence the device characteristics. In the implemented system, the temperature sensors register any on-chip temperature changes, and the estimation algorithm update the W' with a forgetting factor, ζ.[30] The estimate at time $t+1$ is

$$\begin{gathered} W'(t+1) = \zeta W'(t) + (1-\zeta) W^0(t+1) \\ 0 < \zeta \leq 1 \end{gathered} \tag{8}$$

where $W^0(t+1)$ is an estimate prior to the registered temperature change.

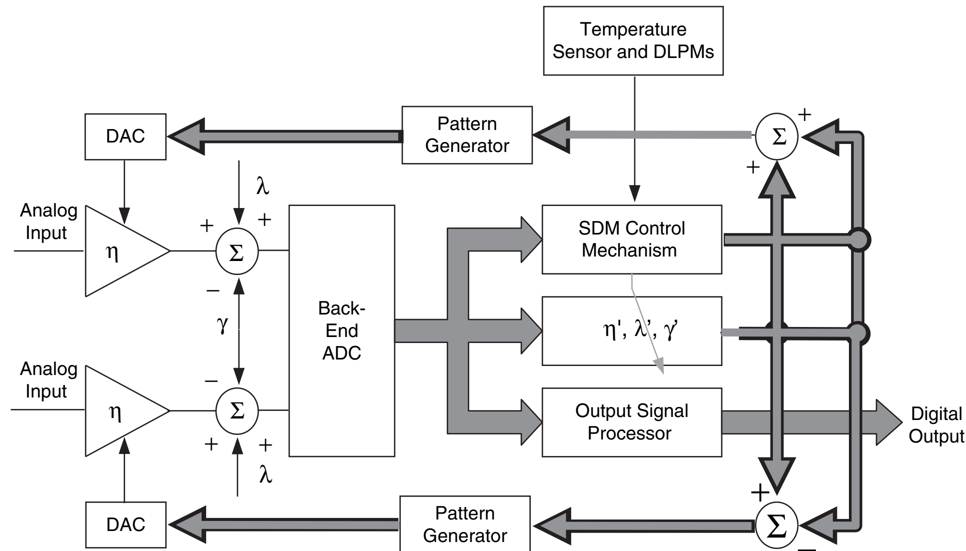

Fig. 6. Estimation method.

Algorithm

Initialization

—Initialize the input vector $D_{\text{in}}(0)$

—Force the inputs and collect the desired output $D_{\text{out}}(0)$

—Measure and set the initial value of the weights $W'(0)$

—Initialize the steepest descent update step $\mu = 1$

—Initialize the forgetting factor ζ

Data collection

—Collect N samples from the DLPM and temperature sensors

—Collect N samples from the AD converter

Update parameter estimate

1. Update the input vector $D_{\text{in}}(t+1)$ based on current available $W(t)$
2. Calculate the error estimate $W'(t)$
3. Generate the output estimate $D'_{\text{out}}(t) = D_{\text{in}}(t) \times W'(t)$
4. Calculate the estimation error $e(t) = D'_{\text{out}}(t) - D_{\text{out}}(t)$
5. Calculate the error estimate $W'(t+1) = W'(t) - \mu \times D_{\text{in}}(t) \times e(t)$
6. If $W'(t+1) > W'(t)$ decrease step size μ and repeat step 5
7. Increase the iteration index, t and repeat steps 1–6 for best estimate
8. Denote the final value of W' by W'_l
9. If temperature changes update $W'(t+1) = \zeta W'(t) + (1-\zeta)$

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4. ALGORITHMS FOR PROCESS VARIATION MONITORING

The complexity of yield estimation, coupled with the iterative nature of the design process, makes yield maximization computationally prohibitive. As a result, circuit designs are verified using models corresponding to a set of worst-case conditions of the process parameters. Worst-case analysis is very efficient in terms of designer effort, and thus has become the most widely practiced technique for statistical verification. However, the worst-case performance values obtained are extremely pessimistic and as a result lead to unnecessarily large and power hungry designs in order to reach the desired specifications. Thus, it would be advantageous to choose a more relaxed design condition. In statistics, several methods, such as listwise and pairwise deletion and structural equation modelling can provide estimates of the selected performance figures based on the combination of the information obtained from multiple DLPM measurements and the differential-nonlinearity (DNL) measurement of each stage of the multi-step A/D converter. In this paper, we utilize a multiple imputation method based on the expectation-maximization (EM) algorithm[31] as it offers maximum likelihood estimates. Additionally, to enable test guidance based on the information obtained through monitoring process variations, we employ the adjusted support vector machine (ASVM) classifier.[32] In comparison with established classifiers (such as quadratic, boosting, neural networks, Bayesian networks), the ASVM classifier is especially resourceful, since it simultaneously minimizes the empirical classification error and maximizes the geometric margin.

4.1. Expectation-Maximization (EM) Algorithm

A maximum likelihood (ML) estimation involves estimation of an unknown (random) parameter vector $\theta \in \Theta$ when the marginal probability $p_{X|\Theta}(x|\theta)$ is at a maximum, given the vector of the DLPM's observations $x_i \in \mathrm{X}$. Obtaining optimum estimates through the ML method involves two

steps: computing the likelihood function and maximizing over the set of all admissible sequences.

Evaluating the contribution of the random parameter θ requires computing an expectation over the joint statistics of the random parameter vector, a task that is analytically intractable. Even if the likelihood function can be obtained analytically, it is invariably a nonlinear function of θ, which makes the maximization step (which must be performed in real time) computationally unfeasible. In such cases, the expectation-maximization (EM) algorithm allows obtaining the maximum likelihood estimates of the unknown parameters by a computational procedure which iterates, until convergence, between two steps.

Two steps, called E-step and M-step are involved in each iteration. In the E-step, the EM algorithm forms the auxiliary function $Q(\theta|\theta^{(t)})$, ($\theta^{(0)}$, $\theta^{(1)}, \ldots, \theta^{(t)}$ is a sequence of parameter estimates), which calculates the expected value of the log-likelihood function with respect to the conditional distribution Y of the DNL measurement of each stage of the multi-step A/D converter, given the vector of the DLPM's observations X under the current estimate of the parameters $\theta(t)$

$$Q(\theta|\theta^{(t)}) = E(\log p(X, Y|\theta)|X, \theta(t)) \tag{9}$$

In the M-step, the algorithm determines a new parameter maximizing Q

$$\theta^{(t+1)} = \arg\max_{\theta} Q(\theta|\theta^{(t)}) \tag{10}$$

At each step of the EM iteration, the likelihood function can be shown to be non-decreasing;[33] if it is also bounded (which is mostly the case in practice), then the algorithm converges. In Ref. [33] it is proven that an iterative maximization of $Q(\theta|\theta^{(t)})$ will lead to a maximum likelihood estimation of θ.

EM Algorithm

Initialization
—Initialize the data set $T_{XY} = \{(x_1, y_1), \ldots, (x_l, y_l)\}$
—Initialize the parameter $\theta^{(0)}$
Data collection
—Collect N samples from the DLPMs
Update parameter estimate
1. Calculate $Q(\theta|\theta^{(n)}) = E(\log p(X, Y|\theta)X, \theta^{(n)})$ —E step
2. Re-estimate θ by maximizing the θ-function —M step
$\theta^{(n+1)} = \text{argmax}_\theta Q(\theta|\theta^{(n)})$, estimate mean and variance
3. Increase the iteration index, n
4. Stop when a stationary point $L(\theta^{(n-1)}|T_{XY}) = L(\theta^{(n)}|T_{XY})$ is found

4.2. Adjusted Support Vector Machine Algorithm

When an optimum estimate of the parameter distribution is obtained as described in the previous section, the next step is to update the test limit values utilizing an adjusted support vector machine classifier. Assuming that the input vectors (e.g., values defining test limits) belong to *a priori* (nominal values) and *a posteriori* (values estimated with the EM algorithm) classes, the goal is to set test limits which reflect observed on-chip variation. Each new measurement is viewed as an r-dimensional vector and the ASVM classifier separates the input vectors into an $r-1$-dimensional hyperplane in feature space Z.

Let $D=\{x_i, c_i)|x_i \in R^r, c_i \in \{-1,1\}\}_{i=1}^n$ be the input vectors belonging to *a priori* and *a posteriori* classes, where the c_i is either 1 or -1, indicating the class to which data x_i from the input vector belongs. To maximize the margin, w and b are chosen such that they minimize the nearest integer $||w||$ subject to the optimization problem described by

$$c_i(w \cdot x_i + b) \geq 1 \tag{11}$$

for all $1 \leq i \leq n$, where the vector w is a normal vector, which is perpendicular to the hyperplane (e.g., defined as $w \cdot x + b = 0$) The parameter $b/||w||$ determine the offset of the hyperplane from the origin along the normal vector w.

In this paper, we solve this optimization problem with a quadratic programming.[34] The quadratic programming problem is solved incrementally, covering all the sub-sets of classes constructing the optimal separating hyperplane for the full data set. Writing the classification rule in its unconstrained dual form reveals that the maximum margin hyperplane and therefore the classification task is now only a function of the support vectors, e.g., the training data that lie on the margin.

$$\max \sum_{i=1}^{n} \alpha_i - \frac{1}{2} \sum_{i,j} \alpha_i \alpha_j c_i c_j x_i^T x_j \tag{12}$$

subject to $\alpha_i \geq 0$ and $\sum_{i=1}^n \alpha_i c_i = 0$,

$$w = \sum_i \alpha_i c_i x_i \tag{13}$$

where the α terms constitute the weight vector in terms of the training set. To allow for mislabeled examples a modified maximum margin technique[34] is employed. If there exists no hyperplane that can divide the *a priori* and *a posteriori* classes, the modified maximum margin technique finds a hyperplane that separates the training set with a minimal number of errors. The method introduces non-negative variables ξ_i, which measure the degree of misclassification of the data x_i

$$c_i(w \cdot x_i + b) \geq 1 - \xi_i \tag{14}$$

for all $1 \leq i \leq n$. The objective function is then increased by a function which penalizes non-zero ξ_i, and the optimization becomes a trade-off between a large margin and a small error penalty. For a linear penalty function, the optimization problem now transforms to

$$\min \frac{1}{2} \|w\|^2 + C \sum_i \xi_i^\sigma \tag{15}$$

such that (9) holds for all $1 \leq i \leq n$. For sufficiently large constant C and sufficiently small σ, the vector w and constant b that minimize the functional (15) under constraints in (11), determine the hyperplane that minimizes the number of errors on the training set and separate the rest of the elements with maximal margin. This constraint in (11) along with the objective of minimizing $||w||$ is solved using Lagrange multipliers. Similarly, non-linear penalty functions can be employed, particularly to reduce the effect of outliers on the classifier; however, the problem can become non-convex and thus, finding a global solution becomes considerably more complex.

5. EXPERIMENTAL RESULTS

A prototype of the multi-step A/D converter with dedicated embedded process monitors was fabricated in a standard single poly, six metal 90 nm CMOS (Fig. 7). The stand-alone A/D converter occupies an area of 0.75 mm^2 operates at 1.2 V supply voltage and dissipates 55 mW (without output buffers). Dedicated embedded monitors (12 per stage subdivided into three specific groups and placed in and around the partitioned multi-step A/D converter) and the complete DfT are restricted to less than 10% of the overall area and consume 8 mW and 0.4 mW when in active and passive mode, respectively. Each DLPM consists of 12 differential pairs or ladder resistors corresponding to gain-, decision- or referenced-based monitor, respectively. The DLPM circuits are small and stand-alone, they match the physical layout of the extracted device under test, and consume no power while in off state. Additionally, the test-chip contains a temperature sensor (located between coarse A/D converter and fine residue amplifiers), which consumes only 11 μW. The multi-stage circuit calibration (MSCC) algorithm requires about 1.5 k logic gates as calibration overhead, occupies an area of 0.14 mm^2 and consumes 11 mW of power.

5.1. Application of Results for A/D Converter Test Window Generation/Update

The algorithms for the A/D converter's test window generation/update, namely, the EM and ASVM algorithms are performed off-line and are implemented in Matlab. All experimental results are carried out on a single processor Linux system with an Intel Core 2 Duo CPUs with 2.66 GHz and 3 GB of memory. To illustrate the concept of test window generation/update, consider only the coarse stage, which is a simple four bit flash stage, consisting of the reference ladder and sixteen comparators. Some DNL errors are present in the coarse stage (Fig. 8), which originates from the gain, decision and reference ladder inaccuracies. To avoid loading of the test scheme onto the error contributors in the sensitive analog signal paths, and to be able to mimic and analyze the stage-under-test (SUT) behavior, the basic element to be measured in each group of the gain-, decision- and reference ladder-based DLPMs is an exact replica of the original circuit in the targeted stage-under-test. Figures 9–11 illustrate the histogram estimated from 1680 samples extracted from 48 specific DLPMs in coarse stage and measured across 35 prototype devices. The monitoring circuit is designed to maximize the sensitivity of the circuit to the target parameter to be measured. The DLPM measurements are directly related to asymmetries between the branches composing the circuit, giving an estimation of the offset when both DLPM inputs are grounded or set at a predefined common-mode voltage. The circuit is small and stand-alone, it matches the physical layout of the extracted device under test, and consumes no power while in off state. Repetitive single die-level process monitor measurements for each group of monitors are performed to minimize noise errors.

Since different transistors are measured sequentially the *dc* repeatability of the *dc* gate voltage source must be larger than the smallest gate-voltage offset to be measured. The repeatability of the source in the measurement set-up was better than six digits. The extracted DLPM and DNL

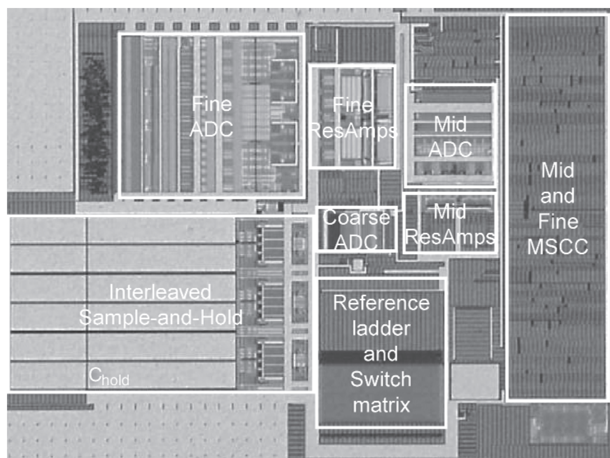

Fig. 7. Chip micrograph.

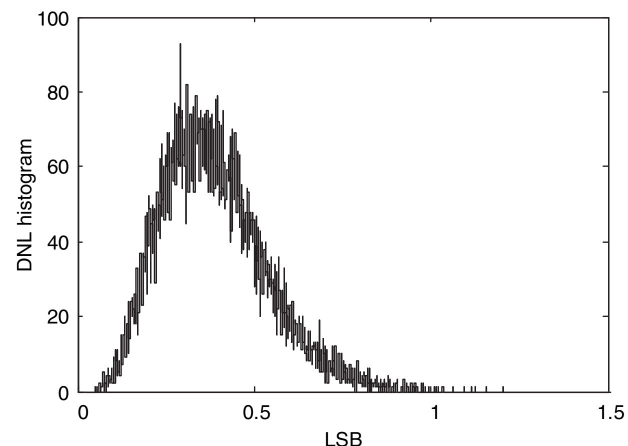

Fig. 8. Coarse A/D converter DNL histogram.

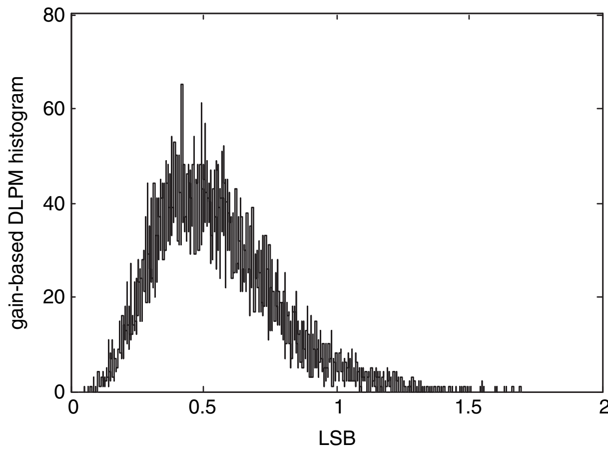

Fig. 9. Gain-based DLPM histogram.

measurements of each stage of the multi-step A/D converter are correlated with the EM-algorithm. The mean μ and the variance σ of λ, η, and γ are estimated based on the EM-algorithm (Figs. 12 and 13). As the main statistical concern is the estimation of the (randomly varying) performance functions λ, η, and γ, the EM algorithm substitutes the DLPM measurements in the log likelihood function, not in the incomplete data set; the missing values are substituted by the conditional expectations of their functions as they appear in the log-likelihood function. The DLPM measurement is the set of observations, whereas each element of the DNL measurement set is defined as a two-component vector consisting of an observation and an indicator specifying which component of the mixture occurred during that observation. To make the problem manageable, the process parameter variation model is assumed to follow a Gaussian distribution.

The mixtures of Gaussians are initialized by applying the EM equations to the observed mixtures of two univariate Gaussian components based on the DLPM and the coarse A/D converter DNL measurements. This observed process related information allows design re-centering,

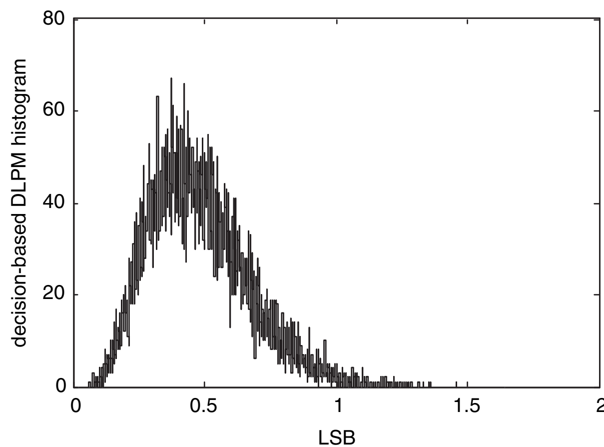

Fig. 10. Decision-based DLPM histogram.

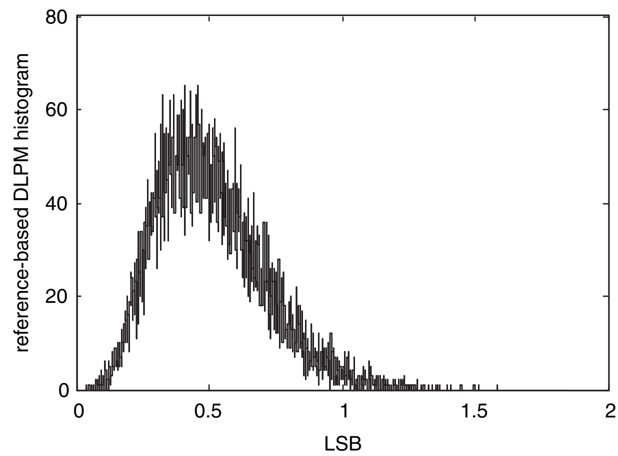

Fig. 11. Reference based DLPM histogram.

e.g., test limit setting with the ASVM classifier. Through the quadratic programming optimization, the input vectors belonging to *a priori* (nominal values) and *a posteriori* (values estimated with the EM algorithm) classes are divided into a number of sub-sets. The quadratic programming problem is solved incrementally, covering all the sub-sets of classes constructing the optimal separating hyperplane for the full data set. Note that during this process the value of the functional vector of parameters is monotonically increasing, since more and more training vectors are considered in the optimization leading to a smaller and smaller separation between the two classes. As illustrated in Figure 14, the high limit value is updated in the corresponding functional test specs of the stage-under-test with 0.35 LSB. Following a similar procedure, the high limit values of the mid and fine stages and the overall multi-step A/D converter are updated with 0.3, 0.2 and 0.15 LSB, respectively. This on the fly test limit setting leads to increased yield as illustrated in Figure 15.

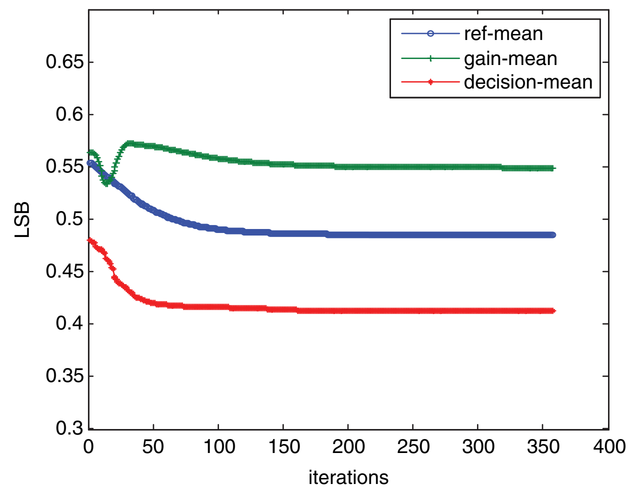

Fig. 12. Estimating mean values of λ, η, and γ with respect to the number of iterations of the EM.

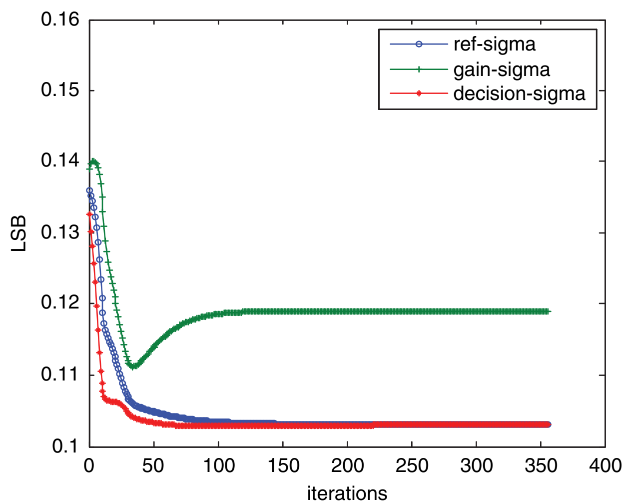

Fig. 13. Estimating variance values of λ, η, and γ with respect to the number of iterations of the EM.

The cumulative differential non-linearity is obtained across a projected 10000 devices showing similar characteristics as a measured prototype.

5.2. Application of Results for A/D Converter Debugging and Calibration

The test shell contains all functional control logic, the digital test bus, a test control block (TCB) and a CTAG isolation chain. Testing of each stage is performed sequentially starting from the first stage. Since there is no feedback from the mid and fine A/D converters to the coarse result value, it is not necessary to set these two A/D converters at a fixed value to test the coarse A/D converter. However, since the calibration D/A converter settings do show in the

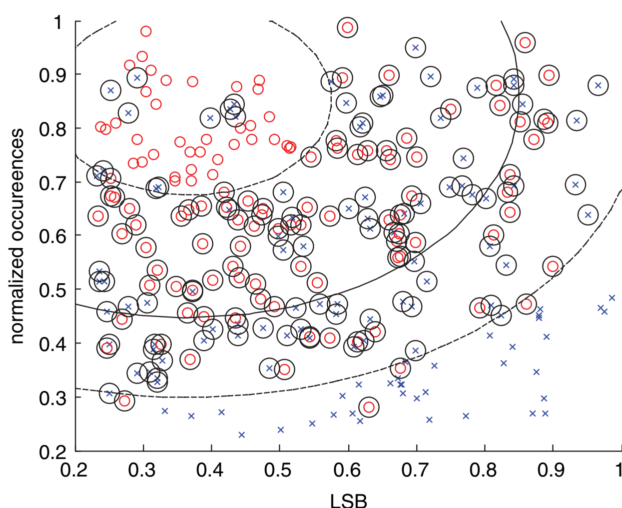

Fig. 14. Fitting a posteriori probability to the SVM output. The support vectors, marked with larger circles, define the margin of separation between the classes of multiple runs of DLPM (crosses) and DUT measurements (smaller circles).

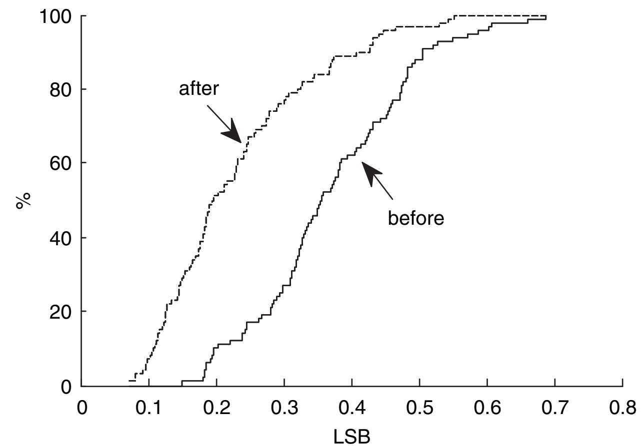

Fig. 15. DNL cumulative histograms of 10 000 devices before and after adjusting the tolerance limits.

mid A/D converter results, the sub-D/A converter is set to a known value to prevent interference with the mid A/D converter test results. Similar to the mid A/D converter, the fine A/D converter cannot be monitored directly due to the overlap in the A/D converter ranges. The predefined input signals are extracted when the A/D converter operates in a normal application mode. At a certain moment the scan chains are set to a hold mode to acquire the requested value. Now, the residue signals derived through the predefined input signals evaluate the fine A/D converter performance. The calibration signals need to be active as well for the fine A/D converter test. To verify offsets, a similar procedure as in the mid A/D converter is followed. The calibration D/A converter settings have to be known and set to a known value to prevent interference with test results.

The calibration technique was verified for all stages with full scale inputs. If the analog input to the calibrated A/D converter is such that the code transition is i, then the code transition of the ideal A/D converter is either i or $i+1$. The offset between the digital outputs of these two converters for the range of analog inputs is denoted Δ_{i1} and Δ_{i2}, respectively. If a calibrated A/D converter has no errors in the internal reference voltages γ and neither has stage gain errors η, the difference between the calibrated and ideal A/D converter outputs is constant regardless of the analog input, thus $\Delta_{i1} = \Delta_{i2}$. If errors γ and η are included, then the calibrated A/D converter shows unique missing codes. The difference between Δ_{i1} and Δ_{i2} gives the error due to missing codes that occur when the ideal A/D converter changes from code i to code $i+1$. The unique error due to missing codes at all other transitions can be measured in a similar manner. With errors from missing codes at each measured transition, the calibrated A/D converter stage is corrected by shifting the converter's digital output as a function of the transition points such that the overall transfer function of the calibrated A/D converter is free from missing codes. As long as the input is sufficiently rapid to

generate a sufficient number of estimates of Δ_{i1}, Δ_{i2}, for all i, there is no constraint on the shape of the input signal to the A/D converter. A constant offset between the calibrated and ideal A/D converter appears as a common-mode shift in both Δ_{i1} and Δ_{i2}. Since the number of missing codes at each code transition is measured by subtracting Δ_{i2} from Δ_{i1}, the common mode is eliminated and thus input-referred offsets of the calibrated A/D converter have no impact in the calibration scheme (under the practical assumption that the offsets are not large enough to saturate the output of the converter stages).

It is important to note that the steepest-descent debugging and calibration algorithm, which captures random statistical process variations of device characteristics (manifested through λ, η, and γ errors) in the observed multi-step A/D converter, can operate independently from DLPM and temperature sensor measurements. Statistical data extracted through the DLPM measurements coupled with conditional distribution of DNL data obtained with the EM algorithm supplement the debugging process by enhancing observation and characterization of the current process variability conditions of parameters of interest. The correction parameters are shown in Figures 16 and 17. The largest correction values significantly decrease with the amount of samples. As an ideal A/D converter offers an ideal reference for the calibrated A/D converter, the error signal used for the algorithm adaptation is highly correlated with the error between them, thus steady state convergence occurs within a relatively short time interval. Different λ, η, and γ are generated randomly, so that the relative errors are uniformly distributed in the interval $[-0.1, 0.1]$. At first, μ is set to $1/4$ to speed up the algorithm, then μ is set to $1/64$ after 1000 iterations to improve the accuracy. Calibration results measured at several temperatures are summarized in Table I. A summary of the converter performance at 30 °C and comparison with previous works is shown in Table II.

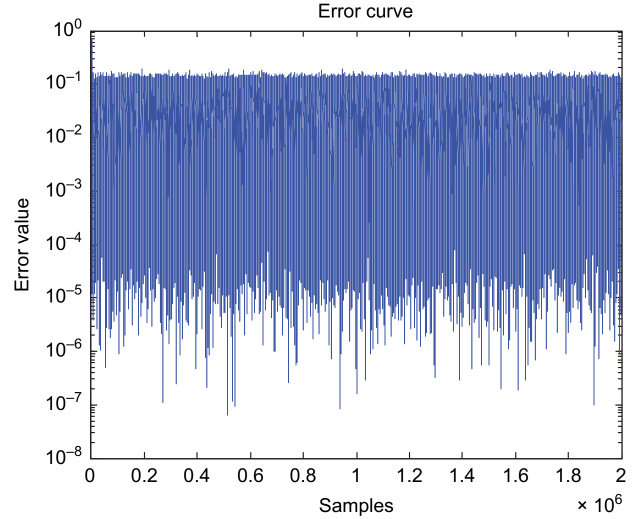

Fig. 17. Mean-square error for two million samples.

A code density test was conducted to obtain static linearity of the proposed A/D converter. DNL (Fig. 18) and INL (Fig. 19) are measured with a signal frequency of 1 kHz and 15 MS/s, and THD and SNR are obtained with 25 MHz input signal and 60 MS/s sampling frequency (Fig. 20). The largest spike, other than the fundamental input signal, is the spurious harmonic which appears at $fs/3 \pm f_{\text{in}}$ and is about 78 dB below the fundamental signal. A locked histogram test revealed a 2.6-ps rms jitter in the system including the clock generator, the synthesizer,

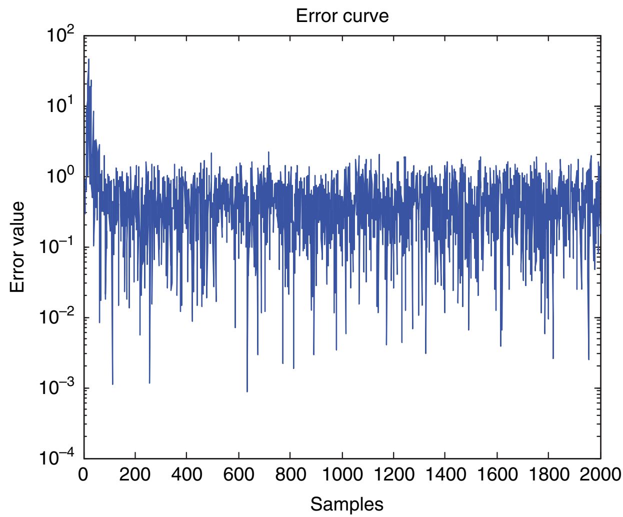

Fig. 16. Mean-square error for two thousand samples. The quality criterion adopted for an estimator is the mean-squared error criterion, mainly because it represents the energy in the error signal, is easy to differentiate and provides the possibilities to assign the weights.

Table I. Summary of the calibration performance.

	Before	(0 °C)	(30 °C)	(90 °C)
Coarse A/D converter				
DNL	±0.5 LSB	±0.5 LSB	±0.4 LSB	±0.4 LSB
INL	±0.7 LSB	±0.7 LSB	±0.6 LSB	±0.6 LSB
THD	−26.1 dB	−26.4 dB	−26.7 dB	−26.5 dB
SNR	23.7 dB	23.9 dB	24.3 dB	23.8 dB
Mid A/D converter				
DNL	±0.7 LSB	±0.7 LSB	±0.5 LSB	±0.6 LSB
INL	±1.8 LSB	±0.8 LSB	±0.6 LSB	±0.7 LSB
THD	−13.8 dB	−24.8 dB	−26.1 dB	−25.3 dB
SNR	12.4 dB	21.3 dB	23.5 dB	22.4 dB
Fine A/D converter				
DNL	±0.9 LSB	±0.9 LSB	±0.6 LSB	±0.8 LSB
INL	±2.6 LSB	±1.0 LSB	±0.9 LSB	±0.9 LSB
THD	−18.3 dB	− 33.7 dB	−35.8 dB	−33.2 dB
SNR	15.6 dB	29.5 dB	31.4 dB	29.1 dB
Total A/D converter				
DNL	±1.4 LSB	±1.2 LSB	±0.7 LSB	±1.1 LSB
INL	±4.1 LSB	±1.5 LSB	±1.2 LSB	±1.4 LSB
THD	−46.6 dB	−69.4 dB	−73.5 dB	−70.9 dB
SNR	41.5 dB	67.3 dB	70.3 dB	68.7 dB

Table II. Summary of A/D converter performance and comparision with prior art.

	[2]	[3]	[4]	[5]	[6]	[7]	[This work]
CMOS technology	0.6 μm	0.35 μm	0.18 μm	0.13 μm	90 nm	90 nm	90 nm
Resolution (bit)	12	12	12	12	12 (nom)	12	12
Supply voltage (V)	5	3.3	1.8	1.2	1.2	1.2	1.2
Sample rate (MS/s)	33	20	40	120	100	200	60
Eff. Bandw. (MHz)	16	10	20	60	50	91	30
DNL (LSB)	±0.8	±0.42	±1	±0.3	±0.54	+0.8/−0.6	±0.7
INL (LSB)	±1	±0.75	+1.7/−1.97	+0.95	±368	+1.3/−1.7	±1.2
SNR (dB)	—	—	62.2	—	70	—	70.3
SNDR (dB)	70.3	70.2	62	74.7	68.8	61.6	68.6
Calibration	Piecew. Lin.	Nested	off chip	off chip	HDC	LMS	SDM
Power (mW)	650	231	72	51.6	130	348	55
Area (mm^2)	3	7.5	1.9	0.56	4	1.36	0.75

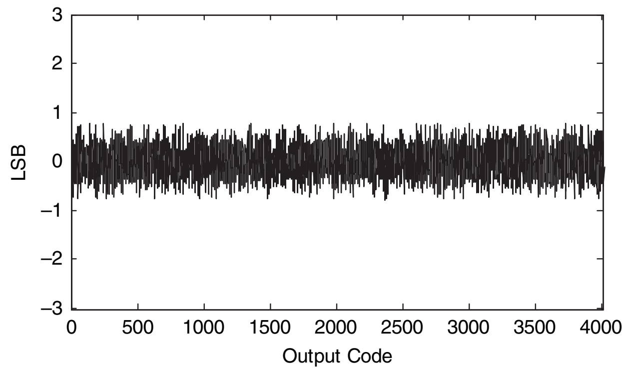

Fig. 18. DNL after calibration.

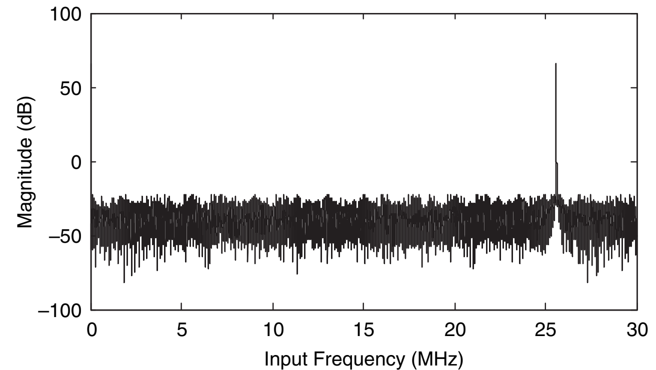

Fig. 20. Frequency spectrum at 60 MS/s with an input frequency of 25.6 MHz.

the A/D comparator chip and the board, which translates to a 66-dB SNR at 15 MHz approximately. This confirms the observation that the performance of this converter is limited by the clock jitter at high input frequencies. The measured behavior of the temperature monitor shows the typical bandgap-curve which reaches a maximum at 810 mV close to the target of 800 mV without trimming. Results from 35 prototype samples show a standard deviation of the bandgap output voltage of 4.5 mV. The temperature sensor switches at intervals of 10 °C as measured on a digital production IC tester. We observe that the improvement of DNL and INL is coincident with the fact that the mismatch increases when decreasing the temperature. Therefore, as the worst case mismatch and temperature condition, the lower end (0 °C) of the used temperature scale (0 °C to 90 °C) is observed. The linearity measurements show bathtub-like features since at the higher temperature end, mobility degradation deteriorates the circuit performance. The DLPM measurements show that at optimal temperature (30 °C), the standard deviation Stdev (ΔV_{Tsat}) decreases by 0.16 mV. This compares reasonably well with the measured improvement in I_{Dsat} matching of 0.032%. The threshold voltage matching coefficient A_{VT}, the standard deviation of percent ΔI_{D} and the current matching coefficient A_{ID} improve by 0.3 mVμm, 0.032% (0.036 μA), and 0.06% μm, respectively.

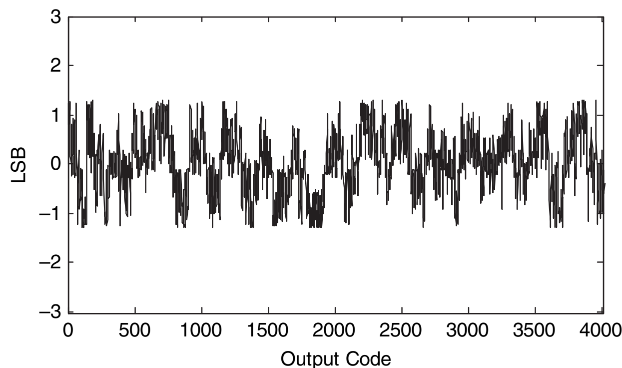

Fig. 19. INL after calibration.

6. CONCLUSION

The feasibility of the calibration method has been verified by experimental measurements from the silicon prototype fabricated in standard single poly, six metal 90 nm CMOS. The stand-alone A/D converter occupies an area of 0.75 mm^2 operates at 1.2 V supply voltage and dissipates 55 mW (without output buffers). The calibration algorithm requires about 1.5 k logic gates, occupies an area of 0.14 mm^2 and consumes 11 mW of power. The monitors allow the readout of local (within

the core) performance parameters as well as the global distribution of these parameters. The flexibility of the concept allows the system to be easily extended with a variety of other performance sensors. The implemented expectation-maximization algorithm and adjusted support vector machine classifier allow us to guide the verification process with the information obtained through monitoring process variations. Fast identification of excessive process parameter variation effects is facilitated at the cost of at most 10% area overhead, and 8 mW and 0.4 mW of power consumption when in active and passive mode, respectively.

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