general, p-Si NWs grown with a higher dopant ratio (SiH_4:B_2H_6 = 1000:1) have lower resistance and smaller on/off ratios of ~10^3; those synthesized with a lower dopant ratio (6000:1) have higher resistance and larger on/off ratios of ~10^4 to 10^5. In addition, the carrier mobility typically varies from 30 to 200 cm^2/V-s, depending on doping.
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Logic Circuits with Carbon Nanotube Transistors

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We demonstrate logic circuits with field-effect transistors based on single carbon nanotubes. Our device layout features local gates that provide excellent capacitive coupling between the gate and nanotube, enabling strong electrostatic doping of the nanotube from *p*-doping to *n*-doping and the study of the nonconventional long-range screening of charge along the one-dimensional nanotubes. The transistors show favorable device characteristics such as high gain (>10), a large on-off ratio (>10^5), and room-temperature operation. Importantly, the local-gate layout allows for integration of multiple devices on a single chip. Indeed, we demonstrate one-, two-, and three-transistor circuits that exhibit a range of digital logic operations, such as an inverter, a logic NOR, a static random-access memory cell, and an ac ring oscillator.

The anticipated limits to the further miniaturization of microelectronics have led to intense research directed toward the development of molecular electronics (*1*). The use of single-wall carbon nanotubes has stimulated these efforts, because these molecules exhibit a range of suitable properties for nanoelectronics. Various basic single-nanotube components have recently been demonstrated, such as molecular wires, diodes, field-effect transistors, and single-electron transistors (*2*–*8*). The next challenge in the development of molecular electronics is to go beyond single-molecule components and integrate such devices onto a chip to demonstrate digital logic operations. Here, we report such logic circuits composed of single-nanotube field-effect transistors. In addition to the realization of logic circuits, our new device layout also enables substantial electrostatic doping for modest gate voltages, which allows us to study the nonconventional screening of charge along the one-dimensional nanotubes.

Our nanotube transistors have a local gate that is insulated from the nanotube by a gate oxide layer of only a few nanometers thickness. In previous circuits, the gate consisted of an oxidized Si wafer (*6, 7, 9*), the tip of an atomic force microscope (*10*–*12*), a second nanotube (*13*), an ionic solution (*14*), or a capping Al film (*15*). The layouts of these devices do not allow integration of multiply connected devices (*16*). For example, the most popular nanotube-transistor layout uses a backgate, which applies the same gate voltage to all transistors on the chip. In contrast, our gate consists of a microfabricated Al wire with a well-insulating native Al_2O_3 layer (*17*), which lies beneath a semiconducting nanotube that is electrically contacted to two Au electrodes (Fig. 1, A and B). In this configuration, the Al_2O_3 thickness of a few nanometers is much shorter than the separation between the contact electrodes (~100 nm), enabling an excellent capacitive coupling between the gate and the nanotube. Moreover, different local Al gates can easily be patterned such that each one addresses a different nanotube transistor. This layout thus allows the integration of multiple nanotube field-effect transistors (FETs) on the same chip (Fig. 1C).

Our nanotube circuits are realized in a three-step process. First, Al gates are patterned using electron beam lithography (*18*) on an oxidized Si wafer. The insulating layer consists of the native oxide that grows by exposing the sample to air. The precise thickness of this layer is difficult to determine, but is on the order of a few nanometers (*19*). Second, single-wall carbon nanotubes produced by laser ablation are dispersed on the wafer from a dichloroethane suspension. With an atomic force microscope, those nanotubes are selected that have a diameter of about 1 nm and that are situated on top of the Al gate wires. Their coordinates are registered with respect to alignment markers. Finally, contact electrodes and interconnect wires are fabricated with electron-beam lithography by evaporating Au directly on the nanotube without an adhesion layer.

Very strong doping of the nanotube channel can be achieved with this layout (Fig. 2A) (*20*). Starting from a negative gate voltage V_g, the current I first decreases, then becomes immeasurably small, and finally increases again. This indicates that V_g shifts the Fermi level successively from the valence band (accumulation regime) to the gap (depletion), and finally to the conduction band (inversion) of the semiconducting nanotube. The nearby Al gate thus makes it possible to change the doping of the nanotube over the full range from the *p*- to the *n*-doped regime.

Our nanotube transistors can be classified as enhancement-mode *p*-type FETs (*21*), because a strong modulation of the current through the nanotube FET is possible when a small negative gate voltage is applied. The current versus bias voltage V_{sd} characteristics (Fig. 3) are typical for FETs (*22*). From the data in Figs. 2 and 3, we can extract a transconductance of our nanotube transistors of 0.3 μS and a lower limit of the on/off ratio of at least 10^5. The maximum current at which the nanotube transistor can operate is on the order of 100 nA and the on-resistance is 26 megaohms for V_{sd} = –1.3 V and V_g = –1.3 V.

For any further development of operational logic circuits, a gain (>1) at large bias voltage is a crucial requirement, because the output of one logic structure must be able to drive the input of the next logic structure. The output typically has to provide a voltage swing of about 1 V. Figure 3 indicates that in our transistors, a change in the output by more than 1 V occurs when the input voltage is changed by 0.1 V. This indicates a large-signal gain >10. A large gain combined with a large output swing can be obtained because the gate is so close to the nanotube. Our technique allows for a much larger gain than has been achieved with thick gate oxides or planar gates used in previous nanotube FETs (*6, 7, 9, 23*).

A major point of our report is that small circuits combining our nanotube transistors can be used for a variety of logic elements. Here, we describe our demonstration of an inverter, a

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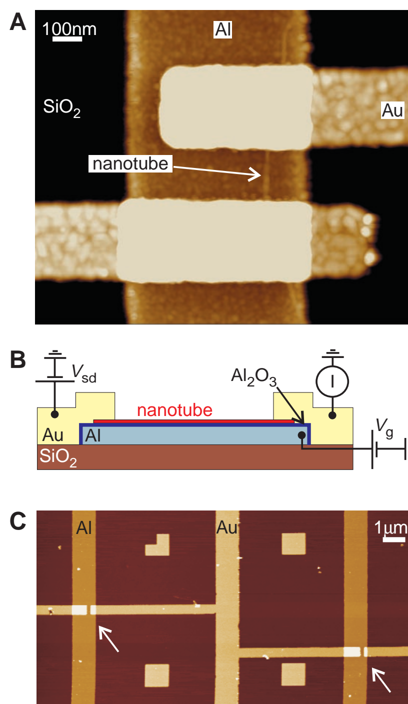

Fig. 1. Device layout. (**A**) Height image of a single-nanotube transistor, acquired with an atomic force microscope. (**B**) Schematic side view of the device. A semiconducting nanotube is contacted by two Au electrodes. An Al wire, covered by a few-nanometers-thick oxide layer, is used as a gate. (**C**) Height-mode atomic force microscope image of two nanotube transistors connected by a Au interconnect wire. The arrows indicate the position of the transistors. Four alignment markers can also be seen.

NOR gate (an inverting logical OR gate), a static random access memory (SRAM) cell, and a ring oscillator. All of these logic elements are realized using a scheme called resistor-transistor logic (*21*). In each of the logic elements, all nanotube transistors were fabricated on the same chip. They are also fully reversible, in contrast to previously reported irreversible logic elements consisting of structured molecular films (*24*). A voltage of –1.5 V across the nanotube was found to be a suitable bias voltage for logic applications. In all logic circuits described here, a voltage of 0 V represented a logical 0 and a voltage of –1.5 V represented a logical 1.

An inverter is a basic logic element that converts a logical 0 into a logical 1, and a logical 1 into a logical 0. Our inverter was constructed from a nanotube transistor and an off-chip 100-megaohm bias resistor (Fig. 4A). When the input voltage is $V_{in} = -1.5$ V (logical 1), the tube resistance is much lower than the bias resistor, setting the output voltage to 0 V (logical 0). When V_{in} is 0 V (logical 0), the nanotube is nonconducting and the output is –1.5 V (logical 1). The output voltage of an inverter should make a rapid transition from one logic level to the other as the gate voltage is swept. In the device of Fig.

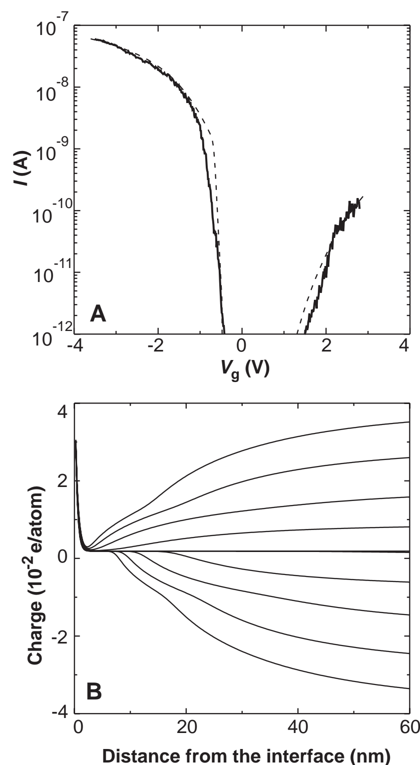

Fig. 2. Strong doping and weak screening of carbon nanotubes. (**A**) Current as a function of the gate voltage for a single-nanotube transistor at room temperature. Data were taken at $V_{sd} = 5$ mV in a vacuum (about 10^{-4} mbar). The doping of the semiconducting nanotube can be changed over a very large range from *p*-doped to *n*-doped. Good contact resistance has been achieved, as is evident from the minimal resistance of 80 kilo-ohms at $V_g = -3.5$ V. Similar $I(V_g)$ measurements on metallic nanotubes showed only minor variations of the current with the gate voltage. The dashed curve corresponds to the theory described in the text (*36*). (**B**) Charge per C atom as a function of distance away from the nanotube-electrode interface for gate voltage values from –3.48 V (top) to 3 V (bottom) with 0.72 V intervals, as resulting from the model fit to the data of (A). The data show a smooth charge variation over a very long range. The sharp increase at the interface corresponds to the metal-induced gap states.

4A, the output voltage changes three times faster than the input voltage in the transition region, indicating a voltage gain of 3 (other inverter devices showed a gain of up to 6).

A NOR gate can be constructed by simply replacing the single transistor in the inverter with two transistors in parallel (Fig. 4B). The layout of the two transistors on the same chip is shown in Fig. 1C. When either or both of the inputs are a logical 1 ($V_{in} = -1.5$ V), at least one of the nanotubes is conducting and the output is 0 V (logical 0). The output is a logical 1 only when both inputs are a logical 0, so that neither nanotube is conducting. In Fig. 4B, the output voltage is plotted as a function of the four possible input states (0,0), (0,1), (1,0), and (1,1), verifying that this circuit indeed operates as a

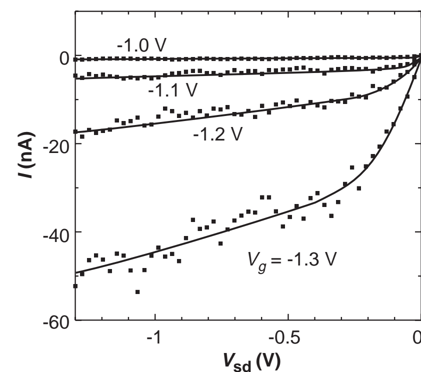

Fig. 3. Device characteristics of the nanotube transistor. Typical I-V_{sd} curves measured at room temperature for various values of V_g. In the linear regime at small source-drain voltages, the current is proportional to V_{sd}. In the saturation regime at higher source-drain voltages (that is, when V_{sd} becomes more negative than $V_g - V_t$), the current through the transistor changes more gradually. For a constant V_{sd} in the saturation regime, $I(V_g)$ has an approximately parabolic dependence $I \sim (V_g - V_t)^2$, as is typical for MOSFETs. The data are for a different transistor than in Fig. 2. Lines are guides to the eye. Large gain (>10) is obtained.

NOR gate. Using variations of the device circuitry, any logical gate can be realized (AND, OR, NAND, XOR, etc.).

A flip-flop memory element (SRAM) was constructed from two inverters (Fig. 4C). When the output of each inverter is connected to the input of the other inverter, two different stable states are possible: the outputs can take on the values (1,0) or (0,1). A logical 1 is written into memory by forcing the circuit into the (0,1) state and a logical 0 is written by forcing the circuit into the (1,0) state. To test the working of the memory cell, we attached a voltage source to one input and wrote a logical 1 to V_{out} by driving V_{in} to 0 V. The switch at V_{in} was then opened and the memory cell maintained a logical 1 at the output until the switch was closed after 70 s. Then we wrote a logical 0 into V_{out} by driving V_{in} to −1.5 V. When the switch was opened again, the memory cell maintained a logical 0 at the output. These data demonstrate the stable memory function of our two-transistor nanotube SRAM circuit.

A three-transistor device was realized in a ring oscillator (Fig. 4D). This circuit, used to generate an oscillating ac voltage signal, was built by connecting three inverters in a ring. A ring oscillator has no statically stable solution, and the voltage at the output of each inverter oscillates as a function of time (Fig. 4D). The 5-Hz frequency of the oscillations is determined by the resistance of the inverters (~1 gigaohm) and the capacitance of the output nodes, which currently is dominated by the ~100 pF parasitic capacitance of the wires connecting to the off-chip bias resistors. This frequency can obviously be increased by many orders of magnitude by

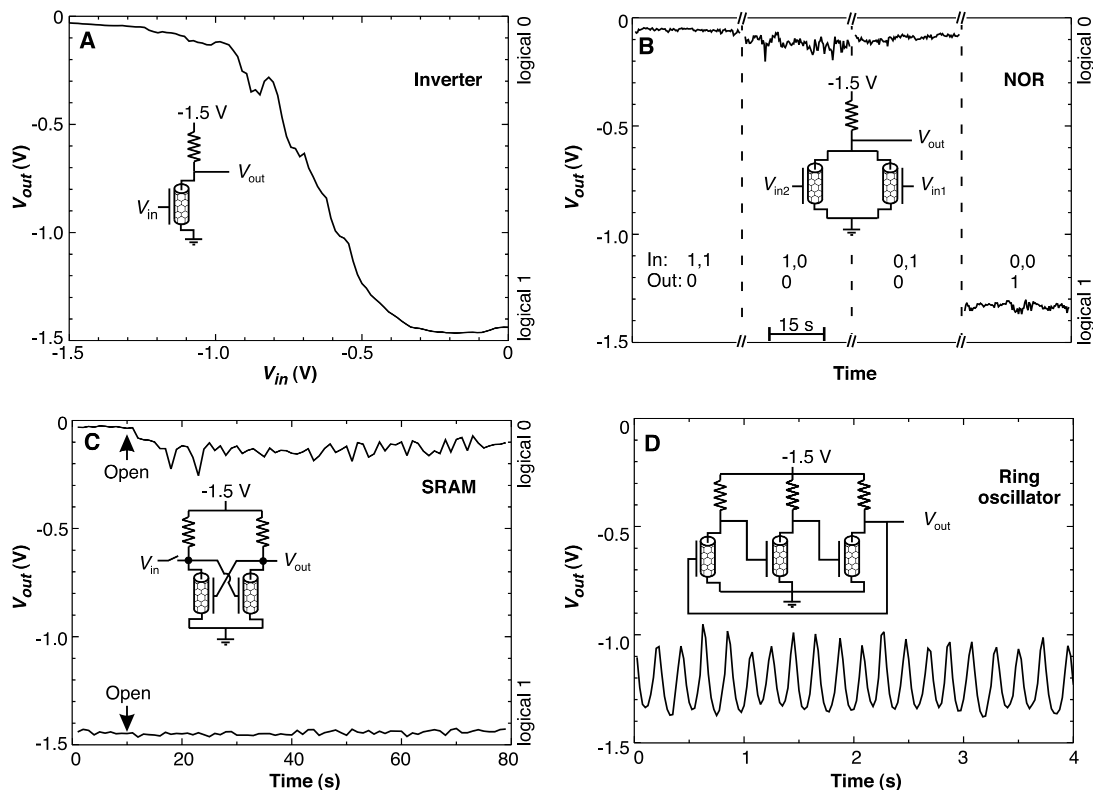

Fig. 4. Demonstration of one-, two-, and three-transistor logic circuits with carbon nanotube FETs. (**A**) Output voltage as a function of the input voltage of a nanotube inverter. (Inset) Schematic of the electronic circuit. The resistance is 100 megaohms. (**B**) Output voltage of a nanotubes NOR for the four possible input states (1,1), (1,0), (0,1), and (0,0). A voltage of 0 V represents a logical 0 and a voltage of –1.5 V represents a logical 1. The resistance is 50 megaohms. (**C**) Output voltage of a flip-flop memory cell (SRAM) composed of two nanotube FETs. The output logical stays at 0 or 1 after the switch to the input has been opened. The two resistances are 100 megaohms and 2 gigaohms. (**D**) Output voltage as a function of time for a nanotube ring oscillator. The three resistances are 100 megaohms, 100 megaohms, and 2 gigaohms.

fabricating the resistors on-chip in the future.

Our nanotube logic circuits act in the same way as conventional silicon electronics, but our new device layout also allows us to probe some interesting new physical phenomena that are unique to nanotubes. As shown in Fig. 2, we can achieve very strong doping of the nanotubes. Measurements of $I(V_g)$ on previously reported layouts (*6, 7*) showed a limited range of doping and the mechanism of the current variation remained unclear. By contrast, the present data provide much more information and allow a comparison with a semi-classical model based on Poisson's equation. In this recently proposed model (*25, 26*), the current variation originates from the modulation of the barrier profile formed at the nanotube-electrode junction. The band bending was calculated self-consistently with inclusion of long-range Coulomb interactions and the density of states of semiconducting nanotubes (*27*). The conductance was determined at 300 K using the WKB approximation and the Landauer formula. The calculated $I(V_g)$ (dashed curve in Fig. 2A) is in quite good agreement with the measurements. The model reproduces the V_g gap size as well as the asymmetry on the *p*- and *n*-side. Details of the calculation are presented as supplementary data (*28*). Similar $I(V_g)$ measurements have been obtained for other samples and could be fitted with the same accuracy.

In their recent theoretical work, Léonard and Tersoff (*26*) calculated the charge distribution near the interface between a doped semiconducting nanotube and an electrode, and showed that the charge distribution decays logarithmically with distance from the interface. This is profoundly different from a conventional three-dimensional Schottky barrier, where the charge depletion region is ended by an abrupt transition. The difference arises from the poor screening in the nanotubes, which derives from their true one-dimensionality. From the fit to our $I(V_g)$ measurements, the charge distribution can be calculated for each gate voltage (Fig. 2B). It can be seen that the charge varies smoothly on a 50-nm scale. Our data thus indicate that the charge distribution in a carbon nanotube varies over a very long spatial range. For the ultimate miniaturization of nanotube transistors, it will be useful to minimize the length scale of this variation by tuning parameters such as the work function difference between nanotube and electrode.

The realization of digital logic with nanotube FET circuits represents an important step toward nanoelectronics. Still, hurdles remain. For example, we are not yet able to position many semiconducting nanotubes on specific locations of a wafer. This might, however, change rapidly with recent progress such as local on-chip nanotube growth (*29*), self-assembly (*30*), liquid-flow alignment (*31*), selective nanotube burning (*32*), and controlled-chirality growth (*33*). Further steps can be undertaken towards increasing device speed, and towards combining *p*- and *n*-doped nanotubes in logic circuits to decrease the power dissipation. Control over such doping can be achieved chemically (*9*) or electrostatically such as in Fig. 2A. The outlook for further development of nanotube-based logic thus is promising. It is very gratifying to observe that logic devices can now be constructed based on the modulation of currents through individual molecules.

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20. Several volts can been applied to the gate without destroying the oxide layer. This is quite remarkable because the insulator layer is only a few nanometers thick, and it indicates the excellent quality of the gate oxide. The breakdown threshold voltage where the layer is destroyed is typically between 2 and >4 V. A small gate leakage current (a few pA) is observed for V_g approaching such large gate voltages. The whole $I(V_g)$ curve may be somewhat shifted horizontally in a hysteretic way after a sweep to such extreme gate voltages (~4 V). For this reason, we refrain from fitting the horizontal position of the $I(V_g)$ curve with the theory that is discussed in the text.
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37. We thank R. E. Smalley for providing the nanotubes, H. W. Ch. Postma and Y. M. Blanter for discussions, E. Swinkels and C. P. Heij for assistance with measurements of the oxide thickness, and B. van den Enden for technical assistance. The research has been supported by the European Community SATURN project and by the Dutch Foundation for Fundamental Research on Material (FOM).

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Bose-Einstein Condensation of Potassium Atoms by Sympathetic Cooling

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We report on the Bose-Einstein condensation of potassium atoms, whereby quantum degeneracy is achieved by sympathetic cooling with evaporatively cooled rubidium. Because of the rapid thermalization of the two different atoms, the efficiency of the cooling process is high. The ability to achieve condensation by sympathetic cooling with a different species may provide a route to the production of degenerate systems with a larger choice of components.

Since the first realizations of Bose-Einstein condensation (BEC) in a dilute gas of alkali atoms (*1–3*), research in the interdisciplinary fields of atom optics and quantum fluids has flourished (*4*). BEC has been observed in five atomic species: H (*5*), ^{4}He (*6*), ^{7}Li (*3*), ^{23}Na (*2*), and the two isotopes ^{85}Rb (*7*) and ^{87}Rb (*1*). Direct forced evaporative cooling of the bosonic isotopes of potassium has been prevented by limitations in the temperature and density ranges achievable by laser cooling (*8*). We show that by taking advantage of thermalization between a small dilute sample of potassium (^{41}K) and evaporatively cooled rubidium (^{87}Rb), these limitations can be overcome. The technique of sympathetic cooling had been proposed for the cooling of ions (*9*) and, in the case of neutral trapped atoms, has been used to obtain quantum degeneracy, but only for two different internal states of the same atom (*10*) or for two isotopes of the same species (*11–13*). The mixing of two different atomic species turned out to be a successful strategy, although their interaction properties could be discovered only by attempting the experiment. In the case of K, sympathetic cooling of its fermionic isotope ^{40}K (*14*) with Rb represents the natural extension of this technique, and may be a new way to explore the physics below Fermi temperature (*15*), as demonstrated in the case of Li (*12*, *16*).

The experimental apparatus is based on a conventional double magneto-optical trap (MOT) apparatus, although the complexity is increased because of the requirement for the simultaneous trapping and cooling of two different atomic species. K and Rb atoms are captured from a vapor background in the first MOT (MOT1) and then transferred by resonant laser beams to a second cell with a much lower background pressure, where they are recaptured in a second MOT (MOT2) and loaded in a magnetic trap. Evaporative cooling of Rb is performed, and the evolution of both samples is monitored by means of absorption imaging.

The laser system to manipulate the two atomic species consists of three sources: a titanium:sapphire laser operating on the K optical transitions (767 nm) and two diode lasers operating on the Rb transitions (780 nm). The two pairs of frequencies at different wavelengths necessary for magneto-optical trapping are then injected simultaneously in a semiconductor tapered amplifier (TA), which provides the required power for the two MOTs (*17*).

The experimental sequence begins with the loading of Rb in MOT2 for 30 s. During this phase, the TA power is totally dedicated to Rb, and 10^9 Rb atoms are loaded into MOT2. Half of the TA power is then switched to K, and about 10^7 K atoms are loaded into MOT2 in 8 s. The overall efficiency of the Rb MOT in this phase is strongly reduced because of nonlinear processes in the TA, resulting in a loss of about 50% of the initial Rb sample (*18*).

The magnetic trap consists of a Ioffe-Pritchard potential created by three coils in quadrupole Ioffe configuration (QUIC) (*19*). Both species are optically pumped into the low-field seeking state $|F = 2, m_F = 2\rangle$, before magnetic trapping. The typical axial and radial oscillation frequencies of Rb in the harmonic trap are $\nu_{ax} = 16$ Hz and $\nu_{rad} = 200$ Hz, respectively, whereas those of K are larger by a factor $(M_{Rb}/M_K)^{1/2} = 1.46$, where M_{Rb} and M_K are the masses of the two species. In the QUIC, we typically load 2×10^8 Rb atoms and 2×10^6 K atoms, with both at a temperature of about 300 μK.

Evaporative cooling of Rb is done with a microwave knife tuned to the hyperfine transition at 6.8 GHz, which induces transitions from the trapped state to the untrapped $|F = 1, m_F = 1\rangle$ state, without affecting the K sample. Thus, the evaporation reduces the temperature of both trapped samples, in principle keeping the K population constant. Actually, we observe losses of K atoms in the first part of the evaporation, which can be minimized by forcing the speed of the evaporation ramp. We attribute these losses

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