IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 6 April 2023, accepted 25 May 2023, date of publication 30 May 2023, date of current version 13 June 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3281500

RESEARCH ARTICLE

Dynamic Time Warping Based Pilot Protection Algorithm for AC and HVDC Transmission Lines

GIOVANNI MANASSERO Jr., (Member, IEEE), AND RODRIGO ROZENBLIT TIFERES, (Member, IEEE)
Departamento de Engenharia de Energia e Automação Elétricas da Escola Politécnica da Universidade de São Paulo, São Paulo 05508-010, Brazil
Corresponding author: Giovanni Manassero Jr. (manassero@usp.br)

This work was supported in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior—Brasil (CAPES) — Finance Code 001.

ABSTRACT This paper presents a pilot protection algorithm for alternating (ac) and direct current (dc) transmission lines, the last in the line commutated converter and voltage source converter topologies. The main contribution of this research lies, in this context, in the development of a protection method for lines of different natures. This method relies on the dynamic time warping (DTW) technique. The solution is attractive as it does not require any line or system parameters and works only with current samples. For ac lines, the algorithm uses DTW to evaluate the line terminals phase currents' and the zero-sequence components' similarities and detect faults. In turn, for dc lines, the method employs DTW technique to evaluate the similarities of cross-currents between poles and terminals and identify internal dc faults. The authors tested the algorithm for each line topology through several fault simulations, also considering the challenging conditions of high impedance internal faults, sampled noises, misalignment between samples, current transformer saturation, power swing, and internal fault with outfeed. This solution was also tested against field-recorded data in existing lines, and the resulting trip times were compared with the ones of the actual protection devices. All results indicate that this solution yields a rapid, effective, secure, and dependable protection.

INDEX TERMS Power transmission lines, line commutated converter, voltage source converter, pilot protection, dynamic time warping.

I. INTRODUCTION

Modern electrical power systems' generation points are predominantly located afar from the load and energy consumption centers. Thus, for the power supply to be as continuous and within quality standards as possible, transmission grids composed of several power lines are essential. Most transmission lines (TLs) operate in alternating current (ac), given the generation with synchronous machines and excellent efficiency of power transformers to raise and lower voltage levels. However, with the technological evolution of power electronics devices that took place in recent decades, high-voltage (HV) direct current (dc) transmission has been proving to be a cost-effective and flexible alternative for energy transportation over long distances, and therefore is progressively more present in nowadays power grids [1], [2], [3].

The two most common topologies of HVdc systems are line commutated converter (LCC) and voltage source converter (VSC). LCC systems, in which the converter stations are composed of thyristors, are used for long-distance bulk power transmission. VSC systems, which in turn are based on transistors and pulse width modulation, have been increasingly used as these solutions operate with weak ac systems and do not present commutation failures, among other aspects [1].

Regardless of the topology or whether the operation is in ac or dc, TLs typically have extensive lengths and are subject to different weather conditions. Thus, the occurrence of faults in lines is significantly higher than in other equipment in

The associate editor coordinating the review of this manuscript and approving it for publication was Arturo Conde.

electrical systems. Thereby, all lines must be equipped with protection systems that detect internal faults rapidly, accurately, and reliably.

In the context of ac lines, pilot protection has been used on an increasing scale as solutions of this nature protect the line in its full extension and typically present fast and accurate fault detection, even in cases involving high impedance faults. Conventional pilot protection solutions for ac lines use the differential function with the phasors of the line terminal currents [4]. The most consolidated technique for estimation and analysis in the frequency domain, due to its low computational burden, is the discrete Fourier transform (DFT) [5]. However, the problems that DFT-based algorithms present due to the dc components in the fault currents and variations in frequency are well-known. In this way, various authors constantly propose new alternatives that dismiss phasor quantities.

References [6] and [7], for instance, present solutions based on traveling waves (TW) propagation. TW-based algorithms identify and locate faults by recording the arrival times of incident and reflected wavefronts. Still, it is noteworthy that wavefront detection requires high sampling rates and may be unfavorably affected by noises and zero-crossing faults. Reference [8], in its turn, proposes algorithms that calculate the energy, active power, and reactive power flows at the terminals to identify internal faults. These methods require both voltage and current sampling, synchronization, and communication, demanding a more sophisticated protection scheme.

The authors of [9] and [10] propose pilot protection methods for ac lines that rely upon distance measurements between the terminal current samples. An internal fault is detected whether the calculated distance exceeds a predetermined minimum value. Still, such minimum distance values depend on the protected line's fault current levels, so their adjustment must be precise and may not generalized to different lines. Reference [11], distinctively, use correlation measures between samples. Yet, one can notice that using such measures as primary quantities for fault detection means that the algorithm's main tripping condition is based on a statistical magnitude rather than a result with physical interpretation.

In [12], ac fault detection depends on probability values calculated by applying Bayesian inference to the current samples. However, calculating fault probabilities requires specific setting parameters whose values that yield the method's best performance may differ from line to line. This approach also proved efficient to protect LCC-HVdc lines [13]. Still, as in the ac context, the algorithm's fault detection speed varies with the setting parameters' values and adjustments.

In the context of HVdc lines, in both LCC and VSC topologies, the most used protection functions are voltage-derivative, under-voltage, and traveling waves [14]. However, these functions may fail to operate in high impedance dc faults (dependability failures). Hence, pilot protection algorithms are also employed as backup when communication and synchronization infrastructure is available.

The conventional current differential protection of HVdc lines typically has intentional coordination delays, reaching up to 1 [s] [3]. These delays are so that external ac faults are not confused by the protection with internal dc faults, as the distributed capacitive currents that arise as a result of external events cause the terminals' currents to differ. Therefore, several solutions and approaches for HVdc pilot protection that do not require such delays have been developed.

Considering LCC-HVdc lines, the authors of [15] present a solution that uses the signed correlation index for fault classification and detection. The pilot protection solution for LCC-HVdc lines proposed in [16] uses Pearson correlation coefficients between numerical current derivative values to detect internal faults. Still, such derivatives may be adversely affected by noises. The solution presented in [17], on the contrary, differentiates internal dc faults from external ac faults using the voltage polarities on the smoothing reactors. In [18], the pilot protection alternative is knowledge-based as it employs a long short term memory neural network. It is worth mentioning, in this context, that the response and performance of knowledge-based solutions directly depend on the quality of network training.

Reference [3] proposes a pilot protection algorithm that uses the distributed parameters and the compensated current in differential mode to cope with the capacitive effect during fault. In turn, the authors of [19] present a distance protection method that reduces the intentional delays of conventional differential protection by using a sequential overlapping difference process that extracts the characteristics of fault TWs. Still, the suggested sampling frequency is 100 [kHZ], that is much higher than the ones used in commercial IEDs.

Considering VSC-HVdc lines, the algorithm presented in [20] detects dc internal faults internal through the concept proposed and defined as multiresolution morphological gradient of TWs. In [21], the discussed solution detects internal faults using the cosine similarity of the recorded TWs. Notably, these solutions need the line's parameters with considerable preciseness. In [22], the developed algorithm uses protection principle based on the aperiodic component energy.

The algorithm in [23] detects and identifies the fault type through the differential current integration. As in the solution proposed in [16], numerical derivatives may be affected depending on the sampled noise levels. On the other hand, the method proposed in [24] uses the mode transformation matrix and transfer impedances to detect dc pole-to-ground faults.

From the literature concerning pilot protection algorithms, one can notice that most approaches used to protect ac and dc lines are distinct. Furthermore, it is worth observing that the algorithms developed for LCC-HVdc lines are considerably different from the solutions proposed for dc systems in the

VSC topology. These differences are because of the nature of each system type (ac, LCC-HVdc, and VSC-HVdc) and faults. Also, it is noted that many solutions, for all the three topologies, depend directly on precise values of the system's inductances and capacitances. Still, in practical situations, such parameters vary with external factors such as temperature and humidity [25], which may influence these methods' responses.

Therefore, this paper proposes a pilot protection algorithm applicable to ac, LCC-HVdc, and VSC-HVdc lines that rely upon the same principle, which is dynamic time warping (DTW). The primary motivation for the development of this research lies, in this context, in the proposal of a solution that can be applied to all three considered line topologies, delivering fast and effective fault detection regardless of the line's layout. The proposed algorithm may be attractive as it only need current samples and dismiss any information and parameters about the protected line. From the perspective of large-scale power systems protection, encompassing lines of different topologies that can be protected with pilot protection schemes, employing a solution based on the same principle and settings may be advantageous for studies and commissioning.

For ac and dc systems, the method presented in this work rely upon an operation and a restraining magnitude, calculated through DTW and used for internal faults detection. On ac lines, the algorithm computes the magnitudes for each phase and the zero-sequence currents. In dc lines, both for LCC and VSC schemes, the operation and restraining magnitudes are calculated via the cross-currents between poles and terminals. To the best of the authors' knowledge, there is no similar approach in the power system protection literature.

The authors tested the algorithm in several fault simulations, considering lines of all the three topologies. The presented solution was also tested against high impedance internal faults and both internal and external faults under the conditions of measurements with sampled noises and misalignment between terminals' samples. For ac lines, cases featuring current transformer (CT) saturation, power swing and outfeed were also considered, alongside data recorded during actual faults in existing 500 [kV] series-compensated lines from the Brazilian interconnected power grid.

The remaining sections of this article are organized as follows: Sec. II presents a comprehensive overview of the DTW; Sec. III describes the proposed method's scheme, block diagram, and its application to ac and dc power TLs; Then, Sec. IV shows the simulated transmission systems and faults and analyzes the algorithm's results; Sec. V presents an evaluation of the method's sensitivity, regarding challenging conditions; Next, Sec. VI shows the proposed solution's performance against actual fault cases in ac TLs; and finally, Sec. VII concludes the paper.

II. DYNAMIC TIME WARPING

The dynamic time warping (DTW) algorithm is a technique that computes a similarity measurement between two

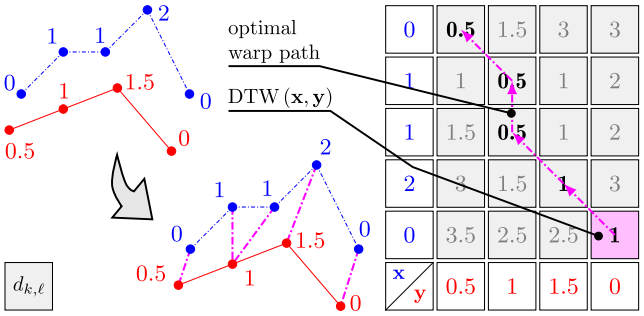

FIGURE 1. Application example of the DTW technique.

time series by determining the optimal alignment between them. Early applications of this approach encompassed mainly spoken word recognition [26], and, in nowadays data science, it is arguably the most appropriate similarity metric for a vast number of applications [27], such as clustering [28], classification [29], and pattern matching [30]. DTW employs a local distance measure to determine the similarity between the evaluated time series by calculating a warping path.

References [31], [32], and [33] propose protection algorithms based on the DTW approach. The first uses the DTW technique associated with a threshold quantity, and the second combines this technique with a ratio-restrained differential. Both references propose algorithms for the protection of just ac transmission lines. The author of [33], in turn, presents a protection function applicable for just ac distribution systems based on the DTW. These references do not deal with HVdc transmission systems and rely on calculated parameters to correctly identify internal faults to avoid security and dependability failures. Therefore, the proposed method in this article do configure a novelty since it can be applied to the three line topologies (ac, LCC-HVdc, and VSC-HVdc) and does not rely on any information and parameters about the protected line.

In this context, consider two time series $\mathbf{x}$ and $\mathbf{y}$. To measure the similarity between these series, the DTW algorithm constructs an $m \times n$ cost matrix $\mathbf{D}$, where m and n are the lengths of $\mathbf{x}$ and $\mathbf{y}$, respectively. The value of each cell in this matrix is

$$d_{k,\ell} = |x(k) - y(\ell)| + \min\left\{d_{k-1,\ell}; d_{k,\ell-1}; d_{k-1,\ell-1}\right\} \quad (1)$$

where k and ℓ indicate the k^{th} and ℓ^{th} line and column of $\mathbf{D}$. From the cost matrix, DTW determines an optimal warp path $\mathbf{W} = \{w_1, w_2, \cdots, w_p\}$, where $\max\{m, n\} \leq p < m + n$, $w_1 = (1, 1)$, and $w_p = (m, n)$, that satisfies: *continuity* (all values from one time series must match one or more values of the other); *boundary conditions* (the first and last values from one time series must match the first and last value of the other, respectively); and *monotonicity* (matches between time series must be monotonically increasing). Finally, the optimal alignment's cost, DTW $(\mathbf{x}, \mathbf{y})$, is the value of $d_{m,n}$, which equals the sum of distances between the two series' elements in the optimal warp path.

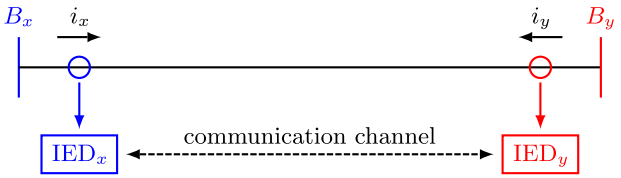

FIGURE 2. Pilot protection topology.

As an application example, consider the two time series $\mathbf{x} = \{0, 1, 1, 2, 0\}$ and $\mathbf{y} = \{0.5, 1, 1.5, 0\}$, as depicted in Fig. 1. The cost matrix $\mathbf{D}$, the optimal warp path $\mathbf{W}$, and the resulting value DTW $(\mathbf{x}, \mathbf{y})$, obtained using the DTW algorithm, are also illustrated in this figure.

III. METHODOLOGY

This work proposes a pilot protection method for ac and dc TLs, both LCC and VSC topologies. Pilot protection algorithms depend on the communication between intelligent electronic devices (IEDs) [34] and data acquisition synchronization, typically implemented *via* ping-pong methods [35].

In this context, Fig. 2 illustrates a two terminal TL, on which are located current measuring equipment and IEDs. Both IEDs sample and digitize the measured currents, exchange these values over the communication channel, and run the protection algorithm. Typically, ac lines use CTs for current measurement, while dc lines use high-precision shunt resistors [14]. Another alternative for measuring line currents, for both ac and dc power transmission systems, is using optical instrument transformers.

Fig. 3 presents the proposed method's block diagram. The data acquisition step consists of measuring, sampling, and digitizing the current signals. These samples update the time series that store previous samples in the data windows. The update process consists of discarding the oldest elements of the series and including these newly sampled elements. Considering the line from Fig. 2, series $\mathbf{x}$ and $\mathbf{y}$ are

$$\begin{aligned} \mathbf{x} &= \{i_x(1), \cdots, i_x(k), \cdots, i_x(m)\} \\ \mathbf{y} &= \{i_y(1), \cdots, i_y(\ell), \cdots, i_y(n)\} \end{aligned} \tag{2}$$

where $i_x(k)$ is the k^{th} current sample in terminal B_x, with $k = \{1, \cdots, m\}$, $i_y(\ell)$ is the ℓ^{th} current sample in terminal B_y, with $\ell = \{1, \cdots, n\}$, and m and n are respectively the lengths of $\mathbf{x}$ and $\mathbf{y}$. From these series, the algorithm computes two cost matrices according to the DTW method. The first matrix considers the series $\mathbf{x}$ and $\mathbf{y}$, while the second considers the series $\mathbf{x}$ and $-\mathbf{y}$. With these matrices, two DTW quantities, called *Op* (operating) and *Re* (restraining), are calculated as in

$$Op = \text{DTW}\,(\mathbf{x}, -\mathbf{y}) \quad \text{and} \quad Re = \text{DTW}\,(\mathbf{x}, \mathbf{y}) \tag{3}$$

During normal operation or external faults, the operating quantity is less than the restraining one. However, when a fault occurs within the protection zone, the operating quantity assumes values greater than the restraining. When this occurs,

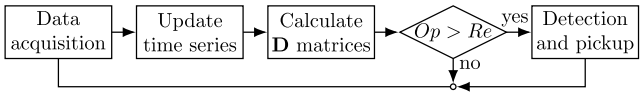

FIGURE 3. Proposed method's block diagram.

the protection function enters the pickup state, in which it is possible to determine the fault type and the phases involved (or the poles, in HVdc systems). If the pickup state remains true for longer than an adjustable time interval, the protection function sends a trip signal.

A. AC TRANSMISSION LINES

In ac TLs, the time series used by the protection method are the phase currents (phase segregated) and the zero sequence current (to increase its sensitivity to high impedance faults). Considering that the line terminals are L (local) and R (remote), these series are

$$\begin{aligned} \mathbf{x}_\varphi &= \{i_{\varphi,L}(1), \cdots, i_{\varphi,L}(k), \cdots, i_{\varphi,L}(m)\} \\ \mathbf{y}_\varphi &= \{i_{\varphi,R}(1), \cdots, i_{\varphi,R}(\ell), \cdots, i_{\varphi,R}(n)\} \end{aligned} \tag{4}$$

where $i_{\varphi,L}(k)$ is the k^{th} current sample at terminal L; $i_{\varphi,R}(\ell)$ is the ℓ^{th} current sample at terminal R; and φ indicates the respective line phase components (A, B, and C) or zero sequence component (0). One can notice that the algorithm calculates four DTW operating and four DTW restraining quantities, as in

$$\begin{aligned} Op_\varphi &= \text{DTW}\,(\mathbf{x}_\varphi, -\mathbf{y}_\varphi) \\ Re_\varphi &= \text{DTW}\,(\mathbf{x}_\varphi, \mathbf{y}_\varphi) \end{aligned} \tag{5}$$

B. DC TRANSMISSION LINES

In dc TLs, the time series used by the method can be the pole currents at both terminals. In this manner, the algorithm can be employed in both bipolar and monopolar HVdc lines. Considering that the terminals of these lines are *Rect* (rectifier substation) and *Inv* (inverter substation), if the pole terminals are used, the time series are

$$\begin{aligned} \mathbf{x}_\varphi &= \{i_{\varphi,Rect}(1), \cdots, i_{\varphi,Rect}(k), \cdots, i_{\varphi,Rect}(m)\} \\ \mathbf{y}_\varphi &= \{i_{\varphi,Inv}(1), \cdots, i_{\varphi,Inv}(\ell), \cdots, i_{\varphi,Inv}(n)\} \end{aligned} \tag{6}$$

where φ is the respective pole (positive P, or negative N).

For monopolar HVdc lines the algorithm uses the currents samples from both terminals. For bipolar HVdc lines, the proposed method may be pole segregated and, in this scenario, the identification of the fault type and the faulted poles is given directly by the algorithm's response for each pole. However, during the method's testing, it was observed that this approach results in considerably high trip times (interval elapsed between the fault's inception and its detection by the protection method), due to the non-linear behavior of the converters' controls.

Therefore, aiming to accelerate fault detection while maintaining security and dependability significantly, the authors propose the use of the presented protection algorithm with

the currents defined in this work as cross-currents between poles and terminals as the time series **x** and **y**, rather than just the pole terminals' currents individually. It is noteworthy that the use of the cross-currents is only possible in bipolar HVdc systems, which is the most popular form of converter interconnection, both in LCC and VSC line topologies [1].

The calculation of the cross-currents, as well as the identification of the fault type and the faulted poles, depend on whether the converters are constructed under the LCC or VSC technology, as presented in sections III-B1 and III-B2.

1) LCC-HVDC

The cross-currents used as the algorithm's time series **x** and **y** are

$$\mathbf{x} = \mathbf{i}_{P,Rect} - \mathbf{i}_{N,Inv} \quad \text{and } \mathbf{y} = \mathbf{i}_{N,Rect} - \mathbf{i}_{P,Inv} \tag{7}$$

where $\mathbf{i}_{P,Rect}$ is the rectifier's positive pole current time series; $\mathbf{i}_{N,Rect}$ is the rectifier's negative pole current time series; $\mathbf{i}_{P,Inv}$ is the inverter's positive pole current time series; and $\mathbf{i}_{N,Inv}$ is the inverter's negative pole current time series, as in

$$\begin{aligned}
\mathbf{i}_{P,Rect} &= \left\{i_{P,Rect}(1), \cdots, i_{P,Rect}(k), \cdots, i_{P,Rect}(m)\right\} \\
\mathbf{i}_{N,Rect} &= \left\{i_{N,Rect}(1), \cdots, i_{N,Rect}(\ell), \cdots, i_{N,Rect}(n)\right\} \\
\mathbf{i}_{P,Inv} &= \left\{i_{P,Inv}(1), \cdots, i_{P,Inv}(\ell), \cdots, i_{P,Inv}(n)\right\} \\
\mathbf{i}_{N,Inv} &= \left\{i_{N,Inv}(1), \cdots, i_{N,Inv}(k), \cdots, i_{N,Inv}(m)\right\}
\end{aligned} \tag{8}$$

The use of the cross-currents yields rapid internal dc faults detection speed and consequently decreases the trip times, in contrast to the use of each pole's terminal currents individually. This happens because the faulted pole converter controls tend to significantly reduce the voltage between terminals as a measure to avoid excessively increasing the circulating currents [14], [36]. In addition, the currents at the rectifier and inverter terminals continue to flow in the same direction. Therefore, the use of the cross-currents as in (7) lowers the similarity between time series **x** and **y** during internal faults, increasing the operating DTW, and decreasing the restraining DTW.

The faulted poles are identified as follows: if both **x** and **y** are negative, the fault is PG; if both are positive, the fault is NG; and if **x** is positive and **y** is negative, the fault is PN.

2) VSC-HVDC

The cross-currents used as the algorithm's time series **x** and **y** are

$$\mathbf{x} = \mathbf{i}_{P,Rect} - \mathbf{i}_{N,Inv} \quad \text{and } \mathbf{y} = \mathbf{i}_{P,Inv} - \mathbf{i}_{N,Rect} \tag{9}$$

As in the LCC-HVdc topology, the use of cross-currents in VSC systems also increases internal dc fault detection speed and reduces trip times compared to the use of each pole's terminal currents individually. Nonetheless, one can notice that while the cross-current **x** is the same for both HVdc topologies, cross-current **y** for VSC systems is opposite to the cross-current **y** for lines operating with LCC. This is necessary because the controls of the faulted pole converters tend to significantly decrease the voltage between the terminals to prevent increases in the flowing currents. Nevertheless, the currents flowing in the faulted pole tend to have approximately the same intensity, regardless of direction, in any fault situation [14], [36]. Hence, using the cross-currents as (9) in the proposed algorithm under the VSC-HVdc scenario decreases the similarity between the time series during internal dc faults, increasing the operating DTW, and decreasing the restraining DTW.

The identification of faulted poles is determined using the absolute values of the sum of the terminal currents of each pole. If $\mathbf{I}_P > \mathbf{I}_N$, the fault is PG; otherwise, the fault is NG. Finally, PN faults present $\mathbf{I}_P \approx \mathbf{I}_N$, and the difference between them is roughly the precision of the current measurement devices.

IV. ALGORITHM APPLICATION

The authors implemented and simulated three transmission systems in Electromagnetic Transients Program (EMTP)/Alternative Transients Program (ATP) [12], [13], [37], [38], [39] to evaluate the protection method proposed in this work. Initially, the authors investigated how the sampling frequency and the time series' size influence the algorithm's performance and found no significant correlation between trip times and sampling frequency and between that and the time series' sizes. The authors also evaluated the response of the proposed method for different sampling frequencies in both terminals and time series with different sizes, obtaining similar results.

After this preliminary assessment, the authors chose to present the results of this section using a sampling frequency of 3.84 [kHz]. Since pilot protection for TLs usually employs IEDs with time series (data windows) of the same size, the authors also chose to present the results using time series of the same size ($m = n = 32$). In addition, the authors used a trip confirmation time interval of 1 [ms] and a restraining quantity multiplication factor of 110% for the zero sequence on the ac lines and for the cross-currents on the HVdc lines. This configuration was used for all three transmission systems: the ac system and the HVdc systems described in sections IV-A, IV-B and IV-C.

A. AC TRANSMISSION SYSTEM

Fig. 4 depicts the five-bus 500 [kV] – 60 [Hz] ac transmission system used to evaluate the algorithm's performance. This system is located in Rio de Janeiro State (Brazil). The CTs transformation ratio is 1200:5, and their nonlinear characteristic is described in [40]. The fault levels at each bus are also illustrated in this figure.

The TLs were modeled using the *line constants* routine, considering the tower geometry and frequency-dependent distributed parameters. The positive and zero-sequence parameters are $r_0 = 0.302$ [Ω/km], $r_1 = 0.017$ [Ω/km], $l_0 = 2.673$ [mH/km], $l_1 = 0.855$ [mH/km], $c_0 = 8.341$ [nF/km], and $c_1 = 13.60$ [nF/km].

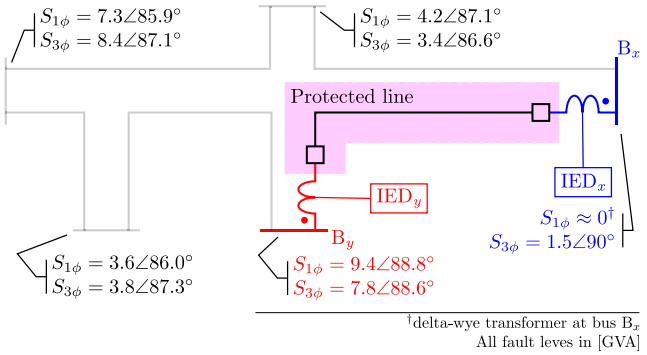

FIGURE 4. 500 [kV] ac transmission system.

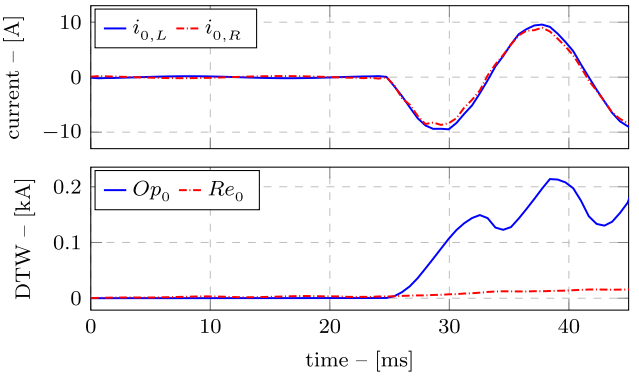

FIGURE 6. 500 [kV] ac TL high-impedance fault.

Line-to-ground, line-to-line, line-to-line-to ground, and line-to-line-to-line fault simulations were performed in the protected TL and in the other line connected to bus B_x to evaluate the trip times and the proposed method's reliability (dependability in internal faults and security in external faults). These simulations comprise nine hundred and twenty-four faults on the protected line and one hundred and sixty-eight faults on the parallel TL near bus B_y. The simulations vary on fault resistance values (from 0 up to 1000 [Ω]), location (10% to 100%, starting from B_x), and inception angles (≈0° and ≈90°). In the parallel circuit, the faults were simulated at bus B_y and 6.1 [km] from this bus.

1) THREE-PHASE FAULT BEHAVIOR

Fig. 5 illustrates the behavior of the proposed method under a solid internal three-phase fault in the TL at B_y. It depicts the terminal currents of phase C and the operating and restraining quantities, Op_C and Re_C.

One can notice that, during pre-fault, the magnitude of Re_C is greater than that of Op_C, and the proposed algorithm correctly identifies normal operation. After the fault inception, the magnitude of Op_C increases and becomes greater than that of Re_C. In this case, the trip time is 5 [ms].

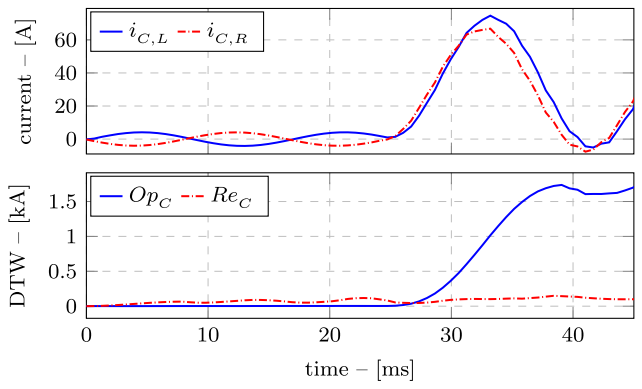

FIGURE 5. 500 [kV] ac TL three-phase internal fault.

2) LINE-TO-GROUND HIGH IMPEDANCE FAULT BEHAVIOR

Fig. 6 presents the zero-sequence currents and the algorithm's operating and restraining quantities, Op_0 and Re_0, behavior over time for an internal high-impedance line-to-ground fault, with resistance of 1000 [Ω], located at B_y.

One can notice that, as in the solid fault, the method correctly identifies the fault as Op_0 exceeds Re_0 after the fault's inception, when the terminals' zero-sequence currents grow into significant values. In this case, the zero-sequence trip time is 7 [ms].

B. LCC-HVDC TRANSMISSION SYSTEM

Fig. 7 shows the ±500 [kV] LCC-HVdc transmission system considered to assess the algorithm's performance in this dc line topology. This system is a bipolar version of the CIGRÉ's benchmark model for HVdc control studies, and it is described in further detail in [15] and [37].

The authors simulated one hundred and sixty-eight internal dc faults (PG, NG, and PN) and thirty-two external faults in the rectifier and inverter ac systems. PG internal dc faults were simulated between 10% and 90% of the line's length, while NG and PN faults were simulated by the authors in the middle of the dc line. The resistances of all pole-to-ground faults and external ac faults range from 0 to 1000 [Ω], while the highest resistance value adopted for PN faults is 10 [Ω]. The authors simulated all faults starting at 50 and 100 [ms].

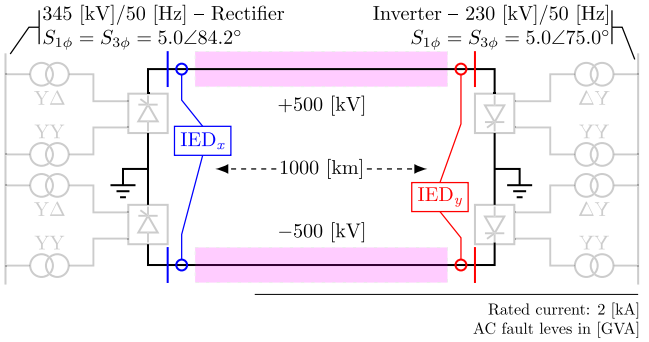

FIGURE 7. 500 [kV] LCC-HVdc transmission system.

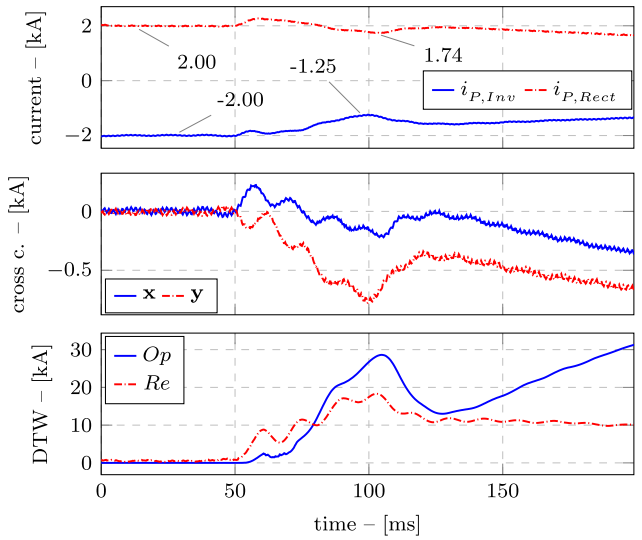

FIGURE 8. LCC-HVdc TL high impedance fault.

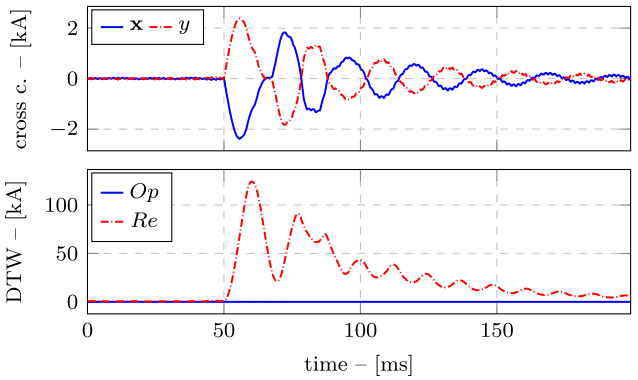

FIGURE 9. LCC-HVdc TL external ac fault.

1) PG HIGH IMPEDANCE FAULT BEHAVIOR

Fig. 8 shows the positive pole's currents (rectifier and inverter terminals), the cross-currents **x** and **y**, and the operating and restraining quantities for an internal dc high impedance fault between pole P and ground (PG). This fault has a fault resistance of 1000 [Ω], is located at 100 [km] from the rectifier's terminal, and starts at 50 [ms].

The authors chose to illustrate the algorithm's behavior to an internal dc high impedance pole to ground fault as these faults are the main reason why pilot protection schemes are employed in HVdc TLs, as mentioned earlier. One can notice that, while the faulted pole's terminal currents are not heavily affected by the internal high impedance fault, the cross-currents **x** and **y** are, which causes the operating quantity *Op* to become more significant than the restraining quantity *Re* after the fault's inception. Also, it is evident that when *Op* exceeds *Re*, both cross-currents are negative, allowing the algorithm to correctly identify this fault as PG. For this case, the algorithm's trip time is 27.9 [ms].

2) EXTERNAL AC FAULT BEHAVIOR

Fig. 9, in its turn, illustrates the cross-currents **x** and **y** and the quantities *Op* and *Re* for an external ac solid fault in the inverter's equivalent system.

One can notice that, both in the pre-fault period and mainly in the post-fault period (after 50 [ms]), the operating quantity never exceeds the restraining one. Therefore, the algorithm does not present a security failure (incorrect tripping) nor demand any intentional coordination delay reaching up to 1100 [ms], as this fault case shows that the distributed capacitive currents do not affect the proposed method's security.

C. VSC-HVDC TRANSMISSION SYSTEM

The ±100 [kV] VSC-HVdc transmission system used to test the proposed method is illustrated in Fig. 10 and detailed in [38] and [39]. The authors simulated one hundred and twenty-one faults in this system, of which one hundred and five were internal dc faults (PG, NG, and PN) and sixteen external faults (eight in the rectifier and eight in the inverter ac systems).

All internal faults were simulated between 10% and 90% of the line's length. The resistances of all pole-to-ground faults and external ac faults range from 0 to 1000 [Ω], while the highest resistance value adopted for PN faults is 10 [Ω]. The authors simulated all faults starting at 60 [ms].

1) NG HIGH IMPEDANCE FAULT BEHAVIOR

Fig. 11 illustrates the negative pole's terminal currents, the cross-currents **x** and **y**, and the algorithm's quantities *Op* and *Re* for an internal dc pole N to ground (NG) high impedance fault, with 1000 [Ω] resistance, at 22.5 [km] from the rectifier's terminal. As in the LCC-HVdc system, the authors chose to illustrate a high impedance fault as these are the primary reason why pilot protection is employed in the HVdc scenario.

One can observe that the fault barely modifies the negative pole's terminal currents. Still, the behavior of the cross-currents **x** and **y** changes considerably after the fault's inception, which causes the operating quantity to become significantly greater than the restraining one. For this case, the algorithm's trip time is 22.4 [ms]. Also, during the fault,

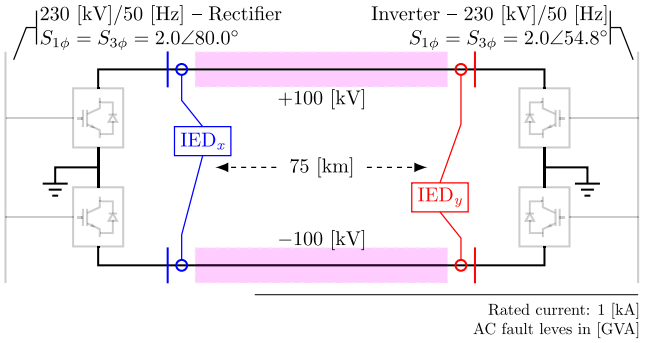

FIGURE 10. 100 [kV] VSC-HVdc transmission system.

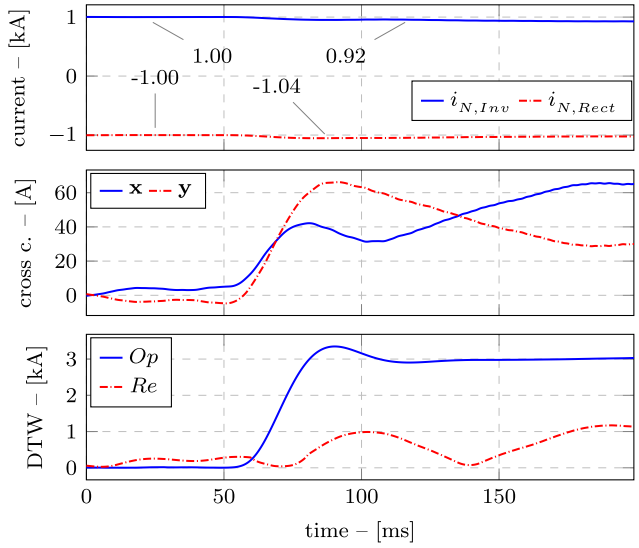

FIGURE 11. VSC-HVdc TL high impedance fault.

$\mathbf{I}_N$ becomes greater than $\mathbf{I}_P$, circa 25× greater, allowing the algorithm to clearly identify the fault as NG.

2) EXTERNAL AC FAULT BEHAVIOR

Fig. 12, then, shows the cross-currents **x** and **y** and the quantities *Op* and *Re* for an external ac solid fault in the inverter's system. As in the LCC-HVdc system, one can see that, both in the pre-fault period and during the fault, the restraining quantity is always more significant than the operating one.

Therefore, the algorithm does not mistake the external ac fault for an internal dc fault and consequently does not present a security failure. In this way, the proposed method does not need lengthy coordination delays for both HVdc topologies.

D. TRIP TIME RESULTS

Tab. 1 (columns 2 to 5) presents the trip times of the proposed algorithm for the three simulated systems (without considering communication delays). This table shows that the average trip times are around 10 [ms] with low standard deviations. Maximum trip times described in this table refer to high impedance faults (fault resistances of 1000 [Ω]) and minimum trip times refer to faults under more favorable conditions. Besides delivering fast trip times, the proposed algorithm did not present any security or dependability failures during the simulations.

When comparing the trip times of the proposed algorithm for the ac line with those presented in [8] and [12], one can notice that both have the same magnitude. However, the method proposed in [8] requires voltage measurements, together with the currents, and does not apply to HVdc lines. Besides, the algorithm proposed in [12] depends on settings that correlate little with the physical phenomenon. Also, comparing the algorithm with the conventional DFT-based differential protection algorithm, also presented in these

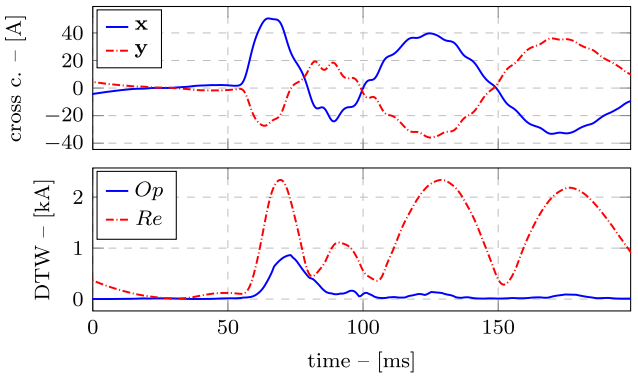

FIGURE 12. VSC-HVdc TL external ac fault.

references, one can see that the proposed solution has considerably lower trip times.

Conventional differential protection of HVdc lines have mandatory trip time delays of up to 1 [s] to avoid security failures, especially under external fault conditions, as previously mentioned. Therefore, the protection algorithm proposed in this work is substantially faster while eliminating the need for these time delays.

When comparing the trip times of the proposed algorithm for the LCC-HVdc line with the one proposed in [22], it is also clear that both have the same magnitude. However, the algorithm proposed in [22] is only applicable to VSC-HVdc. When comparing the trip times of the proposed method for the VSC-HVdc line with the one proposed in [21], one can see that both have the same magnitude. However, the algorithm proposed in [21] uses TWs, and the sampling frequency suggested (5 [kHz]) preclude its use in ac lines.

Finally, the proposed algorithm has advantages over the others, as it presents faster trip times compared to the conventional solutions and trip times similar to algorithms proposed in the recent literature. Furthermore, it is suitable for protecting the three typical transmission systems.

TABLE 1. Trip times [ms] - normal conditions and sensitivity analysis.

System	Normal conditions			
	μ	σ	max.	min.
ac	5.3	0.7	7.0	4.4
LCC-HVdc	12.9	4.7	28.1	4.2
VSC-HVdc	7.3	5.9	22.7	3.4
System	30 [dB] noise			
	μ	σ	max.	min.
ac	5.3	0.6	7.0	4.4
LCC-HVdc	13.2	4.4	28.1	4.2
VSC-HVdc	7.1	5.6	21.1	3.1
System	Misalignment			
	μ	σ	max.	min.
ac	5.4	0.6	7.3	4.7
LCC-HVdc	12.8	5.0	28.4	4.2
VSC-HVdc	7.4	5.9	22.9	3.4

V. SENSITIVITY ANALYSIS

The authors carried out the sensitivity analysis of the algorithm, considering challenging conditions as CT saturation for the ac system, sampled noise in the three systems simulations; and misalignment between samples, also in the three systems.

A. SAMPLED NOISE

To assess the robustness of the algorithm in the presence of noise in the signals stored in the time series, the authors deliberately added noise to the currents obtained through the simulations, with an average signal-to-noise ratio (SNR) of 30 [dB]. The algorithm's reliability was preserved during the simulations, i.e., no dependability or security failures were observed for all simulations. Tab. 1 (columns 6 to 9) presents the trip times for all systems, considering the noisy signals. One can observe that these trip times are alike the trip times presented in columns 2 to 5 indicating that the proposed algorithm is robust against noise-corrupted input data.

B. MISALIGNMENT BETWEEN SAMPLES

Misalignment between terminal line currents data windows can happen when pilot protection synchronization algorithms fail. However, such failures should not produce differences between the sampling instants greater than a sampling period since these algorithms are typically adaptive [34], [35]. Therefore, to reproduce this condition, the authors deliberately imposed a delay in one of the terminal line currents data windows equal to a sampling period. In all simulations, the proposed algorithm maintained its reliability. Comparing the results presented in Tab. 1 (columns 10 to 13), which describes the trip times under misalignment, with those shown in columns 2 to 5, one can notice that they are similar. The similarity indicates that this condition does not significantly affect the algorithm's performance. This behavior is due to the fact that DTW is an excellent algorithm to identify the best alignment between two time series.

C. CT SATURATION

Fig. 13 illustrates the terminal currents in phase B and the operating and restraining quantities, Op_B and Re_B, for an external BC fault on bus B_y of the ac system. In this case, the burden of the CT at terminal B_y was intentionally increased to produce the saturation depicted in this figure. One can notice that during pre-fault, the restraining quantity is greater than the operating one, and during the fault, the restraining quantity increases. After two cycles, saturation occurs and the operating quantity shows a slight increase, while the restraining one shows a slight decrease. However, even when this happens, security is preserved.

When saturation occurs in the protected TL, dependability is also preserved. The average, standard deviation, maximum, and minimum trip times for these simulation cases are 5.4, 0.7, 7.0, and 4.4 [ms]. One can observe that these trip times are alike the ones presented in Tab. 1.

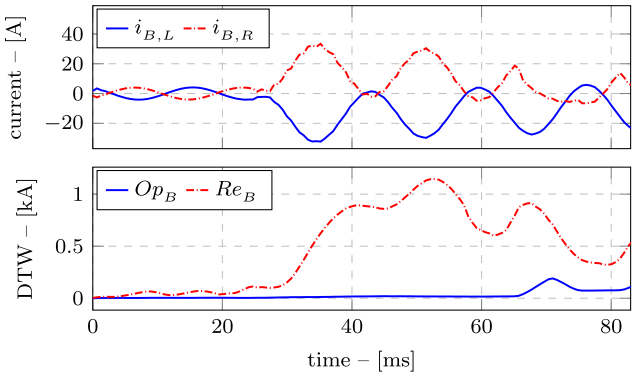

FIGURE 13. External fault with CT saturation.

D. POWER SWING

Disturbances in ac systems may result in power swings that produce variations in the system frequency and may negatively impact protection systems. This occurs because frequency variations impact phasor estimation, delaying fault detection or resulting in security and dependability issues.

In this context, the authors tested the proposed method using the system illustrated in Fig. 14. This figure depicts an equivalent 1300 [MVA] and 50 [Hz] four-pole generator connected to a 19/300 [kV] transformer that feeds two non-transposed double-circuit transmission lines. The circuits' lengths are 50 [km], from bus B_x to B_y, and 50 [km] from bus B_y to the infinite bus.

The authors implemented the system using EMTP/ATP, and the TLs were modeled using the *line constants* routine. More details on the system are presented in [12].

Two subsequent disturbances occur during the 5 [s] simulation time. The first consists of a three-phase short circuit that occurs in the second circuit (circuit 2), 453 [ms], after the start of the simulation. Following this occurrence, the protection of the second circuit opens the respective circuit breakers, isolating it 503 [ms] after the simulation starts. When this circuit is isolated, there is an increase in the impedance of section B_x–B_y; therefore, the equivalent machine mechanically oscillates. The second disturbance, also a three-phase fault, but in the first circuit (circuit 1), occurs 4 [s] after the simulation starts.

Fig. 15 illustrates the equivalent machine power angle, $\delta(t)$ behavior. One can notice that the angle varies from 66° to 75.5° during the power swing. Considering that the first peak occurs at ≈1.5 [s] and the second at ≈4 [s], the power

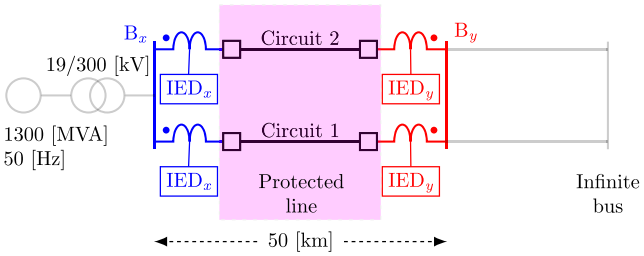

FIGURE 14. Power swing system.

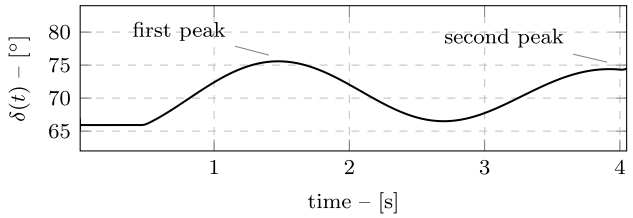

FIGURE 15. Power angle oscillation.

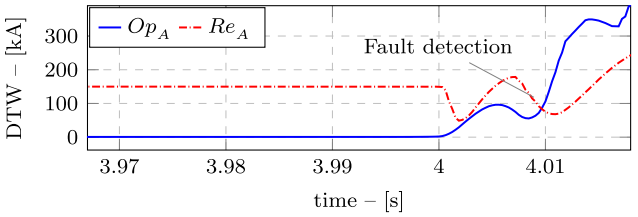

FIGURE 17. Protections' behavior for the second disturbance.

angle frequency oscillation is about 0.4 [Hz]. This oscillation results in frequency variations from 48.48 [Hz] to 51.62 [Hz].

The authors tested the method when independently protecting both circuits (3.2 [kHz] sampling frequency). During the first fault, only the protection of circuit 2 must operate, while the protection of circuit 1 must not detect it. During the power swing, the protection of circuit 1 must not operate, then after the second fault, this protection must detect it.

The authors verified that the algorithm's behavior was correct. The protection of circuit 2 detected the fault approximately 7 [ms] after its inception. Protection of circuit 1 did not detect this fault nor operate during the following power swings. It only correctly detected the fault in circuit 1 approximately 8 [ms] after its inception. Fig. 16 illustrates the behavior of both protections for the first disturbance, while fig. 17 depicts the behavior of the protection of circuit 2 for the second disturbance.

E. OUTFEED

Faults on ac systems usually result in fault currents flowing through both terminals toward their point of occurrence. However, outfeed may occur, impacting protection systems based on the differential function, with speed and reliability implications. In view of this, this section presents the algorithm's performance evaluation considering an outfeed event in the 765 [kV] equivalent system detailed in [8] and [12].

The authors implemented this system using EMTP/ATP. It consists of a two-terminal single transmission line modeled in *line constants* routine whose line length is 265 [km]. The three-phase fault levels at both terminals are 20.1∠87.14° and 22.3∠87.49° [GVA], while the single-phase fault levels are 16.1∠89.14° and 17.9∠89.4° [GVA].

The fault scenario used for testing consists of a phase-to-ground (AN) fault in the system operating under a heavy load that occurs 16.67 [ms] after the simulation starts. The fault resistance is 100 [Ω], and the distance is 16.67% of the total length of the line, starting from terminal B_x.

Fig. 18 illustrates the current signal of phase A, in which the faulted phase current is similar to the load current and flows from terminal B_x to terminal B_y. This phase's operation and restriction magnitudes did not correctly detect the fault. However, the zero sequence operating magnitude exceeds the restraining one about 1 [ms] after fault inception. In this way, the zero-sequence protection correctly detects the fault confirming the speed and reliability of the proposed algorithm.

VI. ACTUAL AC FAULT CASES

Finally, the authors tested the proposed algorithm using line terminal currents data stored in commercial IEDs during nine actual fault cases in three existing 500 [kV] ac transmission systems located in Brazil's mid-west, identified as I, II, and III. All three systems have line shunt reactors installed after the CTs. In addition, the transmission systems I and II are series-compensated, and the TLs' lengths are 366, 291, and 322 [km], respectively. The commercial IEDs have a sampling frequency of 2 [kHz] and use a distance protection function combined with a transfer trip scheme.

Tab. 2 describes the fault events and compares the algorithm's and the commercial IEDs' trip times. One can see

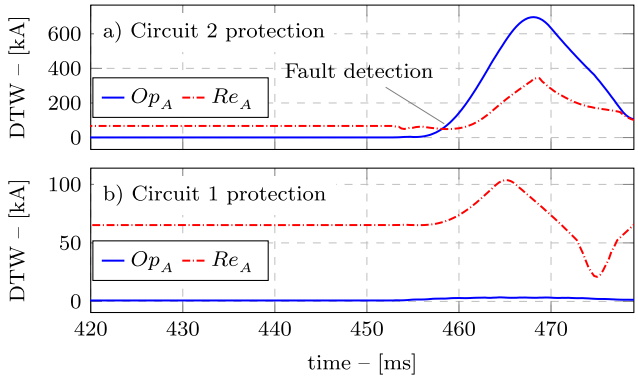

FIGURE 16. Protections' behavior for the first disturbance.

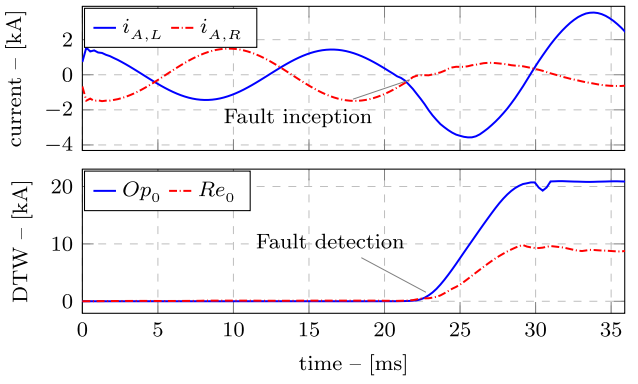

FIGURE 18. Protections' behavior during outfeed.

TABLE 2. Actual faults.

System	No.	Fault type	Cause	Trip time [ms]	
				Prop. method*	Actual
I	1	AG	lightning	4.7	19.1
	2	CG	fire	7.0	24.5
	3	ACG	lightning	5.7	20.6
	4	CG	lightning	5.8	18.6
	5	BC	fire	7.0	19.6
II	6	CA	fire	12.2	21.6
	7	CA	fire	10.2	20.1
III	8	CG	lightning	10.6	25.0
	9	ABG	lightning	8.6	26.5

*Communication delay of $\approx$ 1.5 [ms] not added to the values

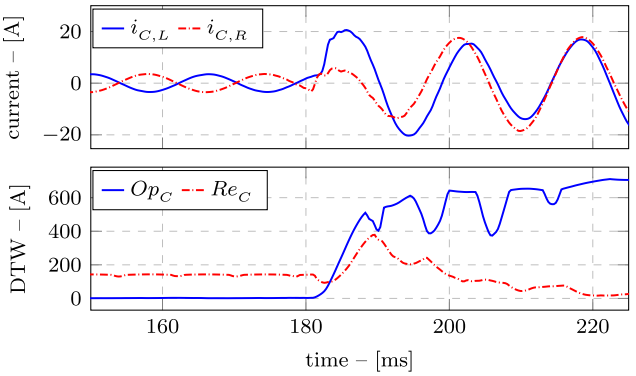

FIGURE 19. Actual 500 kV ac system line-to-ground fault.

that the proposed algorithm is notably faster than the commercial IEDs, even including typical communication delays. Furthermore, distance protection functions require electrical information from the protected lines.

Finally, Fig. 19 presents the line terminal currents in phase C and the corresponding operating and restraining quantities for the actual fault number 4. One can notice that, during pre-fault, the restraining quantity is significantly higher than the operating one, indicating that the algorithm correctly identifies normal operation. During fault, the algorithm correctly detects the fault as the operating quantity exceeds the restraining one, issuing a trip signal after 5.8 [ms].

VII. CONCLUSION

This work presents a method for protecting TLs that is based on a technique called dynamic time warping. The proposed method protects TLs of any nature and uses conventional protection systems' infrastructure. Also, it does not require high sampling rates or sophisticated digital filtering techniques. Furthermore, the method does not require electrical parameters from the protected TL or the power system.

The authors tested the proposed method against simulated faults in a 500 [kV] ac system modeled in EMTP/ATP that accurately describes an actual system located in Rio de Janeiro State, Brazil. In addition, the authors tested the presented solution against faults simulated in two well-established HVdc transmission systems. All the simulation results demonstrate that the DTW-based algorithm is reliable and fast. Additionally, the authors verified the robustness of the solution under challenging conditions such as sampled noise, misalignment between samples, CT saturation, power swing, and outfeed.

Even in these critical conditions, the algorithm maintained its rapidness, security, and dependability. Finally, the authors compared the algorithm with conventional commercial protection IEDs, using actual data from faults in three existing ac systems. The results confirmed that the proposed method is fast and reliable since the trip times are much lower than the commercial solution, while it is secure and dependable.

ACKNOWLEDGMENT

The authors would like to thank the ISA CTEEP transmission company for the support under the ANEEL Research and Development project number 00068-0049/2020.

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GIOVANNI MANASSERO Jr. (Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees from Universidade de São Paulo, São Paulo, Brazil, in 1999, 2001, and 2006, respectively. He joined Universidade de São Paulo, in 2009, where he is currently a Professor with the Electric Energy and Automation Engineering Department and the Head of the Research Laboratory for Protection and Automation of Electrical Systems. His research interests include power systems protection, and modeling and simulation.

RODRIGO ROZENBLIT TIFERES (Member, IEEE) was born in Brazil, in 1998. He received the B.Sc. and Ph.D. degrees in electrical engineering from Universidade de São Paulo (USP), São Paulo, Brazil, in 2020 and 2022, respectively. He is currently a Postdoctoral Researcher with the Electrical Power Systems and Automation Engineering Department, USP. His research interests include the development of power systems protection algorithms, power systems modeling and simulation, fault location methods, and substation automation.