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Embedded Prototype System for Monitoring Heart Rate

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Abstract. The vital signs monitoring is very important for patients that suffers some chronic disease because they reflect basic and essential functions in the body. In Mexico, in the last few years, we have noticed that the mortality rate in patients with heart disease has increased significantly due to late diagnosis and lack medical care to patients who have been diagnosed. This work presents a proposal embedded system, that allows continuous monitoring of heart rate with an optical sensor and a Microblaze soft-core embedded in a Spartan-6 FPGA of Xilinx. The Microblaze processor works whit the local processor bus for managing peripherals. Core SPI is used to interface with the sensor. The system detects the heartbeat through the sensor which is placed on the index finger of the patient, the signal is acquired by the soft-core, where the heart rate is obtained through the autocorrelation function. Finally, UART core is used to send data to a computer where is implemented a server application that enables remote monitoring of sensor information.

Keywords: Embedded system, FPGA, heart rate.

1 Introduction

Vital signs are clinical parameters that reflect the physiological state of the human organism, and essentially provide the data which will establish the guidelines for evaluating the homeostatic condition of the patient. Vital signs indicate the present health status of the patient, as well as changes or evolution, either positively or negatively. Vital signs include: temperature, respiratory rate, heart rate and blood pressure, among others.

Monitoring of vital signs and biomedical covers a wide spectrum in different contexts today, so, it has been a concurrent research topic in the last decade [1-5]. Currently, there are systems designed to monitoring vital signs through different technologies.

In [2, 3, 5], the use of technology based on a microcontroller, has been proposed in order to monitoring many different vital signs like heart rate, breathing and others. In

[4] is used an embedded system with an ARM processor and a Linux OS for the motoring of an electrocardiographic signal (ECG) of the patient.

This paper presents an embedded system that is developed in a Field Programmable Gate Array (FPGA) in order to monitoring de heart rate (Fc). The use of a FPGA is convenient because allows the use of a soft-core. A soft-core processor is a hardware description language (HDL) model of a specific processor (CPU) that can be customized for a given application and synthesized for an ASIC or FPGA target [7].

Heart rate is the rate at which the heart beats to pump blood throughout the body. In other words, is the number of times the heart beats per unit time, commonly measured in a minute.

When the heart pumps blood through the arteries these expand and contract with the blood flow. By taking the pulse, not only the heart rate is measured, it can also indicate the strength of the heartbeat.

The normal rate for healthy adults ranges from 60 to 100 beats per minute. The rate may fluctuate and increase with exercise, illness and injuries. Girls from age 12, and women in general, tend to have faster than boys and men heartbeat. Athletes, such as runners, who do a lot of cardiovascular conditioning may have heart rates of 40 beats per minute without any complications [6].

The commonly way used to measure the heart rate is counting the beats during a minute placing the index and medium fingers on the wrist, with a distance of 1.5cm of the joint. The proposed system uses the calculation of the heart rate by obtaining the fundamental frequency of the signal. The embedded system obtains a set of samples of the heartbeat, which are taken through an optical sensor, and then apply the technique of autocorrelation in order to calculate the heart rate.

2 Architectural Design Proposal

The proposed architecture of the embedded system is shown in the Figure 1, the architecture consists of three main parts.

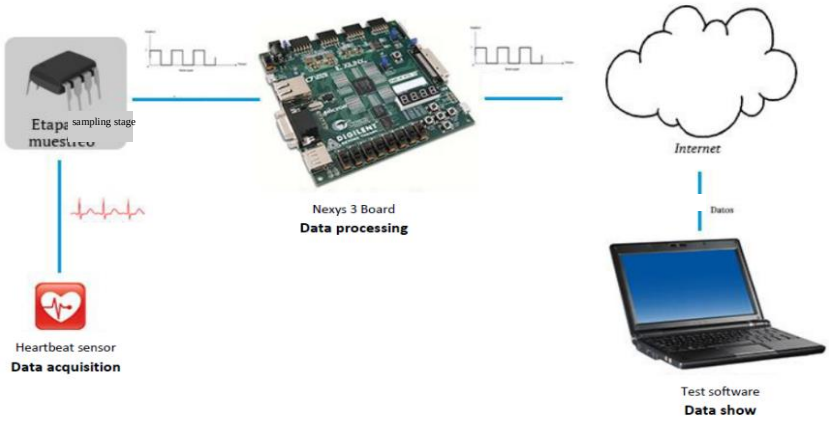

Fig. 1. Proposed architecture of the embedded system.

- **Data acquisition stage.** This stage allows detecting the heartbeat of the patient using an optical sensor with analogical interface. For the correct use of the system, the patient must be relaxed, under normal resting conditions. The obtained signal is sent to a filter circuit and then, it can be converted in a digital signal using the MAX144 ADC.
- **Data processing stage.** Once the data was converted in a digital signal, this signal is sent to the Nexys3 board, which has an embedded soft-core where the heart rate is estimated using the autocorrelation technique. Finally, the result is sent to the software application.
- **Software application.** A web application that can display the acquired patient information was developed. This software allows to storage a patient's clinical history too, where a doctor can check it.

3 Implementation of the Proposed Architecture

The proposed architecture was implemented in stages like the design, in this section, each stage is described.

3.1 Data Acquisition Stage

The Figure 2 shows the circuit that is used for the data acquisition of the sensor.

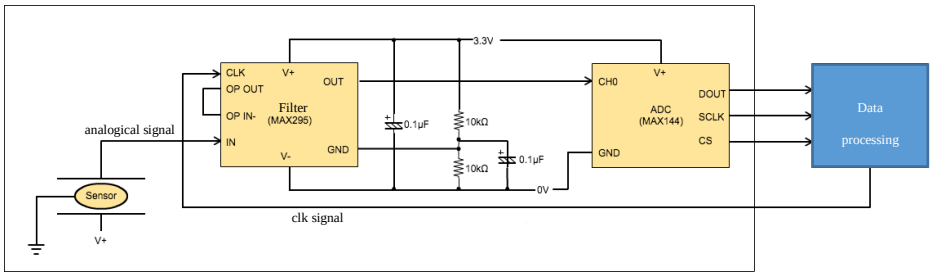

Fig. 2. Schematic circuit diagram for the data acquisition.

For detecting the heartbeat, the sensor that is shown in Figure 3 is used. This is placed and secured in the user's index finger is used. The sensor is a free hardware design and has 3 connector pins, two for supply voltage (5V) and one for signal output, this sensor has an analog output.

Once you have the output signal of the sensor, this is filtered using the MAX295 circuit, this is a filter circuit of eighth order which can be set to a cutoff frequency in a range that goes from 0.1Hz to 50KHz. To set the cutoff frequency of this filter, it was considered that this circuit has a ratio of 50:1, i.e.:

$$F_s = 50F, \tag{1}$$

where *Fs* is the clock frequency and *F* is the filter frequency of the signal to be filtered. The clock signal *Fs* that was used to set the filter was generated using a Core-Timer in the FPGA, which is controlled by the soft-core.

Heartbeat signal can vary within a range of frequencies ranging from .81Hz to 3.66Hz approximately. Taking the maximum frequency of heartbeat and fulfilling the relationship indicated for the sensor, the filter was set with Fs = 200Hz.

Fig. 3. Pulse amped sensor.

To complete the data acquisition stage, the MAX144 circuit, that is a 12-bit ADC with an operating voltage of 2.7V to 5.2V and handle the SPI protocol, was used. According to the specifications, to be configured for operation by an external clock signal, this generates a 16-bit frame with the format showed in Figure 4.

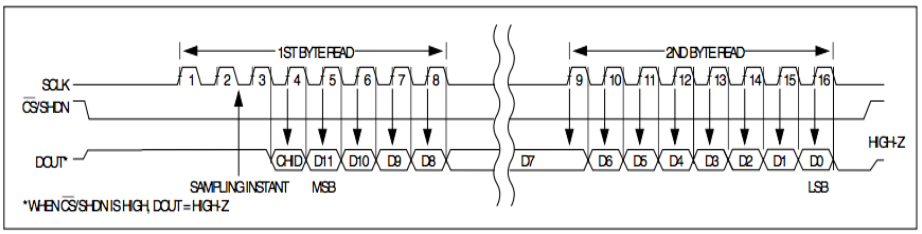

Fig. 4. MAX 144 ADC output frame.

The first three bits remain at high level, the fourth bit (CHD) allows to set the channel and the last 12 bits (D) containing the data resulting from the analog-digital conversion. Once the sensor signal has been digitized, this is sent to the FPGA.

3.2 Data Processing Stage

Once the signal has been digitized, this is sent to a Spartan 6 - FPGA Spartan 6 where the architecture shown in Figure 5 was configured.

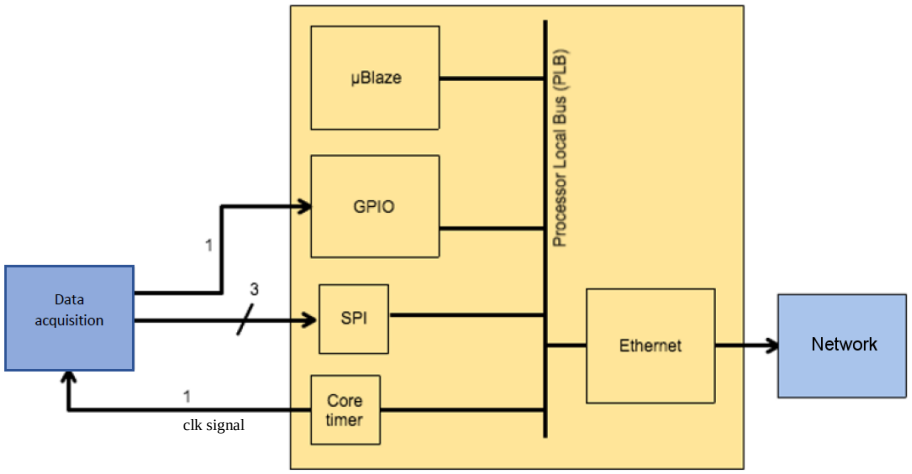

Fig. 4. Embedded system configured in Spartan 6 FPGA.

The architecture consists of a XPS General Purpose Input / Output driver that sends the voltage supply for the heartbeat sensor.

The LogiCORE IP XPS Timer / Counter can generate a clock signal that is sent to the stage of data acquisition, this clock signal has a frequency of 200Hz and is what allows to set the low pass filter for a cutoff frequency 4Hz approximately.

Dedicated Core XPS SPI Interface, which allows the reception of data from the ADC, was used. It allows the data reception from ADC circuit through two frames of 8 bits length to complete a unique frame of 16-bits due to this is the work protocol.

Finally the soft-core MicroBlaze embedded in the FPGA, which allows you to calculate heart rate and control peripherals through a general purpose bus PLB was configured.

The diagram of Figure 6 describes the flow of operations performed to obtain the heart rate from a set of samples acquired. In the process, can be noticed that a set of samples is acquired using the *adquirir_muestra()* function, this function gets a 16-bits frame from two frames of 8 bits from the data acquisition module. Once one has the entire frame, the mask 0xFFF is applied and subtracted 2048 to remove the DC component, finally the last 12 bits have the value of the sample that is stored in an array, the process is repeated until to get 2000 samples, when the array is complete, the *autocor()* function, defined by Eq. (2), is executed to obtain the autocorrelation of the samples:

$$r_{xx}(l) = \sum_{n=0}^{N-l-1} x(n)x(n+l); l = 0, 1, 2, \dots, n. \quad (2)$$

The code of the function is shown below.

```
For(m=0; m<l; m++){
   rxx=0
   for(n=0;n<N-m;n++){
      rxx = rxx+(muestra[n]*muestra[n+m])
   }
   Res[m]=rxx;
}
```

To calculate the heart rate is necessary obtain the fundamental frequency of the signal, this can be done by many techniques, for example, Fast Fourier Transform, Discrete Fourier Transform or Autocorrelation. In this case, autocorrelation technique was chosen for its low computational complexity. Table 1 shows the comparison of the computational complexity between these techniques.

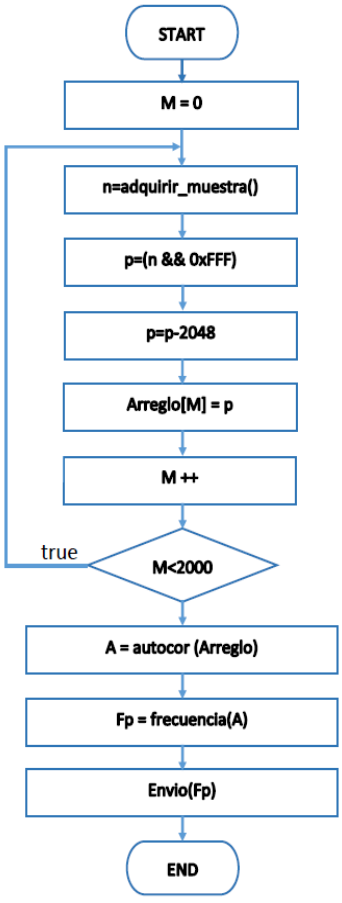

Fig. 5. Flowchart of calculation of the heart rate.

Table 1. Comparison of the computational complexity.

Algorithm	Computational complexity
Fast Fourier Transform	$n\log_2 n$
Discrete Fourier Transform	n^2
Autocorrelation	n

Once you have the resultant vector of the autocorrelation, the function *frecuencia()* is executed to estimate the heart rate. This function looks for the second highest peak, which represents the fundamental frequency of the signal.

In order to calculate the period of the occurrence of a heartbeat, the next relation is necessary:

$$t_s = \frac{X}{300}, \tag{3}$$

where X is the value of the second highest peak of the autocorrelation result and the constant of 300 it is the working frequency of architecture. Once obtained $t_s$the Fc is calculated such that:

$$F_C = \frac{60}{t_s}. \tag{4}$$

The F_C value obtained is sent by the Core UART to the computer in order to be stored in the application server.

3.3 Web Application

A web application was designed and implemented, in order to test the system. The web application allows register a patient and do the monitoring of F_C, and generate a record of the measurements performed for the patient. Medical personal has the option to check these and do new measurements, in the Figure 7, the main screen is shown and in Figure 8 an example of the medical history is shown.

Fig. 6. Web application main screen (screenshot in Spanish).

Fig. 7. Medical history example (screenshot in Spanish).

4 Test and Results

The hardware configuration of the embedded system was done using Xilinx Platform Studio (XPS), where the necessary drivers to Nexys 3 FPGA must be chosen, also the processors, the Microblaze soft-core and the GPIO, UART, Timer/Counter and SPI Cores, as well as, make the assignation of the memory space. Then, the in-out signals must be configured with the FPGA pins.

In the Figure 9, the sensor test with the filter circuit is shown. The X axis represents time while de Y axis represents voltage. It can be noticed the reduction of noise between the original sensor signal output (top graph) and the signal resultant of the filter (bottom graph).

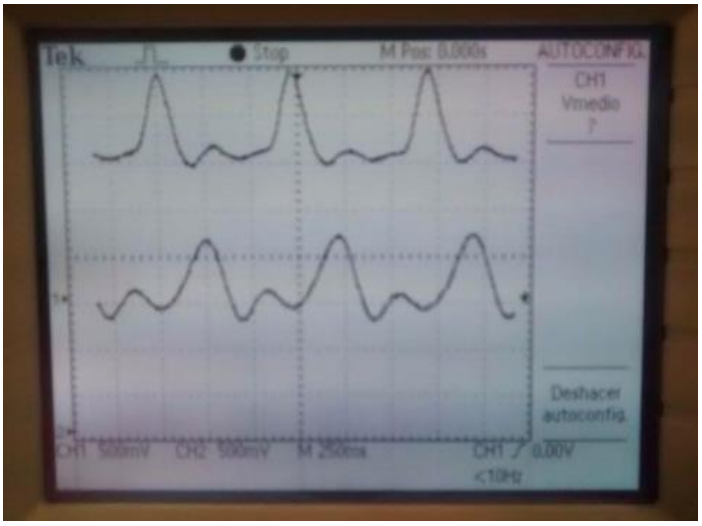

Fig. 9. Test of the sensor and the filter circuit (screenshot in Spanish).

In the Figure 10 is shown a plot of the set of 2000 samples in the X axis and his magnitude in the Y axis, that were got by the sensor and then were digitized, this graph was plotted using Matlab software.

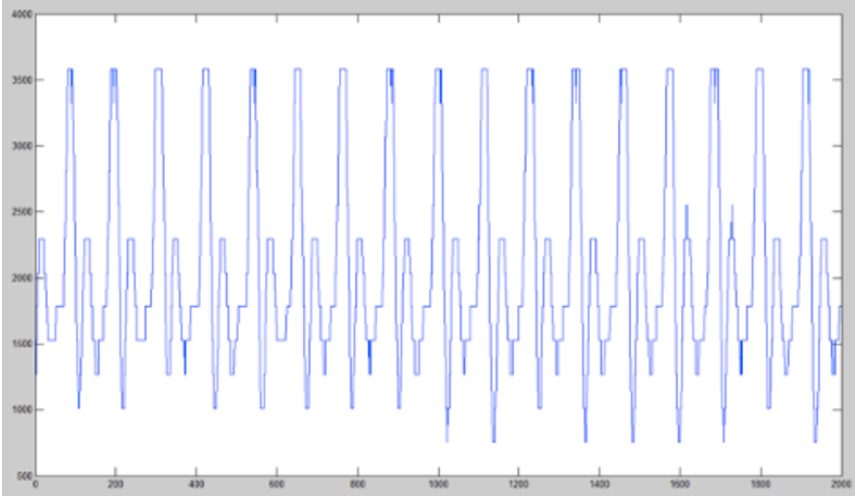

Fig. 10. Graph of the set of Samples of the original signal.

In the Figure 11, the result of the autocorrelation of the samples is shown. In this case, the second highest peak is corresponding to X=234, solving the Eq. (3) and (4) with this value, Fc=76 heartbeats per minute is obtained. Finally, this result can be stored and monitored in the trail software as is shown in the Figure 12.

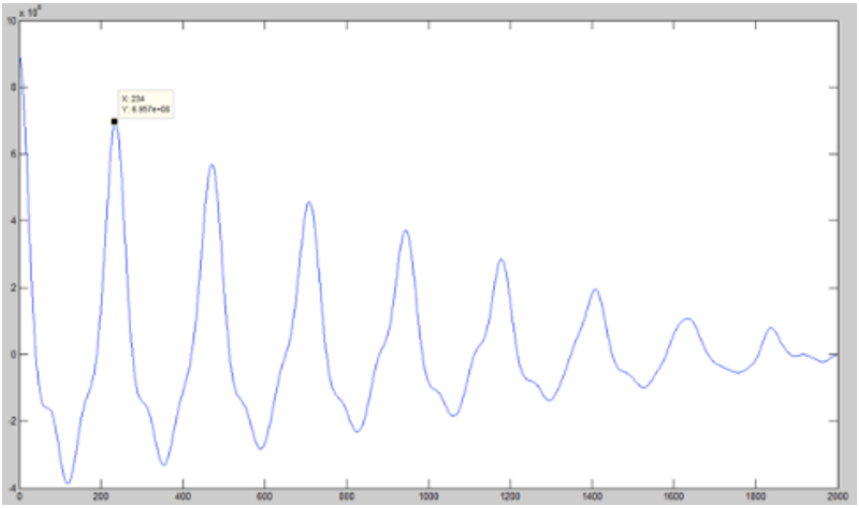

Fig. 11. Graph of the autocorrelation result.

Fig. 12. Example of the web application (screenshot in Spanish).

5 Conclusions

In this work, a proposal for an embedded system to monitoring heart rate using a Nexys 3 FPGA and a softcore Microblaze is presented. An analogical sensor is configurated and conditioned, and the output signal is filtered using the Maxim Integrated MAX295 that allows an output response without noise, then and Maxim Integrated MAX144 ADC is used in order to get a digital signal with a resolution of 12 bits.

The embedded system architecture was designed using the Microblaze soft-core which is used to the reception and the processing of the data obtained through the sensor in order to get the heart rate, this tool also allows the use of personalized cores, in this case, the GPIO, UART, Timer/Counter and SPI Cores were configurated

A web application was designed and developed using web technologies like PHP, HTML, JavaScript and the data base handler MySQL. The web application shows the information obtained from the embedded system and it can store the clinical history of the patient.

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References

1. Ying-Wen, B.: Design and Implementation of an Embedded Monitor System for Body Breath Detection by Using Image Processing Methods. Digest of Technical Papers International Conference on Consumer Electronics (ICCE), pp. 193–194 (2010)

2. Siddharth, N., Sasikala, M.: Design of Vital Sign Monitor based on Wireless Sensor Networks and Telemedicine Technology. In: International Conference Green Computing Communication and Electrical Engineering (ICGCCEE), pp. 1–5 (2014)
3. Baccini, P. H.: Developing an Affective Point-of-Care Technology. In: IEEE Symposium on Computational Intelligence in Healthcare and e-health (CICARE), pp. 77–84 (2014)
4. Han-Pang, H., Lu-Pei, H.: Development of a Wearable Biomedical Heath-Care System. In: IEEE/RSJ International Conference on Intelligent Robots and Systems, pp. 1760–1765 (2005)
5. Kalovrektis, K.: Development of Wireless embedded system using ZigBEE protocol to avoid white Gaussian noise and 50 Hz Power line noise in ECG and Pressure Bloodsignals. In: Panhellenic Conference on Informatics, PCI 08, pp. 113–117 (2008)
6. DALCAME Grupo de Investigación Biomédica.: Frecuencia Cardíaca. Available: http://www.dalcame.com/fc.html#.VWvWO89_NBe.
7. Tong, J., Anderson, I., Khalid, M.: Soft-Core Processors for the Embedded Systems. In: 18th International Conference on Microelectronics (ICM), pp. 170–173 (2006)