A TDC-Based Front-End for Rapid Impedance Spectroscopy

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***Abstract*—Impedance spectroscopy (IS) is an important technique for monitoring and detection of biomaterials. In order to enable point-of-care systems, low-cost IS systems capable of rapidly measuring a wide range of biomaterials are required. This paper presents an IS front-end which utilizes a time-to-digital converter (TDC) and a peak detector circuit (PDC) for quick measurement of both impedance phase and magnitude, respectively. Designed in a 0.18µm CMOS process, the front-end is capable of performing impedance measurements in 6µs at frequencies ranging from 100Hz-10MHz and with a 100Ω-1MΩ dynamic range. Simulation results with cell impedance models show that the system achieves <2.5% magnitude and <2.2° phase error. The front-end consumes 28mW total power and occupies 0.4mm^2 area.**

I. Introduction

Low-cost impedance spectroscopy (IS) biosensor platforms have the potential to enable point-of-care disease diagnosis/prognosis and monitoring of biomaterials [1]-[3]. In a typical IS system, a stimulus AC electrical signal is applied through sensor electrodes and the cell impedance is obtained as $Z=V/I$, where V and I represent the voltage across and the current flowing through the sample, respectively. This AC stimulus signal is swept over a frequency range and both the magnitude and phase of the complex impedance Z is extracted to generate the impedance spectrum.

Cellular impedance is typically measured over a frequency range of 10Hz-10MHz. Due to their capacitive component, cellular impedance magnitude can vary over a wide range of 100 Ω -10MΩ, with the highest impedance observed at the lowest frequencies. This high impedance value, coupled with the requirement to keep the stimulus AC signal below 10mV in order to avoid cellular damage, sets the sensitivity requirements for the transimpedance amplifiers (TIAs) typically used in IS front-ends. Measurement time is also very important in applications such as flow cytometry [4], where the measurements are required to handle cellular flow rates, and in large sensor array systems in order to reduce array scan times [5]. While high performance impedance analyzers are available, such as the Agilent 4294A, these bulky instruments are not suitable for point-of-care applications. This motivates impedance spectroscopy systems with a higher level of integration, which provides the potential for both lower cost and higher performance due to reduced interconnect parasitic.

The most commonly proposed coherent demodulation impedance spectroscopy front-ends suffer from long measurement times due to the settling times of the low-pass filters required to extract magnitude and phase information from the in-phase and quadrature mixers [5], [6]. Architectures which directly measure impedance magnitude and phase offer potentially quicker measurement time [7], [8]. The work of [7] places the stimulus oscillator in a closed-loop feedback system which includes the impedance under test and measures impedance magnitude with a peak detector circuit (PDC). Although, this closed-loop feedback system requires several stimulus cycles to settle and limits the measurement time to the ms range. The open-loop architecture of [8] utilizes a filtered synchronous full-wave rectifier to measure impedance magnitude, which reduces the impact of front-end TIA offset, but limits both the high-frequency accuracy due to comparator delays required to generate a self-mixing signal and the measurement speed due to filter settling time. Moreover, both [7], [8] utilize XOR phase detectors to extract phase information, which can reduce measuring range and accuracy because of the non-monotonic characteristic and duty-cycle sensitivity.

This paper presents an impedance spectroscopy front-end which allows for measurement time theoretically just slightly more than $1/f_s$, where f_s is the stimulus signal frequency, for frequencies up to 100kHz. Section II describes the proposed IS front-end which utilizes an open-loop architecture with a PDC for impedance magnitude measurement and an SR-latch phase detector followed by a time-to-digital convertor (TDC) for fast phase measurement. The main circuit blocks are analyzed in Section III, where a variable-gain TIA allows for a wide impedance measurement range of 100Ω-1MΩ over a frequency range of 100Hz-10MHz and an improved peak detector allows for accurate low-frequency measurements. Section IV presents simulation results with cell impedance models from a 0.18µm CMOS prototype. Finally, Section V concludes the paper.

II. Proposed IS Front-End

Fig. 1 shows the proposed IS front-end, which utilizes a TIA to convert the current produced by applying an AC stimulus to a cell sample into a voltage for impedance magnitude and phase measurement. This voltage's amplitude and phase shift relative to the stimulus signal is obtained by employing a PDC and a phase detector with TDC functionality, respectively. If we denote the stimulus signal as $|Vs|\cdot\sin(\omega t)$, the TIA output is

$$V_{TIA} = -\frac{|Vs|*\sin(\omega t-\varphi)*|Z_{TIA}|}{|Z|} \quad (1)$$

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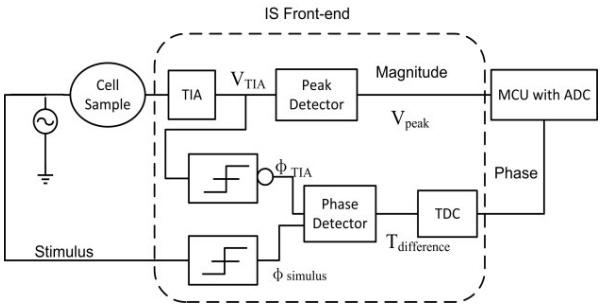

Figure 1. Proposed IS front-end.

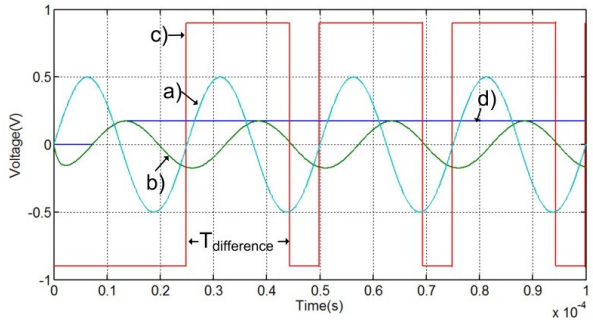

Figure 2. IS front-end operation: a) 40kHz stimulus signal (×50), b) TIA output, c) Phase detector output, d) PDC output.

where |Z| represents sample impedance magnitude, $|Z_{TIA}|$ is the TIA gain, and φ is the phase shift introduced by sample. The simulation results of Fig. 2 show that the TIA output amplitude, V_{peak}, can be effectively extracted with a PDC, and thus used to calculate the cell impedance magnitude.

$$|Z| = \frac{|Vs|*|Z_{TIA}|}{V_{peak}} \quad (2)$$

Two comparators are also employed to convert the TIA output and the original stimulus signals into square waves which are fed to a SR-latch phase detector that compares the rising-edge time difference. Note, the TIA signal inversion is achieved by applying the TIA output into the negative input of the differential comparator. As shown in Fig. 2, the duty cycle of phase detector output is directly proportional to the impedance phase shift.

$$\varphi = \frac{T_{difference}}{T_{cycle}} * 2\pi \quad (3)$$

where T_{cycle} represents the stimulus period and $T_{difference}$ is the rising-edge time difference. A subsequent divide-by-two counter-based TDC then rapidly digitizes this phase information. Following the IS front-end, a microcontroller (MCU) can be utilized to stored the TDC phase information and digitize the PDC output for further processing.

In order to conduct an impedance measurement at a specific frequency, f_s, ideally only one full stimulus circle ($1/f_s$) is necessary for the PDC to extract V_{peak}. While this is the case at low-frequency, the µs level PDC response time does place a lower-bound on the measurement time; necessitating multiple cycles for frequencies above 100 kHz. However, this µs-range measurement time is acceptable for fast flow-rate cytometry [4] and allows for dramatic improvements in sensor array scan rates [5].

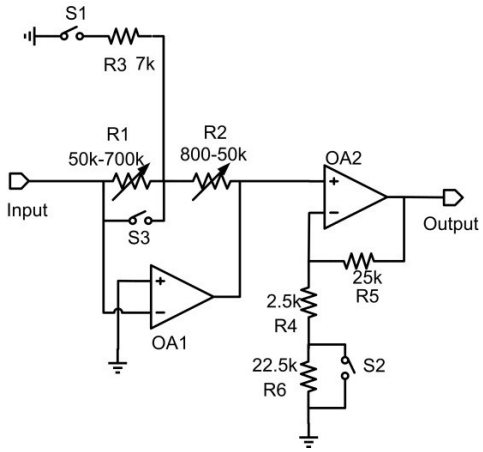

Figure 3. TIA schematic.

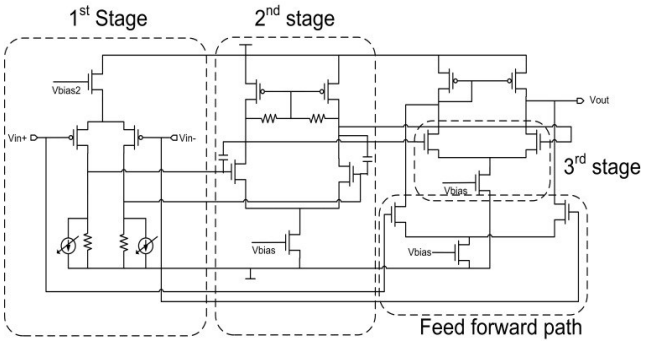

Figure 4. Opamp schematic.

III. System Blocks

A. Transimpedance Amplifier

The TIA shown in Fig. 3 converts the stimulus current from the sample into a voltage for magnitude and phase detection. With a 10mV stimulus voltage, the TIA is required to sense an input current ranging from 10nA-100µA and obtain adequate sensitivity for operation up to 10MHz. The first stage, consisting of opamp *OA1*, tunable feedback resistor array *R1*, *R2*, and gain enhancement resistor *R3*, perform the current-to-voltage conversion. Assuming a large *OA1* gain, the first stage output is approximated as

$$V_{OA1\_R3\_enable} \approx -Vs * \left[\frac{(R1*R2)}{Z*R3} + \frac{(R1+R2)}{Z}\right] \quad (4)$$

with *R3* enabled, while the gain reduces to

$$V_{OA1\_R3\_disable} \approx -Vs * \frac{(R1+R2)}{Z} \quad (5)$$

with *R3* opened. An additional programmable voltage gain of 2 or 11 is supplied by the second stage *OA2* feedback amplifier, allowing an overall tunable TIA gain ranging from 1.6kΩ-63MΩ.

Fig. 4 shows the TIA's opamp schematic, consisting of three gain stages and one feed-forward path. In order to reduce input-referred flicker noise, the first stage adopts a PMOS input differential pair and passive resistor loads. The opamp achieves 54.5dB gain, 1GHz gain-bandwidth, and a relatively high 74.2° phase margin due to the transmission zero created by the feed-forward path. Cancellation of the overall TIA

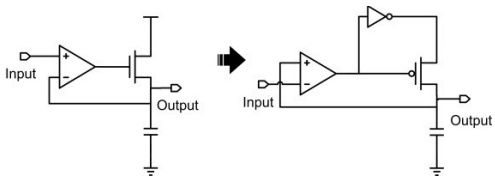

Figure 5. Peak detector circuits: a) Converntial NMOS topology b) Proposed PMOS version.

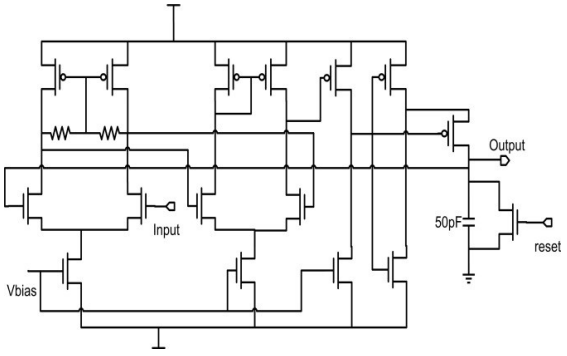

Figure 6. Detailed PDC schematic.

input-referred offset is achieved with two digitally-tunable current sources in parallel with the first-stage loads.

B. Peak Detector Circuit

In order to extract the TIA output amplitude, a PDC locks to the maximum value of V_{TIA}. A conventional PDC is shown in Fig. 5(a). Here an error amplifier controls the NMOS conductivity to charge the hold capacitor when the input voltage is higher than output, and ideally otherwise shuts off the transistor. A key limitation of this circuit in low-frequency applications involves the NMOS leakage current slowly charging the hold capacitor to VDD. Also, the maximum output value is limited to VDD-V_{thN}, which is a severe issue in low-voltage designs.

The proposed peak detector of Fig. 5(b) addresses these issues. Here a PMOS transistor is connected to the hold capacitor allowing for a higher peak output voltage. In order to reduce hold-stage leakage, the PMOS gate is controlled with the error amplifier output and the source is tied to an inverter also driven by the error amplifier. When the PDC input is higher than the output, the error amplifier output forces a low voltage on the PMOS gate and the inverter output forces VDD to the PMOS source, allowing the hold capacitor to charge up. In the hold state the PMOS is shut off with the gate driven to VDD and the source driven to VSS, providing much less leakage current to discharge the holding capacitor and superior low-frequency performance. The detailed PDC schematic is shown in Fig. 6, which includes the transistor that resets the PDC between measurements.

C. Phase Detection Comparators

Fig. 7 shows the comparators used to amplify the original stimulus and the TIA output to square waves for phase detection. Two differential-pair pre-amplify stages and one CMOS inverter stage provide sufficient gain, with a dummy CMOS inverter stage included to equalize the second-stage loading. Similar to the offset-correction scheme used in the

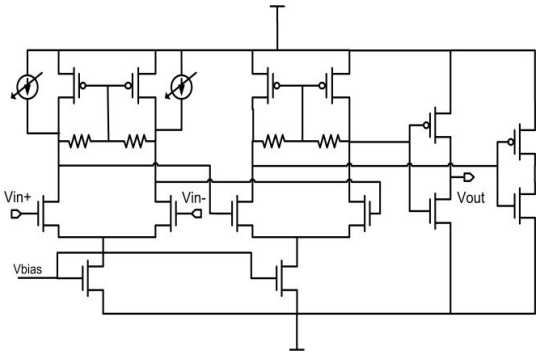

Figure 7. Comparator schematic.

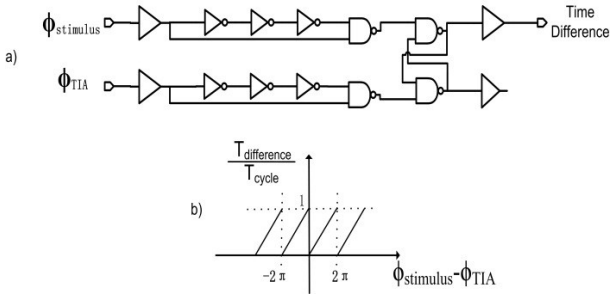

Figure 8. Phase detector: a) Schematic, b) Phase transfer characteristic.

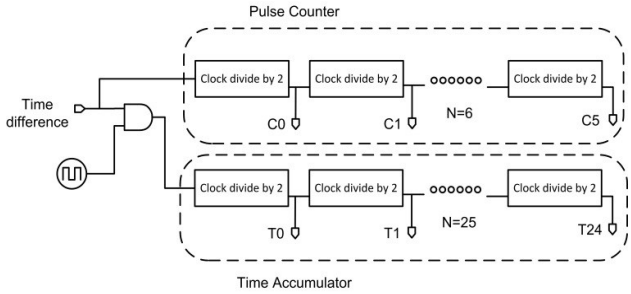

Figure 9. Divide-by-2 counter based TDC.

TIA, two digitally-controlled current sources in parallel with the first-stage input loads allow for cancellation of the comparator offset.

D. SR-Latch Phase Detector

The phase detector (Fig. 8) consists of a set-reset latch preceded by rising-edge pulse generators. This phase detector is superior to an XOR-based version [7], [8] due to its monotonic phase transfer characteristic and insensitivity to input duty cycle. The topology is capable of distinguishing a minimum 200ps time difference, which corresponds to a 0.72^{o} phase error at the maximum f_s = 10MHz.

E. Time-to-Digital Converter

In order to cover a relatively large input 0.1µs-10ms input range, the counter-based TDC shown in Fig. 9 is utilized. This TDC consists of both a time accumulator, which digitizes the time when phase detector output is high, and a pulse counter, which counts the number of phase detector pulses or measurement cycles. A single-measurement precision of 300ps is achieved by gating the phase detector output with a 3.33GHz clock signal. The time accumulator counts the

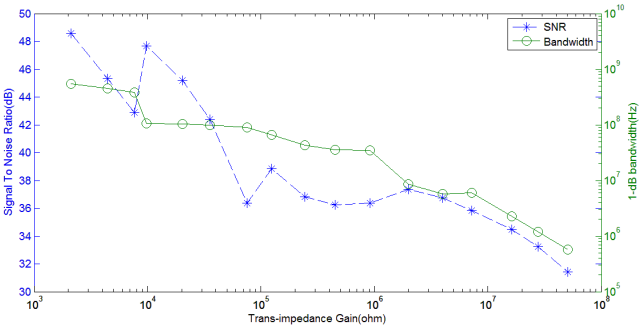

Figure 10. TIA bandwidth and output SNR.

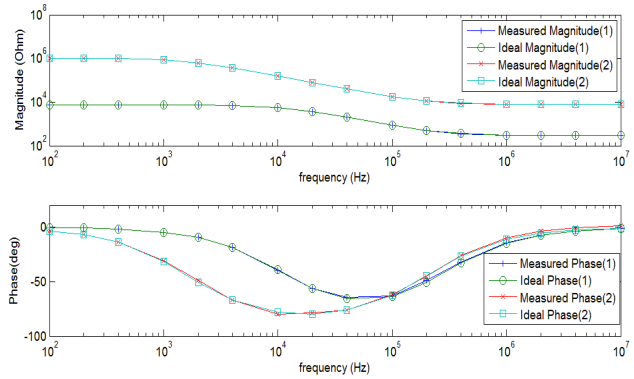

Figure 11. IS front-end cell model measurements.

number of these gated pulses with 25 D-flip-flop-based divide-by-two stages, allowing for a dynamic range in excess of 10^7. Both dynamic and static D-flip-flops are used under different working speed. By utilizing a similar pulse counter, the time difference can be accumulated over several stimulus cycles to provide increased phase accuracy.

IV. Results

The IS front-end is designed in a 1.8V 0.18µm CMOS process. Fig. 10 shows the simulated TIA output signal-to-noise ratio (SNR) and 1-dB bandwidth versus different transimpedance gain settings. The bandwidth decreases roughly proportional to the increase in TIA gain, with a >10MHz bandwidth up to a gain of 1MΩ and a 580kHz bandwidth at the maximum gain setting. While 10MHz measurements are not possible for TIA gain settings above 1MΩ, this high gain setting is generally not required for high frequency measurements due to typical cell impedance magnitudes' frequency response. The output SNR results are for a $400mV_{rms}$ output signal level, assuming a 10mV input and a constant ratio between the TIA gain and sample impedance. An SNR in excess of 30dB is achieved over the entire TIA gain setting range, with the discontinuities in the curve due to the different gain modes of operation.

Two cell impedance models are used to verify the performance of the IS front-end: 1) a low-impedance model consisting of a 300Ω resistor in series with the parallel combination of a 7kΩ resistor and a 2nF capacitor, and 2) a high-impedance model consisting of an 8kΩ resistor in series with the parallel combination of a 1MΩ resistor and a 100pF capacitor. Prior to applying the cell models, the IS front-end is first calibrated with a known-value resistor in order to determine both the exact transimpedance gain and intrinsic TIA phase shift. As shown in the simulation results of Figure 11, for both cell models the measurement magnitude and phase curves fit well with the ideal curves. Over a frequency range of 100Hz-10MHz, the maximum magnitude and phase errors are 2.5% and 2.2°, respectively.

TABLE I. Performance Summary

Parameter	Value
Technology	0.18µm CMOS
Supply Voltage	±0.9V
Frequency range	100Hz ~ 10MHz
Impedance magnitude range	100Ω ~ 1MΩ
Measurement time	>Max(6µs,1/fs)
Magnitude Measurement error	<2.5%
Phase Measurement error	<2.2°
Power Consumption	28mW
Active Area	$0.4mm^2$

Table I summarizes the IS front-end performance. Utilizing the PDC and SR-phase detector/TDC for rapid magnitude and phase measurements allows for a maximum measurement time of $1/f_s$ at low frequencies and 6µs at higher frequencies. The front-end consumes 28mW total power and occupies $0.4mm^2$ area.

V. Conclusion

A CMOS IS front-end which utilizes a time-to-digital converter (TDC) and a peak detector circuit (PDC) for rapid measurement of both impedance phase and magnitude, respectively, was presented. This fast IS front-end can enable cytometry systems capable of fast flow rates monitoring and improve scan rate for massive sensor array systems.

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