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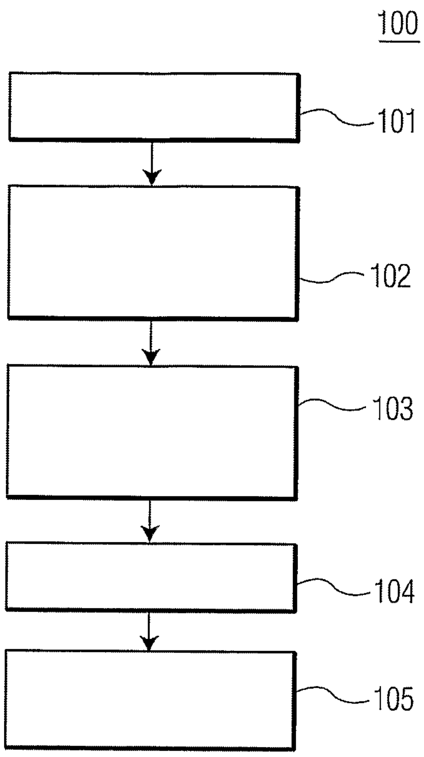
(54) Title: METHOD OF FORMING DIELECTRIC LAYERS WITH LOW DIELECTRIC CONSTANTS



(57) Abstract: A method (100) of depositing a dielectric material includes providing (101) a substrate with at least one layer over the substrate. The method further includes pre-wetting (102) a top surface of a top layer with a substance, spin coating (103) the solution and forming (104) the dielectric material. The dielectric material is illustratively SiO_2 that is relatively porous, and has a relatively low dielectric constant. The pre-wetting results in a reduction in processing costs due to a reduction in lost solution. Moreover, the dielectric layer (209) has an improved thickness uniformity.

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METHOD OF FORMING DIELECTRIC LAYERS WITH LOW DIELECTRIC CONSTANTS

Interconnection technology is constantly challenged to meet ever-increasing demands for high density of elements and high performance in very large scale and ultra large scale integration integrated circuits, or VLSI IC's and ULSI IC's, respectively.

As is well known, the speed of circuits varies inversely with the product of the resistance (R) of the circuit and the capacitance (C) of the interconnections of the IC. This so-called RC time constant must be minimized as much as possible to foster adequate signal transmission and switching speed, and to minimize signal cross-talk.

With the ever-increasing demand for greater integration and miniaturization of components in IC's a major limiting factor on the system speed can be the IC's RC limitations. Accordingly, there is a great interest in reducing the resistance and capacitance of the interconnections of the IC.

One way to reduce the RC time constants of the interconnections of an IC is to reduce the capacitance created between the various elements of the IC, by using inter-level and intra-level dielectrics (ILD's) that have a comparatively lower dielectric constant (ε_r or k). These materials usefully have a dielectric constant less than 3.9, the dielectric constant of dense SiO_2.

One type of low-k ILD is porous SiO_2 formed from hydrosilsesquioxane (HSQ), which is a flowable oxide that may be deposited by spin-on coating techniques. After the spin-on process is complete, the material is baked, and the solvent is removed, leaving silicon dioxide (glass), which is porous. The dielectric constant of the porous oxide layer is illustratively on the order of approximately 2.0 to approximately 3.8, and certainly less than 3.9. As can be appreciated, the greater the degree of porosity, the lower the dielectric constant.

The referenced dielectric materials deposited by spin-coating are often referred to as spin-on-glass (SOG) materials. While these materials have shown promise in providing low-k ILD's, their deposition can be exceedingly costly. Moreover, the thickness of the deposited ILD can be non-uniform across the wafer, which can adversely impact the consistency of the electrical characteristics of the devices and circuits formed from the processed wafer. As such, what is needed is a method of forming SOG layers in IC applications that addresses at least the referenced shortfalls of known techniques.

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According to an example embodiment, a method of depositing a dielectric material includes providing a substrate with at least one layer over the substrate. The method further includes pre-wetting a top surface of a top layer with a substance, spin coating the solution and forming the dielectric material.

According to another example embodiment, a semiconductor structure includes a layer of porous low-k dielectric material disposed over a substrate, wherein the material has a thickness across the layer, and the thickness has a uniformity across a surface with a standard deviation of +0.728%.

The invention is best understood from the following detailed description when read with the accompanying drawing figures. It is emphasized that the various features are not necessarily drawn to scale. In fact, the dimensions may be arbitrarily increased or decreased for clarity of discussion.

Fig. 1 is a flow-chart of a process of fabricating a dielectric layer in accordance with an example embodiment.

Figs. 2a-2e shows cross-sectional views of an integrated circuit during a fabrication sequence of forming a dielectric layer in accordance with an example embodiment.

In the following detailed description, for purposes of explanation and not limitation, example embodiments disclosing specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one having ordinary skill in the art having had the benefit of the present disclosure, that the present invention may be practiced in other embodiments that depart from the specific details disclosed herein. Moreover, descriptions of well-known devices, methods and materials may be omitted so as to not obscure the description of the present invention.

Fig. 1 is a flow-chart of a process 100 of forming a low-k dielectric layer over a semiconductor wafer in accordance with an example embodiment. Illustratively, the wafer includes a semiconductor substrate, and at least one other layer formed thereover. The layer or layers over the substrate may be the usual layers in an IC, including but not limited to doped and undoped semiconductor layers, dielectric layers metal layers, including patterned metal layers, and other layers within the purview of one of ordinary skill in the art in the semiconductor processing art.

At step 101, a wafer is provided. At step 102, a solvent is dispensed over the upper-most surface of the wafer. Advantageously, the solvent is chosen to provide an adequate cleaning of the top surface of the wafer. Characteristically, the solvent significantly reduces

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if not substantially eliminates the surface tension at the surface of the wafer. As described more fully below, the surface tension retards the adhering of the slurry of the SOG to the wafer, thereby impeding the deposition of the slurry.

In accordance with an illustrative embodiment, the slurry is a solution of hydrosilsequioxane polymer (HSQ) in a solution of hexamethyldisiloxane (Siloxane). The solution is illustratively 80% Siloxane / 20% HSQ by volume. In this example embodiment, the solvent used as the pre-wet is beneficially Siloxane as well. At step 102, approximately 3.0 ml to approximately 5.0 ml of the Siloxane is dispensed onto the wafer as it is rotated at approximately 75 rpm for approximately 2.5 seconds. Next, the wafer is spun at a rate of approximately 1000 rpm for approximately 4.0 seconds to spread the solvent more evenly across the entire wafer surface.

At step 103, the HSG/Siloxane solution is dispensed onto the wafer by known spin-on techniques. For optimum uniformity the SOG spread step is advantageously increased from approximately 70 rpm to approximately 75 rpm, and the rotation time is changed from 1.5 to 2.0 sec. A 'high-speed' rotation step follows the initial slurry deposition step. The rotation rate of the wafer in the 'high speed' is adjusted for optimum thickness, depending on the desired thickness of the applied SOG film. For example, for an SOG layer having a mean thickness of 4500 Angstroms the rotation rate of the wafer in high-speed step is approximately 4000 rpm. For a layer with a mean thickness of 2000 Angstroms, the rotation rate is approximately 2000 rpm.

After spin step is completed, and, as shown at step 104, the wafer is subjected to a heat treatment (baked) according to known methods. This results in the fabrication of a porous low-k SiO_2 layer. Finally, the wafer may be further processed at step 105. This further processing may include metallization processing and device fabrication per known techniques.

The fabrication sequence of the illustrative method is shown in Figs. 2a-2f, where an illustrative wafer is processed to form a low-k ILD by an exemplary method.

Fig. 2a shows a wafer 201, which includes a substrate 204, which is illustratively a semiconductor such as monocrystalline silicon. The substrate has at least one other layer disposed thereover in this stage of the processing of the wafer. These illustrative layers 202 and 203 may be other dielectric layers (e.g., ILD's), other semiconductor layers, metal layers within an oxide, and other layers within the purview of the artisan of ordinary skill. It is also noted that the low-k ILD of the example embodiments may be fabricated over the substrate directly and other layers, including those mentioned above and at least one low-k ILD the example embodiments may be formed over the first low-k ILD.

Fig. 2b shows the rotation 206 of the wafer 201 and the deposition of the pre-wet solvent 205, which is illustratively siloxane. This sequence is substantially the same as that described in connection with step 102 of Fig. 1.

After the pre-wet is completed, and as shown in Fig. 2c the slurry 207 is deposited while the pre-wetted wafer 201 is spun as at 206. This sequence is essentially the same as that described at step 103. Fig. 2d shows the slurry 208 deposited over the top surface of the wafer 201.

After the slurry is deposited, the wafer is baked, resulting in the low-k dielectric material layer's 209 being formed over the wafer 201 and as shown in Fig. 2e. This layer 209 may be an ILD, or other dielectric layer as needed. After the fabrication of the low-k dielectric layer 209, the wafer may be further processed as needed.

The processing after the pre-wetting of the wafer as at step 102 of Fig. 1 and Fig. 2b is, for the most part, well-known, and is as described for example in texts such as VLSI Principles and Technology, Silicon and Gallium Arsenide, 2nd Edition, 1994, by Soreb Ghandi, page 725. The disclosure of this reference is specifically incorporated herein by reference. However, it is noted that differences between known processing sequences and those of example embodiments will be readily apparent to one skilled in the semiconductor processing arts.

While the deposition of the slurry of step 103, and the heat treatment of step 104 may be well-known, the pre-wet of the example embodiments of step 102 of Fig. 1 and of Fig. 2b is clearly advantageous compared to known methods.

For purposes of illustration and not limitation, the method of the exemplary embodiments results in a significant reduction in the amount of slurry that is required to deposit a layer of slurry of a sufficient thickness to fabricate a low-k ILD of sufficient thickness. To this end, by performing a pre-wet as described in connection with an exemplary embodiment, the amount of slurry required to form a layer having a certain thickness was reduced from 4.0 ml by a known technique, which does not include a pre-wet, to 1.4 ml of slurry when the pre-wet of the example embodiments is used. This reduction by nearly 65% of the amount of slurry used results in a significant reduction in wasted slurry. Because the components of the slurry can be among the most expensive in processing semiconductor wafers.

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In addition to the cost savings, applicants have determined that by using the prewetting technique of the example embodiments, the uniformity across the wafer of the resultant SOG layer (low-k ILD) is significantly improved compared to known techniques. To this end, a standard method of depositing the SOG by spin-coating results in a layer having a mean thickness of 4482.73 Angstroms, with a standard deviation in thickness of ±39.3589.73 Angstroms, or ± 0.878%. Contrastingly, and while reducing the waste of the slurry, a layer of SOG fabricated using the pre-wet of the example embodiments had a thickness of 4433.09 Angstroms with a standard deviation of ±32.2566 Angstroms, or ±0.728%. Of course, this standard deviation is merely illustrative, and the standard deviation in the thickness may be less than ±0.728%. This improvement in uniformity in the thickness of the layer results in, among other benefits, electrical characteristics across circuits formed from the wafer that are more uniform and consistent.

According to another example embodiment, the thickness uniformity and reproducibility may be further improved compared to the example embodiments above, by 'priming' the wafers with hexamethyldisilazane (HMDS) before applying the pre-wet. To wit, before step 102 or the sequence of Fig. 2b, the HMDS vapor is applied, followed by a vacuum heat treatment (bake) at 120 °C for approximately 10 minutes.

The example embodiments described so far primarily focus on the use of HSQ in Siloxane solution as the material for the SOG, with Siloxane as the pre-wet. It is noted that other materials may be used as the pre-wet and the SOG slurry. For example, octamethyltrisiloxane and decamethyltetrasiloxane may be used as the pre-wet to possibly further improve the process latitude and to possibly further reduce the volume of SOG solution (slurry) required for forming the low-k dielectric for each wafer.

In yet other example embodiments, in order to achieve further economy in the amount of slurry required and in the uniformity of the films deposited, octamethyltrisiloxane (in concentration of approximately 5 to approximately 50% by volume) in combination with hexamethyldisiloxane as the solvent for HSQ instead of Siloxane alone.

The example embodiments having been described in detail in connection through a discussion of exemplary embodiments, it is clear that modifications of the invention will be apparent to one having ordinary skill in the art having had the benefit of the present disclosure. Such modifications and variations are included in the scope of the appended claims.

CLAIMS

What is claimed is:

1. A method 100 of depositing a dielectric material, the method comprising: providing 101 a substrate with at least one layer over the substrate; pre-wetting 102 a top surface of a top layer with a substance; spin coating 103 a solution and forming 104 the dielectric material.

2. The method as recited in claim 1, wherein the substance includes hexamethyldisiloxane (Siloxane).

3. The method as recited in claim 1, wherein the solution includes hydrosilsesquioxane (HSQ).

4. The method of claim 3, wherein a solvent of the solution is Siloxane.

5. The method as recited in claim 1, wherein the pre-wetting further comprises spinning the wafer while depositing the substance.

6. The method as recited in claim 1, wherein the dielectric material is SiO_2.

7. The method as recited in claim 2, wherein the method further comprises, before the pre-wetting, priming the wafer with a vapor of hexamethyldisilazane (HMDS), and after said priming, but before said pre-wetting, applying heat to the substrate.

8. The method as recited in claim 1, wherein the substance is octamethyltrisiloxane.

9. The method as recited in claim 1, wherein the substance is decamethytetrasiloxane.

10. The method as recited in claim 2, wherein the substance includes octamethyltrisiloxane.

11. A semiconductor structure 201, comprising: a layer of porous low-k dielectric material 209 disposed over a substrate 202,203,204, wherein the material has a thickness across the layer, and the thickness has a uniformity across a surface with a standard deviation of +0.728%.

12. A semiconductor structure as recited in claim 11, wherein the surface is a top surface of a wafer.

13. A semiconductor structure as recited in claim 11, wherein the layer is an inter-layer dielectric layer.

14. A semiconductor structure as recited in claim 11, wherein the layer is an intra-layer dielectric layer.

15. A semiconductor structure as recited in claim 11, wherein the layer has a dielectric constant in the range of approximately 2.0 to approximately 3.8.

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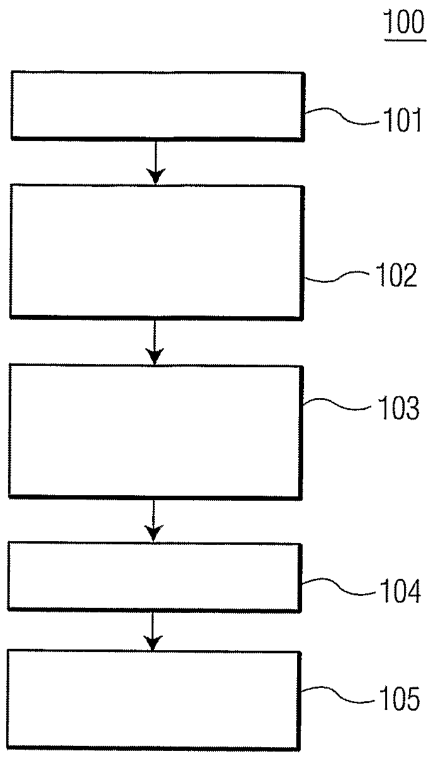

FIG. 1

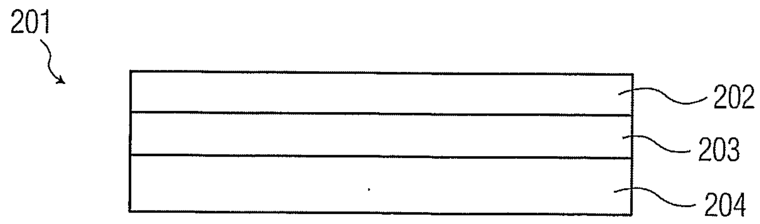

FIG. 2A

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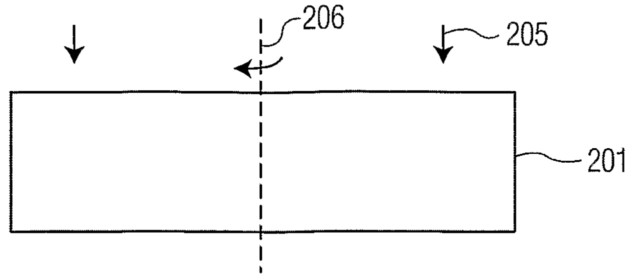

FIG. 2B

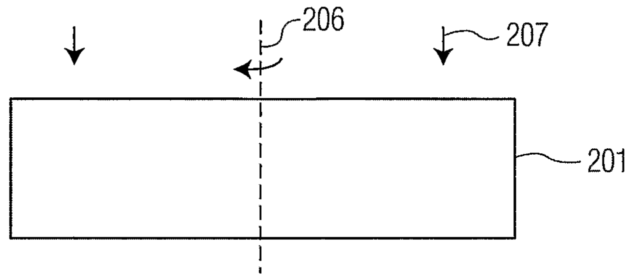

FIG. 2C

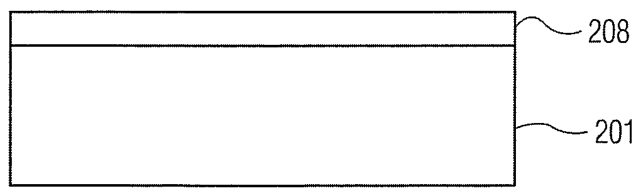

FIG. 2D

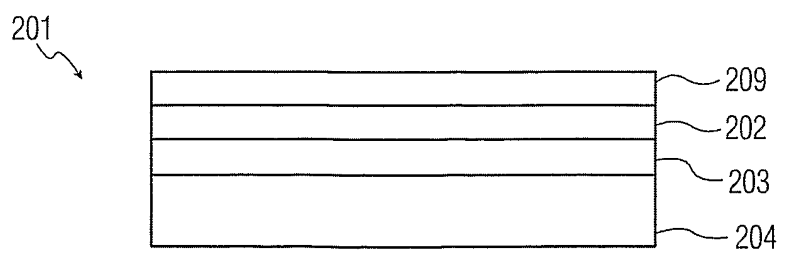

FIG. 2E

INTERNATIONAL SEARCH REPORT

International Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/312 H01L21/316

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
20 December 2004	29/12/2004

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INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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