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(71) 가 가 2 2 3

(72) 2 2 3 가 가

(74)

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(54) 가

(100) (10) , (20) , (30) , (40) ,  
(50) H (60) , (70) , DLL(80) , I/O (90) , QS (110) .  
TMDQS (70) L TMDQS (70) L  
DQS DQS DQS (70) L  
QS (110) (70) H TMDQS , CLK QS (110) CLK

1

1 1 ,

2 1 ,

3 1 QS ,

4 1 , QS ,

5 1 ,

6	1	,	QS	,
7	1	,		
8	1	,		
9	1	,		
10	1	,		
11	1			,
12	1			,
13	2		,	
14	13		,	
15	13		,	
16	13			,
17	3		,	
18	17		,	
19	17			,
20	17			
21	17			
22	17			,
23	4		,	
24	23			,
25	5		,	
26	25			
27	25			
28	25			,
29	6		,	
30	29			,

31	7	,
32	31	,
33	DDR-SDRAM	,
34	33	DDR-SDRAM
35	33	DDR-SDRAM

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1, 2, 5, 6, 701, 703, 721, 723 : P MOS

3, 4, 7, 8, 702, 704, 712, 714, 722, 724 : N MOS

10, 210 : 20, 220 :

30, 230 : 40, 240 :

50~56, 250 : 60, 260 :

61~64 : 70~2 :

80, 270 : DLL 90, 280 : I/O

100~106 : 110, 290 : QS

120 : 121, 122 :

200 : DDR-SDRAM 610 :

620 : 630 :

640 : 650 :

651~65m : 705, 715, 725 :

WL1~WLn : BL1, /BL1~BLm, /BLm :

MC : BS1, BS2 :

TG1, TG2, TG3, TG4, TG5, TG6 :

DFA1, DFA2 :

WRE : N1~N4 :

VDD : GND :

가

DDR-SDRAM(Double Data Rate Synchronou

s Dynamic Random Access Memory)

33 , DDR-SDRAM(200) (210) , (220) , (230) ,  
 (240) , (250) , (260) , DLL(Delay Locked Loop)(270) , I/O (280) ,  
 QS (290) , BS1, BS2

(210) A0-A12 BA0, 1 A0-A12 A0-A12  
 BA0, 1 (220) BUFF\_CLK, BUFF\_/CLK (240)

(220) CLK, /CLK CKE INTVREF INTVREF CLK, /CLK  
 CKE INTVREF (220) INTVREF BUFF\_C  
 LK, BUFF\_/CLK (230), (240) DLL(270) , (220) BUFF\_C  
 KE (240)

(230) /CS, /RAS, /CAS,  
 /WE INTVREF DM , (230) /CS /CS  
 INTVREF (220) BUFF\_CLK, BUFF\_/CLK (240)

(240) (220) BUFF\_CLK, BUFF\_/CLK  
 CKE가 H( High) BUFF\_CLK, BUFF\_/CLK CKE가 L( Low) ,  
 (240) BUFF\_CLK, BUFF\_/CLK

(240) , BUFF\_CLK, BUFF\_/CLK (230)  
 /WE /CS, DM /RAS, /CAS,  
 (200)

(240) L /CS (200)가 (200)가  
 , H (240) (210) BA0, 1 (260)  
 (240) (210) (240) /RAS가 H  
 L (220) A0 A12 (2) BUFF\_CLK, BUFF\_/CLK

(240) /CAS가 H L (220)  
 (210) BUFF A0 A12 (260)

(240) /WE QS (290)  
 (240) , INTDQS DQ0 DQ7 (260) I/O (280)  
 INTDQS I/O (280)  
 QS (290) (240) , (260) BS2  
 DQ0 DQ7 DQS I/O (280) , DLL(270) DLLCLK\_P DLLCLK\_N  
 N DQS QS (290) , DLL(270) DLLCLK\_P DLLCLK\_  
 , (240) DM I/O (280) , (



(240) (250) (250) DLL(270) (240)

(240) (250) DLL(270)

BA0, 1 (240) BA0, 1 (240) DDR-SDRAM(200) BA0, 1 (210) BUFF\_CLK, BUFF\_/CLK

(240) (210) BA0, 1 (260)

12 A0-A12가 (240) DDR-SDRAM(200) (210) A0-A (240)

A0-A12 (230) A0-A12 (240) BUFF\_CLK, BUFF\_/CLK /RAS가 DDR-SDRAM(200) /RAS

(240) L /RAS (240) BUFF\_CLK, BUFF\_/CLK

A0-A12 (240) L /RAS (210) BUFF\_CLK, BUFF\_/CLK

(230) L INTVREF /CAS가 L DDR-SDRAM(200) /CAS (240)

L /CAS (240) L /CAS (210) A0 (260)

-A12 (240) L /CAS (210) A0 (260)

QS (290) INTVREF (280) DQS (290) DQS (290) DQS INTDQS I

I/O (280) DQW (290) DQS DQW INTDQS I/O (280) DQ0-DQ7 (280)

DQW QS (290) INTDQS

(260) ( ) (240) ( ) ( )

240) DQW

DDR-SDRAM(200) DQW INTDQS DQS

DDR-SDRAM(200)

35 (230) QS (290) DDR-SDRAM(200) VREF가 VREF DDR-SDRAM(200) (220), INTVREF

DDR-SDRAM(200) CLK, /CLK, (240)가 DDR-SDRAM(200) CKE L /CS가

DDR-SDRAM(200)가 /RAS, L H /CAS가 /WE, H DDR-SDRAM(200)



1 가 , / 1  
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 , 가,  
 가 . , .  
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 ( 1)  
 1 , 1 (100) (10) , (20) , ( (30) , (40) , (50) , (60) , (70) , DLL(80) , I/O (90) , QS (110) , BS1, 2 (60) (61 64) .  
 (100) , DDR-SDRAM .  
 (10) A0 A12 BA0, 1 , A0 A12 BA0  
 , 1 BA0, 1 (20) BUFF\_CLK, BUFF\_/CLK (10) A0-A12 (40) .  
 (20) CLK, /CLK CKE INTVREF CLK, /CLK  
 BUFF\_CLK, BUFF\_/CLK (10), (30), (40) DLL(80) ,  
 VREF CKE (40) INTVREF  
 (30) /CS, DM /RAS, /CAS,  
 /WE /RAS, INTVREF /CS /WE /CS DM  
 , BIUFF\_/CLK (40) , BUFF\_CLK  
 (40) , (20) BUFF\_CLK, BUFF\_/CLK C (4 BU  
 KE가 H( High) , BUFF\_CLK, BUFF\_/CLK CKE가 L( Low) , BU  
 FF\_CLK, BUFF\_/CLK .  
 , (40) , BUFF\_CLK, BUFF\_/CLK (30)  
 /WE /CS, DM /RAS, /CAS,  
 (100) .  
 , H , (40) , L /CS (100)가 (100)가 ,  
 (40) (10) BA0, 1 (61 64)  
 , (40) , /RAS가 H L  
 (10) A0 A12 (61 64) (20)  
 ) BUFF\_CLK, BUFF\_/CLK .  
 , (40) , /CAS가 H L  
 (10) A0 A12 (61 64) (20)

, (40) , /WE  
(40) , INTDQS (61 64) DQ0-DQ7 (61 64) I/O (90) QS (110) , (40) ,  
LLCLK\_P , DLLCLK\_N (61 64) BS2 DQ0-DQ7 (61 64) I/O (90) DLL(80) , DLL(80) D  
DLLCLK\_P DLLCLK\_N DQS QS (110) .

(40) , (40) DM I/O (90) . DM H , ( (40) , DM ,  
, H (61 64) DM I/O (90) , L DM H DM ,  
H (61 64) I/O (90) , L (40) , DM ,  
I/O (90) DM I/O (90) , L DM

(40) , (50) CAS CL (50) DLL(80)  
가 ,

(50) CAS CL (40) CAS CL (40) (40) (50) . ,  
(50) DLL(80) (100) H L (40) TMDQS (70) (50)

(60) (61 64) , , (70) DQS (70)  
DQS TMDQS CLK CLK DQS CLK  
, QS (110) .

DLL(80) (20) BUFF\_CLK, BUFF\_/CLK , CLK, /CLK  
(90) QS (110) DLLCLK\_P, DLLCLK\_N , DLLCLK\_P, DLLCLK\_N I/O

I/O (90) , DQ0-DQ7 (61 64) QS (110) , I/O (90) ,  
, INTDQS (61 64) BS2 DLL(80) , DLLCLK\_P,  
DLLCLK\_N DQ0-DQ7 .

QS (110) , (70) DQS INTDQS CLK  
(90) INTVREF , QS (110) , , DLL(80) DLLCLK\_P, DLLCLK\_N  
DQS

/RAS BS1 (40) A0 A12, BA0, 1 BS2 (61  
64) (61 64) I/O (90) .

(100) EXT VDD (100)  
( ) EXT VDD , VBL (60) .

2 (61 64) (610) , (620) , (630) ,  
(640) , (650) .

(610) (40) ,  
(620) (620) (610)  
( WL1 WLn , n ) .

(630) (40) ,

( BL1, /BL1 BLm, /BLm , m ) (640) ,  
 , I/O (90) ( BL1, /BL1 BLm, /BLm )  
 ) (640) , ( BL1, /BL1 BLm, /BLm  
 I/O (90) )

(650) BL1, /BL1 BLm, /BLm , WL1 WLn ,  
 (651 65m) , n x m MC (651 65m)  
 BL1, /BL1 BLm, /BLm (651 65m) ,  
 MC ( BL1, /BL1 BLm, /BLm )  
 VBL(=EXTVDD/2)

n x m MC ( BL1 BLm, /BL1 /BLm ) ( WL1 W  
 Ln ) ( WL1 WLn ) ( B  
 L1 BLm, /BL1 /BLm ) MC 가 .

3 , (70) P MOS (701, 703) , N MOS (702, 704)  
 , (705) . P MOS (701) , 가 N MOS (702)  
 , 가 N MOS (702)

P MOS (703) , 가 N MOS (704) ,  
 가 N MOS (704)

P MOS (701) N MOS (704) (50)  
 TMDQS

P MOS (703) (701) N MOS (704) (702) TG1 . , P M  
 OS (703) N MOS (704) TG2 .

(705) (50) TMDQS , TMDQS N  
 MOS (702) P MOS (703)

QS (50)가 L TMDQS (70) , (705) L TMD  
 H N MOS (702) P MOS (703)  
 , P MOS (701) N MOS (704) L TMDQS

3) N , P MOS (701) N MOS (702) , P MOS (70)  
 MOS (704) . TG1 , MOS DQS (70)  
 DQS DQS0 QS (110)

TMDQS (50)가 H TMDQS (70) , (705) H  
 L N MOS (702) P MOS (703) H TMDQS  
 , P MOS (701) N MOS (704)

703) N , P MOS (701) N MOS (702) , P MOS ( )  
 MOS (704) . TG2 , MOS CLK  
 CLK DQS0 QS (110)

, (70) L TMDQS DQS ,  
 DQS QS (110) , H TMDQS DQS CLK ,  
 CLK QS (110)

4 DFA1 , P MOS (20), (30) QS (110) DFA1 .  
 (1) N MOS (3) (1, 2) N MOS (3, 4) . P MOS  
 VDD GND

P MOS (2) N MOS (4) VDD GND  
 . P MOS (1) N MOS (3) P MOS (2) N MOS  
 (4)

P MOS (1, 2) N1 N MOS (4) N MOS (3)  
 INTVREF . N MOS (4) SGN

SGN , DFA1 (30) /CS  
 DFA1 QS (110) (70) DQS C  
 LK .

DFA1 , SGN INTVREF  
 N1 , DFA1 , SGN  
 INTVREF , H N1 SGN  
 INTVREF , L N1

5 (20) DFA2 DFA2 P MOS (5) N MOS (7)  
 (5, 6) N VDD MOS (7, 8) GND . P MOS (5) N MOS (7)

P MOS (6) N MOS (8) VDD GND  
 . P MOS (5) N MOS (7) P MOS (6) N MOS

P MOS (5, 6) N2 N MOS (8) MOS (7)  
 CLK CLK . N MOS (8) /CLK /

DFA2 , CLK /CLK  
 BUFF\_CLK, BUFF\_/CLK N3, N2

6 DFA1, 2 DFA  
 1 (30) , N MOS (4) /WE D  
 FA1 (30) , N MOS (4) /WE

N MOS (4)가 H /WE /WE DFA1  
 , H /WE N1 INTVREF ,

H DFA1 , H /WE INTVREF N1  
 /WE N1

, N MOS (4)가 L /WE /WE DF  
 A1 , L /WE N1 INTVREF ,

L DFA1 , L /WE INTVREF N1  
 /WE N1

, DFA1 , N MOS (4) /WE /WE  
 INTVREF , /WE

N1

DFA1 , /WE /CS, /RAS,  
 /CAS DM N MOS (4) MOS (4)

, /WE가 N MOS (4)

(30) /WE INTVREF

DFA1 QS (110) DQS

DFA1 QS (110) , N MOS (4)

DQS

N MOS (4)가 L DQS DFA

1 , L DQS INTVREF

L DFA1 , L DQS INTVREF INTDQS N1

N MOS (4)가 H DQS DF

A1 , H DQS INTDQS N1 INTVREF

H DFA1 , H DQS INTVREF INTDQS N1

QS DFA1 , N MOS (4) D

DQS N1 INTVREF DQW DQS

DQ0-DQ7 I/O (90)

DFA1 DQS DQS가 N MOS CLK가 N MOS (4)

QS (110) DQS CLK INTVREF

DFA1 (20) DFA1 MOS (4) CKE

DFA1 CKE

(7) CLK DFA2가 (20) MOS (8) CLK N MOS /CLK

DFA2 , /CLK CLK

UFF\_CLK N3 BUFF\_CLK N2

N MOS (7)가 H CLK , N MOS (8)가 L

/CLK BUFF\_CLK N3 DFA2 , L BUFF\_CLK N2

, N MOS (7)가 L CLK , N MOS (8)가 H

/CLK BUFF\_CLK N3 DFA2 , H BUFF\_CLK N2

DFA2가 , /CLK CLK INTVREF

LK DFA2 INTVREF CLK, /C

UFF\_CLK, BUFF\_CLK, BUFF\_CLK

6 LV INTVREF 가 H L

7 8 (100)

DDR-SDRAM

(100)가 (70) DQS (70) L QS (10) (50) L TMDQS TMDQS DQS

7 (100) (20), (30) QS (110) VREF가 VREF

INTVREF

CLK, /CLK (20) DFA2 CKE가 (100) CLK, /CLK (40) DLL(80) (100)

BUFF\_CLK, BUFF\_/CLK (20) DFA1 (30), CKE (40)

CKE (40)

L /CS가 (100) (30) /

CS INTVREF L /CS (40)

L (40) BUFF\_CLK BUFF\_/CLK CKE가 H (40) BUFF\_C (100)

LK BUFF\_/CLK L /CS

L /WE, H /RAS L (30) L /CAS /

/CAS가 (100) /RAS L (30) L /CAS (40)

WE, H INTVREF /RAS L /CAS (40)

(40) (30) L /WE, H

/RAS L

(40) (50) DLL(80) (40)

(40) (50) DLL(80)

BA0, 1 (100) (10) BUFF\_CLK, BUFF\_/CLK

(40) (40) BA0, 1 (60)

(61 64)

2가 /RAS가 H L A0-A1 A0-A1

A0-A12 (100) (10) A0-A12 (40) L (30)

/RAS가 (100) L

L /RAS BUFF\_CLK (40)

(40) ( )가 L /RAS, H (10)

/CAS H /WE

A0-A12 (60) X (61 64) , X BUFF\_CLK  
 가 , /CAS가 H L A0-A12  
 (100) (10) Ab-A12 ,  
 A0-A12 BUFF\_CLK, BUFF\_/CLK (40)  
 , L /CAS가 (30) INT  
 VREF L /CAS BUFF\_CLK /CAS (40) L  
 (40) ( )가 H /RAS L  
 /CAS (10) A0-A12  
 Y (61 64) Y BUFF\_CLK, BUFF\_/CLK (60)  
 , QS (110) DQS (70) , QS (110)  
 DQS INTDQS I/O INTVREF (90)  
 I/O (90) DQS DQWH DQ0-DQ  
 7 DQWH INTDQS , I/O (90) DQW (60)  
 H QS (110) (61 64)  
 , (60) , (610) (40) X , X  
 X (620) (620)  
 WLi(1 i n)  
 , (630) (40) Y , DQWH Y  
 BLj, /BLj BLj, /BLj(1 j m) MC (640) WLi  
 , (100) , DQWH INTDQS DQS MC  
 , 8 , MC (100) , (20),  
 (30) QS (110) VREF가 VREF INTVREF  
 (100) , CLK, /CLK, (40)가 CKE L /CS가  
 (100) , H /WE, H  
 /RAS L (100)가 , H /CAS가 (100)  
 (30) H /WE, H /RAS L  
 /CAS /CAS INTVREF (30)  
 H /CAS /WE, H /RAS L  
 (40) (30) H /WE, H  
 /RAS L /CAS  
 40 , (50) DLL(80) (40) (50) CAS (

CL (40) (50) CAS CL  
DQ0-DQ7 I/O (90)

, DLL(80) (20) BUFF\_CLK, BUFF\_/CLK , CLK, /CLK  
DLLCLK\_P, DLLCLK\_N , DLLCLK\_P, DLLCLK\_N I

/O (90) QS (110)

, BA0, 1 (100)  
BA0, 1 ( 61 64 )가

, A0-A12가 (100)  
X Y가 (60) ( 61 64 )  
X Y MC가

, 가 MC (60) (640)  
DQRH BS2 I/O (90)

, I/O (90) (50) CAS CL( 8 CAL=2  
DQRH , DLL(80) DLLCLK\_P DLLCLK\_N  
LCLK\_N DQ0-DQ7 , QS (110) DLL(80) DLLCLK\_P DL  
DQS

, (100) 가 BUFF\_CLK, BUFF\_/CLK  
LLCLK\_N , DQRH (100) DLLCLK\_P, D

, (100) , L TMDQS가 (50) (70)  
DQS DLLCLK\_P DLLCLK\_N

MC

9 10 (100)  
, DDR-SDRAM 가

(100)가 (50) H TMDQS  
(70) CLK , QS (110) (70) H TMDQS , TMDQS  
CLK

9 (100) , (20), (30) QS (110) VREF가  
INTVREF VREF

( 61 64 ) , (60) (61 64) 가 ,  
WLi BLj, /BLj가

, QS (110) CLK (70) , CLK INTVREF  
O (90) , QS (110) CLK INTDQS I/  
INTDQS(=CLK)

I/O (90) CLK DQWL1 DQ0-DQ7 ,  
DQWL1 , I/O (90) DQWL1 QS (110)  
( 61 64 )  
) (60)

, , DQWL1 CLK (100)  
, INTDQS(=CLK) MC

, 10 , MC  
 (30) QS (110) VREF가 VREF (100) , (20), INTVREF  
 ( (61 64) ) (60) (61 64) 가 ,  
 , 가 MC (60) (640)  
 DQRL1 BS2 I/O (90)  
 , (40) DLL(80) DLLCLK\_P DQRL1  
 DQ0-DQ7 I/O (90)  
 2.0) , I/O (90) (50) CAS CL( 10 CAL=  
 DQ0-DQ7 , DLL(80) DLLCLK\_P DQRL1  
 , QS (110) DLL(80) DLLCLK\_P DQS  
 , (100) DQRL1 (100) 가 BUFF\_CLK MC  
 , DLLCLK\_P  
 , (100) , H TMDQS가 (50) (70)  
 , CLK DLLCLK\_P MC  
 , (100) (50)가 L TMDQS (70)  
 , (70) L TMDQS QS (110) CLK TMDQS CLK (70)  
 100) DQS DDR-SDRAM  
 , TMDQS (50)가 H TMDQS (70) (70) H  
 CLK QS (110) DQS (100) DDR-SDRAM CLK  
 , 가  
 S) 1 , DQS ( DQ  
 ( CLK) 2 CLK  
 , L TMDQS 「 1 」 , H TMDQS 「 2 」  
 , (10), (20), (30), (40), DLL(80), I/O (90), QS (110),  
 (610), (620), (630) (640) (70)  
 「 」  
 , CLK, /CLK, BUFF\_CLK, BUFF\_/CLK, DQS DLLCLK\_P, DLLCLK  
 \_N , BUFF\_CLK, BUFF\_/CLK  
 , (100) H TMDQS L TMDQS가 (50)  
 (50) , (100)가 TMDQS가 , L TMDQS가  
 (50) (100)가 , H TMDQS가

(100)가 A0-A12, 가 WRE BA0, 1, EXT VDD, VREF /CS

DQS (100)가 WRE (100)가

1 DQS CLK

가 가,

( 2)

13 (51) 2 (70) (101) (71) (100) (50) (120) 가

(51) TMDQS TMVREF (71) (50)

1 (120) VREF2 EXT VDD (120) EXT VDD 2 VR

EF2 (71)

(71) VREF (71) (51) VREF2 (120)

VREF F2 INTVREF (20), (30) QS VREF (110) VRE

14 GND (122) (120) (121, 122) VDD (121, 122) EXT VDD VDD (121)

VREF2 N4 (120) EXT VDD 2 1

15 (715) (71) P MOS (711, 713) , N MOS (712, 714)

P MOS (711) , P MOS (711) 가 N MOS (712) (712) TMVREF

, N MOS (712) (715) (51)

P MOS TG3 (711) N MOS (712) VREF TG3

P MOS (713) , P MOS (713) (715) (714) TMVREF

, N MOS (714) (51)

P MOS TG4 (713) N MOS (714) VREF2 TG4

(71) (71) L (715) L TM

VREF (51)가 H L TMVREF N MOS (712) P MOS (713)

, P MOS (711) N MOS (714) L TMVREF

3) N , P MOS (711) N MOS (712) , P MOS (71) VR  
 EF N MOS (714) INTVREF TG3

TMVREF (51)가 H TMVREF (71) (715) H  
 L N MOS (712) P 1 MOS (713)  
 , P MOS (711) N MOS (714) H TMV REF

713) N , P MOS (711) N MOS (712) , P MOS (120) (  
 N MOS (714) INTVREF TG4

VREF (71) (51) TMVREF  
 VREF VREF2 (120) INTVREF VREF2

, (20), (30) QS (110) , (71) VREF가  
 INTVREF VREF LV( 6 )

, (20), (30) QS (110) , (71) VREF2가  
 INTVREF VREF2 LV( 6 )

VREF VREF2 , DDR-SDRAM , DDR-SDRAM  
 가 100 MHz VREF ± 2% VREF  
 /WE CLK, /CLK VREF

TVDD VREF2 VREF , EX  
 TVDD 1 , EXTVDD EXTVDD  
 VREF2 VREF

LV , (20), (30) QS (110) VREF2

, (101)가 (101)가 VREF2 VREF  
 (101)가

, (51) , (101)가 , L TMVREF  
 (71) VREF (71) , L TMVREF  
 (30) QS (110) INTVREF (20),

, (51) , (101)가 , H TMVREF  
 (71) VREF2 (71) , H TMVREF  
 (120) (20), (30) QS (110) VREF2 INTVR

, (70) (101) , 7 8 , TMDQS TMVREF  
 (71) 1

EF, (70) (101), 9 10, TMDQS TMVR  
 1 (71)

, 2, VREF ( VREF)  
 1 ( EXTVDD) VREF2 2

, L TMVREF 「 1 」, H TMVREF 「 2 」

, (101) H TMVREF L TMVREF가 (51)  
 (51) (101)가 (101)가, L TMVREF가  
 REF가 (51) (51) (101)가, H TMVREF가 TMV

, (101)가 11, /CS  
 A0-A12, BA0, 1, EXTVDD VREF  
 가 WRE

, (101)가 16, VREF  
 가 WRE VREF  
 VREF VREF

2, VREF VREF2  
 가, VREF

( 3)

17 (52), 3 (70) (102), (100) (50) (1  
 00) (72)

) (52) TMDQS (50) TM/CLK (72) (50)

/CLK (72) (52) TM/CLK INTVREF /CLK INTVREF  
 (20) /CLK0

18 (725), (72) P MOS (721, 723), N MOS (722, 724)

P MOS (721), 가 N MOS (722) TM/CLK  
 . P MOS (721) (52)  
 . N MOS (722) (725)

P MOS (721) N MOS (722) TG5,  
 TG5 /CLK

P MOS (723), 가 N MOS (724)  
 . P MOS (723) (725)  
 MOS (724) (52) TM/CLK . N

P MOS (723) N MOS (724) TG6,  
 TG6 INTVREF

CLK (52)가 L TM/CLK (72) (725) L TM/  
 H MOS N MOS (721) N MOS (724) L (723) TM/CLK  
 , P MOS  
 3) N , P MOS MOS (721) N MOS (722) , P MOS (72  
 MOS (724) , TG5 /CLK /CLK0  
 , TM/CLK (52)가 H TM/CLK (72) (725) H  
 L MOS N MOS (721) N MOS (724) H (723) TM/CLK  
 , P MOS (721) N MOS (722) , P MOS (723) ( (723) N MOS (724) H INTVREF )  
 /CLK0  
 , INTVREF (72) (52) /CLK TM/CLK INTVREF /CLK  
 (20) /CLK0  
 , 3 , (20) DFA2 , 19 , /CLK0  
 N MOS (8)  
 , N MOS (8)가 /CLK0 /CLK  
 DFA2 /CLK0 INTVREF INTVREF INTVREF , N MOS (8)가  
 INTVREF INTVREF DFA2 CLK (8)가  
 BUFF\_CLK N3 BUFF\_CLK N2  
 BUFF\_CLK INTVREF , N DFA2 H L  
 /CLK0 INTVREF MOS (8)  
 , (20) , (72) /CLK0 INTVREF ,  
 BUFF\_/CLK  
 BUFF\_/CLK (20) , (72)가 /CLK 2 BUFF\_CLK,  
 (72)가 INTVREF , BUFF\_/CLK  
 , DLL(80) (20) BUFF\_/CLK DLLCLK\_N ,  
 DLLCLK\_N I/O (90) QS (110) DLLCLK\_N ,  
 , (52) , (102)가 , L TM/CLK  
 /CLK (72) , /CLK (72) L TM/CLK  
 (20)  
 , (52) , (102)가 , H TM/CLK  
 (72) , INTVREF (71) H (20) TM/CLK IN  
 TVREF  
 , (102) , 7 8 , TMDQS TM/CLK  
 (70) (72) 1  
 20 21 , (102)

(102)가 (72) VREF, (72) H, (52) H, TM/CLK, TM/CLK, VREF (20)

20 VREF (102), (20), (30), (72) VREF가 QS (110)

CLK (52) H, TM/CLK, CKE가 (72) (102)

(20) (72) H, TM/CLK, INTVREF, BUFF\_/CLK (10), (30), (20) CLK, DLL(80), (20) CKE, (40) DFA1

, L INTVREF /CS가 (102), (30) /CS, L (40) /CS, L

CS BUFF\_/CLK (40) BUFF\_/CLK, CKE H, CKE가 H, L (40) BUFF\_/CLK (102)

, L /WE, H, /RAS L, /RAS L, /CAS (40) /CAS, /

WE, H INTVREF (102) /RAS L, (30) L, /CAS (40) /CAS, /

, (40) /RAS L, (30) L, /CAS, /WE, H

(40) (52) DLL(80), (40) DLL(80)

BA0, 1 (102) BA0, 1, BUFF\_/CLK (10) (40)

(40) (61 64) (10) BA0, 1, (60)

2가 /RAS가 H, L, (10) A0-A12, A0-A12, (40) A0-A12, (10) A0-A1

L /RAS가 (102) BUFF\_/CLK, (102) /RAS, L, (30) /RAS, L, /RA

S BUFF\_/CLK (40) /RAS, H, /WE, X, BUFF\_/CLK (10)

(40) /CAS H, ( )가 L, /RAS, H, (10) A0-A12, X, (61 64), ( )

가 /CAS가 H, L, (10) A0-A12, A0-A12

A0-A12      BUFF\_/CLK      (40)      .  
 , L      /CAS가      (30)      IN  
 TVREF      L      /CAS      (40)      .  
 /CAS      가 H      /RAS L      Y  
 (40)      BUFF\_/CLK      (10)      A0-A12      (61 64)  
 ,      Y      BUFF\_/CLK      (60)      (      Y  
 )      .  
 , QS      (110)      DQS      INTVREF      , QS  
 (110)      INTDQS      I/O      (90)      .  
 I/O      (90)      DQS      DQWL2      DQ0-DQ7  
 S      (110)      DQWL2      INTDQS      , I/O      (90)      DQWL2      Q  
 (61 64)      )      .      INTDQS      (60)      (      (

,      (60)      ,      (610)      (40)      X      ,      X  
 X      WLi      (620)      .      (620)      X      X  
 ,      (630)      (40)      Y      ,      Y  
 WLi      BLj, /BLj      MC      DQWL2      (640)      Y  
 BLj, /BLj      .      .  
 (102)      ,      DQWL2      INTDQS      DQS      MC      .  
 ,      21      ,      MC      (102)      ,      (20),      (

30),      (72)      VREF가      VREF      (102)      ,      (20),      INTVREF  
 QS      (110)      VREF      (102)      ,      (20),      INTVREF  
 .  
 (      (61 64)      ,      )      WLi      (61 64)      가      ,  
 .  
 ,      가      MC      ,      (60)      (640)  
 DQRL2      BS2      I/O      (90)      .  
 ,      (40)      DLL(80)      DLLCLK\_N      DQRL2  
 DQ0-DQ7      I/O      (90)      .  
 , I/O      (90)      ,      (52)      CAS      CL( 21      CAL  
 =2.0)      DQ0-DQ7      , DLL(80)      , QS      (110)      DLLCLK\_N      DLLCLK\_N      DQRL2      DQS  
 .  
 ,      (102)      ,      가      BUFF\_/CLK      DLLCLK\_N      MC  
 DQRL2      (102)      .  
 ,      (102)      , H      TM/CLK가      (52)      (72)  
 DQS      DLLCLK\_N      DLLCLK\_N      MC  
 .      ,      (102)

1, 3, /CLK ( /CLK)  
 ( VREF) INTVREF 2 .  
 , L TM/CLK 「 1 」 , H TM/CLK 「 2 」  
 , (102) H TM/CLK L TM/CLK가 (52)  
 (52) (102)가 (102)가 , L TM/CLK가  
 CLK가 (52) , H TM/CLK가  
 (102)가 11 /CS  
 A0-A12, BA0, 1, EXT VDD , VREF  
 가 WRE .  
 (102)가 , 22 /CLK , /CLK  
 가 WRE . , /CLK  
 1 .  
 3 , , /CLK /CLK INTVREF  
 가, , 가  
 ( 4)  
 23 , 4 (103) (100) (50)  
 (53) , (71) (120) 가 ,  
 (100) .  
 (53) (50) 가 , TMVREF (71) .  
 (71) (120) 2 .  
 (103)가 , (53) , L TMDQS  
 (70) , L TMVREF (71) .  
 (70) L TMDQS (71) L DQS DQS  
 (110) , (71) L VREF VREF  
 (30) QS (110) . TMVREF INTVREF (20),  
 , (103)가 , (53) , H TMDQS  
 (70) , H TMVREF (71) .  
 (70) H TMDQS CLK CLK QS (110)  
 (71) H TMVREF VREF2 (120) (20),  
 VREF2 (30) QS (110) . INTVREF  
 (103) L TMVREF 7 8 가  
 (103) , 1 가  
 , 2 , (120) , (71) 가

가 (103) H TMVREF 9 10  
 (103) (120) 1 (71)

가

4 1 DQS ( DQS)  
 VREF ( VR  
 CLK  
 EF) ( CLK) 2 ( EXTVDD) VREF2 2

L TMDQS TMVREF 「 1 」 , H TMDQS TMVREF  
 「 2 」

4 (103)  
 2

(103) H TMDQS TMVREF L TMDQS TMVREF가  
 (53) TMVREF가 (53) (103)가 , L  
 TMDQS , H TMDQS TMVREF가 (53) (103)가

(103)가 11 /CS  
 A0-A12, WRE BA0, 1, EXTVDD VREF

DQS (103)가 24 WRE  
 DQS VREF 2

(70) (71) 1  
 2

(70) (71) 2

1 2

4 VREF DQS CLK  
 INTVREF

가 , 가,  
 가 ,

( 5)

25 5 (104) (100) (50)  
 (54) (72) 가 , (100)

(54) (50) 가 , TM/CLK (72)

(72) 3

(104)가 , L (70) , L TM/CLK (54) , L (72) TMDQS

QS (70) L TMDQS (72) L DQS (70) /CLK (110) /CLK (20) TM/CLK DQS /CLK

(104)가 , H (70) , H TM/CLK (54) , H (72) TMDQS

(70) H TMDQS (72) H CLK TM/CLK CLK INTVREF QS (110) (20)

(104) L (104) TM/CLK 7 8 가 (104) (72) 가 1

26 /CLK BUFF\_CLK (104) 9 H 26 TM/CLK 가 3 (103) (72) 가 1

(104) 10 H 27 TM/CL K 가 27 /CLK BUFF\_CLK (90) (72) 가 (103) 3 I/O (90) , 3 1 I/O

5 , DQS ( DQS) 1 /CLK ( /CLK) 1 CLK 2 ( VREF) INTVREF 2

, L TMDQS TM/CLK 「 1 」 , H TMDQS TM/CLK 「 2 」

5 , (104) , 2

(54) (104) H TMDQS TM/CLK L TMDQS TM/CLK가 , L TMDQS TM/CLK가 (54) (104)가 (54) (104)가

(104)가 A0-A12, BA0, 1, 11 EXT VDD , VREF /CS 가 WRE

DQS (104)가 , 28 /CLK /CLK 2 가 WRE

(70) (72) 1  
 2

(70) (72) 2

1 3

5 , /CLK , INTVREF DQS CLK ,  
 가, 가

( 6)

29 (55) 6 (72) (105) 가 , (101) (101) (51)  
 (55) (51) 가 , TM/CLK (72)

(105) 2 (101) 3 (102)

(105)가 , L (55) , L TMVREF  
 (71) , L TM/CLK (72)

(71) L TMVREF VREF VREF ,  
 VREF (20), (30) QS (110)  
 (20) (72) L INTVREF TM/CLK /CLK /CLK

(105)가 , H (55) , H TMVREF  
 (72) , H TM/CLK (72)

(71) H TMVREF (120) VREF2  
 QS (110) VREF2 (72) H INTVREF (20), (30)  
 (20) INTVREF TM/CLK INTVREF

(105) 7 8 L  
 TM/CLK , TMVREF , (70)  
 (71) 1 3

(105) 20 21 , L  
 TMVREF 가 , (105) (71) 가 ,

6 , /CLK ( /CLK)  
 1 , VREF ( VREF)  
 1 ( VREF2 INTVREF 2

( EXT VDD)

K, L, 2, TMVREF, TM/CLK, 「 1 」, H, TMVREF, TM/CL  
 「 2 」, (105),  
 6, (105) H, TMVREF, TM/CLK, L, TMVREF, TM/CLK가  
 2, 2, (55) TMVREF, TM/CLK가, (55) (105)가, (105)가, L  
 (105)가, H, TMVREF, TM/CLK가, (55) TMVREF, TM/CLK가, (55)  
 (105)가, A0-A12, 가, WRE, BA0, 1, 11, EXTVDD, VREF, /CS  
 /CLK, (105)가, 가, WRE, 30, VREF, VREF  
 /CLK, 2, (71), (72), 2, 1  
 (71), (72), 2  
 1, (71), (72), 2  
 1, 3, VREF, VREF2  
 6, /CLK, INTVREF, 가, 가,  
 ( 7)  
 31, 7, (106), (100)가, (50)  
 (56), (100), (71, 72), (120)  
 TM/CLK, (56), (72), (50)가, TMVREF, (71),  
 72), (71), 3, (120), 2, ( )  
 (106)가, (70), (72), TMVREF, (71), (56), L, TMDQS, L, L, TM/CLK  
 (70), (72), (71), (56), L, TMDQS, DQS, DQS, VREF  
 QS, (70), L, TMDQS, (71), L, DQS, TMVREF, QS, (110), VREF  
 (72), L, TM/CLK, (20), /CLK, (30), QS, (110), (20)

(106)가 (70) , H (72) . TMVREF (71) (56) , H (71) , H TMDQS TM/CL

) (70) H (71) H TMDQS CLK CLK QS (110) VREF2 (72) H (20) TM/CLK (30) QS (110) (120) INTVREF (71)

8 가 (106) L (106) TMVREF TM/CLK 7 1 (72) 가 (120) (71) 3 2

가 (106) H (106) TMVREF 26 27 (72) 가 (120) (71) 3 2

7 1 , DQS ( DQS) EF) 1 , VREF ( VR /CLK K) 1 , /CLK ( /CL ( CLK) 2 , CLK VREF2 INTVREF 2 ( EXT VDD)

, L TMDQS, TMVREF, TM/CLK 「 1 」 , H TMDQS, TMV REF, TM/CLK 「 2 」 .

, 7 (106) , 3

, (106) H TMDQS, TMVREF, TM/CLK L TMDQS, TMVRE F, TM/CLK가 (56) TMDQS, TMVREF, TM/CLK가 (56) (10) 6)가 , H TMDQS, TMVREF, TM/CLK가 (56)

, (106)가 A0-A12, 11 , VREF /CS 가 WRE EXT VDD

, DQS, (106)가 , 32 가 WRE , DQS, VREF /CLK 3

, (70), (71) (72) 1 2

, (70), (71) (72) 1 2

1 3 .

7 , , , DQS CLK  
 , /CLK , VREF INTVREF INTVREF ,  
 가, , 가 ,  
 . , .  
 1 7 DDR-SDRAM , DDR-SDRAM  
 DQS, VREF /CLK , CLK,  
 VREF2 INTVREF ,  
 / / 1 3  
 , .  
 , .  
 가

(57)

1.

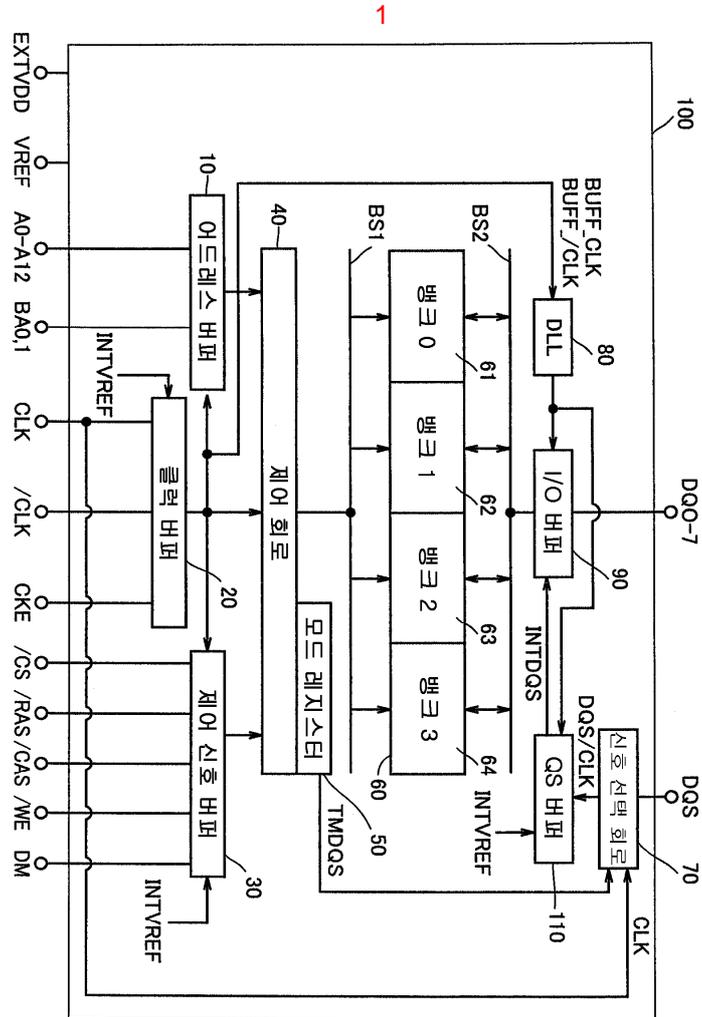
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 , 2 , 1  
 , 1 , 2

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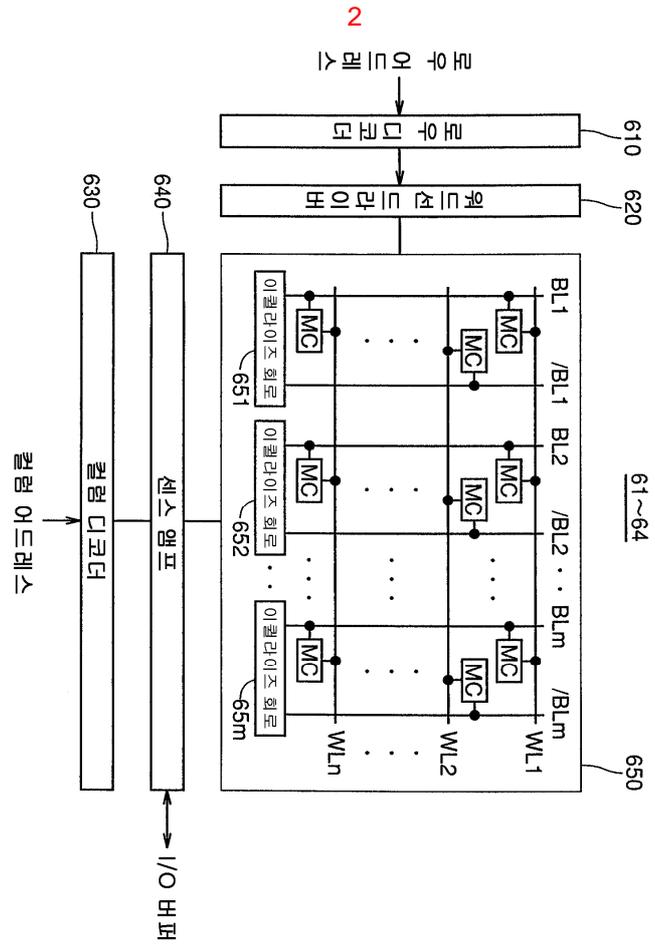
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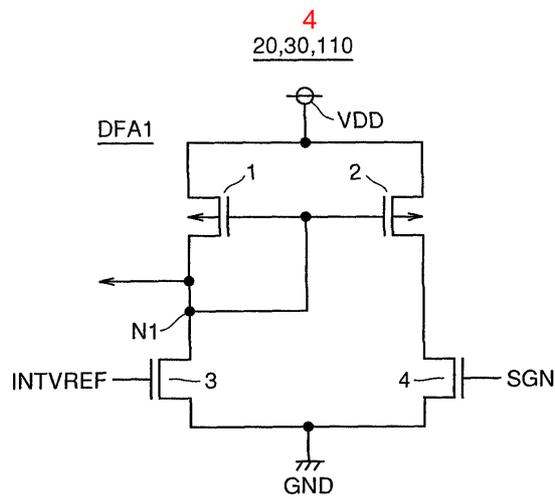
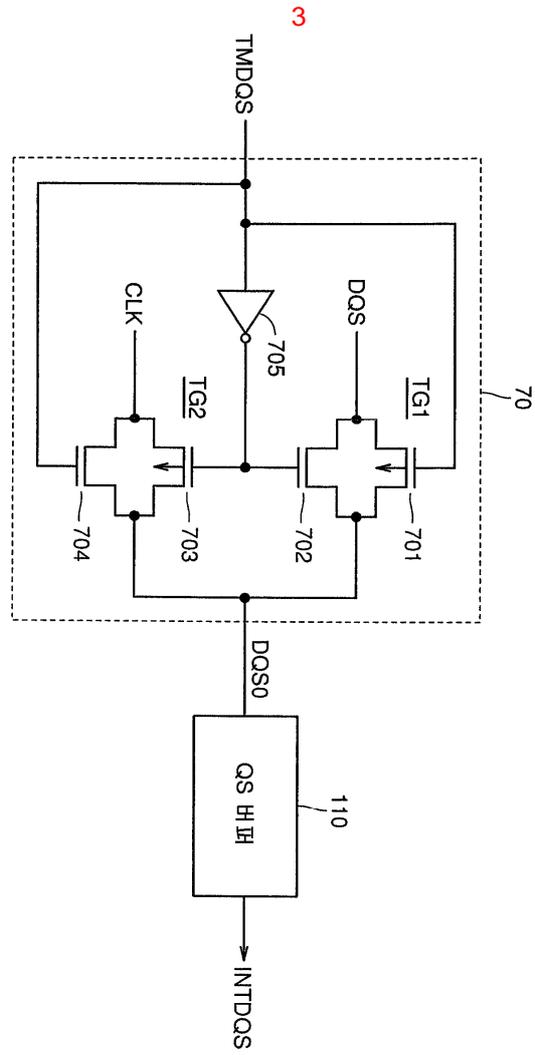
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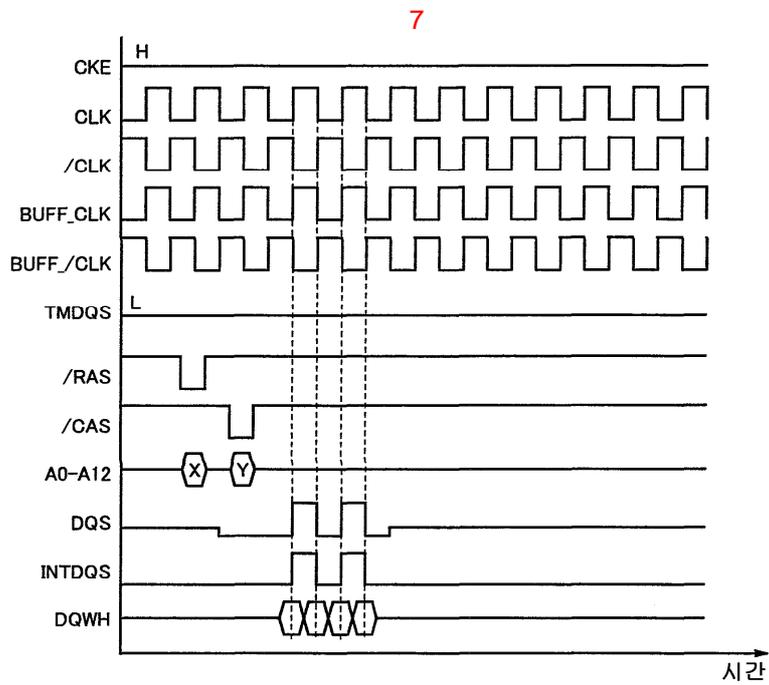
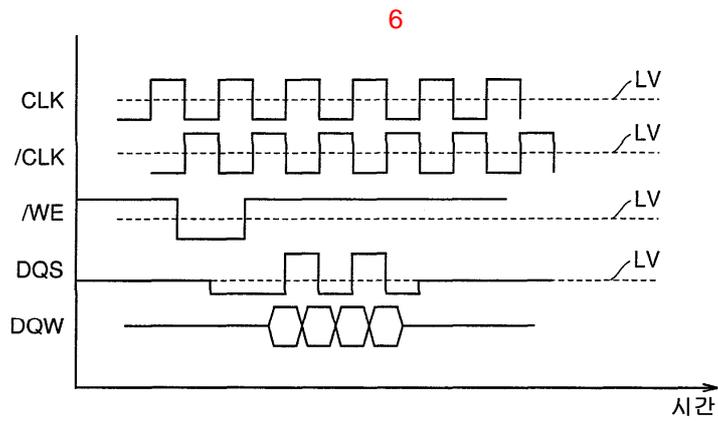
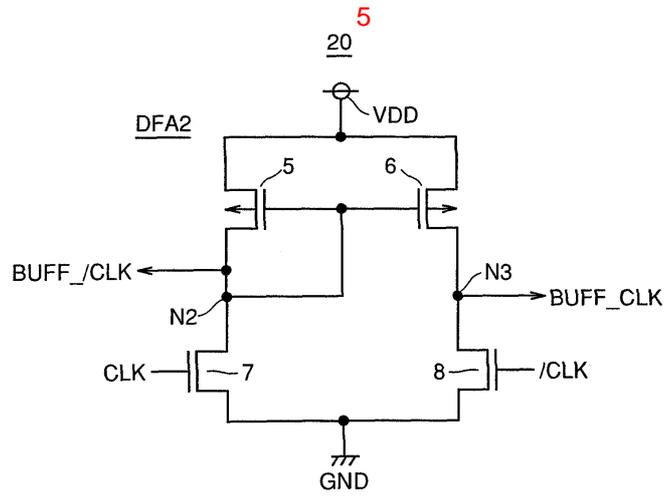
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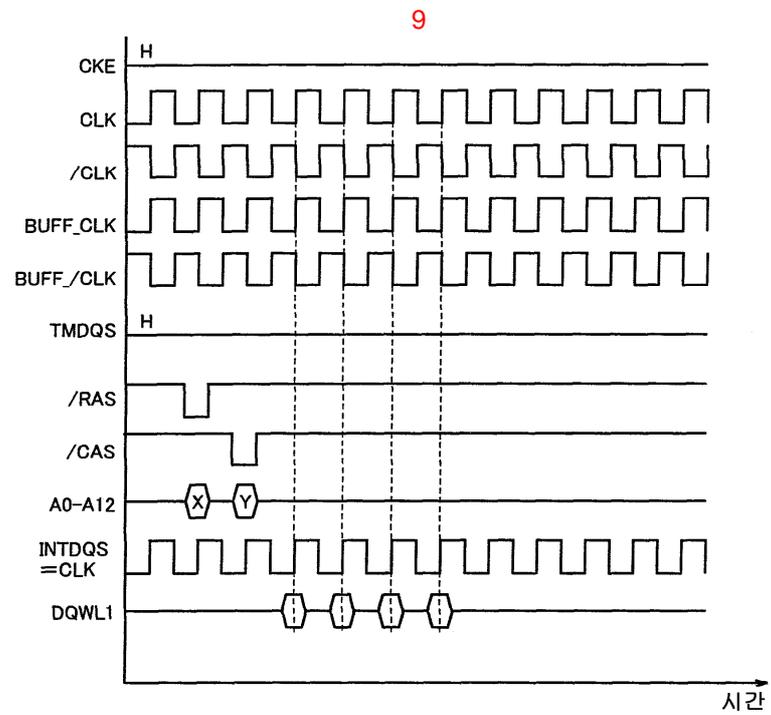
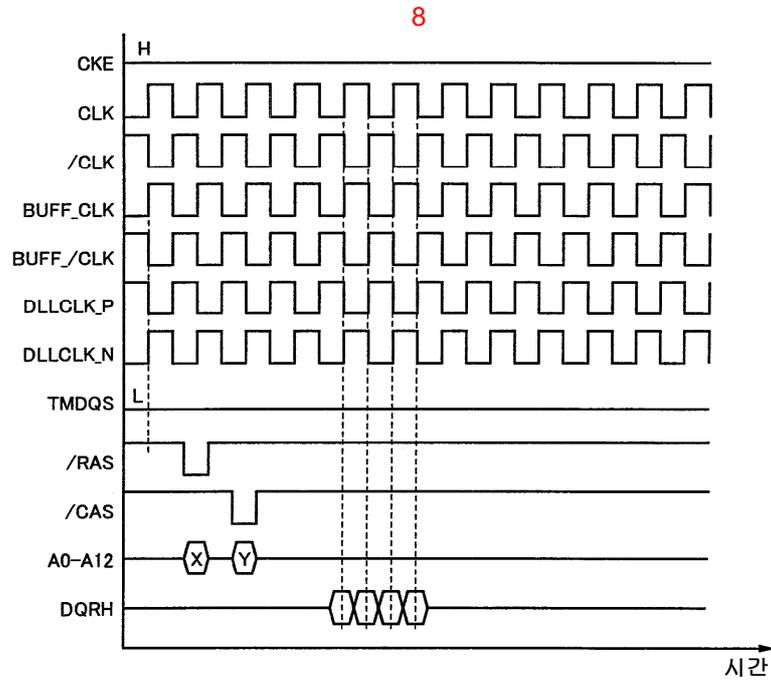


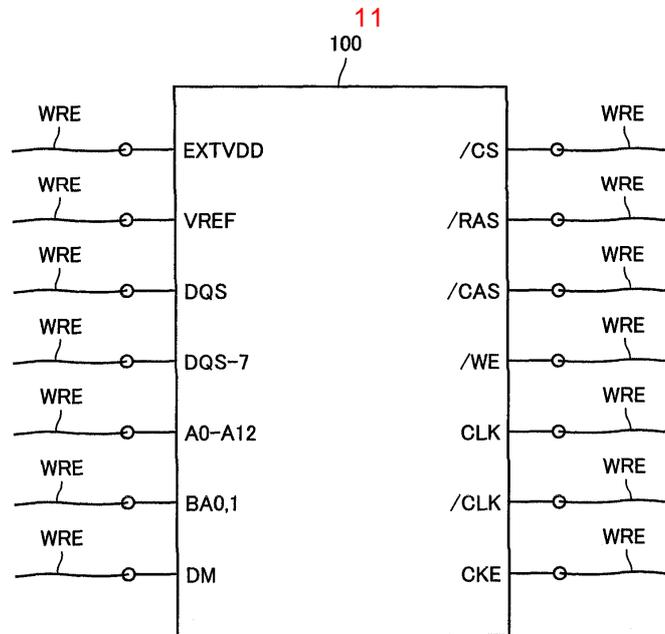
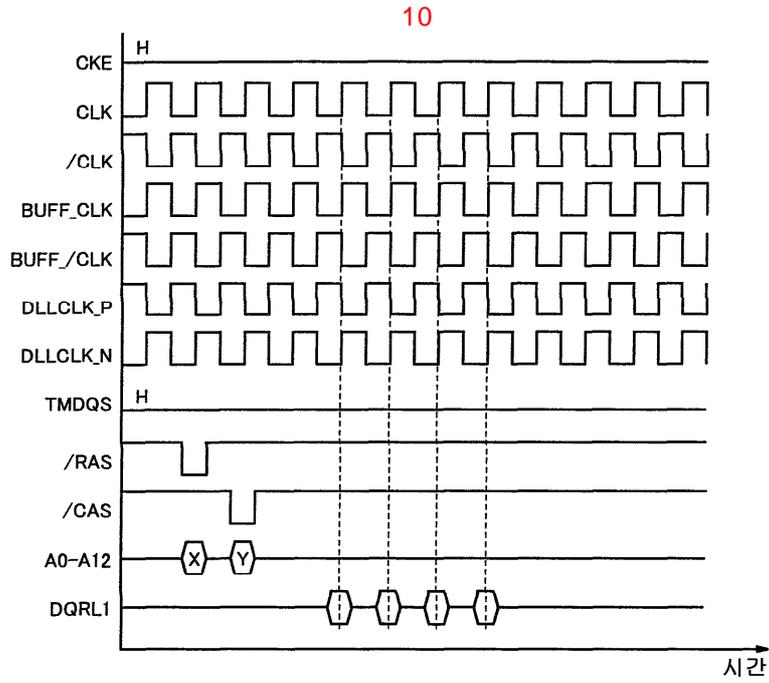
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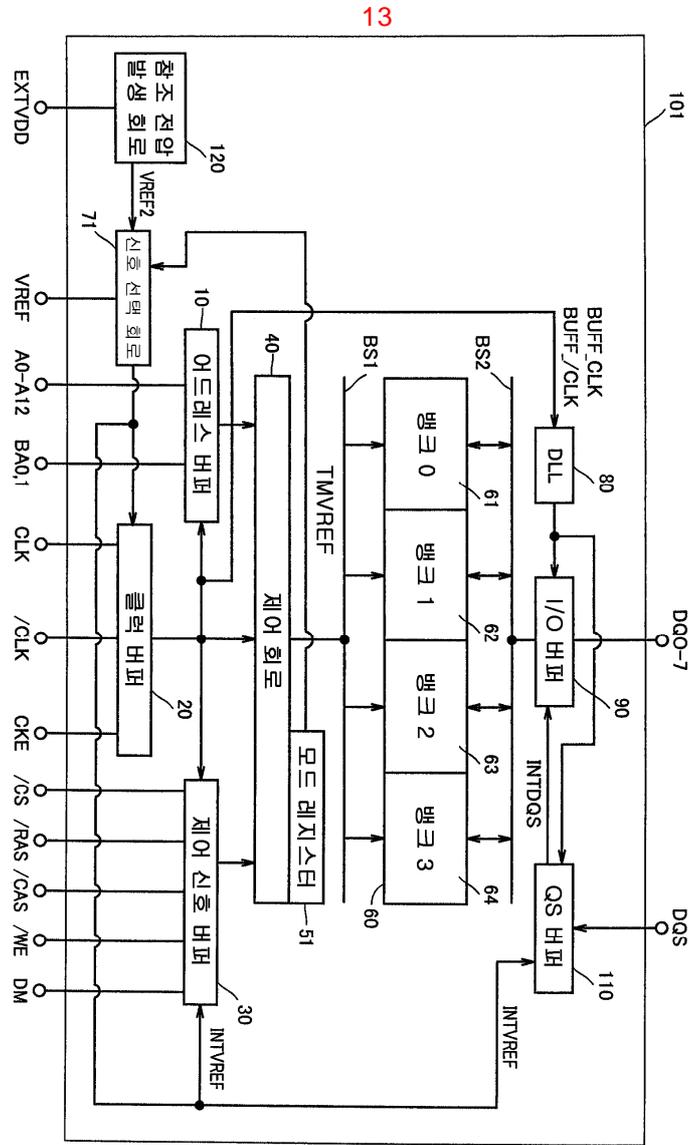
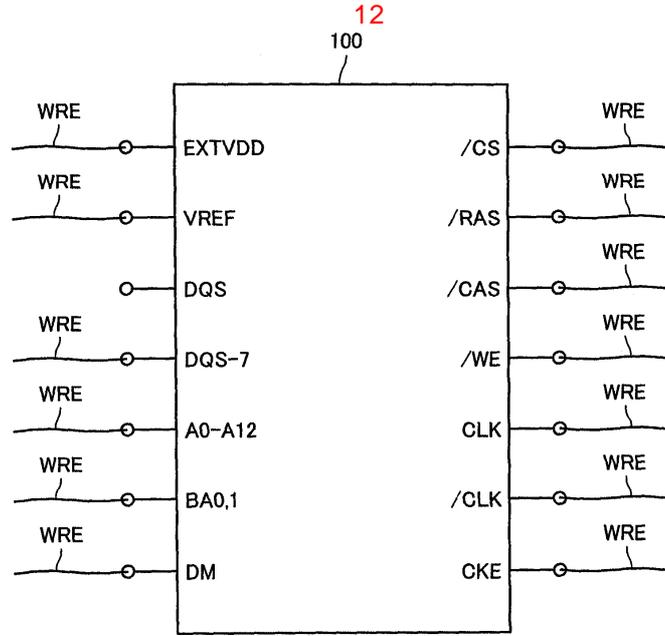






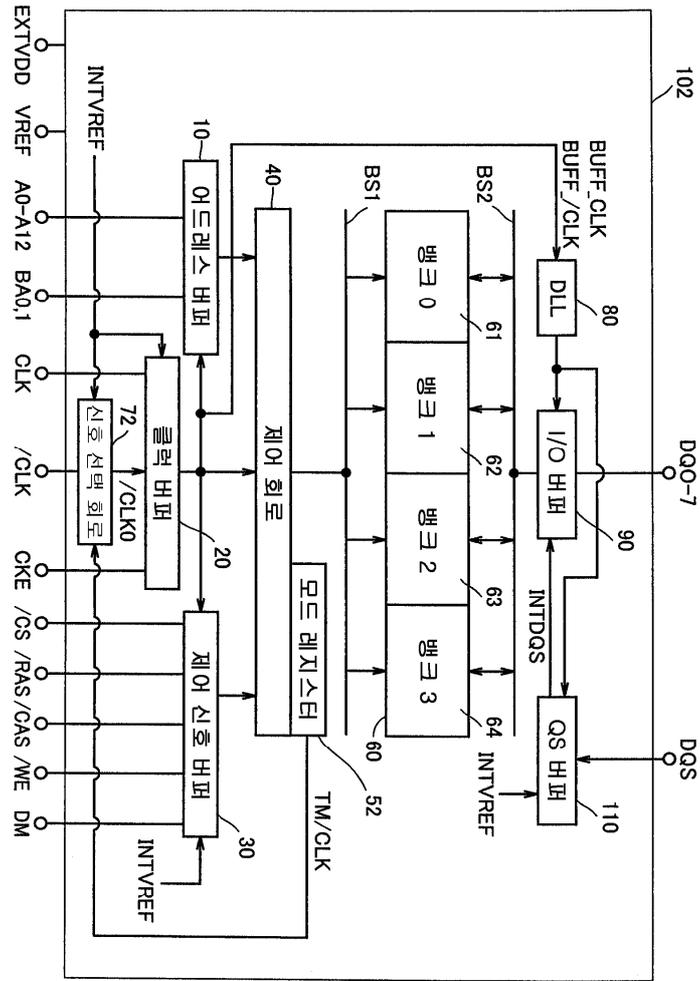




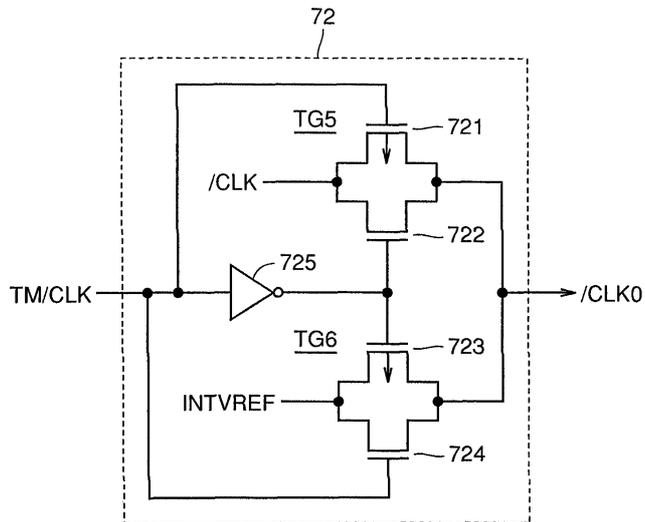


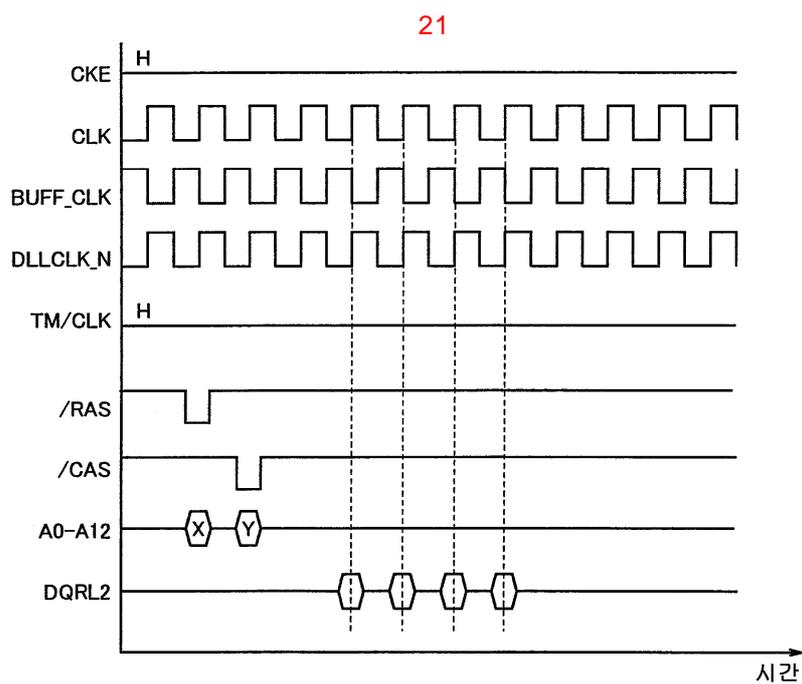
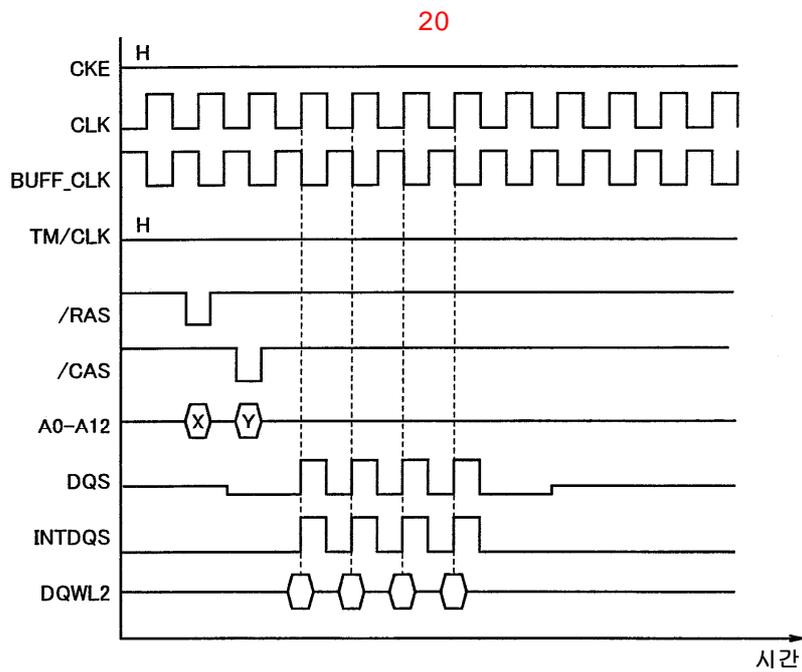
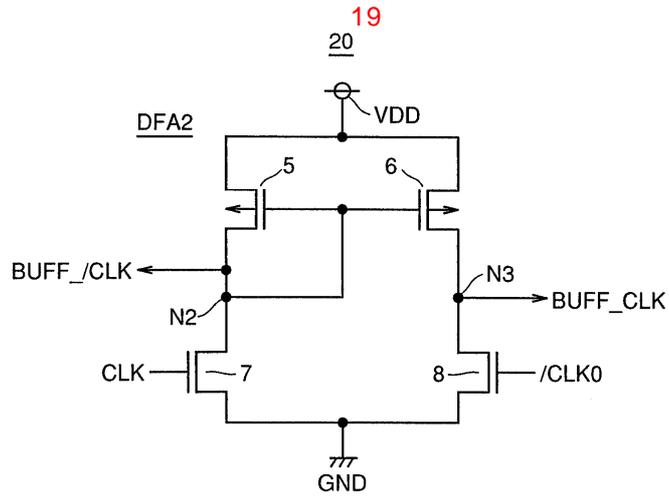


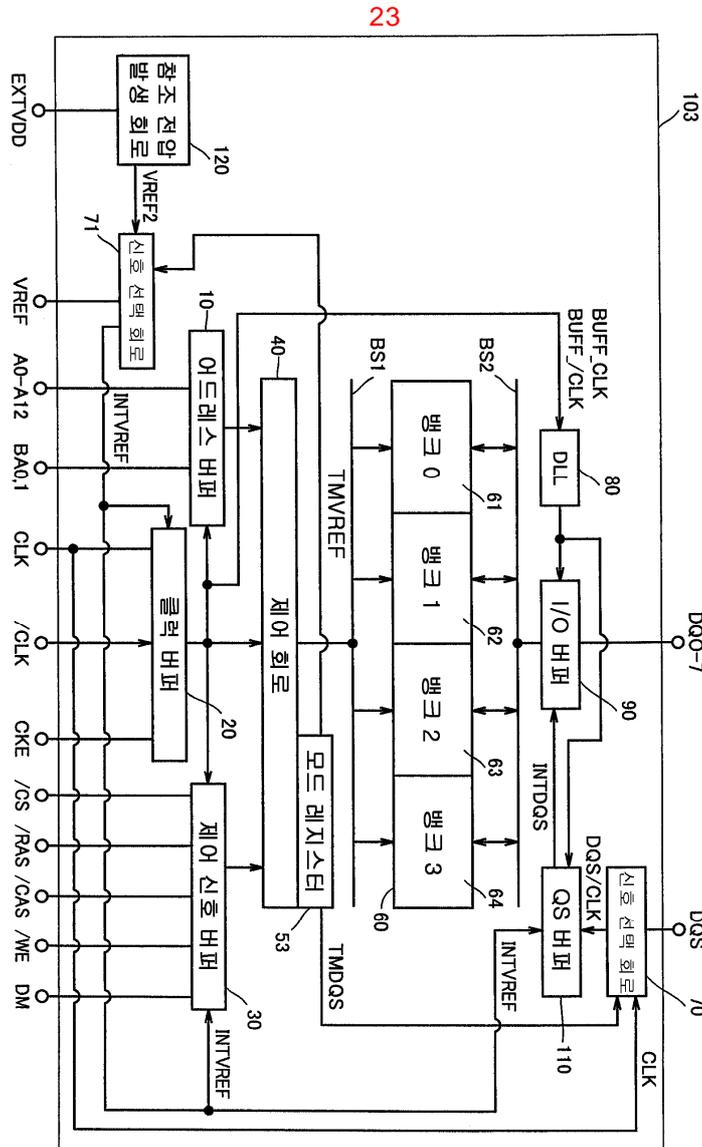
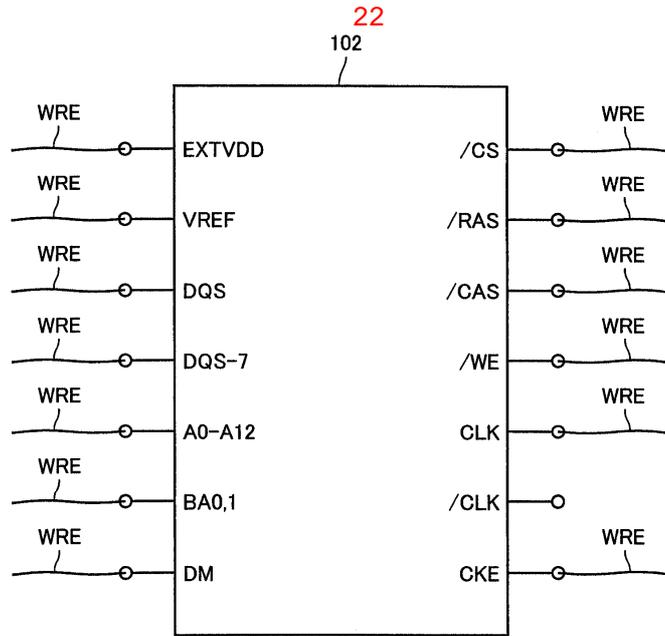
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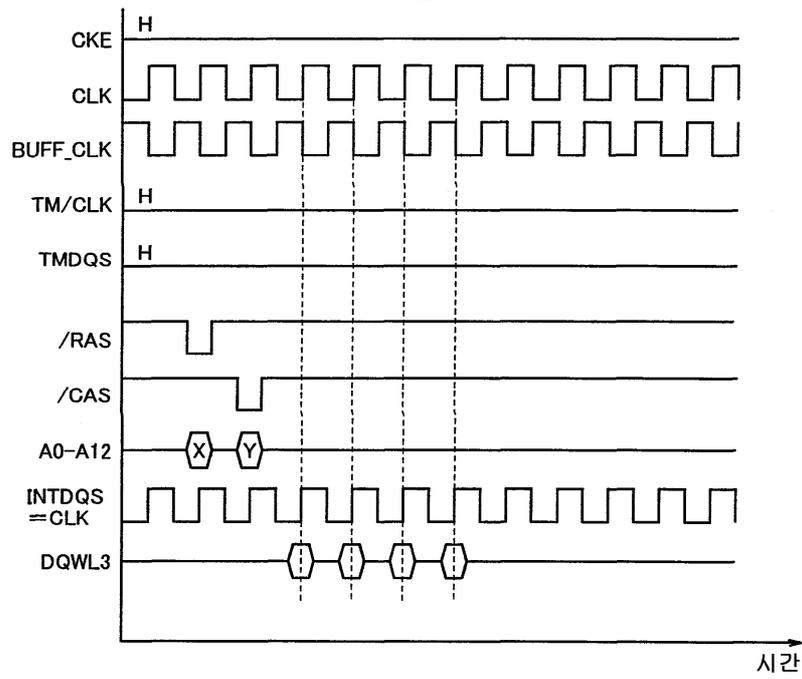




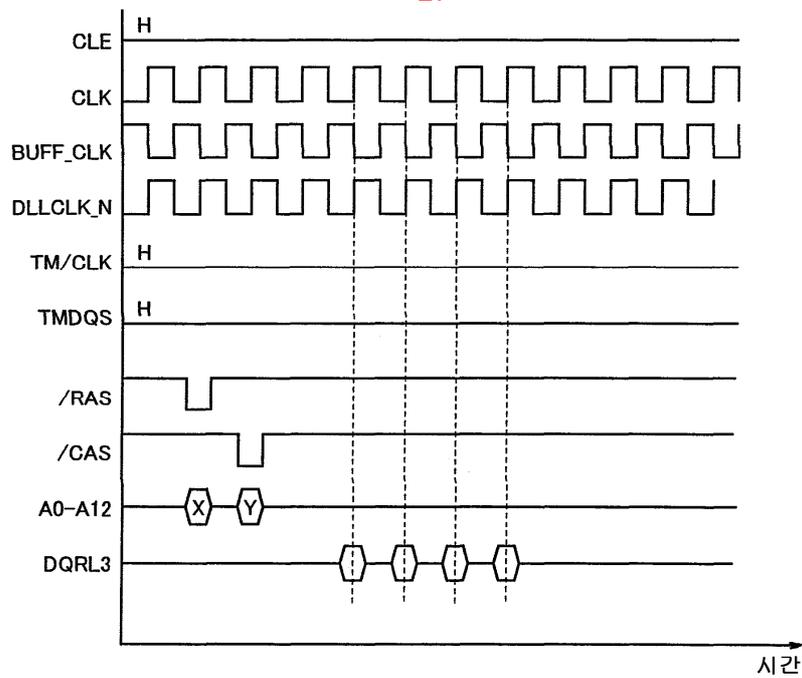


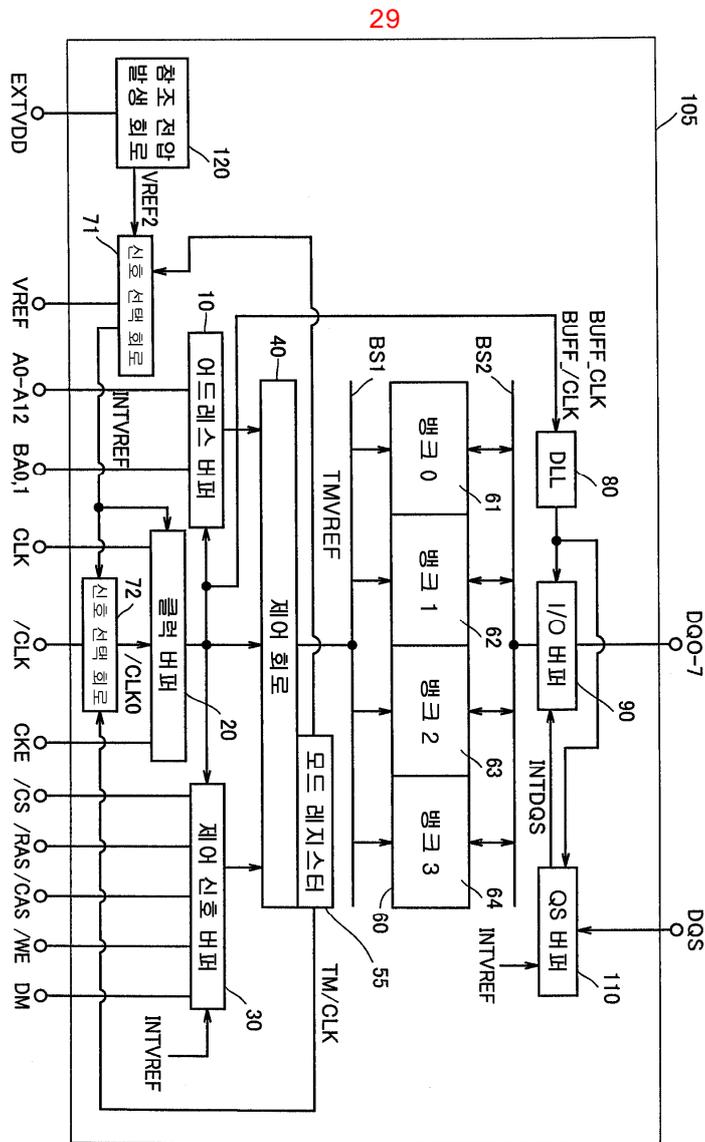
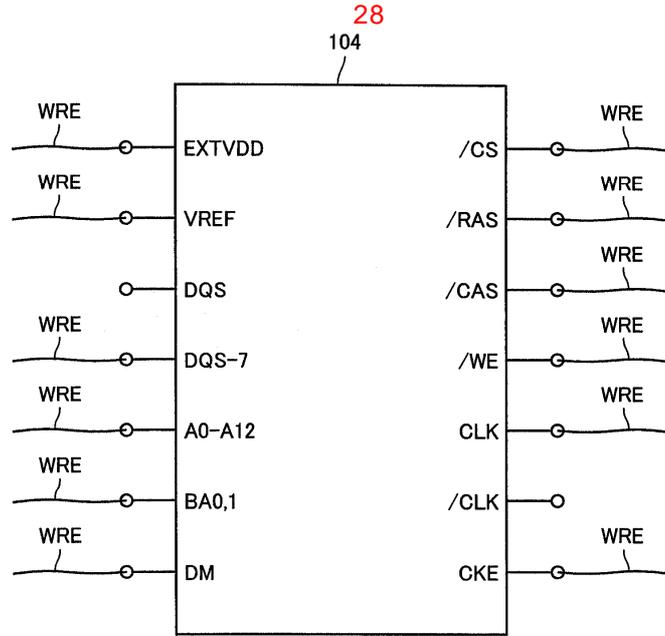


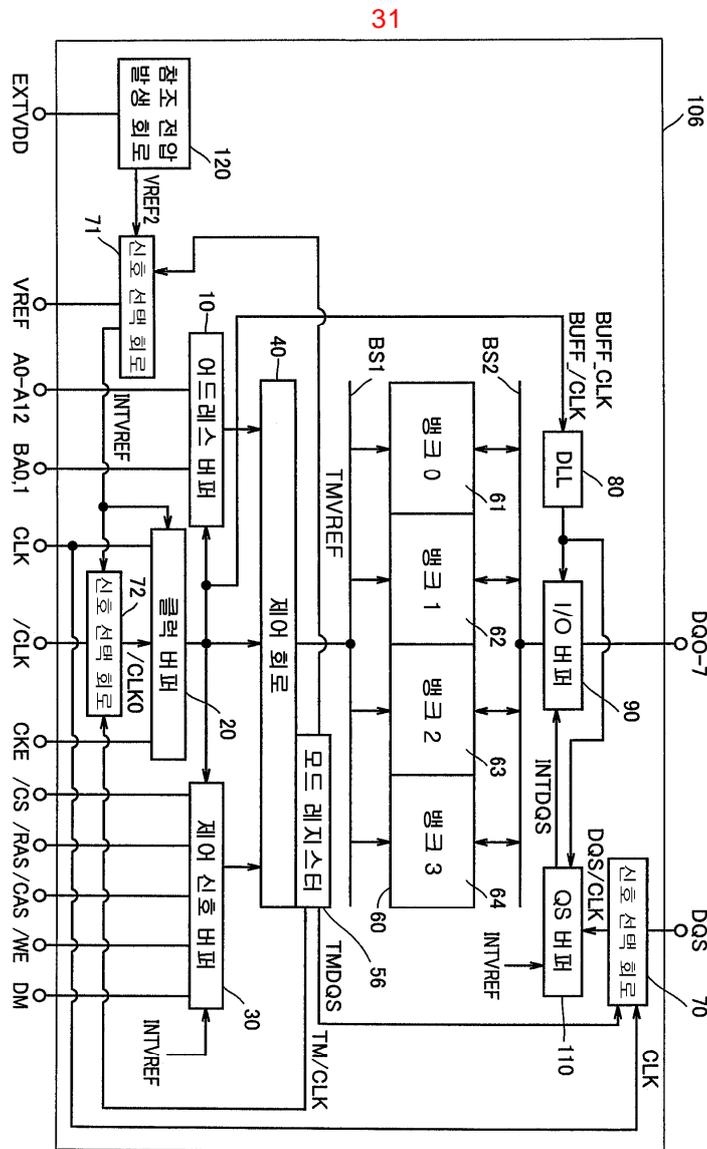
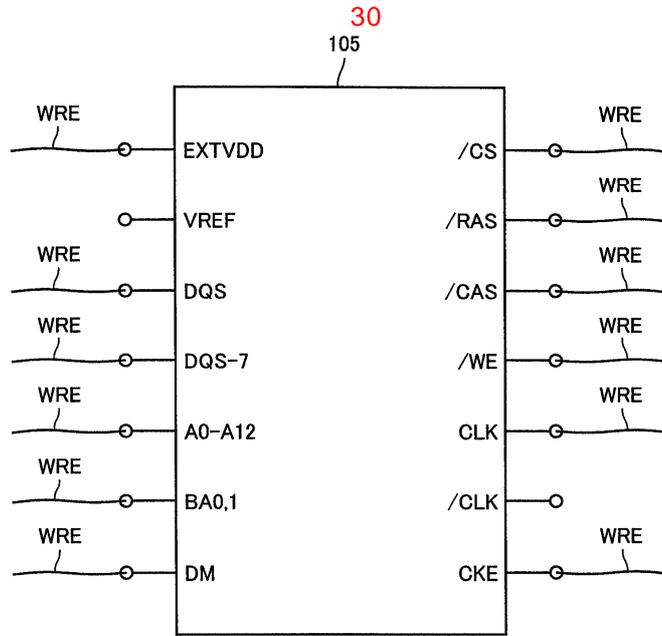
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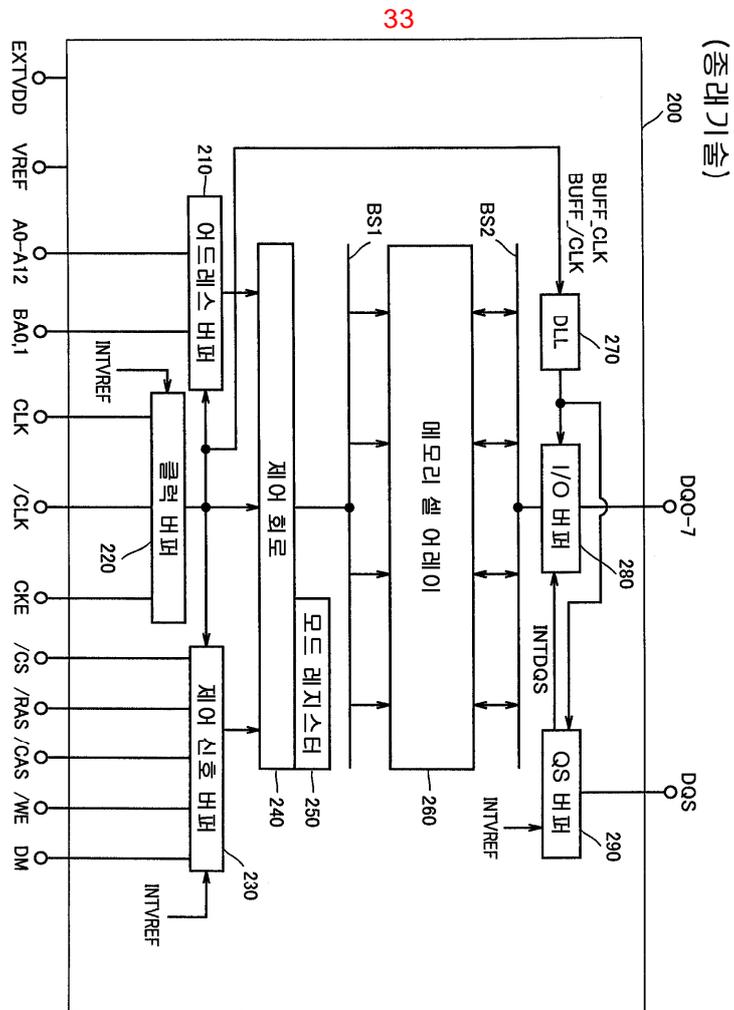
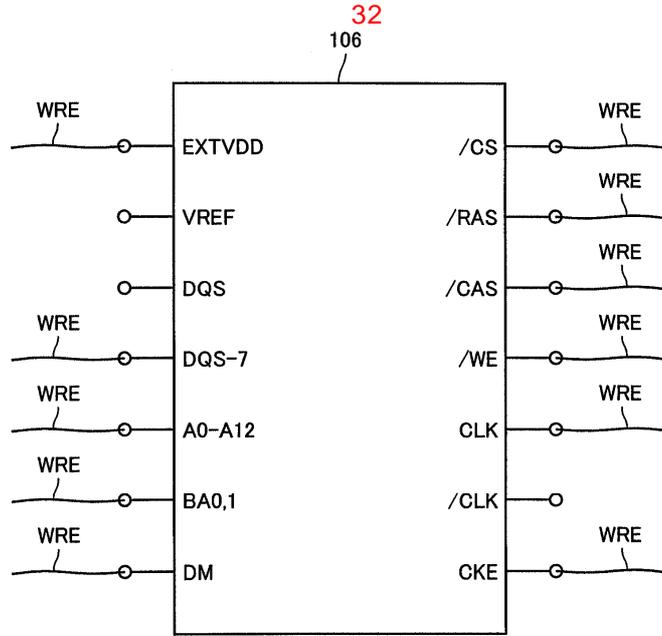


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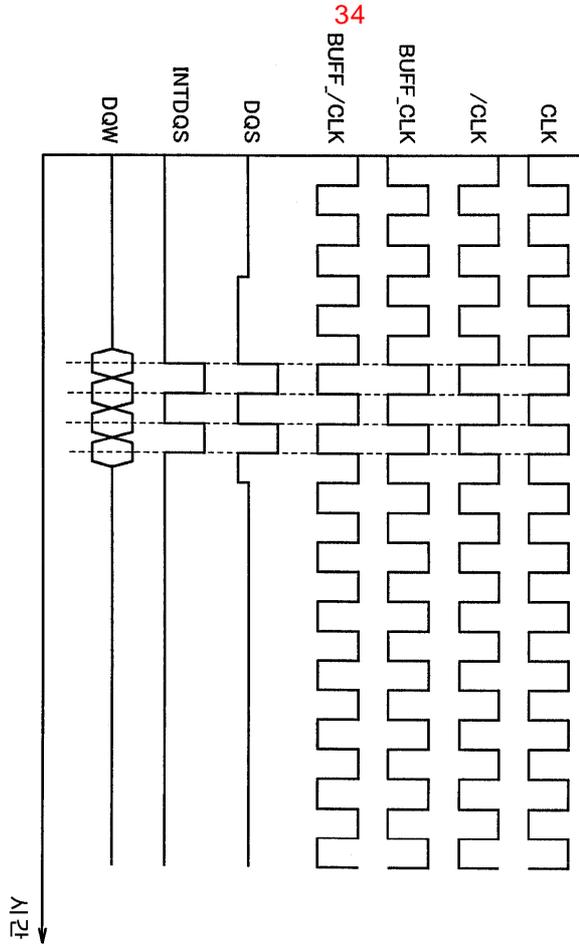








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