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(71) Applicant *(for all designated States except US)*: **CAPRES A/S** [DK/DK]; DTU Bygn. 373, DK-2800 Lyngby (DK).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **PETERSEN, Christian Leth** [CA/CA]; 4861 Ridgelawn Drive, Burnaby, BC V5C3Y1 (CA).

(74) Agent: **MIKKELSEN, Jacob**; BUDDE, SCHOU & OSTENFELDD A/S, Vester Søgade 10, DK-1601 Copenhagen V (DK).

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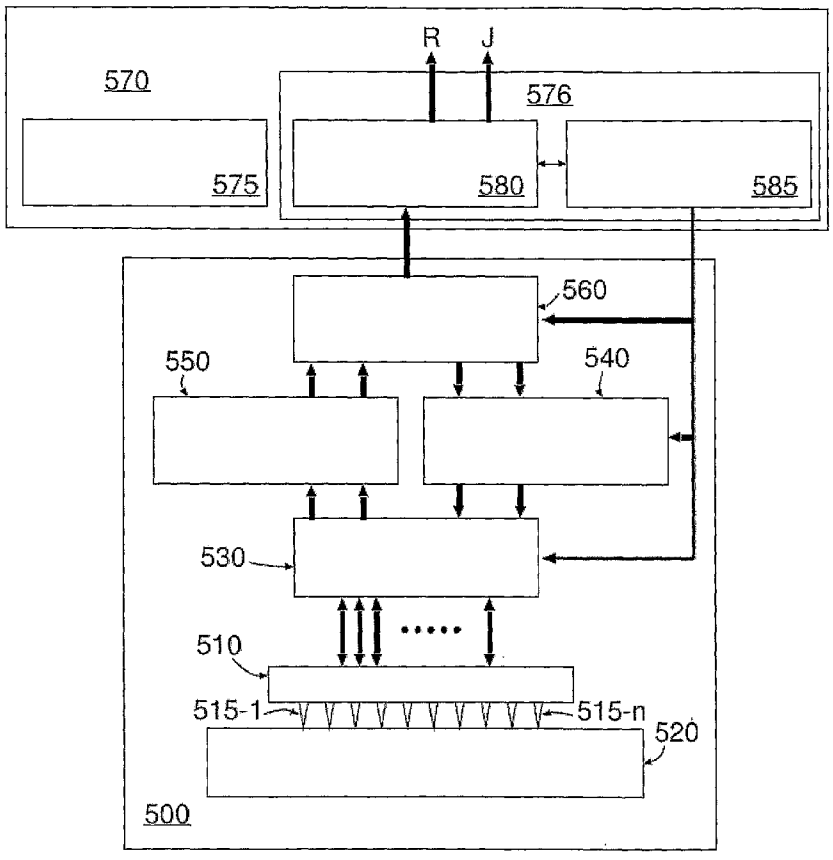
(54) Title: METHOD FOR SHEET RESISTANCE AND LEAKAGE CURRENT DENSITY MEASUREMENTS ON SHALLOW SEMICONDUCTOR IMPLANTS



(57) Abstract: A method for accurately determining the sheet resistance and leakage current density of a shallow implant in a semiconductor surface (520) includes making one or more four-point resistance measurements with an induced current below 100 μA on the semiconductor surface (520) with a plurality of electrode spacing sets, at least one set having an average spacing below 100 μm. The sheet resistance and implant leakage is determined through fitting the measured data to theoretical data to within a predetermined error.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Method for sheet resistance and leakage current density measurements on shallow semiconductor implants

The present invention generally relates to methods for obtaining an electrical property of a test sample. The present invention relates to the measurement of sheet resistance and probe current leakage on shallow implanted regions in a semiconductor surface, and more particularly to the accurate and non-destructive measurement of sheet resistance on ultra shallow junctions.

A method for accurately determining the sheet resistance and leakage current density of a shallow implant in a semiconductor surface includes making one or more four-point resistance measurements with an induced current below 100 μA on the semiconductor surface with a plurality of electrode spacing sets, at least one set having an average spacing below 100 μm. The sheet resistance and implant leakage is determined through fitting the measured data to theoretical data to within a predetermined error.

Alternatively the sheet resistance and implant leakage may be determined through fitting the measured data to theoretical data so as to obtain a minimal error, e.g. minimising the error using numerical or other methods.

Related methods and techniques may be found in patent publications such as US 4,703,252, US 6,842,029, US 7,078,919 and WO 2005/022135. Reference is made to the above US patent publications, all of which are hereby incorporated in the present specification by reference in their entirety for all purposes.

A transistor in a semiconductor circuit consists of two implanted regions, called the source and drain, connected electrically by a channel under a gate electrode. The Source Drain Extension (SDE) is a shallow implant that interfaces the channel under the gate with the deep source and drain. As transistors are made smaller, the SDE must be made extremely shallow to create a high performance device, as SDE depth is a key factor in transistor performance, especially fast switching speeds and low power requirements. At the 100 nm device technology node, depths of 20-30

nm are required, and future technology will need even shallower junctions. The term Ultra-Shallow Junction refers to this extremely thin SDE.

Historically, macroscopic four-point probes have been the accepted way to measure the active dose in implanted surfaces. A macroscopic four-point probe is typically a millimetre-sized device with four spring-loaded transition metal needles in a single row. When the needles press against a surface, a current driven through the outer two pins generates a detectable voltage across the inner pins. This four-point measurement technique has been the standard way to measure sheet resistance on semiconductors for many years. However, macroscopic four-point probes perform poorly on the advanced ultra-thin films of today, as the spring-loaded needles tend to create surface damage and film penetration. The macroscopic probes also require large homogenous areas for measurements without edge artifacts. These limitations are particularly problematic on ultra shallow junctions. Several new technologies have appeared to address the issues with the conventional probes. These include macroscopic probes with low contact force and capacitive non-contact probes. These probing technologies address the destructive nature of conventional probing but fail to address the dimensional aspect of measurements on ultra shallow junctions: Macroscopic probes will consistently report too low USJ sheet resistance values, especially on high resistance implants with high leakage. Larger probe spacing will lead to larger deviations. While soft-touch or non-contact versions of the macroscopic probes solve issues with punch-through and surface damage, they tend to be even larger than the conventional probes, and thus suffer even more from this length scale problem.

Micro-scale measurements are needed to accurately determine the actual sheet resistance over the full range of USJ implant depths. The small dimensions and ultra-low contact force of microscopic probes make it possible to do non-destructive USJ implant characterizations in an area smaller than a typical bonding pad, thus providing for the first time a viable method for USJ sheet resistance characterization on patterned (product) wafers. The present invention addresses the shortcomings of the conventional technologies by using microscopic four-point probes to determine the sheet resistance of ultra-shallow junctions.

The present invention takes advantage of the fact that sheet resistance measurements in a two-layer system will vary with the length scale at which they are performed. At the limit of very small electrode spacing, the measurement will reflect only transport in the top layer, irrespective of the bottom layer condition. At large electrode spacing, the measured resistance will be the parallel combination of the two layers. The length scale separating these two regimes depends on the resistance area product of the interface in between the layers and the sheet resistance of the layers. For Ultra Shallow Junctions this length scale is on the order of 1000 µm or more.

By measuring surface sheet resistance on a semiconductor wafer with a shallow implanted region at a set of different probe spacings it is possible to determine the actual sheet resistance of the shallow implanted region.

A first aspect of the present invention relates to a method for determine an electrical property of a shallow implant which may comprise the steps of:

providing a multi-point probe having four electrical conductive electrodes, two of the electrical conductive electrodes having an electrode spacing of less than 100 µm,

positioning the four electrical contact points of the multi-point probe in contact with an area of the shallow implant,

performing a four point measurement by inducing a current of less than 100 µA in the test sample via the multi-point probe,

extracting the electrical property based on a mathematical relation between the four-point resistance measurement and electrode spacing between the four electrical conductive electrodes.

The multi-point probe may comprise more than the above mentioned four electrodes, e.g. five, six, eight, ten or even more electrodes. The multi-point probe may e.g. be of a kind with a base and a plurality of cantilever arms extending parallel from the body. Such multi-point probes are e.g. described in US 2004/0056674 and/or US 2002/0153909. Reference is made to the two US

publications, both of which are hereby incorporated in the present specification by reference in their entirety for all purposes. See for instance the probe illustrated in figure 6 of US 2004/0056674 and the corresponding description.

The multi-point probe may be received in a system having positioning means for moving the probe relative to the test sample, e.g. using small actuators or the like. In one embodiment, the probe may be held in a movable holder, while the test sample may be held in a stationary holder. The electrical property mentioned in the first aspect of the present invention may be sheet resistance or current leakage density.

The four-point measurement may be performed a number of times in succession. The electrical property may be calculated or extracted based on a plurality of measurements. The spacing between the electrodes may be determined e.g. by visual inspection using an optical microscope or a scanning tunnelling microscope or any other inspection method. Alternative the spacing may be known from production of the probe.

A second aspect of the present invention relates to a method for determining the sheet resistance and current leakage density of a shallow implants in the surface of a semiconductor substrate, the method may comprise:

a. Performing one or more four-point resistance measurements on the semiconductor surface at a plurality of electrode spacing sets, the induced current in the four-point resistance measurements being below 100 μA, and for at least one of the plurality of electrode spacing sets having an average electrode separation below 100 μm.

b. Extracting sheet resistance of the shallow implant in the semiconductor surface based on a mathematical relation between the one or more four-point resistance measurements and the plurality of electrode spacing sets.

It is an advantage of the present invention that the method according to the first and/or second aspect may further comprise using a mathematical relation between the one or more four-point resistance measurements and the plurality electrode

spacing sets to extract the saturation leakage current density of the shallow implant in the semiconductor surface.

The mathematical or physical relation is described in more detail with reference to the drawings.

In a further embodiment of the present invention, at least one of the plurality of electrode spacing sets may have an average spacing above 300 µm. The electrode spacing is preferably known for all sets of the plurality of electrodes. The electrode spacing may be determined by inspection or e.g. known from production of the probe. In a still further embodiment of the present invention, at least one of the plurality of electrode spacing sets may have an average spacing below 20 µm, and the limiting behaviour of theoretical data is used to determine the sheet resistance of the shallow implant, the limiting theoretical behaviour being given by the following formula:

$$R\big|_{s\to 0} = \frac{\log 2}{2\pi} R_t$$

where R is the measured four-point resistance, s is the four-point probe electrode spacing, and R_t is the sheet resistance of the shallow implant.

In a particular embodiment of the present invention, the sheet resistance and saturation leakage current density of the shallow implant may be determined by adjusting the plurality of variables until the theoretical data fit the measured data within a predetermined error. The theoretical and measured data may be fitted by using the following formula:

$$R = \frac{R_t R_b}{R_t + R_b} \frac{1}{2\pi} \left(\frac{2R_t}{R_b} \left(K_0\left(\frac{s}{\lambda}\right) - K_0\left(\frac{2s}{\lambda}\right) \right) + \log 4 \right)$$

where $\lambda = kT/(J_s q(R_t+R_b))$; R_a and R_b being the sheet resistance of the shallow implant and the semiconductor substrate, respectively, K_0 is the modified Bessel function of the second kind of order zero, s is the four-point probe electrode spacing,

k is the Boltzmann constant, T is the temperature, J_s is the saturation leakage current density, and q is the elementary charge.

The adjustment, or fitting, of the variables may e.g. be performed using a least-squares method or any other numerical method or numerical fitting or approximation.

In an even further embodiment of the present invention, the electrical resistivity, ρ, of the semiconductor substrate may be measured experimentally by Secondary Ion Mass Spectrometry, or any other method, and the substrate sheet resistance is determined by the relation $R_b = \rho/t$, t being the thickness of the semiconductor substrate.

The first aspect of the present invention may include any features of the second aspect of the present invention, and the second aspect of the present invention may include any features of the first aspect of the present invention.

A third aspect of the present invention relates to a system for measuring sheet resistance and saturation leakage current on a shallow implant in a semiconductor substrate, the system may comprise:

a probe with a first plurality of electrodes for establishing electrical contact with the surface of the semiconductor substrate;

a voltage controlled current source for inducing a current between a first pair of electrodes;

a high-impedance electrometer for measuring a voltage difference between a second pair of selected electrodes;

a multiplexer comprising a second plurality of electrical connection lines, two of which are connected to the current source and another two of which are connected to the electrometer;

a lock-in amplifier for generating a periodic reference signal controlling the voltage controlled current source, and for detecting the in-phase output of the high-impedance electrometer; and

a computer system with a central processing unit and memory comprising a computer implementation of the method according to the first and/or second aspect of the present invention.

The probe may be of a kind as described in relation to the first and/or second aspect above.

The second pair of selected electrodes used for measuring the voltage difference as recited above is preferably different from the first pair of selected electrodes used for inducing a current.

In a presently preferred embodiment of the present invention, the first pair of electrodes and the second pair of electrodes do not include common electrodes.

In an even further embodiment of the present invention the first plurality may be four. Preferably the first plurality of electrodes is an even number, but may in alternative embodiments be constituted by a probe having an uneven number of electrodes.

The computer implementation of the method may include any of the features of the first and/or second aspect of the present invention.

The measuring method is performed when the electrodes are in electrical contact with the semiconductor substrate. The apparatus may include moving means for positioning the probe into contact with the surface of the semiconductor substrate.

The computer system may further comprise communication means and/or output means for transmitting and/or outputting the result of the measurement. Examples could be a network connection, a printer, a screen, a hard disk, a flash drive or any other means for receiving the result of the measurement.

The system according to the third aspect of the present invention may be adapted to perform any of the steps mentioned in relation to the first and/or second aspect of the present invention.

The present invention is now to be described in greater detail with reference to the figures, in which:

FIG. 1 is a graph of the length scale dependence of measured sheet resistance on a two-layer system;

FIG. 2 is a graph of the expected variation of measured sheet resistance with probe spacing, the shaded area indicating the transitional regime between the single sheet and parallel sheets limits;

FIG. 3 is a method for accurately determining the sheet resistance of an ultra shallow junction by measuring four-point resistance repeatedly at different length scales;

FIG. 4 shows example four-point measurements on an ultra shallow junction. The solid line is the predicted behaviour according to the invention;

FIG. 5 is a block diagram of an apparatus for measuring the sheet resistance and saturation leakage current density according to one embodiment of the present invention.

FIG. 1 illustrates how surface sheet resistance measurements on a two-layer system will vary with the length scale at which they are performed. At the limit of very small electrode spacing, 110, the measurement will reflect only transport in the top layer, irrespective of the bottom layer condition. At large electrode spacing, 130, the measured resistance will be the parallel combination of the two layers. At an intermediate length scale, 120, the measured sheet resistance will lie in between the two limiting cases. The length scale separating these two limiting regimes depends on the resistance area product of the interface in between the layers and the sheet resistance of the layers.

To determine this length scale, we consider a simple sandwich of two thin infinite layers with sheet resistance R_t (top) and R_b (bottom). A four-point resistance

measurement performed on the top surface with a very small probe will only detect the top layer, and the measured four-point resistance is given by

$$R = \frac{\log 2}{2\pi} R_t \qquad (1)$$

On the other hand, if the measurement is done with a very large probe, the result will be a parallel combination of the two layers:

$$R = \frac{\log 2}{2\pi} \frac{R_t R_b}{R_t + R_b} \qquad (2)$$

At a certain transition length scale the measured resistance will lie in between the values of Eq. 1 and Eq. 2. The length scale is determined by the resistance area product, RA, of the interface between the two layers, and is expressed by:

$$\lambda = \sqrt{\frac{RA}{R_t + R_b}} \qquad (3)$$

and the four-point resistance for a probe with pin spacing s is then:

$$R = \frac{R_t R_b}{R_t + R_b} \frac{1}{2\pi} \left(\frac{2R_t}{R_b} \left(K_0\left(\frac{s}{\lambda}\right) - K_0\left(\frac{2s}{\lambda}\right) \right) + \log 4 \right) \qquad (4)$$

where K_0 is the modified Bessel function of the second kind of order zero. This behaviour is shown in FIG. 2 for an example system with $R_t = R_b = 1000\ \Omega/\text{sq}$. It is apparent that a transition occurs at $s = \lambda$, and that there is a transitional region from 0.1λ to 5λ, indicated by a shaded area on the figure, where the measured resistance differs significantly from the limits in Eq. 1 and Eq. 2. In the case of a shallow implanted region in a semiconductor surface such as an ultra shallow junction, the interface is effectively a p-n type barrier with a strongly non-linear behavior. The current density through the barrier can be expressed

$$J = J_s\left(\exp\left(\frac{qV}{kT}\right)-1\right) \qquad (5)$$

where q is the elementary charge, T is the temperature, k is the Boltzmann factor, V is the potential across the interface and J_s the saturation current density. If the potential across the interface is much smaller than the thermal voltage at T = 300 K, kT/q = 25,9 mV, expression Eq. 5 reduces to

$$J = \frac{VJ_s q}{kT} \qquad (6)$$

This is a valid approximation on most implants when the four-point measurements are performed at a current setpoint of a few µA, leading to a potential drop on the order of a few mV between the inner electrodes (typical USJ sheet resistance lies in a narrow range of 500-2000 Ω/sq). The potential across the barrier will only be a fraction of this inner electrode potential. In this regime, the resistance-area product RA for the barrier is

$$RA = \frac{kT}{J_s q} \qquad (7)$$

Let us consider a very large leakage current of 10^{-3} A/cm^2, a high USJ sheet resistance R_t = 2000 Ω/sq, and a highly resistive substrate R_b = 500 Ω/sq. Eq. 3 then gives us a length scale of λ 1020 µm. By the argument above, only four-point probe measurements performed on a length scale below 100 µm will therefore always generate accurate representations of USJ sheet resistance.

The above argument considers a system of two thin layers. This is a valid assumption on typical USJ implants, as they are implanted in a thin transistor halo region of significantly higher conductivity than the surrounding substrate. A system with a semi-infinite bottom layer has also been analyzed, and the conclusions drawn above hold true in this case as well.

In a preferred embodiment of the present invention, microscopic measurements are made at different length scale as illustrated on FIG. 3. A series of four-point measurements are performed on the sample surface with different electrode spacing, 310, at least one electrode spacing being below 100 µm. Next, the length scale dependence of the measurements is determined, 320. Finally, the ultra shallow junction sheet resistance and current leakage density is determined by fitting the measured data to the theoretical model in Eq. 4.

In a second preferred embodiment, a single four-point measurement is performed on the semiconductor surface with an electrode spacing less than 20 µm. The sheet resistance of the ultra shallow junction is then determined by the limiting behavior of Eq. 4 for small electrode spacing s:

$$R\big|_{s\to 0} = \frac{\log 2}{2\pi} R_t \qquad (8)$$

FIG. 4 shows measurements according to the invention on two semiconductor shallow implants with a depth of 50 nm (square bullets) and 70 nm (circle bullets) respectively.

The microscopic four-point probe measurements were performed using micro-fabricated probes at probe spacing ranging from 3 to 60 µm. The macroscopic measurement was performed with a conventional tungsten needle probe. The current setpoint was 50 µA. For both implants, the measured sheet resistance is essentially constant over the microscopic range, while the macroscopic measurement is significantly lower. This is expected from FIG. 1.

The bottom layer sheet resistance was R_b = 15 Ω/sq. A fit of the data to Eq. 4 then leads to R_t = 3006 Ω/sq and λ = 1.92 mm for the 50 nm thick implant and R_t = 1847 Ω/sq and λ = 5.66 mm for the 70 nm implant. The fitted theoretical predictions are shown as solid lines in FIG. 4.

The saturation current density can be determined from the data in FIG. 4 by the relation:

$$J_s = \frac{kT}{q\lambda^2(R_t + R_b)} \qquad (9)$$

This gives $J_s = 2.31 \times 10^{-4}$ A/cm^2 for the 50 nm implant and $J_s = 4.35 \times 10^{-5}$ A/cm^2 for the 70 nm implant.

FIG. 5 is a block diagram of an apparatus for measuring the sheet resistance and saturation leakage current density according to one embodiment of the present invention. The apparatus consists of a shallow junction test device 500 connected to a computer system 570.

The shallow junction test device 500 consists of a probe 510 with multiple electrodes, 515-1 to 515-n, n being the total number of electrodes, in contact with the surface of a semiconductor substrate 520 with a shallow implant.

In a preferred embodiment of the invention the probe electrodes are electrically conducting micro-fabricated cantilevers, and the spacing between adjacent electrodes is between 1 μm and 300 μm. In the preferred embodiment, at least one of the electrode spacing sets has an average electrode separation below 100 μm.

In another preferred embodiment, at least one of the electrode spacing sets has an average electrode separation above 300 μm.

The probe connects to a voltage controlled current source 540 for inducing a current between a pair of probe electrodes and a high-impedance electrometer 550 for measuring a voltage difference between another pair of probe electrodes. The probe electrodes connected to the electrometer and current source are selectable through an n-to-4 multiplexer 530 connected to each of the probe electrodes.

The current source is driven by an oscillatory reference signal from a lock-in amplifier 560, and the electrometer output connects to the lock-in amplifier input for detecting the in-phase component of the measured voltage with respect to the driven current.

The computer system 570 consists of a central processing unit 575 operating on a memory unit 576. The memory unit contains program instructions for a controller module 585 enabling making one or more four-point resistance measurements with a current set-point below 100 μA at a predetermined multiple of electrode spacing sets. The memory unit also contains program instructions for a data analysis module 580 that determines the sheet resistance of shallow implant by fitting the measured data to Eq. 4 to within a predetermined error, and determines the saturation leakage current density from evaluating Eq. 9.

The computer system 570 may of course comprise other elements, such as electrical power supply, IO devices etc.

Fig. 1 schematically illustrates the sheet resistance along the y-axis and probing length scale along the x-axis.

Fig. 2 schematically illustrates the sheet resistance [Ω/sq] along the y-axis and normalised probe spacing s/λ along the x-axis.

Fig. 3 schematically illustrates three steps in a method for accurately determining the sheet resistance of an ultra shallow junction. The method comprises the steps 310 Measure four-point resistance for a variety of electrode spacing sets. 320 Determine sheet resistance spacing dependence from measured data. 330 Determine shallow implant sheet resistance and leakage through curve fitting.

Fig. 4 schematically illustrates the sheet resistance [Ω/sq] along the y-axis and probe length scale [μm] along the x-axis.

Fig. 5 schematically illustrates a block diagram of an apparatus for measuring the sheet resistance and saturation leakage current density. The apparatus comprises:

500:	Shallow junction test device
510:	Probe
515-1 - 515-n:	Probe arms.
520:	Semiconductor substrate with shallow implant
530:	Multiplexer
540:	Voltage controlled current source
550	Electrometer
560:	Lock-in amplifier.
570:	Computer system
575	Processor
576	Memory
580	Data analysis module
585	Controller module

The present invention may be characterized by the following points:

1. A method for determining the sheet resistance and current leakage density of a shallow implants in the surface of a semiconductor substrate, the method comprising:
a. Making one or more four-point resistance measurements on said semiconductor surface at a plurality of electrode spacing sets, the induced current in said four-point resistance measurements being below 100 μA, and for at least one of said plurality of electrode spacing sets having an average electrode separation below 100 μm.
b. Using a known relation between said one or more four-point resistance measurements and said plurality of electrode spacing sets to extract the sheet resistance of said shallow implant in said semiconductor surface.

2. A method according to point 1, further comprising using a known relation between said one or more four-point resistance measurements and said plurality electrode spacing sets to extract the saturation leakage current density of said shallow implant in said semiconductor surface.

3. A method according to point 2, wherein at least one of said plurality of electrode spacing sets has an average spacing above 300 μm.

4. A method according to point 1, wherein at least one of said plurality of electrode spacing sets has an average spacing below 20 μm, and the limiting behavior of theoretical data is used to determine the sheet resistance of said shallow implant, the limiting theoretical behaviour being given by the following formula:

$$R\big|_{s\to 0} = \frac{\log 2}{2\pi} R_t$$

where R is the measured four-point resistance, s is the four-point probe electrode spacing, and R_t is the sheet resistance of said shallow implant.

5. A method according to point 3, wherein the sheet resistance and saturation leakage current density of said shallow implant is determined by adjusting the plurality of variables until the theoretical data fit the measured data within a predetermined error, the theoretical and measured data being fit by using the following formula:

$$R = \frac{R_t R_b}{R_t + R_b} \frac{1}{2\pi} \left(\frac{2R_t}{R_b} \left(K_0\left(\frac{s}{\lambda}\right) - K_0\left(\frac{2s}{\lambda}\right) \right) + \log 4 \right)$$

where $\lambda = kT/(J_s q(R_t+R_b))$; R_a and R_b being the sheet resistance of said shallow implant and said semiconductor substrate, respectively, K_0 is the modified Bessel function of the second kind of order zero, s is the four-point probe electrode spacing, k is the Boltzmann constant, T is the temperature, J_s is the saturation leakage current density, and q is the elementary charge.

6. A method according to point 5, wherein the electrical resistivity, ρ, of said semiconductor substrate is measured experimentally by Secondary Ion Mass Spectrometry or another method known to those skilled in the art, and the substrate sheet resistance is determined by the relation $R_b = \rho/t$, t being the thickness of said semiconductor substrate.

7. A system for measuring the sheet resistance and saturation leakage current on a shallow implant in a semiconductor substrate, the system comprising:

a. A probe with a plurality of electrodes in contact with the surface of said semiconductor substrate;

b. A voltage controlled current source for inducing a current between a pair of selected electrodes;

c. A high-impedance electrometer for measuring a voltage difference between a pair of selected electrodes;

d. A multiplexer comprising a plurality of electrical connection lines, two of which are connected to said current source and another two of which are connected to said electrometer;

e. A lock-in amplifier for generating a periodic reference signal controlling said voltage controlled current source, and for detecting the in-phase output of said high-impedance electrometer;

f. A computer system with a central processing unit and memory containing program instructions for: Making one or more four-point resistance measurements on said semiconductor surface at a plurality of electrode spacing sets, the induced current in said four-point resistance measurements being below 100 μA, and for at least one of said plurality of electrode spacing sets having and average electrode separation below 100 μm; Using a known relation between said one or more four-point resistance measurements and said plurality of electrode spacing sets to extract the sheet resistance of said shallow implant in said semiconductor surface; Using a known relation between said one or more four-point resistance measurements and said plurality of electrode spacing sets to extract the saturation leakage current density of said shallow implant in said semiconductor surface.

Claims:

1. A method for determine an electrical property of a shallow implant comprising the steps of:

providing a multi-point probe having four electrical conductive electrodes, two of said electrical conductive electrodes having an electrode spacing of less than 100 µm,

positioning said four electrical contact points of said multi-point probe in contact with an area of said shallow implant,

performing a four point measurement by inducing a current of less than 100 µA in said test sample via said multi-point probe,

extracting said electrical property based on a mathematical relation between said four-point resistance measurement and electrode spacing between said four electrical conductive electrodes.

2. A method for determining the sheet resistance and current leakage density of a shallow implants in the surface of a semiconductor substrate, the method comprising:

a. Performing one or more four-point resistance measurements on said semiconductor surface at a plurality of electrode spacing sets, the induced current in said four-point resistance measurements being below 100 µA, and for at least one of said plurality of electrode spacing sets having an average electrode separation below 100 µm.

b. Extracting sheet resistance of said shallow implant in said semiconductor surface based on a mathematical relation between said one or more four-point resistance measurements and said plurality of electrode spacing sets.

3 The method according to claim 1 or 2, further comprising using a mathematical relation between said one or more four-point resistance measurements and said plurality electrode spacing sets to extract the saturation leakage current density of said shallow implant in said semiconductor surface.

4. The method according to any of the claims 1-3, wherein at least one of said plurality of electrode spacing sets has a spacing of above 300 μm.

5. The method according to any of the claims 1-4, wherein at least one of said plurality of electrode spacing sets has an average spacing below 20 μm, and the limiting behaviour of theoretical data is used to determine the sheet resistance of said shallow implant, the limiting theoretical behaviour being given by the following formula:

$$R|_{s\to 0} = \frac{\log 2}{2\pi} R_t$$

where R is the measured four-point resistance, s is the four-point probe electrode spacing, and R_t is the sheet resistance of said shallow implant.

6. The method according to any of the claims 1-5, wherein the sheet resistance and saturation leakage current density of said shallow implant is determined by adjusting the plurality of variables until the theoretical data fit the measured data within a predetermined error, the theoretical and measured data being fit by using the following formula:

$$R = \frac{R_t R_b}{R_t + R_b} \frac{1}{2\pi} \left(\frac{2R_t}{R_b} \left(K_0\left(\frac{s}{\lambda}\right) - K_0\left(\frac{2s}{\lambda}\right) \right) + \log 4 \right)$$

where $\lambda = kT/(J_s q(R_t+R_b))$; R_a and R_b being the sheet resistance of said shallow implant and said semiconductor substrate, respectively, K_0 is the modified Bessel function of the second kind of order zero, s is the four-point probe electrode spacing, k is the Boltzmann constant, T is the temperature, J_s is the saturation leakage current density, and q is the elementary charge.

7. The method according to any of the claims 1-6, wherein the electrical resistivity, ρ, of said semiconductor substrate is measured experimentally by Secondary Ion Mass Spectrometry or any other method and the substrate sheet resistance is determined by the relation $R_b = \rho/t$, t being the thickness of said semiconductor substrate.

8. A system for measuring the sheet resistance and saturation leakage current on a shallow implant in a semiconductor substrate, said system comprising:

a probe with a first plurality of electrodes for establishing electrical with the surface of said semiconductor substrate;

a voltage controlled current source for inducing a current between a first pair of electrodes;

a high-impedance electrometer for measuring a voltage difference between a second pair of selected electrodes;

a multiplexer comprising a second plurality of electrical connection lines, two of which are connected to said current source and another two of which are connected to said electrometer;

a lock-in amplifier for generating a periodic reference signal controlling said voltage controlled current source, and for detecting the in-phase output of said high-impedance electrometer; and

a computer system with a central processing unit and memory comprising a computer implementation of the method according to any of the claims 1-7.

9. The system according to claim 8, wherein said first pair of electrodes and said second pair of electrodes does not include common electrodes.

10. The system according to any of the claims 8 or 9, wherein said first plurality is four.

11. The system according to any of the claims 8-10, wherein said system is adapted to perform any of the steps of the method according to any of the claims 1-7.

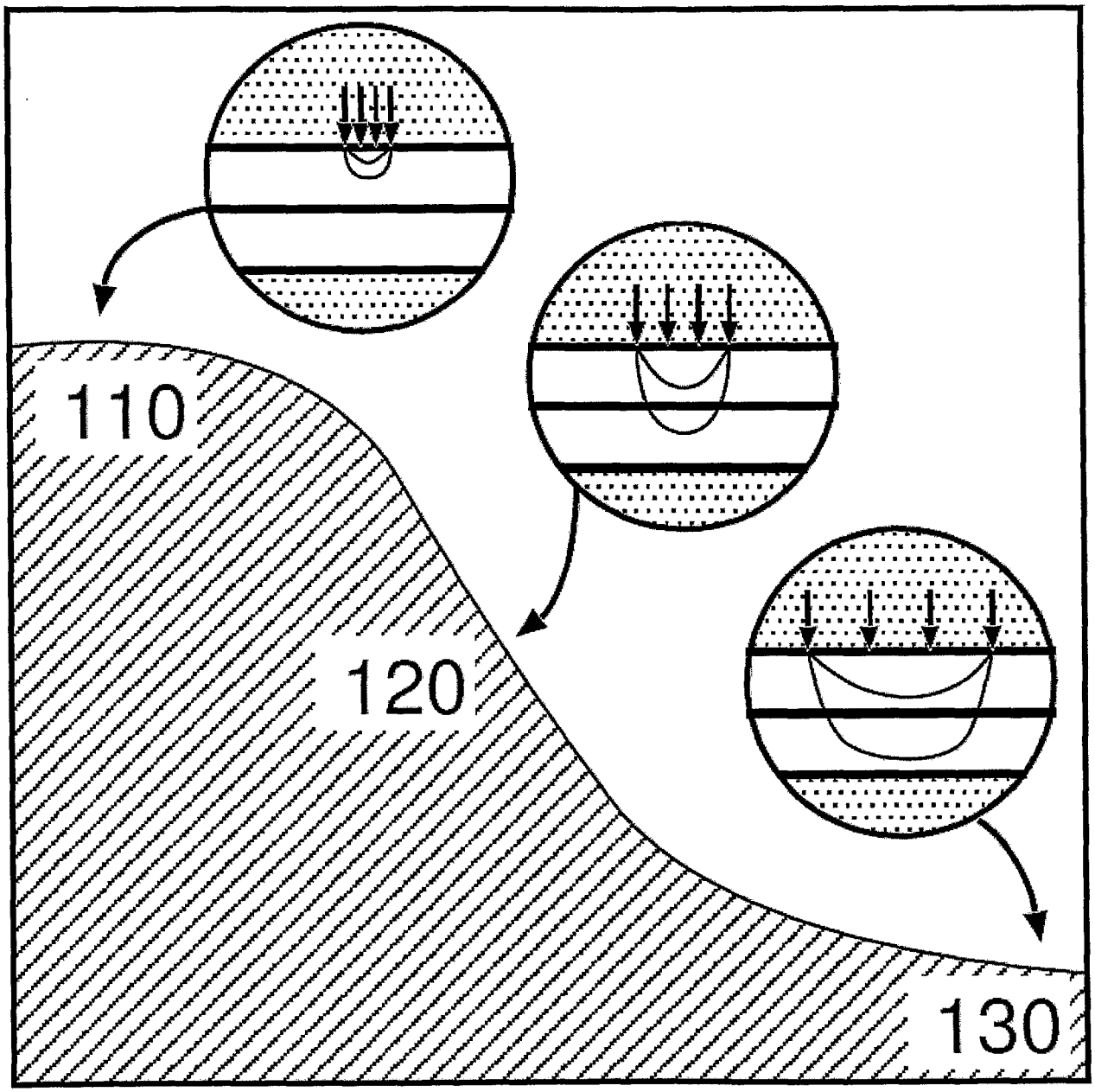

Fig. 1

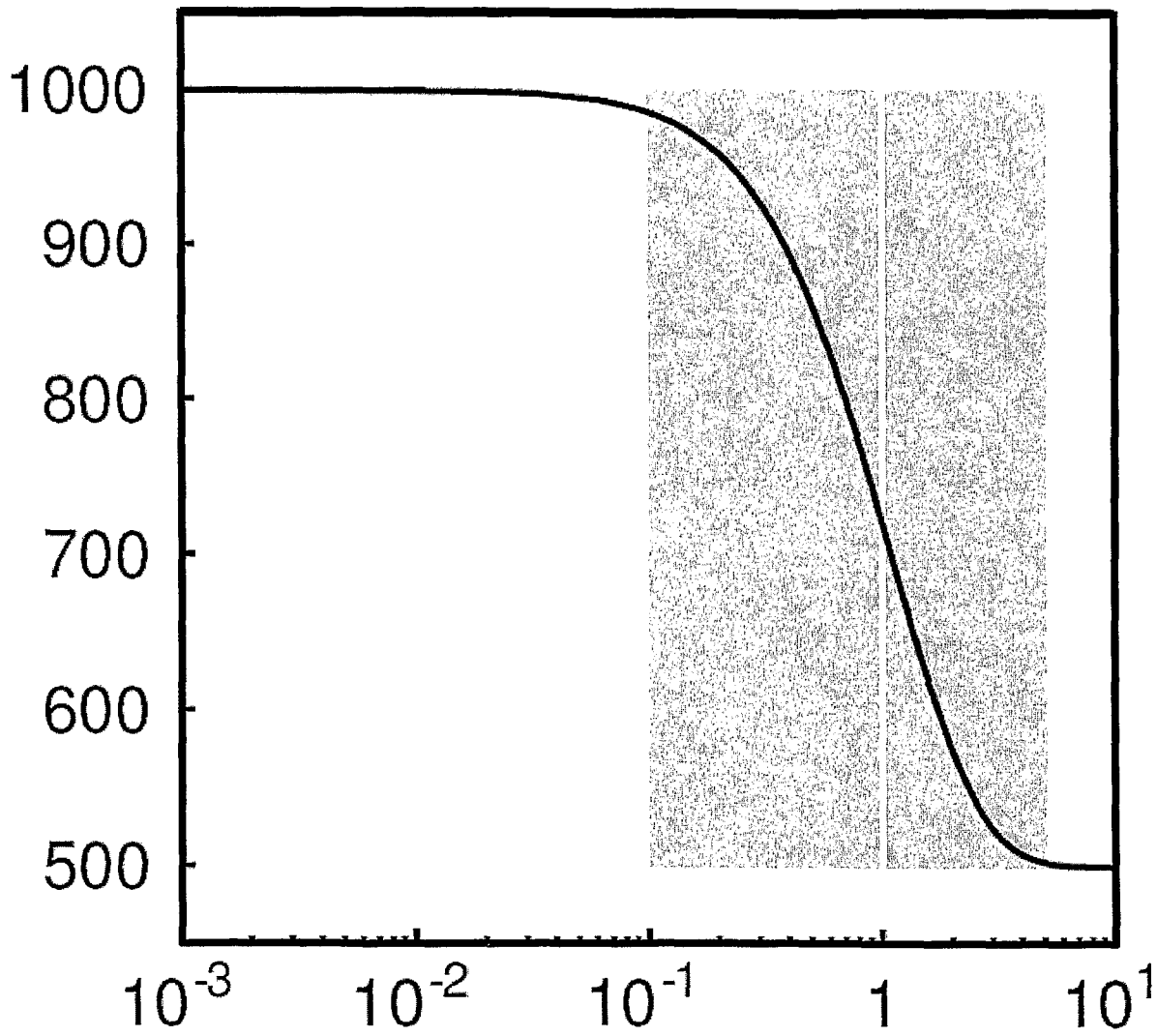

Fig. 2

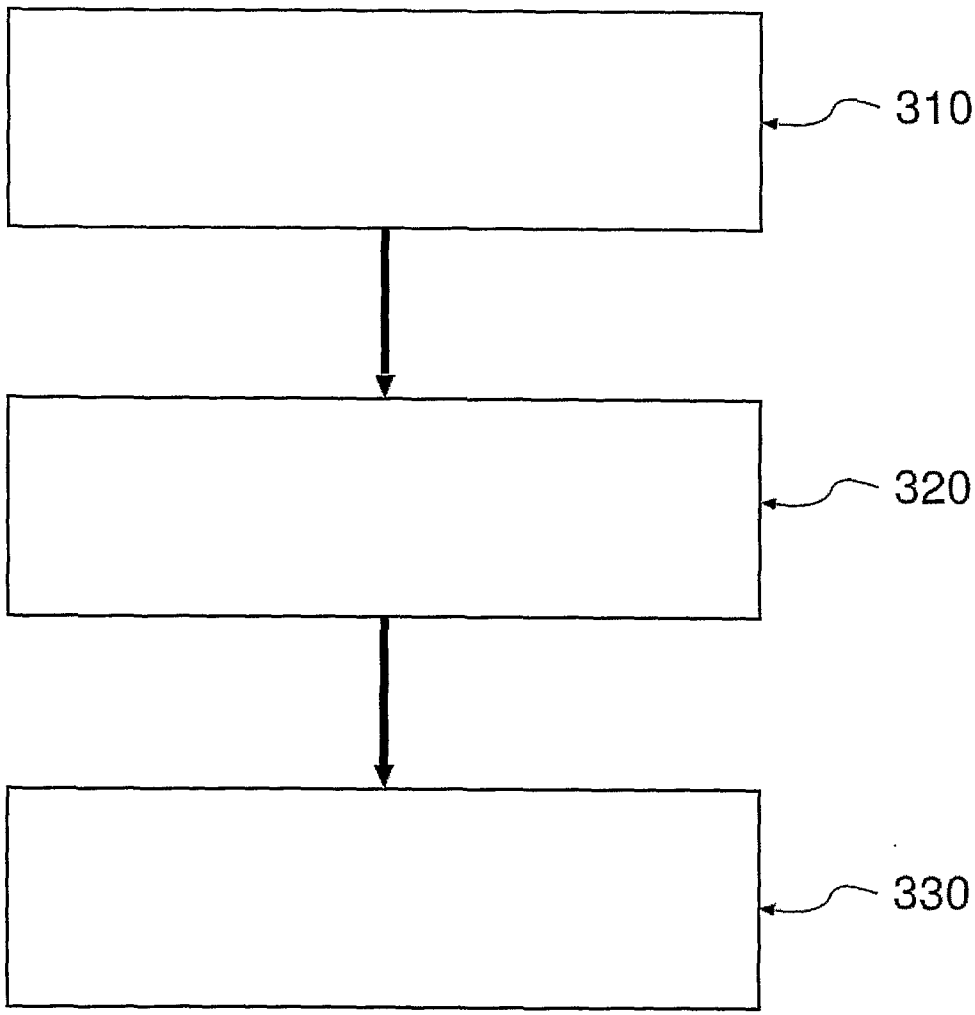

Fig. 3

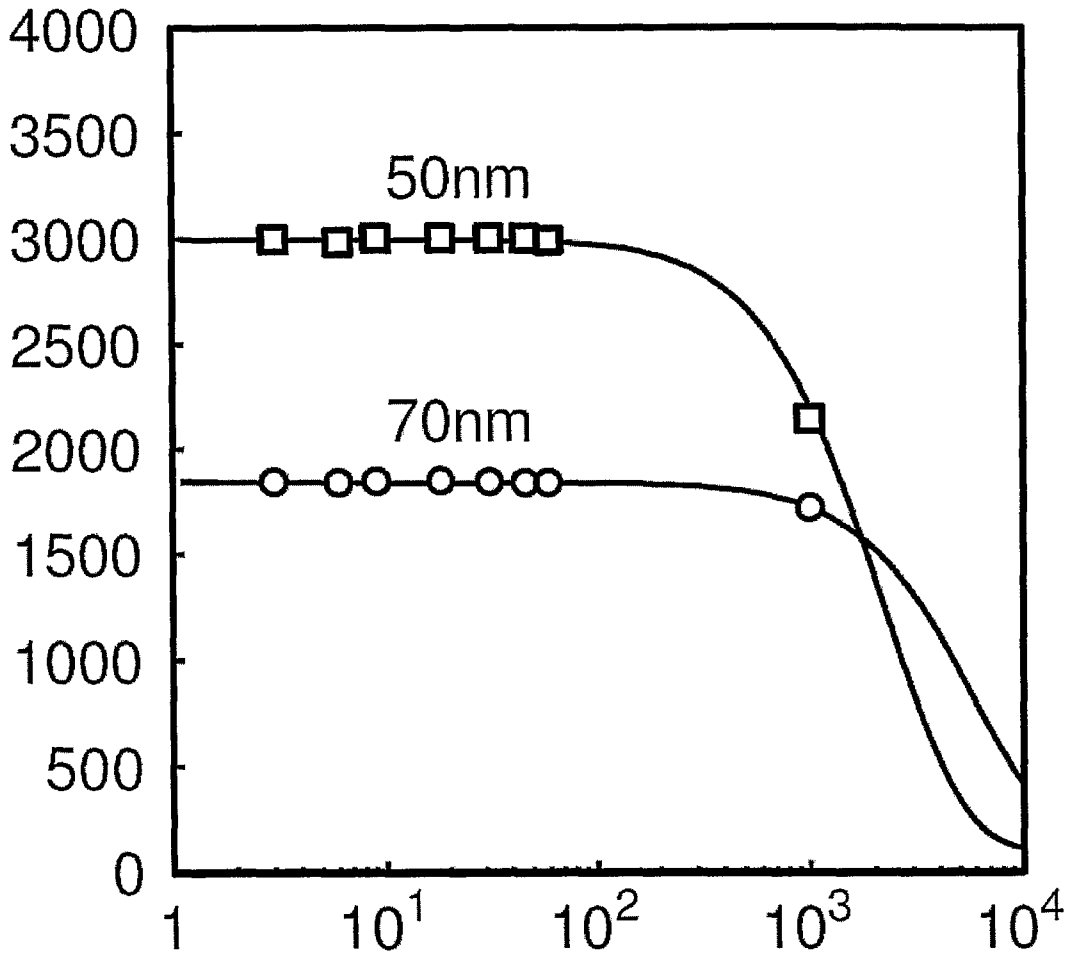
4000
3500
3000
2500
2000
1500
1000
500
0
50nm
70nm
1
10^1
10^2
10^3
10^4

Fig. 4

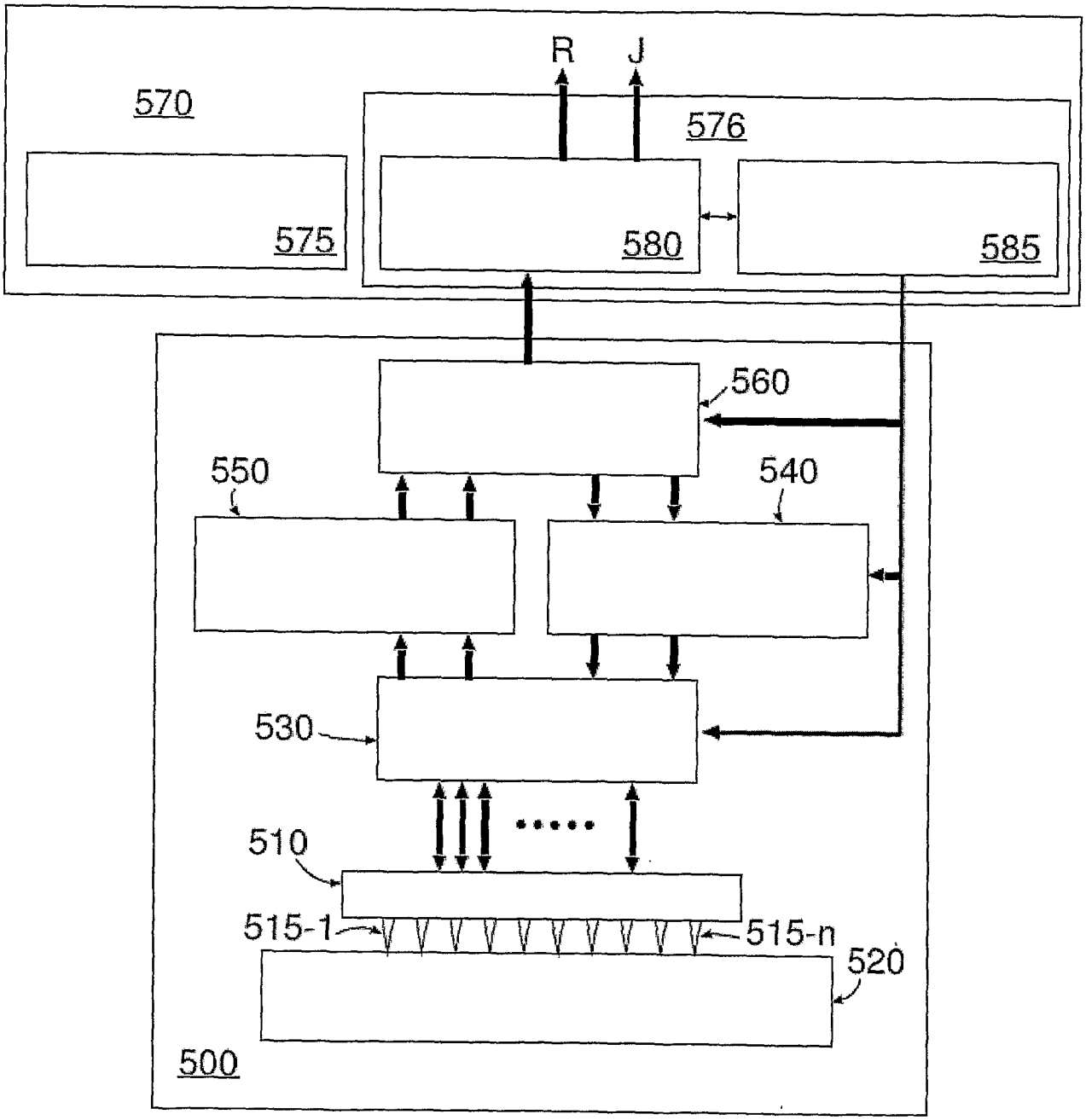

Fig. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/DK2007/000192

A. CLASSIFICATION OF SUBJECT MATTER
INV. G01R31/312

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	KINDER R ET AL: "DETERMINATION OF THE DEPTH OF SHALLOW IMPLANATED P+-N JUNCTIONS BY THE FOUR-POINT PROBE METHOD" PHYSICA STATUS SOLIDI (A). APPLIED RESEARCH, BERLIN, DE, vol. 157, 1996, pages 393-398, XP009042017 ISSN: 0031-8965 the whole document	1-7
Y	KELLER S ET AL: "Microscopic four-point probe based on SU-8 cantilevers" 14 December 2005 (2005-12-14), REVIEW OF SCIENTIFIC INSTRUMENTS, AMERICAN INSTITUTE OF PHYSICS, US, PAGE(S) 125102-125102 , XP012079131 ISSN: 0034-6748 the whole document	1-7

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 June 2007	29/06/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Vytlacilová, Lenka

INTERNATIONAL SEARCH REPORT

International application No
PCT/DK2007/000192

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	SMITS F M: "MEASUREMENT OF SHEET RESISTIVITIES WITH THE FOUR-POINT PROBE" 1958, BELL SYSTEM TECHNICAL JOURNAL, AT AND T, SHORT HILLS, NY, US, PAGE(S) 711-718 , XP009033160 ISSN: 0005-8580 the whole document	1-7
A	US 5 691 648 A (CHENG DAVID [US]) 25 November 1997 (1997-11-25) figures 3,4	8-10

Form PCT/ISA/210 (continuation of second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/DK2007/000192

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5691648 A	25-11-1997	US 5495178 A	27-02-1996