(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
20 June 2019 (20.06.2019)

WIPO | PCT

(10) International Publication Number
WO 2019/117883 A1

(51) International Patent Classification:
H01L 29/15 (2006.01) *H01L 39/02* (2006.01)
H01L 29/66 (2006.01)

(21) International Application Number:
PCT/US2017/065932

(22) International Filing Date:
13 December 2017 (13.12.2017)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054-1549 (US).

(72) Inventors: **YOSCOVITS, Zachary R.**; 16145 NW Schendel Avenue, Unit 21B, Beaverton, Oregon 97006 (US). **LAMPERT, Lester**; 17564 NW Springville Rd., Unit 4, Portland, Oregon 97229 (US). **CAUDILLO, Roman**; 2305 SE 16th Avenue, Portland, Oregon 97214 (US). **ROBERTS, Jeanette M.**; 17898 NW Pumpkin Ridge Road, North Plains, Oregon 97133 (US). **GEORGE, Hubert C.**; 7016 NW Eleanor Avenue, Portland, Oregon 97229 (US). **THOMAS, Nicole K.**; 1125 NW 12th Ave, Apt 309, Portland, Oregon 97209 (US). **SINGH, Kanwaljit**; Wierdsmaplein 41, 3072 MJ Rotterdam (NL). **MICHALAK, David J.**; 1511 SW Park Avenue, Apt 811, Portland, Oregon 97201 (US). **PILLARISETTY, Ravi**; 1330 SW 3rd Ave, Apt. 1103, Portland, Oregon 97201 (US). **CLARKE, James S.**; 5676 NW 204th Place, Portland, Oregon 97229 (US).

(74) Agent: **HARTMANN, Natalya**; Patent Capital Group, 2816 Lago Vista Lane, Rockwall, Texas 75032 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP,

(54) Title: QUBIT DEVICES WITH JOSEPHSON JUNCTIONS FABRICATED USING AIR BRIDGE OR CANTILEVER

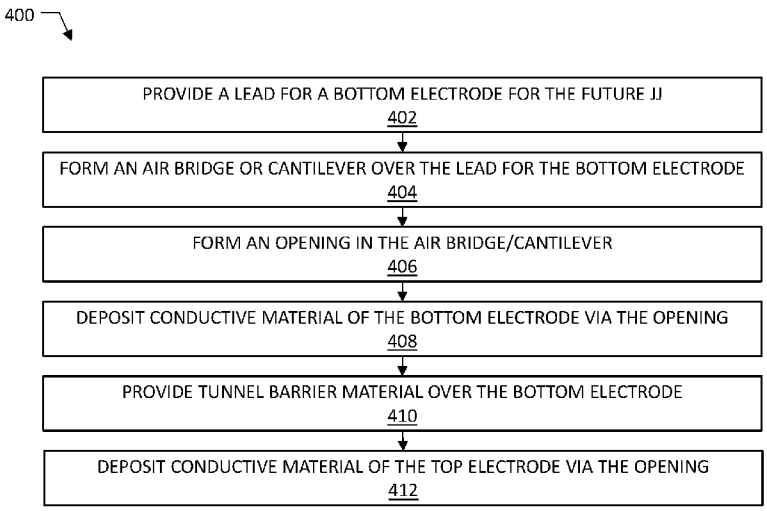

FIG. 4

(57) Abstract: One aspect of the present disclosure proposes a method of fabricating quantum circuit assemblies that include Josephson Junctions. The method is based on providing a structure that forms a bridge or a cantilever over a lead for the bottom electrode of a future Josephson Junction, forming an opening in the bridge/cantilever so that the opening is above the lead for the bottom electrode, and then depositing bottom and top electrode materials, as well as the tunnel barrier material for the Josephson Junction, through the opening. Such a method may result in Josephson Junctions having an improved performance compared to Josephson Junctions fabricated using existing techniques, and may be efficiently used in large-scale manufacturing.

WO 2019/117883 A1

[Continued on next page]

KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

QUBIT DEVICES WITH JOSEPHSON JUNCTIONS FABRICATED USING AIR BRIDGE OR CANTILEVER

Technical Field

[0001] This disclosure relates generally to the field of quantum computing, and more specifically, to Josephson Junctions for use in quantum circuits and to methods of fabrication thereof.

Background

[0002] Quantum computing refers to the field of research related to computation systems that use quantum-mechanical phenomena to manipulate data. These quantum-mechanical phenomena, such as superposition (in which a quantum variable can simultaneously exist in multiple different states) and entanglement (in which multiple quantum variables have related states irrespective of the distance between them in space or time), do not have analogs in the world of classical computing.

[0003] Quantum computers use so-called quantum bits, referred to as qubits (both terms "bits" and "qubits" often interchangeably refer to the values that they hold as well as to the actual devices that store the values). Similar to a bit of a classical computer, at any given time, a qubit can be either 0 or 1. However, in contrast to a bit of a classical computer, a qubit can also be 0 and 1 at the same time, which is a result of superposition of quantum states – a uniquely quantum-mechanical phenomenon. Entanglement also contributes to the unique nature of qubits in that input data to a quantum processor can be spread out among entangled qubits, allowing manipulation of that data to be spread out as well: providing input data to one qubit results in that data being shared to other qubits with which the first qubit is entangled.

[0004] Compared to well-established and thoroughly researched classical computers, quantum computing is still in its infancy, with the highest number of qubits in a solid-state quantum processor currently being below 100. One of the main challenges resides in protecting qubits from decoherence so that they can stay in their information-holding states long enough to perform the necessary calculations and read out the results. Another challenge resides in fabricating qubits in a manner that may be used in large-scale manufacturing.

Brief Description of the Drawings

[0005] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0006] FIG. 1 provides a schematic illustration of an exemplary superconducting quantum circuit, according to some embodiments of the present disclosure.

[0007] FIGS. 2A-2C provide a schematic illustration of a photoresist mask provided over a substrate for fabricating a Josephson Junction using a double-angle shadow evaporation approach.

[0008] FIGS. 3A-3C provide a schematic illustration of fabricating Josephson Junctions using a conventional double-angle shadow evaporation approach.

[0009] FIG. 4 provides a flow chart of an air bridge/cantilever method for fabricating Josephson Junctions for quantum circuit assemblies, according to some embodiments of the present disclosure.

[0010] FIGS. 5A-5F are cross-sections illustrating various exemplary stages in the manufacture of a quantum circuit assembly using the air bridge/cantilever method of FIG. 4, in accordance with various embodiments of the present disclosure.

[0011] FIGS. 6A and 6B are top views of a wafer and dies that may include one or more of quantum circuit assemblies disclosed herein.

[0012] FIG. 7 is a cross-sectional side view of a device assembly that may include one or more of quantum circuit assemblies disclosed herein.

[0013] FIG. 8 is a block diagram of an exemplary quantum computing device that may include one or more of quantum circuit assemblies disclosed herein, in accordance with various embodiments.

Detailed Description

Overview

[0014] As briefly described above, quantum computing, or quantum information processing, refers to the field of research related to computation systems that use quantum-mechanical phenomena to manipulate data. One example of quantum-mechanical phenomena is the principle of quantum superposition, which asserts that any two or more quantum states can be added together, i.e. superposed, to produce another valid quantum state, and that any quantum state can be represented as a sum of two or more other distinct states. Quantum entanglement is another example of quantum-mechanical phenomena. Entanglement refers to groups of particles being generated or interacting in such a way that the state of one particle becomes intertwined with that of the others. Furthermore, the quantum state of each particle cannot be described independently. Instead, the quantum state is given for the group of entangled particles as a whole. Yet another example of quantum-mechanical phenomena is sometimes described as a "collapse" because it asserts that when we observe (measure) particles, we unavoidably change their properties in that, once observed, the particles cease to be in a state of superposition or entanglement (i.e. by trying to ascertain anything about the particles, we collapse their state).

[0015] Put simply, superposition postulates that a given particle can be simultaneously in two states, entanglement postulates that two particles can be related in that they are able to instantly coordinate their states irrespective of the distance between them in space and time, and collapse

postulates that when one observes a particle, one unavoidably changes the state of the particle and its' entanglement with other particles. These unique phenomena make manipulation of data in quantum computers significantly different from that of classical computers (i.e. computers that use phenomena of classical physics). Therefore, both the industry and the academics continue to focus on a search for new and improved physical systems whose functionality could approach that expected of theoretically designed qubits.

[0016] Physical systems for implementing qubits that have been explored until now include e.g. superconducting qubits, single trapped ion qubits, silicon (Si) quantum dot qubits, photon polarization qubits, etc.

[0017] Out of the various physical implementations of qubits listed above, superconducting qubits are promising candidates for building a quantum computer. All of superconducting qubits operate based on the Josephson effect, which refers to a macroscopic quantum phenomenon of supercurrent, i.e. a current that, due to zero electrical resistance, flows indefinitely long without any voltage applied, across a device known as a Josephson Junction.

[0018] Josephson Junctions are integral building blocks in superconducting quantum circuits where they form the basis of quantum circuit elements that can approximate functionality of theoretically designed qubits. Therefore, improvements with respect to fabricating Josephson Junctions for use in quantum circuit assemblies are always desirable. In particular, it would be desirable to have methods for fabricating Josephson Junctions that have adequate performance and can be manufactured on large-scale.

[0019] Embodiments of the present disclosure propose methods of fabricating quantum circuit assemblies that include Josephson Junctions, as well as qubit devices comprising Josephson Junctions. In one aspect of the present disclosure, a method of fabricating a quantum circuit assembly with at least one Josephson Junction is disclosed. The disclosed method is based on providing a structure that forms a bridge or a cantilever over a lead for the bottom electrode of a future Josephson Junction, thus giving rise to the name "air bridge/cantilever method" used herein to describe this method. The air bridge/cantilever method further includes forming an opening in the bridge/cantilever so that the opening is above the lead for the bottom electrode, and then depositing bottom and top electrode materials, as well as the tunnel barrier material for the Josephson Junction, through the opening. Such a method may result in Josephson Junctions having an improved performance compared to Josephson Junctions fabricated using existing techniques, e.g. because it may help decrease amount of spurious (i.e. unintentional and undesirable) two-level systems (TLS's), thought to be the dominant source of superconducting qubit decoherence, in the vicinity of Josephson Junctions. In addition, such a method may be efficiently used in large-scale

manufacturing, providing a substantial improvement with respect to conventional approaches, such as e.g. double-angle shadow evaporation approach, which include fabrications steps that are not suitable for implementing with larger wafer sizes used by leading edge device manufactures.

[0020] In order to provide substantially lossless connectivity to, from, and between the qubits, some or all of the electrically conductive portions of various quantum circuit elements described herein (e.g. electrodes of Josephson Junctions and leads to such electrodes) may be made from one or more superconductive materials. However, some or all of these electrically conductive portions could be made from electrically conductive materials which are not superconductive. In the following, unless specified otherwise, reference to an electrically conductive material or circuit element implies that a superconductive material can be used, and vice versa (i.e. reference to a superconductor implies that a conductive material which is not superconductive may be used). Furthermore, any material described herein as a "superconductive/superconducting material" may refer to one or more materials, including alloys of materials, which exhibit superconducting behavior at typical qubit operating conditions (e.g. materials which exhibit superconducting behavior at very low temperatures at which qubits typically operate), but which may not exhibit such behavior at higher temperatures (e.g. at room temperatures). Examples of such materials include aluminum (Al), niobium (Nb), niobium nitride (NbN), titanium nitride (TiN), niobium titanium nitride (NbTiN), indium (In), and molybdenum rhenium (MoRe), all of which are particular types of superconductors at qubit operating temperatures, as well as their alloys.

[0021] While some descriptions are provided with reference to superconducting qubits, in particular to transmons, a particular class of superconducting qubits, at least some teachings of the present disclosure may be applicable to implementations of any qubits, including superconducting qubits other than transmons and/or including qubits other than superconducting qubits, which may employ non-linear inductive elements, such as Josephson Junctions, all of which implementations are within the scope of the present disclosure. For example, the quantum circuit device assemblies described herein may be used in hybrid semiconducting-superconducting quantum circuits.

[0022] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0023] In the drawings, some schematic illustrations of exemplary structures of various devices and assemblies described herein may be shown with precise right angles and straight lines, but it is to be understood that such schematic illustrations may not reflect real-life process limitations which may

cause the features to not look so “ideal” when any of the structures described herein are examined using e.g. scanning electron microscopy (SEM) images or transmission electron microscope (TEM) images. In such images of real structures, possible processing defects could also be visible, such as e.g. not-perfectly straight edges of materials, tapered vias or other openings, inadvertent rounding of corners or variations in thicknesses of different material layers, occasional screw, edge, or combination dislocations within the crystalline region, and/or occasional dislocation defects of single atoms or clusters of atoms. There may be other defects not listed here but that are common within the field of device fabrication.

[0024] Various operations may be described as multiple discrete actions or operations in turn in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0025] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges. As used herein, the notation "A/B/C" means (A), (B), and/or (C).

[0026] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. The accompanying drawings are not necessarily drawn to scale. Unless otherwise specified, the use of the ordinal adjectives “first,” “second,” and “third,” etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0027] The terms “over,” “under,” “between,” and “on” as used herein refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between two layers may be

directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer "on" a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening layers.

[0028] In the following detailed description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. For example, the terms "oxide," "carbide," "nitride," etc. refer to compounds containing, respectively, oxygen, carbon, nitrogen, etc. The terms "substantially," "close," "approximately," "near," and "about," generally refer to being within +/- 20% of a target value based on the context of a particular value as described herein or as known in the art. Similarly, terms indicating orientation of various elements, such as e.g. "coplanar," "perpendicular," "orthogonal," "parallel," or any other angle between the elements, generally refer to being within +/- 5-10% of a target value based on the context of a particular value as described herein or as known in the art. Furthermore, as used herein, terms indicating what may be considered an idealized behavior, such as e.g. "superconducting" or "lossless", are intended to cover functionality that may not be exactly ideal but is within acceptable margins for a given application. For example, a certain level of loss, either in terms of non-zero electrical resistance or non-zero amount of spurious TLS's may be acceptable such that the resulting materials and structures may still be referred to by these "idealized" terms. Specific values associated with an acceptable level of loss are expected to change over time as fabrication precision will improve and as fault-tolerant schemes may become more tolerant of higher losses, all of which are within the scope of the present disclosure.

[0029] Still further, while the present disclosure may include references to microwave signals, this is done only because current qubits are designed to work with such signals because the energy in the microwave range is higher than thermal excitations at the temperature that qubits are typically operated at. In addition, techniques for the control and measurement of microwaves are well known. For these reasons, typical frequencies of qubits are in 1-10 GHz, e.g. in 4-10 GHz, range, in order to be higher than thermal excitations, but low enough for ease of microwave engineering. However, advantageously, because excitation energy of qubits is controlled by the circuit elements, qubits can be designed to have any frequency. Therefore, in general, qubits could be designed to operate with signals in other ranges of electromagnetic spectrum and embodiments of the present disclosure could be modified accordingly. All of these alternative implementations are within the scope of the present disclosure.

Quantum computing and Josephson Junctions

[0030] FIG. 1 provides a schematic illustration of an exemplary superconducting quantum circuit 100 that may include any of the quantum circuit assemblies described herein.

[0031] As shown in FIG. 1, an exemplary superconducting quantum circuit 100 may include two or more qubits 102 (reference numerals following after a dash, such as e.g. qubit 102-1 and 102-2 indicate different instances of the same or analogous element). Each of the superconducting qubits 102 may include one or more Josephson Junctions 104 electrically connected to one or more other circuit elements 106, which, in combination with the Josephson Junction(s) 104, form a non-linear circuit providing a unique two-level quantum state for the qubit. In general, a Josephson Junction includes two superconductors coupled by a so-called weak link that weakens the superconductivity between the two superconductors. In some embodiments, weak links of Josephson Junctions may be implemented by e.g. providing a thin layer of an insulating or a semiconducting material, typically referred to as a "barrier" or a "tunnel barrier," sandwiched, in a stack-like arrangement, between two layers of superconductor, which two superconductors typically referred to, respectively, as a "bottom/base electrode" and a "top electrode" of a Josephson Junction. Josephson Junction provides a non-linear inductive element to the circuit and allows the qubit to become an anharmonic oscillator. The anharmonicity is determined by the ratio of the charging energy, which stems from the total capacitance between a first and second element of the qubit, and the Josephson energy of the non-linear inductive element (e.g., Josephson Junction). The anharmonicity is what allows the state of the qubit to be controlled to a high level of fidelity. In addition to controlling the anharmonicity, the charging and Josephson energies also control the qubit frequency.

[0032] Typically, when a qubit employs only one Josephson Junction, a frequency of the qubit cannot be changed substantially beyond what is defined by the design unless one of the qubit capacitive elements is tunable. Employing two or more Josephson Junctions, e.g. arranged in a so-called superconducting quantum interference device (SQUID), allows controlling the frequency of the qubit, which, in turn, allows greater control as to whether and when the qubit interacts with other components of a quantum circuit, e.g. with other qubits. In general, a SQUID of a superconducting qubit includes a pair of Josephson Junctions and a loop of a conductive, typically superconductive material (i.e. a superconducting loop), connecting a pair of Josephson Junctions. Applying a net magnetic field in a certain orientation to the SQUID loop of a superconducting qubit allows controlling the frequency of the qubit. In particular, applying magnetic field to the SQUID region of a superconducting qubit is generally referred to as a "flux control" of a qubit, and the magnetic field is generated by providing direct current (DC) or a pulse of current through an electrically conductive or superconductive line generally referred to as a "flux bias line" (also known

as a "flux line" or a "flux coil line"). By providing flux bias lines sufficiently close to SQUIDs, magnetic fields generated as a result of currents running through the flux bias lines extend to the SQUIDs, thus tuning qubit frequencies.

[0033] Turning back to FIG. 1, within each qubit 102, the one or more Josephson Junctions 104 may be directly electrically connected to one or more other circuit elements 106, which, in combination with the Josephson Junction(s) 104, form a non-linear oscillator circuit providing multi-level quantum system where the first two to three levels define the qubit under normal operation. The circuit elements 106 could be e.g. shunt capacitors, superconducting loops of a SQUID, electrodes for setting an overall capacitance of a qubit, or/and ports for capacitively coupling the qubit to one or more of a readout resonator, a coupling resonator, and a direct microwave drive line, or electromagnetically coupling the qubit to a flux bias line.

[0034] As also shown in FIG. 1, an exemplary quantum circuit 100 typically includes a plurality of non-resonant transmission lines 108, and a plurality of resonators 110. The non-resonant transmission lines 108 are typically used for providing microwave signals to different quantum circuit elements and components, such as e.g. various control lines for various qubits, and may be considered to implement external control of qubits. For example, for superconducting qubits, examples of the non-resonant transmission lines 108 include flux bias lines, microwave lines, and readout lines. On the other hand, the resonators 110 may be viewed as implementing internal control lines for qubit. For superconducting qubits, examples of the resonators 100 include coupling and readout resonators.

[0035] In general, a resonator 110 of a quantum circuit differs from a non-resonant microwave transmission line 108 in that a resonator is deliberately designed to support resonant oscillations (i.e. resonance), under certain conditions. In contrast, non-resonant transmission lines may be similar to conventional microwave transmission lines in that they are designed to avoid resonances, especially resonances at frequencies/wavelengths close to the resonant frequencies/wavelengths of any resonant object used in the quantum computing circuits, e.g., qubits, bus resonators, or readout resonators in the proximity of such non-resonant lines. Once non-resonant transmission lines are manufactured, some of them may inadvertently support some resonances, but, during its design, efforts are taken to minimize resonances, standing waves, and reflected signals as much as possible, so that all of the signals can be transmitted through these lines without, or with as little resonance as possible.

[0036] On-chip capacitive coupling between quantum or control elements can be achieved either through use of coupling components such as a coupling component on a neighboring qubit, a lumped element capacitor, a lumped element resonator, or a transmission line segment. A

transmission line segment is a resonator that is made by employing fixed boundary conditions, and these boundary conditions control the frequencies/wavelengths which will resonate within a given transmission line segment used to implement a resonator. In order to satisfy boundary conditions for resonance, each end of a transmission line segment resonator can be either a node, if it is shorted to ground (e.g. where one end of the transmission line segment structure is electrically connected to a ground plane), or an antinode, if it is capacitively or inductively coupled to ground or to another quantum circuit element. Thus, resonators 110 differ from non-resonant microwave transmission lines 108 in how these lines are terminated at the relevant ends. A line used to route a signal on a substrate, i.e. one of the non-resonant transmission lines 108, typically extends from a specific source, e.g. a bonding pad or another type of electrical connection to a source, to a specific load (e.g. a short circuit proximate to SQUID loop, a quantum dot device, another bonding pad, or another electrical connection to a load). In other words, non-resonant transmission lines 108 terminate with direct electrical connections to sources, ground sinks, and/or loads. On the other hand, a transmission line resonator is typically composed of a piece of transmission line terminated with either two open circuits (in case of a half-wavelength resonator) or an open and a short circuit (in case of a quarter-wavelength resonator). In this case, for a desired resonant frequency, transmission line length may e.g. be a multiple of a microwave wavelength divided by 2 or 4, respectively. However, other terminations are possible, for example capacitive or inductive, and in this case the required line length to support resonance will be different from that identified above. For example, capacitive terminations may be used for resonators which are coupled to qubits, to a feedline, line, or to another resonator by a capacitive interaction.

[0037] Besides line termination by capacitive or inductive coupling or a short circuit, in order to support resonant oscillations, transmission line segments of the resonators 110 need to be of a specific length that can support such oscillations. That is why, often times, resonators 110 may be laid out on a substrate longer than the actual distance would require (i.e. a non-resonant transmission line would typically be laid out to cover the distance in the most compact manner possible, e.g. without any curves, wiggles, or excess length, while a resonator may need to have curves, wiggles, and be longer than the shortest distance between the two elements the resonator is supposed to couple in order to be sufficiently long to support resonance).

[0038] One type of the resonators 110 used with superconducting qubits are so-called coupling resonators (also known as “bus resonators”), which allow one method to couple different qubits together in order to realize quantum logic gates. These types of resonators are analogous in concept and have analogous underlying physics as readout resonators, except that a coupling or “bus” resonator involves only capacitive couplings between two or more qubits whereas a readout

resonator involves capacitive coupling between two or more qubits and a feedline. A coupling resonator may be implemented as a microwave transmission line segment that includes capacitive or inductive connections to ground on both sides (e.g. a half-wavelength resonator), which results in oscillations (resonance) within the transmission line. While the ends of a coupling resonator have open circuits to the ground, each side of a coupling resonator is coupled, either capacitively or inductively, to a respective (i.e. different) qubit by being in the appropriate location and sufficient proximity to the qubit. Because different regions of a coupling resonator have coupling with a respective different qubit, the two qubits are coupled together through the coupling resonator. Thus, coupling resonators may be employed for implementing logic gates.

[0039] Another type of the resonators 110 used with superconducting qubits are so-called readout resonators, which may be used to read the state(s) of qubits. In some embodiments, a corresponding readout resonator may be provided for each qubit. A readout resonator, similar to the bus coupling resonator, is a transmission line segment. On one end it may have an open circuit connection to ground as well as any capacitively or inductively coupled connections to other quantum elements or a non-resonant microwave feedline. On the other end, a readout resonator may either have a capacitive connection to ground (for a half-wavelength resonator) or may have a short circuit to the ground (for a quarter-wavelength resonator), which also results in oscillations within the transmission line, with the resonant frequency of the oscillations being close to the frequency of the qubit. A readout resonator is coupled to a qubit by being in the appropriate location and sufficient proximity to the qubit, again, either through capacitive or inductive coupling. Due to a coupling between a readout resonator and a qubit, changes in the state of the qubit result in changes of the resonant frequency of the readout resonator. In turn, changes in the resonant frequency of the readout resonator can be read externally via connections which lead to external electronics e.g. wire or solder bonding pads.

[0040] For the non-resonant transmission lines 108, some descriptions of flux bias lines were provided above and, in the interests of brevity are not repeated here. In general, running a current through a flux bias line, provided e.g. from a wirebonding pads or any other connection element, allows tuning (i.e. changing) the frequency of a corresponding qubit 102 to which a given flux bias line is connected. As a result of running the current in a given flux bias line, magnetic field is created around the line. If such a magnetic field is in sufficient proximity to a given qubit 102, e.g. by a portion of the flux bias line being provided next (sufficiently close) to the qubit 102, the magnetic field couples to the qubit, thereby changing the spacing between the energy levels of the qubit. This, in turn, changes the frequency of the qubit since the frequency is directly related to the spacing between the energy levels via the equation $E=h\nu$ (Planck's equation), where E is the energy (in this

case the energy difference between energy levels of a qubit), h is the Planck's constant and v is the frequency (in this case the frequency of the qubit). As this equation illustrates, if E changes, then v changes. Different currents and pulses of currents can be sent down each of the flux lines allowing for independent tuning of the various qubits.

[0041] Typically, the qubit frequency may be controlled in order to bring the frequency either closer to or further away from another resonant item, for example a coupling resonator or a coupled neighbor qubit, to implement multi-qubit interactions, as may be desired in a particular setting.

[0042] For example, if it is desirable that a first qubit 102-1 and a second qubit 102-2 interact, via a coupling resonator (i.e. an example of the resonators 110) connecting these qubits, then both qubits 102 may need to be tuned to be at nearly the same frequency or a detuning equal, or nearly equal, to the anharmonicity. One way in which such two qubits could interact is that, if the frequency of the first qubit 102-1 is tuned very close to the resonant frequency of the coupling resonator, the first qubit can, when in the excited state, relax back down to the ground state by emitting a photon (similar to how an excited atom would relax) that would resonate within the coupling resonator. If the second qubit 102-2 is also at this energy (i.e. if the frequency of the second qubit is also tuned very close to the resonant frequency of the coupling resonator), then it can absorb the photon emitted from the first qubit, via the coupling resonator coupling these two qubits, and be excited from its ground state to an excited state. Thus, the two qubits interact, or are entangled, in that a state of one qubit is controlled by the state of another qubit. In other scenarios, two qubits could interact via exchange of virtual photons, where these three elements do not have to be tuned to be at the same frequency with one another. In general, two or more qubits could be configured to interact with one another by tuning their frequencies to specific values or ranges.

[0043] On the other hand, it may sometimes be desirable that two qubits coupled by a coupling resonator do not interact, i.e. the qubits are independent. In this case, by applying magnetic flux, by means of controlling the current in the appropriate flux bias line, to one qubit it is possible to cause the frequency of the qubit to change enough so that the photon it could emit no longer has the right frequency to resonate on the coupling resonator or on the neighboring qubit via a virtual photon transfer through the bus. If there is nowhere for such a frequency-detuned photon to go, the qubit will be better isolated from its surroundings and will live longer in its current state. Thus, in general, two or more qubits could be configured to reduce interactions with one another by tuning their frequencies to specific values or ranges.

[0044] The state(s) of each qubit 102 may be read by way of its corresponding readout resonator of the resonators 110. As explained below, the state of qubit 102 induces a shift in the resonant frequency in the associated readout resonator. This shift in resonant frequency can then be read

out using its coupling to a feedline. To that end, an individual readout resonator may be provided for each qubit. As described above, a readout resonator may be a transmission line segment that includes a capacitive connection to ground on one side and is either shorted to the ground on the other side (for a quarter-wavelength resonator) or has a capacitive connection to ground (for a half-wavelength resonator), which results in oscillations within the transmission line (resonance) that depends upon the state of a proximal qubit. A readout resonator may be coupled to its corresponding qubit 102 by being in an appropriate location and sufficient proximity to the qubit, more specifically in an appropriate location and sufficient proximity to a first element (or "island) of the qubit 102 that capacitively couples to the readout resonator, when the qubit is implemented as a transmon. Due to a coupling between the readout resonator and the qubit, changes in the state of the qubit result in changes of the resonant frequency of the readout resonator. In turn, by ensuring that the readout resonator is in sufficient proximity to a corresponding microwave feedline, changes in the resonant frequency of the readout resonator induce changes in the transmission coefficients of the microwave feedline, detected externally.

[0045] A coupling resonator, or, more generally, a coupling component, allows coupling different qubits together, e.g. as described above, in order to realize quantum logic gates. A coupling component could be comprised of a coupling component on a neighboring qubit, a lumped element capacitor, a lumped element resonator, or a coupling transmission line segment. A coupling transmission line segment (e.g., coupling resonator or bus resonator) is similar to a readout resonator in that it is a transmission line segment that includes capacitive connections to various objects (e.g., qubits, ground, etc.) on both sides (i.e. a half-wavelength resonator), which also results in oscillations within the coupling resonator. Each side/end of a coupling component is coupled (again, either capacitively or inductively) to a respective qubit by being in appropriate location and sufficient proximity to the qubit, namely in sufficient proximity to a first element (or "island") of the qubit that capacitively couples to the coupling component, when the qubit is implemented as a transmon. Because each side of a given coupling component has coupling with a respective different qubit, the two qubits are coupled together through the coupling component. Thus, coupling components may be employed in order to implement multi-qubit interactions.

[0046] In some implementations, a microwave line may be used to not only readout the state of the qubits as described above, but also to control the state of the qubits. When a single microwave line is used for this purpose, the line operates in a half-duplex mode where, at some times, it is configured to readout the state of the qubits, and, at other times, it is configured to control the state of the qubits. In other implementations, microwave lines may be used to only readout the state of the qubits as described above, while separate drive lines, may be used to control the state of the

qubits. In such implementations, microwave lines used for readout may be referred to as readout lines, while microwave lines used for controlling the state of the qubits may be referred to as drive lines. Drive lines may control the state of their respective qubits 102 by providing to the qubits a microwave pulse at the qubit frequency, which in turn stimulates (i.e. triggers) a transition between the states of the qubit. By varying the length of this pulse, a partial transition can be stimulated, giving a superposition of the states of the qubit.

[0047] Flux bias lines, microwave lines, readout lines, drive lines, coupling components, and readout resonators, such as e.g. those described above, together form interconnects for supporting propagation of microwave signals. Further, any other connections for providing direct electrical interconnection between different quantum circuit elements and components, such as e.g. connections from electrodes of Josephson Junctions to plates of the capacitors or to superconducting loops of SQUIDs or connections between two ground lines of a particular transmission line for equalizing electrostatic potential on the two ground lines, may also be referred to as interconnects. Still further, the term "interconnect" may also be used to refer to elements providing electrical interconnections between quantum circuit elements and components and non-quantum circuit elements, which may also be provided in a quantum circuit, as well as to electrical interconnections between various non-quantum circuit elements provided in a quantum circuit. Examples of non-quantum circuit elements which may be provided in a quantum circuit may include various analog and/or digital systems, e.g. analog to digital converters, mixers, multiplexers, amplifiers, etc.

[0048] In various embodiments, various conductive circuit elements of supporting circuitry included in a quantum circuit such as the quantum circuit 100 could have different shapes and layouts. In general, the term "line" as used herein in context of signal lines or transmission lines does not imply straight lines, unless specifically stated so. For example, some resonant or non-resonant transmission lines or parts thereof (e.g. conductor strips of resonant or non-resonant transmission lines) may comprise more curves, wiggles, and turns while other resonant or non-resonant transmission lines or parts thereof may comprise less curves, wiggles, and turns, and some transmission lines or parts thereof may comprise substantially straight lines. At least some of the Josephson Junctions 104 included within the qubits 102 shown in FIG. 1 may be fabricated according to various embodiments of the improved method described herein.

[0049] The qubits 102, the non-resonant transmission lines 108, and the resonators 110 of the quantum circuit 100 may be provided on, over, or at least partially embedded in a substrate (not shown in FIG. 1). The substrate may be any substrate suitable for realizing quantum circuit assemblies described herein. In one implementation, the substrate may be a crystalline substrate

such as, but not limited to a silicon or a sapphire substrate, and may be provided as a wafer or a portion thereof. In other implementations, the substrate may be non-crystalline. In general, any material that provides sufficient advantages (e.g. sufficiently good electrical isolation and/or ability to apply known fabrication and processing techniques) to outweigh the possible disadvantages (e.g. negative effects of spurious TLS's), and that may serve as a foundation upon which a quantum circuit may be built, falls within the spirit and scope of the present disclosure. Additional examples of substrates include silicon-on-insulator (SOI) substrates, III-V substrates, and quartz substrates.

[0050] In various embodiments, quantum circuits such as the one shown in FIG. 1 may be used to implement components associated with a quantum integrated circuit (IC). Such components may include those that are mounted on or embedded in a quantum IC, or those connected to a quantum IC. The quantum IC may be either analog or digital and may be used in a number of applications within or associated with quantum systems, such as e.g. quantum processors, quantum amplifiers, quantum sensors, etc., depending on the components associated with the IC. The IC may be employed as part of a chipset for executing one or more related functions in a quantum system.

Josephson Junctions fabricated using double-angle shadow evaporation

[0051] In order to highlight the advantages offered by novel quantum circuit assemblies fabricated using the air bridge/cantilever method proposed herein, it would be helpful to first explain how Josephson Junctions are fabricated using the double-angle shadow evaporation (also sometimes referred to as a "hanging resist" method) in conventional quantum circuits.

[0052] In summary, the name "double-angle shadow evaporation" reflects the fact that the method involves metal deposition, typically carried out by metal evaporation, at two different angles of incidence with respect to the substrate (hence, double-angle). The name further reflects the fact that metal deposition is performed through a hanging photoresist mask which casts a shadow on at least a part of the substrate, obscuring metal deposition on that part (hence, shadow evaporation/evaporation).

[0053] FIGS. 2A-2C provide a schematic illustration of one example of a photoresist mask 200 provided over a substrate 202 for fabricating Josephson Junctions using a double-angle shadow evaporation approach. Each of FIGS. 2A-2C provides a view of the same photoresist mask 200 over the substrate 202, but perspectives of these views are different. FIG. 2A provides a top down view (i.e. a view from a point above the substrate 202). FIG. 2B provides a cross-sectional view with a cross-section of the structure of FIG. 2A taken along a horizontal dashed line shown in FIG. 2A. Finally, FIG. 2C provides a cross-sectional view with a cross-section of the structure of FIG. 2A taken along a vertical dashed line shown in FIG. 2A. A legend provided within a dashed box at the bottom

of FIGS. 2A-2C illustrates patterns used to indicate different elements shown in FIGS. 2A-2C, so that the FIGs are not cluttered by many reference numerals.

[0054] Josephson Junctions may be created by a double-angle shadow evaporation approach using a two-layer photoresist mask 200 that includes a bottom photoresist layer 204 and a top photoresist layer 206 as shown in FIGS. 2A-2C. The bottom layer 204 is undercut from the top layer 206 in that some portions of the top layer 206 hang, or are suspended, over the bottom layer 204. The bottom layer 204 is undercut in such a manner that the top layer 206 of photoresist forms a suspended bridge 208, known as a Dolan bridge, over a section of the substrate 202. Ways for fabricating such undercuts in photoresist are well known in the art of photolithographic processing and, therefore, are not described here in detail.

[0055] In order to form a Josephson Junction, metals are then deposited through the photoresist mask 200 with the suspended bridge. Conventionally, this is done as illustrated in FIGS. 3A-3C.

[0056] Each of FIGS. 3A-3C illustrates a result of different subsequent fabrication steps. FIG. 3C provides two views of the same structure. The view on the right side of FIG. 3C is a top down view (i.e. a view similar to that shown in FIG. 2A). The view on the left side of FIG. 3C is a cross-sectional view with a cross-section of the structure of FIG. 3C taken along a horizontal dashed line shown in FIG. 3C (i.e. a view similar to that shown in FIG. 2B). Each of FIGS. 3A and 3B only provide a cross-sectional view similar to that of the left side of FIG. 3C but at an earlier fabrication step. Similar to FIGS. 2A-2C, a legend provided within a dashed box at the bottom of FIGS. 3A-3C illustrates patterns used in the figures to indicate different elements shown in FIGS. 3A-3C. Moreover, similar reference numerals in FIGS. 2A-2C and FIGS. 3A-3C are used to illustrate analogous elements in the figures. For example, reference numerals 202 and 302, shown, respectively, in FIGS. 2 and 3 refer to a substrate, reference numerals 204 and 304 - to a bottom mask layer, and so on. When provided with reference to one of the FIGS. 2A-2C and FIGS. 3A-3C, discussions of these elements are applicable to other figures, unless stated otherwise. Thus, in the interests of brevity, discussions of similar elements are not repeated for each of the figures but, rather, the differences between the figures are described.

[0057] As previously described herein, a Josephson Junction may include a thin layer of dielectric sandwiched between two layers of superconductors, the dielectric layer acting as the barrier in a superconducting tunnel junction. According to the double-angle shadow evaporation approach, such a device is conventionally fabricated by, first, depositing a layer of a first superconductor 310 on the substrate 302, as shown in FIG. 3A, through the two-layer mask such as e.g. the one shown in FIGS. 2A-2C. The first superconductor is deposited at an angle with respect to the substrate 302, as shown in FIG. 3A with an angle $\theta 1$. Slanted dotted-dashed lines in FIG. 3A illustrate the direction of

deposition of the first superconductor 310. A layer of the first superconductor 310 may have a thickness between e.g. about 10 and 200 nanometers (nm), e.g. between about 30 and 100 nm.

[0058] The first superconductor 310 forms a bottom (base) electrode of the future Josephson Junction. A layer of insulator 311 (also referred to herein as a "dielectric layer 311" or a "dielectric 311"), shown in FIGs. 3B and 3C, is then provided over the first superconductor 310 to form a tunnel barrier of the future Josephson Junction. The tunnel barrier is formed by oxidizing the first superconductor 310, thus creating a layer of first superconductor oxide on its surface. Such an oxide may have a thickness between e.g. about 1 and 5 nm, typically for qubit applications between about 1 and 2 nm.

[0059] The fact that the choice of a tunnel barrier in a double-angle shadow evaporation method is constrained to an oxide of the base electrode superconductor limits the choice of the superconductor used as the first superconductor 310 in that the superconductor must be such that a controlled layer of oxide may be created on it. In practice, aluminum oxide is the only controlled oxide that may be formed from a metal. Therefore, currently aluminum is the only superconducting metal that is used for the base electrode of Josephson Junctions fabricated using the double-angle shadow evaporation technique.

[0060] After the layer of dielectric 311 is provided on the first superconductor 310, a second superconductor 312 is deposited through the mask but at a different angle with respect to the substrate 302 than θ1. FIG. 3B illustrates the second angle as an angle θ2 and slanted dotted-dashed lines in FIG. 3B illustrate the direction of deposition of the second superconductor 312. In some embodiments, the first and the second superconductors 310, 312 are deposited at the opposite angles, if measured with respect to a normal to the substrate 302. Conventionally, the second superconductor 320 is aluminum because the first superconductor must be aluminum, as described above. A layer of the second superconductor 312 may have a thickness between e.g. about 10 and 200 nm, typically between about 30 and 100 nm. The second superconductor 312 forms a counter electrode (i.e. counter to the bottom electrode formed by the first superconductor 310) of the future Josephson Junction, typically referred to as a "top" electrode.

[0061] The first and second superconductors 310, 312 are usually deposited using a non-conformal process, such as e.g. evaporative deposition. After deposition of the second superconductor 312, the deposition mask is removed, removing with it any first and/or second superconductor 310, 312 deposited on top of it.

[0062] In general, the above-described process of creating patterned structures of one or more target materials (in this case, structures made of the first and second superconductors 310, 312) on the surface of a substrate using a sacrificial material such as photoresist is referred to as a lift-off

method. Lift-off is a type of an additive technique, as opposed to subtracting techniques like etching, and may be applied in cases where a direct etching of structural material would have undesirable effects on one or more layers below.

[0063] After the deposition mask is removed, the resulting Josephson Junction is left on the substrate 302 as shown in FIG. 3C as a Josephson Junction 314. The Josephson Junction 314 is formed by the small region of overlap under the photoresist bridge 308 (i.e. the area under the bridge 308 where the first superconductor 310, covered with a layer of a thin insulating material is overlapped by the second superconductor 312). Dimensions of the Josephson Junction 314 along x-axis and y-axis, shown in FIG. 3C as d_x and d_y, respectively, are typically between about 50 and 1000 nm for any of d_x and d_y.

[0064] As a result of performing the double-angle shadow evaporation as described above, junctions of the first and second superconductors may also form on each side of the Josephson Junction 314, such junctions shown in FIGS. 3B and 3C as junctions 316. However, because these junctions are of much larger dimensions than the Josephson Junction 314, e.g. measured several thousands of nm in the x-direction and hundreds of nm or more in the y-direction, they are essentially infinite for the Josephson effect to take place and, therefore, act as superconductors rather than Josephson Junctions.

[0065] One problem with the fabrication approach described above is that it includes steps which are not suitable for manufacturing on the larger wafer sizes used in the semiconductor industry. For example, angled metal deposition step does not produce a uniform film across the wafer and would prohibit uniform qubit performance across large area. Moreover, the fabrication approach described above relies on lift-off of metal films to produce wires remaining on the wafer. The lift-off technique is not amenable to the chemical waste systems of wafer cleaning tools and would not facilitate high volume manufacturing or even an extension to many qubits on a single wafer.

[0066] Another problem with the double-angle shadow evaporation approach is that the resulting Josephson Junction is surrounded by dielectric material on several sides. For example, as shown on the left side (i.e. cross-section) view of FIG. 3C indicating the boundaries of the Josephson Junction 314 with vertical dashed lines, the dielectric 311 that forms the tunnel barrier of the Josephson Junction 314 extends further, outside of the boundaries of the Josephson Junction 314, e.g. into the area 318 immediately adjacent to the Josephson Junction, because the dielectric 311 is provided across the entire bottom superconductor 310. The right side (i.e. top) view of FIG. 3C illustrates that the dielectric material 311 surrounds the Josephson Junction 314 on three of the four sides. As described above, one major source of loss, and thus decoherence in superconducting qubits are spurious TLS's, e.g. those caused by defects in the areas surrounding Josephson Junctions.

Dielectrics surrounding the tunnel barriers and superconductors of Josephson Junctions, such as e.g. the dielectric portions 318 shown in FIG. 3C, may be one of the causes of spurious TLS's, leading to qubit decoherence.

[0067] Yet another problem with the use of the double-angle shadow evaporation approach is that it limits materials which may be employed in forming Josephson Junctions. As described above, Josephson Junctions fabricated the double-angle shadow evaporation approach can only use Al as the superconductor for the base electrode. This may be problematic because interconnects in quantum circuits are typically made from other superconducting materials such as e.g. Nb, TiN and NbTiN and interfaces between the different superconducting materials used for Josephson Junctions and interconnects connected thereto present yet another source of losses. Any losses are especially significant in context of quantum circuits where, sometimes, energy as small as that of a single photon is to be transmitted, making loss tolerance very low.

[0068] An air bridge/cantilever method disclosed herein may improve on at least some of the problems described above.

Josephson Junctions fabricated using an air bridge or cantilever

[0069] FIG. 4 provides a flow chart of an air bridge/cantilever method 400 for fabricating Josephson Junctions for quantum circuit assemblies, according to some embodiments of the present disclosure.

[0070] Although the operations of the method 400 are illustrated in FIG. 4 once each and in a particular order, the operations may be performed in any suitable order and repeated as desired. For example, one or more operations may be performed in parallel to manufacture multiple quantum circuit assemblies as described herein substantially simultaneously. In another example, the operations may be performed in a different order to reflect the architecture of a particular quantum circuit component in which one or more quantum circuit assemblies with Josephson Junctions fabricated according to the air bridge/cantilever method are to be included.

[0071] In addition, the exemplary manufacturing method 400 may include other operations not specifically shown in FIG. 4, such as e.g. various cleaning or planarization operations as known in the art. For example, in some embodiments, the substrate may be cleaned prior to or/and after any of the processes of the method 400 described herein, e.g. to remove surface-bound organic and metallic contaminants, as well as subsurface contamination. In some embodiments, cleaning may be carried out using e.g. a chemical solutions (such as peroxide), and/or with ultraviolet (UV) radiation combined with ozone, and/or oxidizing the surface (e.g., using thermal oxidation) then removing the oxide (e.g. using hydrofluoric acid (HF)). In another examples, the structures/assemblies described herein may be planarized prior to or/and after any of the processes of the method 400 described herein, e.g. to remove overburden or excess materials. In some embodiments, planarization may be

carried out using either wet or dry planarization processes, e.g. planarization be a chemical mechanical planarization (CMP), which may be understood as a process that utilizes a polishing surface, an abrasive and a slurry to remove the overburden and planarize the surface.

[0072] Various operations of the method 400 may be illustrated with reference to exemplary embodiments shown in FIGS. 5A-5F, but the method 400 may be used to manufacture any suitable quantum circuit assemblies with Josephson Junctions according to any embodiments of the present disclosure. FIGS. 5A-5F are cross-sections illustrating various example stages in the manufacture of a quantum circuit assembly using the air bridge/cantilever method of FIG. 4 in accordance with some embodiments of the present disclosure. Each one of FIGS. 5A-5F illustrates a top down view (top left illustration in each of FIGS. 5A-5F) of the x-y plane of the coordinate system indicated in these FIGS., a first cross-sectional view (bottom left illustration in each of FIGS. 5A-5F) along the z-y plane, and a second cross-sectional view (top right illustration in each of FIGS. 5A-5F) along the x-z plane. Thus, the top down view shown in FIGS. 5A-5F is the view looking down from a plane indicted in FIG. 5A as a plane AA, the first cross-sectional view is a cross-section along a plane indicted in FIG. 5A as a plane BB, and the second cross-sectional view is a cross-section along a plane indicted in FIG. 5A as a plane CC. In FIGS. 5A-5F, same reference numerals refer to the same or analogous elements/materials shown.

[0073] The method 400 may begin with providing, over a substrate, a layer of an electrically conductive material shaped to form a first/bottom electrode lead for the future Josephson Junction (process 402 shown in FIG. 4, a result of which is illustrated with an assembly 502 shown in FIG. 5A). The assembly 502 illustrates a substrate 522, which could be any of the substrates described above, with a first/bottom electrode lead 524 provided over the substrate.

[0074] In various embodiments, the electrically conductive material forming the bottom electrode lead provided in the process 402 may include any conducting or superconducting material suitable for providing electrical connectivity in a quantum circuit, such as e.g. Al, Nb, NbN, NbTiN, TiN, MoRe, etc., or any alloy of two or more superconducting/conducting materials, and a thickness of the bottom electrode lead (i.e. a dimension measured along the z-axis of the coordinate system as shown in FIGS. 5A-5F) provided in the process 402 may be between about 50 and 500 nanometers, including all values and ranges therein, e.g. between about 100 and 250 nm.

[0075] In various embodiments, any suitable deposition and patterning techniques may be used for providing the bottom electrode lead 524 in the process 402. Examples of deposition techniques for depositing a layer of an electrically conductive material for forming the bottom electrode lead 524 include atomic layer deposition (ALD), physical vapor deposition (PVD) (e.g. evaporative deposition, magnetron sputtering, or e-beam deposition), chemical vapor deposition (CVD), or electroplating.

Examples of patterning techniques include photolithographic or electron-beam (e-beam) patterning, possibly in conjunction with a dry etch, such as e.g. radio frequency (RF) reactive ion etch (RIE) or inductively coupled plasma (ICP) RIE, to pattern the layer of an electrically conductive material into the bottom electrode lead 524 of the specified geometries for a given implementation.

[0076] The method may then proceed with providing an air bridge or a cantilever of an electrically conductive material over the bottom electrode lead 524 (process 404 shown in FIG. 4, a result of which is illustrated with an assembly 504 shown in FIG. 5B). The assembly 504, as well as the subsequent assemblies shown in FIGS. 5A-5F, illustrates an example of an air bridge 526 formed over a portion of the bottom electrode lead 524. However, illustrations of FIGS. 5A-5F are equally applicable to cantilevers, e.g. a cantilever which would be formed if, looking from the left to the right in the top and first cross-sectional views of FIG. 5B, the air bridge 526 shown there would end at a dashed line 525 (i.e. if there electrically conductive material of the "air bridge" 526 would not be shown to the right of the dashed line 525). Therefore, in the following, the air bridge 526 shown in FIG. 5B and subsequent FIGS. is referred to as an air bridge/cantilever 526.

[0077] In various embodiments, the electrically conductive material forming the air bridge/cantilever 526 provided in the process 404 may include any conducting or superconducting material suitable for providing electrical connectivity in a quantum circuit, such as e.g. any of such materials described above, and may be the same or different from the electrically conductive material of the bottom electrode lead 524. The reason why the air bridge/cantilever 526 is to be formed from an electrically conductive material is because later on the air bridge/cantilever 526 will serve as a top electrode lead for the Josepshon Junction.

[0078] Providing the air bridge/cantilever 526 in the process 404 creates a region 527, indicated in FIG. 5B, above the bottom electrode lead 524, which region may be seen as a partial cavity around the bottom electrode lead 524 where a portion of the air bridge/cantilever 526 is suspended above a portion of the bottom electrode lead 524. In some embodiments, a distance between the suspended portion of the air bridge/cantilever 526 and the bottom electrode lead 524 (i.e. a dimension measured along the z-axis of the coordinate system as shown in FIGS. 5A-5F and indicated in FIG. 5B as a distance "d1") may be between about 50 and 50000 nm, including all values and ranges therein, e.g. between about 100 and 1000 nm, or between about 300 and 500 nm.

[0079] As shown in FIG. 5B, if the bottom electrode lead 524 is provided in a first plane that is substantially parallel to the plane of the substrate 522, then the suspended portion of the air bridge/cantilever 526 which will later form the top electrode lead for the Josephson Junction is provided in a second plane that is substantially parallel to the plane of the substrate 522, the second plane being further away from the substrate than the first plane. If the suspended portion is then

projected onto the first plane (i.e. the plane of the bottom electrode lead 524), then the bottom electrode lead 524 would be perpendicular to the projection of the suspended portion, in some embodiments of the present disclosure. In other embodiments, the suspended portion of the air bridge/cantilever 526 does not have to be perpendicular to the bottom electrode lead 524, as long as the suspended portion extends sufficiently over the bottom electrode lead 524 to form an opening over the bottom electrode lead 524 in a later fabrication process (namely, in a process 406 of the method 400 shown in FIG. 4). Formation of such an opening will also influence various dimensions of the air bridge/cantilever 526 provided in the process 404. Thus, the air bridge/cantilever 526 provided in the process 404 can be of any dimensions suitable for supporting the opening formed in the process 406, e.g. suitable in terms of having sufficient mechanical stability to remain suspended over the bottom electrode lead 524 during subsequent fabrication processes and, later on, during operation of the assembly. Some such dimensions for the air bridge/cantilever 526 will be described below, together with the dimensions of the opening formed in the process 406.

[0080] In various embodiments, any suitable deposition and patterning techniques may be used for providing the air bridge/cantilever 526 in the process 404, such as e.g. techniques which rely on use of a sacrificial material in order to form the region 527 around the bottom electrode lead 524. One example of such a technique could be to use a sacrificial material to form a structure around the bottom electrode lead 524 of the shape, dimensions, and location of the region 527, then deposit the electrically conductive material of the air bridge/cantilever 526, and then remove the sacrificial material, e.g. by etching, thus creating an open region 527 around the bottom electrode lead 524 as shown in FIG. 5B. In such a technique, the sacrificial material would need to have sufficient etch selectivity with respect to the other materials around, such as e.g. materials of the substrate 522, of the bottom electrode lead 524, or of the air bridge/cantilever 526, so that etching of the sacrificial structure would not substantially etch these other materials. As known in the art, two materials are said to have "sufficient etch selectivity" when etchants used to etch one material do not substantially etch the other, enabling selective etching of one material but not the other. In some embodiments, the sacrificial material which may be used to form the region 527 may be a sacrificial dielectric material, such as e.g. a dielectric material including, or being, one or more of a silicon oxide (i.e. a compound comprising silicon and oxygen, e.g. SiO_2), a hafnium oxide (i.e. a compound comprising hafnium and oxygen, e.g. HfO_2), a silicon nitride (i.e. a compound comprising silicon and nitrogen, e.g. SiN), a silicon oxynitride (i.e. a compound comprising silicon, oxygen, and nitrogen, e.g. SiON), an aluminum oxide (i.e. a compound comprising aluminum and oxygen, e.g. Al_2O_3), an aluminum hafnium oxide (i.e. a compound comprising aluminum, hafnium, and oxygen, e.g. AlHfO),

a carbon-doped oxide (i.e. a compound comprising carbon and oxygen), organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. Besides appropriate etching characteristics, some other considerations in selecting a suitable material for forming the sacrificial structure may include e.g. possibilities of smooth film formation, low shrinkage and outgassing, and good dielectric properties (such as e.g. low electrical leakage, suitable value of a dielectric constant, and thermal stability).

[0081] In other embodiments, other suitable techniques may be used for providing the air bridge/cantilever 526 in the process 404, all of which being within the scope of the present disclosure.

[0082] The method 400 may then continue with providing an opening in the suspended portion of the air bridge/cantilever in an area that is above the bottom electrode lead for the future Josephson Junction (process 406 shown in FIG. 4, a result of which is illustrated with an assembly 506 shown in FIG. 5C). The assembly 506 illustrates an opening 529 in the suspended portion of the air bridge/cantilever 526 in an area that is above the bottom electrode lead 524. While the opening 529 is shown in FIG. 5C as a square opening, other shapes may be used in other embodiments, e.g. the opening 529 may be substantially circular, oval, polygonal, or irregularly shaped . In some embodiments, the area of the opening 529 (i.e. a dimension measured in the x-y plane of the coordinate system as shown in FIGS. 5A-5F) may be between about 100 and 5,000,000 nm^2, including all values and ranges therein, e.g. between about 500 and 100,000 nm^2, or between about 10,000 and 25000 nm^2. Bottom and top electrodes of the future Josephson Junction will be provided via the opening 529, and, therefore, dimensions of the opening 529 should be small enough so that the Josephson Junction formed using the opening would exhibit the Josephson effect and not merely act as a superconductor, as was described above with reference to the junctions 316 shown in FIG. 3C.

[0083] As described above, dimensions of the air bridge/cantilever 526 should be able to support formation of the opening 529 in the process 406. For example, in some embodiments, a width of the air bridge/cantilever 526 (i.e. a dimension measured along the x-axis of the coordinate system as shown in FIGS. 5A-5F and indicated in FIG. 5C as a distance "d2") may be at least about 1.2 times greater than the width of the opening 529 (measured in the in the same dimension as that of the air bridge/cantilever 526), e.g. at least about 2 times greater, or at least about 3 times greater. In another example, in some embodiments, a length of the suspended portion of the air bridge/cantilever 526 (i.e. a dimension measured along the y-axis of the coordinate system as shown in FIGS. 5A-5F and indicated in FIG. 5C as a distance "d3") may be at least about 2 times greater than

analogous dimension of the opening 529 (i.e. also measured along the y-axis), e.g. at least about 2.5 times greater, or at least about 3 times greater. In yet another example, in some embodiments, a thickness of the suspended portion of the air bridge/cantilever 526 (i.e. a dimension measured along the z-axis of the coordinate system as shown in FIGS. 5A-5F and indicated in FIG. 5C as a distance "d4") may be between about 10 and 2000 nm, including all values and ranges therein, e.g. between about 50 and 1000 nm, or between about 100 and 500 nm.

[0084] In various embodiments, any suitable techniques may be used for providing the opening 529 in the process 406, such as e.g. reactive ion etching.

[0085] As is seen in FIG. 5C, formation of the opening 529 results in exposing a portion 531 of the bottom electrode lead 524 underneath the suspended portion of the air bridge/cantilever 526. The method 400 may then proceed with depositing an electrically conductive, preferably superconductive, material through the opening to form a first/bottom electrode of the future Josephson Junction (process 406 shown in FIG. 4, a result of which is illustrated with an assembly 508 shown in FIG. 5D). The assembly 508 illustrates an electrically conductive material 528 deposited over the air bridge/cantilever 526, where, because of the opening 529, some of the material 528 is deposited on the exposed area 531 of the bottom electrode lead 524, thus forming a bottom electrode 533 of the future Josephson Junction.

[0086] In some embodiments, a thickness of the first electrode 533 (i.e. a dimension measured along the z-axis of the coordinate system as shown in FIGS. 5A-5F and indicated in FIG. 5D as a distance "d5") may be between about 10 and 2000 nm, including all values and ranges therein, e.g. between about 50 and 1000 nm, or between about 100 and 500 nm. In some embodiments, an area of the bottom electrode 533 may be smaller than the area of the opening 529, e.g. between about 1 and 50 % smaller, including all values and ranges therein, e.g. between about 5 and 30 % smaller, or between about 10 and 20 % smaller.

[0087] In various embodiments, the electrically conductive material 528 forming the bottom electrode 533 provided in the process 408 may include any conducting or superconducting material suitable for providing electrical connectivity in a quantum circuit, such as e.g. any of such materials described above, and may be the same or different from the electrically conductive materials of the bottom electrode lead 524 or/and the air bridge/cantilever 526. Any suitable deposition techniques, possibly in combination with patterning, may be used for providing the electrically conductive material 528 forming the bottom electrode 533 in the process 408, such as e.g. those described above.

[0088] Next, the method 400 may include providing, over the bottom electrode, a layer of a material that can serve as a tunnel barrier of the future Josephson Junction (process 410 shown in

FIG. 4, a result of which is illustrated with an assembly 510 shown in FIG. 5E). One way to provide such a tunnel barrier material is to oxidize the conductive material 528 of the bottom electrode 533, and this is what is schematically illustrated in the assembly 510 showing a tunnel barrier material 530 in a form of a layer of oxide formed in the exposed portions of the conductive material 528, including on the sidewalls, of the bottom electrode 533. For example, the bottom electrode 533 could be made from Al and the tunnel barrier material 530 would then be an oxide of Al. However, in other embodiments, a tunnel barrier material, which could be either a dielectric or a semiconductor material, may be deposited over the bottom electrode 533 through the opening 529. In such other embodiments, depending on the nature of the tunnel barrier material 530 and depending on the deposition technique used to provide the tunnel barrier material 530, such a material may or may not be present on the sidewalls of the bottom electrode 533 as shown in FIG. 5E, all of which embodiments are within the scope of the present disclosure.

[0089] In various embodiments, the tunnel barrier material 530 could be selected as any dielectric material of sufficiently high quality (i.e. low losses in terms of spurious TLS's), such as e.g. silicon oxide, hafnium oxide, or aluminum oxide. In some embodiments, the tunnel barrier material 530 may include an oxide deposited over the bottom electrode 533 using e.g. CVD or/and plasma-enhanced CVD (PECVD). In still other embodiments, the tunnel barrier material 530 may include a dielectric material formed over the bottom electrode 533 using coating techniques involving cross-linking of liquid precursors into solid dielectric materials. In some embodiments, the surface of the bottom electrode 533 may be cleaned or treated prior to applying the dielectric to reduce surface contamination and minimize interface traps and/or promote adhesion, for example using chemical or plasma clean, or applying heat in a controlled environment. In some embodiments, an "interface layer" may be provided between the bottom electrode 533 and the tunnel barrier material 530 deposited thereon to prevent, decrease, or minimize spontaneous and uncontrolled formation of other interfacial layers. In some embodiments, an adhesion promoter or adhesion layer may be applied prior to deposition of the tunnel barrier material 530.

[0090] When the tunnel barrier material 530 is formed as an oxide of the conductive material 528, the process 410 may include performing a controlled oxidation process to oxidize a layer at the exposed upper, and possibly sidewall, surface(s) of the conductive material 528. In some embodiments, such a layer of oxide 530 may be provided as a two-step process. In the first step, inferior-quality surface oxide may be removed (i.e. surface oxide which may have formed on the conductive material 528 spontaneously, i.e. uncontrollably, in previous steps and/or exposure to ambient conditions), e.g. using a light sputtering step such as e.g. argon (Ar) sputtering. In the second step which follows the first step, high quality surface oxide of controlled thickness and

quality is grown with a controlled oxidation step in substantially pure oxygen, e.g. 1-10 minutes in substantially pure oxygen at a pressure of about .1 – 1 millibar, where the exact time and pressure may be selected so as to set the oxide thickness and quality of the oxide and thus the desired resistance of the Josephson Junction, in conjunction with its area, and thereby set the frequency of the qubit, in conjunction with the charging energy Ec and the Josephson energy Ej for the particular qubit design.

[0091] FIG. 5E further illustrates that, in some embodiments, the tunnel barrier material 530 may be provided not only over the bottom electrode 533, but also over the suspended portion of the air bridge/cantilever 526. In other embodiments, extent of the tunnel barrier material 530 in areas other than the bottom electrode 530 may be different than what is shown in FIG. 5E, e.g. deposition of the tunnel barrier material 530 in areas where it does not serve the purpose of acting as a tunnel barrier of a Josephson Junction may be reduced or eliminated, e.g. using an appropriate mask or removing the tunnel barrier material 530 from such areas.

[0092] A portion of the tunnel barrier material 530 provided over the upper surface of the bottom electrode 533 forms a tunnel barrier 535, indicated in FIG. 5E, of the future Josephson Junction. In various embodiments, a thickness of the tunnel barrier material 530 over the bottom electrode 533 (i.e. a dimension measured along the z-axis of the coordinate system as shown in FIGS. 5A-5F and indicated in FIG. 5E as a distance "d6") may be between about 1 and 8 nm, including all values and ranges therein, e.g. between about 1 and 4 nm, or between about 1 and 2 nm.

[0093] The method 400 may conclude with depositing an electrically conductive, preferably superconductive, material over the tunnel barrier material through the opening 529 (which may be decreased in dimensions somewhat due to deposition of the electrically conductive material 528 and/or of the tunnel barrier material 530) to form a second/top electrode of the future Josephson Junction (process 412 shown in FIG. 4, a result of which is illustrated with an assembly 512 shown in FIG. 5F). The assembly 512 illustrates an electrically conductive material 532 deposited over the tunnel barrier material 530 and filling up the opening 529. The assembly 512 also illustrates that some of the material 532 may be deposited over the air bridge/cantilever 526, although in other embodiments extent of the conductive material 532 in areas other than above the bottom electrode 533 may be different from what is shown in FIG. 5F. A portion of the conductive material 532 deposited over the bottom electrode 533 forms a top electrode 537, indicated in FIG. 5F, of the Josephson Junction.

[0094] In various embodiments, the electrically conductive material 532 forming the top electrode 537 provided in the process 412 may include any conducting or superconducting material suitable for providing electrical connectivity in a quantum circuit, such as e.g. any of such materials described

above, and may be the same or different from the electrically conductive materials of the bottom electrode lead 524, the air bridge/cantilever 526, and/or the electrically conductive material 528 forming the bottom electrode 533. Any suitable deposition techniques, possibly in combination with patterning, may be used for providing the electrically conductive material 532 forming the top electrode 537 in the process 412, such as e.g. those described above.

[0095] After the process 412, the resulting Josephson Junction is left over the bottom electrode lead 524 as shown in FIG. 5F as a Josephson Junction 514. The Josephson Junction 514 is formed by the small region within the perimeter of the opening 529 where the bottom electrode 533 and the top electrode 537 sandwich the tunnel barrier 535 between them. In various embodiments, each of the dimensions of the Josephson Junction 514 along x-axis and y-axis shown in FIG. 5F may be between about 50 and 1000 nm.

[0096] As a result of performing the air bridge/cantilever method as described above, junctions of the first and second electrically conductive/superconductive materials 528 and 532 may also form over the air bridge/cantilever 526, such junctions shown in FIG. 5F as junctions 516. However, because these junctions are of much larger dimensions than the Josephson Junction 514, e.g. measured hundreds of nm or more in each of the x- and the y-directions, they are essentially infinite for the Josephson effect to take place and, therefore, act as superconductors rather than Josephson Junctions.

[0097] Characteristic and indicative of the use of the air bridge/cantilever method described above is the fact that the sidewalls of Josephson Junction 514, e.g. the sidewalls of the bottom electrode 533 and of the top electrode 537, with zero or more further layers provided thereon (e.g. on the sidewalls of the bottom electrode 533 a layer of the tunnel barrier material 530 may be present), in particular one or more such sidewalls which are underneath the suspended portion of the air bridge/cantilever 526 and are underneath the opening 529, may be surrounded by vacuum in some implementations, since fabrication and operation of the quantum systems is typically carried out under vacuum. In this context, it is understood that "vacuum" is an idealized term in that a perfect vacuum (i.e. zero pressure) can never be achieved in practical situations. Therefore, the term "vacuum" is used to cover non-zero pressures as long as they are sufficiently low to be considered nearly vacuum. In other implementations, the gap or open space of the region 527 remaining after the Josephson Junction 514 is formed could contain air or any other gas or a mixture of gasses. Whether vacuum or a combination of gasses, in contrast to Josephson Junctions fabricated using the double-angle shadow evaporation method as described above, amount of the potentially lossy dielectric material surrounding the Josephson Junction 514 may be reduced, which may advantageously reduce the amount of spurious TLS's and improve coherence time of a qubit with

such a Josephson Junction. In other words, the proposed method may enable fabricating high performance Josephson Junctions, compared to those fabricated using existing techniques. In addition, the proposed method can be efficiently used in large-scale manufacturing, providing a substantial improvement with respect to conventional approaches, such as e.g. the double-angle shadow evaporation method, which, as described above, includes fabrications steps that are not suitable for implementing with larger wafer sizes used by device manufacturers. Yet another advantage of the proposed method is the ability to use a larger selection of conductive/superconductive materials to form the first and second electrodes of Josephson Junctions, which may reduce losses due to interfaces with materials used to form interconnects in quantum circuits.

[0098] To summarize, as a result of performing the air bridge/cantilever method as described above, a Josephson Junction such as the Josephson Junction 514 shown in FIG. 5F, or a similar Josephson Junction according to embodiments not specifically shown in FIG. 5F but described above, may be formed. The bottom electrode 533 of the Josephson Junction 514 may be directly electrically connected to the bottom electrode lead 524, and the top electrode 537 may be connected to the air bridge/cantilever 526, via the large-size junctions 516, where the air bridge/cantilever 526 acts as the top electrode lead for the Josephson Junction 514. Such a top electrode lead based on the air bridge/cantilever 526 includes a suspended portion (e.g. of dimensions as described with reference to FIG. 5C), where the suspended portion is a portion that forms a bridge or a cantilever over the first electrode lead 524. In particular, at least a portion of the suspended portion, e.g. a portion 539 indicated in FIG. 5F, may be suspended over a portion of the substrate 522, indicated in FIG. 5F as a portion 541, immediately adjacent to (i.e. extending from) a portion of the substrate, indicated in FIG. 5F as a portion 543, over which the first electrode lead 524 is provided. The opening 529 in the air bridge/cantilever 526 above the Josephson Junction 514 may be filled with the material 532 of the top electrode 537, as shown in FIG. 5F, and the sidewalls of the Josephson Junction 514, possibly with one or more thin layers thereon, may be open to vacuum or a mixture of gasses in regions 545 indicated in FIG. 5F.

[0099] In various embodiments, Josephson Junctions as described herein, e.g. the Josephson Junction 514, could be a part of a superconducting qubit, e.g. a part of a charge qubit, in particular a part of a transmon, or a part of a flux qubit. In some embodiments, the Josephson Junction 514 could be a part of a SQUID, where the second Josephson Junction of such a SQUID is not shown in FIGS. 5A-5F but could be fabricated using analogous processes using the air bridge/cantilever method 400 described above, e.g. at the same time with the Josephson Junction 514.

Exemplary qubit devices

[0100] Quantum circuit assemblies/structures with Josephson Junctions as described above may be included in any kind of qubit devices or quantum processing devices/structures. Some examples of such devices/structures are illustrated in FIGS. 6A-6B, 7, and 8.

[0101] FIGS. 6A-6B are top views of a wafer 1100 and dies 1102 that may be formed from the wafer 1100, according to some embodiments of the present disclosure. The dies 1102 may include any of the quantum circuits disclosed herein, e.g., the quantum circuit 100, may include any of the quantum circuit assemblies described herein, such as e.g. the quantum circuit assembly 512, or any further embodiments of such an assembly as described herein, and may include one or more Josephson Junctions fabricated using the air bridge/cantilever method described herein. The wafer 1100 may include semiconductor material and may include one or more dies 1102 having conventional and quantum circuit device elements formed on a surface of the wafer 1100. Each of the dies 1102 may be a repeating unit of a semiconductor product that includes any suitable conventional and/or quantum circuit qubit device. After the fabrication of the semiconductor product is complete, the wafer 1100 may undergo a singulation process in which each of the dies 1102 is separated from one another to provide discrete "chips" of the semiconductor product. A die 1102 may include one or more quantum circuits 100, including any Josephson Junctions fabricated using the air bridge/cantilever method described herein, as well as any other IC components. In some embodiments, the wafer 1100 or the die 1102 may include a memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 1102. For example, a memory array formed by multiple memory devices may be formed on a same die 1102 as a processing device (e.g., the processing device 2002 of FIG. 8) or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array.

[0102] FIG. 7 is a cross-sectional side view of a device assembly 1200 that may include any of the embodiments of the quantum circuit assemblies disclosed herein. The device assembly 1200 includes a number of components disposed on a circuit board 1202. The device assembly 1200 may include components disposed on a first face 1240 of the circuit board 1202 and an opposing second face 1242 of the circuit board 1202; generally, components may be disposed on one or both faces 1240 and 1242.

[0103] In some embodiments, the circuit board 1202 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired

circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 1202. Signal transfer between components or layer may happen with both low resistance DC connections or by either in-plane or out-of-plane capacitive connections. In other embodiments, the circuit board 1202 may be a package substrate or flexible board.

[0104] The IC device assembly 1200 illustrated in FIG. 7 may include a package-on-interposer structure 1236 coupled to the first face 1240 of the circuit board 1202 by coupling components 1216. The coupling components 1216 may electrically and mechanically couple the package-on-interposer structure 1236 to the circuit board 1202, and may include solder balls (as shown in FIG. 7), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure. The coupling components 1216 may include other forms of electrical connections that may have no mechanical contact, such as parallel plate capacitors or inductors, which can allow high-frequency connection between components without mechanical or DC connections.

[0105] The package-on-interposer structure 1236 may include a package 1220 coupled to an interposer 1204 by coupling components 1218. The coupling components 1218 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 1216. Although a single package 1220 is shown in FIG. 7, multiple packages may be coupled to the interposer 1204; indeed, additional interposers may be coupled to the interposer 1204. The interposer 1204 may provide an intervening substrate used to bridge the circuit board 1202 and the package 1220. The package 1220 may be a quantum circuit device package as described herein, e.g. a package including any of the quantum circuits disclosed herein, e.g., the quantum circuit 100, may include any of the quantum circuit assemblies described herein, such as e.g. the quantum circuit assembly 512, or any further embodiments of such an assembly as described herein, and may include one or more Josephson Junctions fabricated using the air bridge/cantilever method described herein, or may be a conventional IC package, for example. Generally, the interposer 1204 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 1204 may couple the package 1220 (e.g., a die) to a ball grid array (BGA) of the coupling components 1216 for coupling to the circuit board 1202. In the embodiment illustrated in FIG. 7, the package 1220 and the circuit board 1202 are attached to opposing sides of the interposer 1204; in other embodiments, the package 1220 and the circuit board 1202 may be attached to a same side of the interposer 1204. In some embodiments, three or more components may be interconnected by way of the interposer 1204.

[0106] The interposer 1204 may be formed of a crystalline material, such as silicon, germanium, or other semiconductors, an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some embodiments, the interposer 1204 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 1204 may include metal interconnects 1210 and vias 1208, including but not limited to through-silicon vias (TSVs) 1206. The interposer 1204 may further include embedded devices 1214, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as RF devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 1204. The package-on-interposer structure 1236 may take the form of any of the package-on-interposer structures known in the art.

[0107] The device assembly 1200 may include a package 1224 coupled to the first face 1240 of the circuit board 1202 by coupling components 1222. The coupling components 1222 may take the form of any of the embodiments discussed above with reference to the coupling components 1216, and the package 1224 may take the form of any of the embodiments discussed above with reference to the package 1220. The package 1224 may be a package including one or more quantum circuits with Josephson Junctions fabricated using the air bridge/cantilever method as described herein, or may be a conventional IC package, for example. In some embodiments, the package 1224 may take the form of any of the embodiments of the quantum circuit 100 with any of the quantum circuit assemblies described herein.

[0108] The device assembly 1200 illustrated in FIG. 7 includes a package-on-package structure 1234 coupled to the second face 1242 of the circuit board 1202 by coupling components 1228. The package-on-package structure 1234 may include a package 1226 and a package 1232 coupled together by coupling components 1230 such that the package 1226 is disposed between the circuit board 1202 and the package 1232. The coupling components 1228 and 1230 may take the form of any of the embodiments of the coupling components 1216 discussed above, and the packages 1226 and 1232 may take the form of any of the embodiments of the package 1220 discussed above. Each of the packages 1226 and 1232 may be a qubit device package as described herein or may be a conventional IC package, for example. In some embodiments, one or both of the packages 1226 and 1232 may take the form of any of the embodiments of the quantum circuit 100 with any of the quantum circuit assemblies described herein, or a combination thereof.

[0109] FIG. 8 is a block diagram of an exemplary quantum computing device 2000 that may include any of the quantum circuits with any of the quantum circuit assemblies disclosed herein. A number of components are illustrated in FIG. 8 as included in the quantum computing device 2000, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the quantum computing device 2000 may be attached to one or more PCBs (e.g., a motherboard), and may be included in, or include, any of the quantum circuits with any of the quantum circuit assemblies described herein. In some embodiments, various ones of these components may be fabricated onto a single system-on-a-chip (SoC) die. Additionally, in various embodiments, the quantum computing device 2000 may not include one or more of the components illustrated in FIG. 8, but the quantum computing device 2000 may include interface circuitry for coupling to the one or more components. For example, the quantum computing device 2000 may not include a display device 2006, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 2006 may be coupled. In another set of examples, the quantum computing device 2000 may not include an audio input device 2018 or an audio output device 2008, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 2018 or audio output device 2008 may be coupled. In further examples, the quantum computing device 2000 may include a microwave input device or a microwave output device (not specifically shown in FIG. 7), or may include microwave input or output device interface circuitry (e.g., connectors and supporting circuitry) to which a microwave input device or microwave output device may be coupled.

[0110] The quantum computing device 2000 may include a processing device 2002 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 2002 may include a quantum processing device 2026 (e.g., one or more quantum processing devices), and a non-quantum processing device 2028 (e.g., one or more non-quantum processing devices). The quantum processing device 2026 may include any of the quantum circuits disclosed herein, e.g., the quantum circuit 100, may include any of the quantum circuit assemblies described herein, such as e.g. the quantum circuit assembly 512, or any further embodiments of such an assembly as described herein, and may include one or more Josephson Junctions fabricated using the air bridge/cantilever method described herein, and may perform data processing by performing operations on the qubits that may be generated in the quantum circuits 100, and monitoring the result of those operations. For example, as discussed above, different

qubits may be allowed to interact, the quantum states of different qubits may be set or transformed, and the quantum states of different qubits may be read. The quantum processing device 2026 may be a universal quantum processor, or specialized quantum processor configured to run one or more particular quantum algorithms. In some embodiments, the quantum processing device 2026 may execute algorithms that are particularly suitable for quantum computers, such as cryptographic algorithms that utilize prime factorization, encryption/decryption, algorithms to optimize chemical reactions, algorithms to model protein folding, etc. The quantum processing device 2026 may also include support circuitry to support the processing capability of the quantum processing device 2026, such as input/output channels, multiplexers, signal mixers, quantum amplifiers, and analog-to-digital converters.

[0111] As noted above, the processing device 2002 may include a non-quantum processing device 2028. In some embodiments, the non-quantum processing device 2028 may provide peripheral logic to support the operation of the quantum processing device 2026. For example, the non-quantum processing device 2028 may control the performance of a read operation, control the performance of a write operation, control the clearing of quantum bits, etc. The non-quantum processing device 2028 may also perform conventional computing functions to supplement the computing functions provided by the quantum processing device 2026. For example, the non-quantum processing device 2028 may interface with one or more of the other components of the quantum computing device 2000 (e.g., the communication chip 2012 discussed below, the display device 2006 discussed below, etc.) in a conventional manner, and may serve as an interface between the quantum processing device 2026 and conventional components. The non-quantum processing device 2028 may include one or more digital signal processors (DSPs), application-specific ICs (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices.

[0112] The quantum computing device 2000 may include a memory 2004, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid-state memory, and/or a hard drive. In some embodiments, the states of qubits in the quantum processing device 2026 may be read and stored in the memory 2004. In some embodiments, the memory 2004 may include memory that shares a die with the non-quantum processing device 2028. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random access memory (STT-MRAM).

[0113] The quantum computing device 2000 may include a cooling apparatus 2024. The cooling apparatus 2024 may maintain the quantum processing device 2026, in particular the quantum circuits 100 as described herein, at a predetermined low temperature during operation to avoid qubit decoherence and to reduce the effects of scattering in the quantum processing device 2026. This predetermined low temperature may vary depending on the setting; in some embodiments, the temperature may be 5 degrees Kelvin or less. In some embodiments, the non-quantum processing device 2028 (and various other components of the quantum computing device 2000) may not be cooled by the cooling apparatus 2030, and may instead operate at room temperature. The cooling apparatus 2024 may be, for example, a dilution refrigerator, a helium-3 refrigerator, or a liquid helium refrigerator.

[0114] In some embodiments, the quantum computing device 2000 may include a communication chip 2012 (e.g., one or more communication chips). For example, the communication chip 2012 may be configured for managing wireless communications for the transfer of data to and from the quantum computing device 2000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0115] The communication chip 2012 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip 2012 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 2012 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 2012 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized

(EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 2012 may operate in accordance with other wireless protocols in other embodiments. The quantum computing device 2000 may include an antenna 2022 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0116] In some embodiments, the communication chip 2012 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 2012 may include multiple communication chips. For instance, a first communication chip 2012 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 2012 may be dedicated to longer-range wireless communications such as global positioning system (GPS), EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 2012 may be dedicated to wireless communications, and a second communication chip 2012 may be dedicated to wired communications.

[0117] The quantum computing device 2000 may include battery/power circuitry 2014. The battery/power circuitry 2014 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the quantum computing device 2000 to an energy source separate from the quantum computing device 2000 (e.g., AC line power).

[0118] The quantum computing device 2000 may include a display device 2006 (or corresponding interface circuitry, as discussed above). The display device 2006 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0119] The quantum computing device 2000 may include an audio output device 2008 (or corresponding interface circuitry, as discussed above). The audio output device 2008 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0120] The quantum computing device 2000 may include an audio input device 2018 (or corresponding interface circuitry, as discussed above). The audio input device 2018 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0121] The quantum computing device 2000 may include a GPS device 2016 (or corresponding interface circuitry, as discussed above). The GPS device 2016 may be in communication with a satellite-based system and may receive a location of the quantum computing device 2000, as known in the art.

[0122] The quantum computing device 2000 may include an other output device 2010 (or corresponding interface circuitry, as discussed above). Examples of the other output device 2010 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0123] The quantum computing device 2000 may include an other input device 2020 (or corresponding interface circuitry, as discussed above). Examples of the other input device 2020 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0124] The quantum computing device 2000, or a subset of its components, may have any appropriate form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device.

Select Examples

[0125] The following paragraphs provide examples of various ones of the embodiments disclosed herein.

[0126] Example 1 provides a quantum circuit assembly that includes a substrate; a first electrode lead provided over the substrate; a second electrode lead; and a Josephson Junction including a first electrode electrically connected to the first electrode lead and a second electrode electrically connected to the second electrode lead, where the second electrode lead includes a suspended portion, where the suspended portion is a portion that forms a bridge or a cantilever over the first electrode lead.

[0127] Example 2 provides the quantum circuit assembly according to Example 1, where at least a portion of the suspended portion is suspended over a portion of the substrate immediately adjacent to (i.e. extending from) a portion of the substrate over which the first electrode lead is provided.

[0128] Example 3 provides the quantum circuit assembly according to Examples 1 or 2, where a distance between the suspended portion and the first electrode lead is between about 50 and 50000 nm, including all values and ranges therein, e.g. between about 100 and 1000 nm, or between about 300 and 500 nm.

[0129] Example 4 provides the quantum circuit assembly according to any one of the preceding Examples, where the first electrode and the second electrode are separated by a layer of a dielectric material, e.g. a dielectric material including oxygen.

[0130] Example 5 provides the quantum circuit assembly according to Example 4, where sidewalls of the first electrode are covered with the layer of the dielectric material.

[0131] Example 6 provides the quantum circuit assembly according to Examples 4 or 5, where the dielectric material comprises a material of the first electrode and oxygen, e.g. the dielectric material is an oxide of a material of the first electrode.

[0132] Example 7 provides the quantum circuit assembly according to any one of Examples 4-6, where a thickness of the layer of the dielectric material is between about 1 and 8 nm, including all values and ranges therein, e.g. between about 1 and 4 nm, or between about 1 and 2 nm.

[0133] Example 8 provides the quantum circuit assembly according to any one of the preceding Examples, where sidewalls of the first electrode, with zero or more further layers provided thereon, in particular one or more such sidewalls which are underneath the suspended portion, are surrounded by air or vacuum.

[0134] Example 9 provides the quantum circuit assembly according to any one of the preceding Examples, where the first electrode lead is in a first plane parallel to the substrate, the suspended portion is in a second plane parallel to the substrate, the second plane being a plane at a non-zero distance from the first plane and being further away from the substrate than the first plane, and the first electrode lead is perpendicular to a projection of the suspended portion onto the first plane.

[0135] Example 10 provides the quantum circuit assembly according to any one of the preceding Examples, where a material of the first electrode is provided over the suspended portion.

[0136] Example 11 provides the quantum circuit assembly according to any one of the preceding Examples, where a material of the second electrode is provided over the material of the first electrode.

[0137] Example 12 provides the quantum circuit assembly according to any one of the preceding Examples, where the suspended portion includes an opening over the first electrode lead, the opening filled with a material of the second electrode.

[0138] Example 13 provides the quantum circuit assembly according to Example 12, where an area of the opening is between about 100 and 5,000,000 nm^2, including all values and ranges therein, e.g. between about 500 and 100,000 nm^2, or between about 10,000 and 25000 nm^2.

[0139] Example 14 provides the quantum circuit assembly according to Example 13, where an area of the first electrode is smaller than the area of the opening, e.g. between about 1 and 50 % smaller,

including all values and ranges therein, e.g. between 5 and 30 % smaller, or between 10 and 20 % smaller.

[0140] Example 15 provides the quantum circuit assembly according to any one of the preceding Examples, where a thickness of the first electrode is between about 10 and 2000 nm, including all values and ranges therein, e.g. between about 50 and 1000 nm, or between about 100 and 500 nm.

[0141] Example 16 provides the quantum circuit assembly according to any one of the preceding Examples, where a thickness of the suspended portion is between about 10 and 2000 nm, including all values and ranges therein, e.g. between about 50 and 1000 nm, or between about 100 and 500 nm.

[0142] Example 17 provides the quantum circuit assembly according to any one of the preceding Examples, where the first electrode lead is a portion of a conductive loop of a superconducting quantum interference device (SQUID).

[0143] Example 18 provides a method of fabricating a quantum circuit assembly. The method includes providing a first electrode lead over a substrate; providing a second electrode lead over the substrate so that a portion of the second electrode lead forms a bridge, e.g. an air bridge, or a cantilever over the first electrode lead; providing an opening in the portion of the second electrode lead that forms the bridge/cantilever and is over the first electrode lead; depositing a first electrically conductive, preferably superconductive, material through the opening to form a first electrode of a Josephson Junction; providing a layer including a dielectric material over the first electrode; and depositing a second electrically conductive, preferably superconductive, material through the opening to form a second electrode of the Josephson Junction over the layer including the dielectric material.

[0144] Example 19 provides the method according to Example 18, where providing the layer including the dielectric material includes oxidizing the first electrically conductive material, e.g. by performing a controlled oxidation process to oxidize a layer at the exposed upper and sidewall surface(s) of the first electrically conductive material.

[0145] Example 20 provides the method according to Examples 18 or 19, where providing the second electrode lead includes enclosing at least a portion of the first electrode lead with a sacrificial material, depositing a material of the second electrode lead over the sacrificial material, and etching at least a portion of the sacrificial material so that the portion of the second electrode lead forms the bridge or the cantilever over the first electrode lead.

[0146] Example 21 provides the method according to any one of Examples 18-20, where the first electrically conductive material includes aluminum.

[0147] Example 22 provides the method according to any one of Examples 18-21, where an area of the opening is between about 100 and 5,000,000 nm^2, including all values and ranges therein, e.g. between about 500 and 100,000 nm^2, or between about 10,000 and 25000 nm^2.

[0148] Example 23 provides a quantum computing device that includes a quantum processing device and a memory device. The quantum processing device includes a substrate and a plurality of qubits disposed over or in the substrate, where at least one qubit of the plurality of qubits includes a Josephson Junction having a first and a second electrodes, where the first electrode is electrically connected to a first electrode lead, the second electrode is electrically connected to a second electrode lead, and a portion of the second electrode lead is suspended over the first electrode lead (i.e. is separated from the first electrode lead by a gap comprising vacuum, air, or another gas). The memory device is configured to store data generated by the plurality of qubits during operation of the quantum processing device.

[0149] Example 24 provides the quantum computing device according to Example 23, further including a cooling apparatus configured to maintain a temperature of the quantum processing device below 5 degrees Kelvin.

[0150] Example 25 provides the quantum computing device according to Examples 23 or 24, where the memory device is configured to store instructions for a quantum computing algorithm to be executed by the quantum processing device.

[0151] Example 26 provides the quantum computing device according to any one of Examples 23-25, further including a non-quantum processing device coupled to the quantum processing device.

[0152] In further Examples, the quantum processing device of the quantum computing device according to any one of Examples 23-26 may include a quantum circuit assembly according to any one of Examples 1-17, and/or at least portions of the quantum processing device of the quantum computing device may be fabricated using the method according to any one of Examples 18-22.

[0153] The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

[0154] These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Claims:

1. A quantum circuit assembly comprising:

a substrate;

a first electrode lead over the substrate;

a second electrode lead; and

a Josephson Junction comprising a first electrode electrically connected to the first electrode lead and a second electrode electrically connected to the second electrode lead,

where the second electrode lead comprises a suspended portion forming a bridge or a cantilever over the first electrode lead.

2. The quantum circuit assembly according to claim 1, wherein at least a portion of the suspended portion is suspended over a portion of the substrate adjacent to the first electrode lead.

3. The quantum circuit assembly according to claim 1, wherein a distance between the suspended portion and the first electrode lead is between 50 and 50000 nanometers.

4. The quantum circuit assembly according to claim 1, wherein the first electrode and the second electrode are separated by a layer comprising a dielectric.

5. The quantum circuit assembly according to claim 4, wherein the layer comprising the dielectric is provided over at least portions of sidewalls of the first electrode.

6. The quantum circuit assembly according to claim 4, wherein the dielectric comprises a material of the first electrode and oxygen.

7. The quantum circuit assembly according to claim 4, wherein a thickness of the layer of the dielectric is between 1 and 8 nanometers.

8. The quantum circuit assembly according to any one of claims 1-7, wherein sidewalls of the first electrode, with zero or more further layers thereon, are surrounded by air or vacuum.

9. The quantum circuit assembly according to any one of claims 1-7, wherein:

the first electrode lead is in a first plane parallel to the substrate,

the suspended portion is in a second plane parallel to the substrate, and

the first electrode lead is perpendicular to a projection of the suspended portion onto the first plane.

10. The quantum circuit assembly according to any one of claims 1-7, wherein a material of the first electrode is over the suspended portion.

11. The quantum circuit assembly according to any one of claims 1-7, wherein a material of the second electrode is over the material of the first electrode.

12. The quantum circuit assembly according to any one of claims 1-7, wherein the suspended portion comprises an opening over the first electrode lead, the opening filled with a material of the second electrode.

13. The quantum circuit assembly according to claim 12, wherein an area of the opening is between 100 and 5,000,000 square nanometers.

14. The quantum circuit assembly according to claim 13, wherein an area of the first electrode is smaller than the area of the opening.

15. The quantum circuit assembly according to any one of claims 1-7, wherein a thickness of the first electrode is between 10 and 2000 nanometers.

16. The quantum circuit assembly according to any one of claims 1-7, wherein a thickness of the suspended portion is between 10 and 2000 nanometers.

17. The quantum circuit assembly according to any one of claims 1-7, wherein the first electrode lead is a portion of a conductive loop of a superconducting quantum interference device (SQUID).

18. A method of fabricating a quantum circuit assembly, the method comprising:

providing a first electrode lead over a substrate;

providing a second electrode lead over the substrate so that a portion of the second electrode lead forms a bridge or a cantilever over the first electrode lead;

providing an opening in the portion of the second electrode lead over the first electrode lead;

depositing a first electrically conductive material through the opening to form a first electrode of a Josephson Junction;

providing a layer comprising a dielectric material over the first electrode; and

depositing a second electrically conductive material through the opening to form a second electrode of the Josephson Junction over the layer comprising the dielectric material .

19. The method according to claim 18, wherein providing the layer comprising the dielectric material comprises oxidizing the first electrically conductive material.

20. The method according to claim 18, wherein providing the second electrode lead comprises enclosing at least a portion of the first electrode lead with a sacrificial material, depositing a material of the second electrode lead over the sacrificial material, and etching at least a portion of the sacrificial material so that the portion of the second electrode lead forms the bridge or the cantilever over the first electrode lead.

21. The method according to any one of claims 18-20, wherein the first electrically conductive material comprises aluminum.

22. The method according to any one of claims 18-20, wherein an area of the opening is between 100 and 5,000,000 square nanometers.

23. A quantum computing device, comprising:

a quantum processing device that includes a die comprising a substrate and a plurality of qubits over or in the substrate, where at least one qubit of the plurality of qubits includes a Josephson Junction comprising a first electrode and a second electrode, where

the first electrode is electrically connected to a first electrode lead,

the second electrode is electrically connected to a second electrode lead, and

a portion of the second electrode lead is suspended over the first electrode lead; and

a memory device configured to store data generated by the plurality of qubits during operation of the quantum processing device.

24. The quantum computing device according to claim 23, further comprising a cooling apparatus configured to maintain a temperature of the quantum processing device below 5 degrees Kelvin.

25. The quantum computing device according to claims 23 or 24, wherein the memory device is configured to store instructions for a quantum computing algorithm to be executed by the quantum processing device.

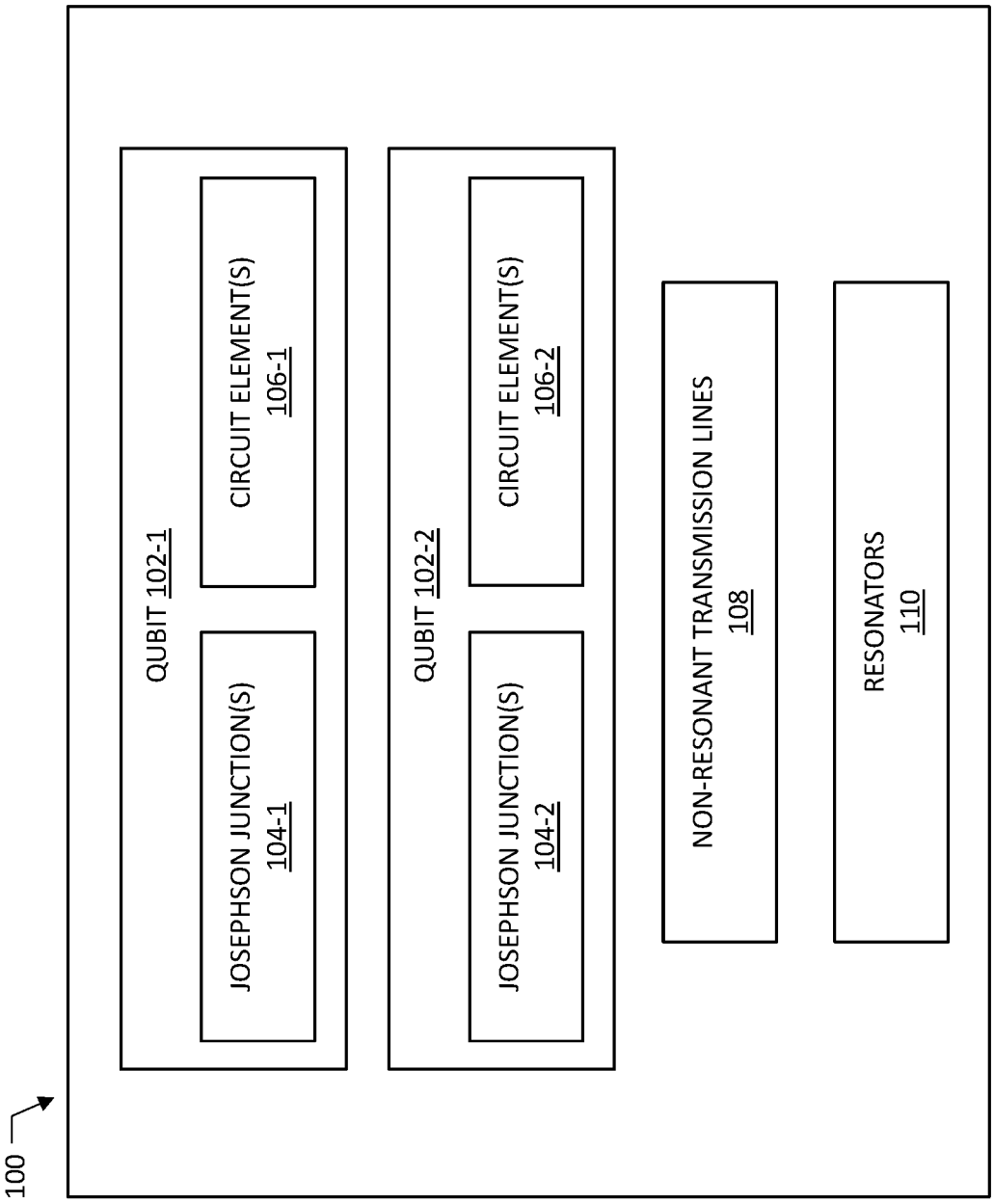
100
QUBIT 102-1
JOSEPHSON JUNCTION(S) 104-1
CIRCUIT ELEMENT(S) 106-1
QUBIT 102-2
JOSEPHSON JUNCTION(S) 104-2
CIRCUIT ELEMENT(S) 106-2
NON-RESONANT TRANSMISSION LINES 108
RESONATORS 110

FIG. 1

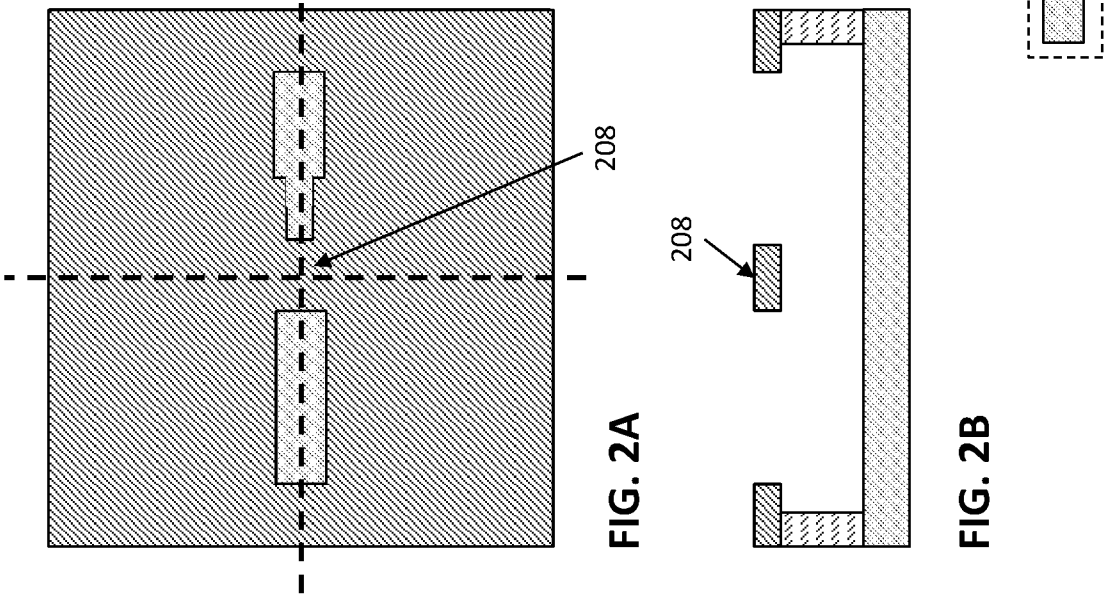

FIG. 2A FIG. 2B FIG. 2C

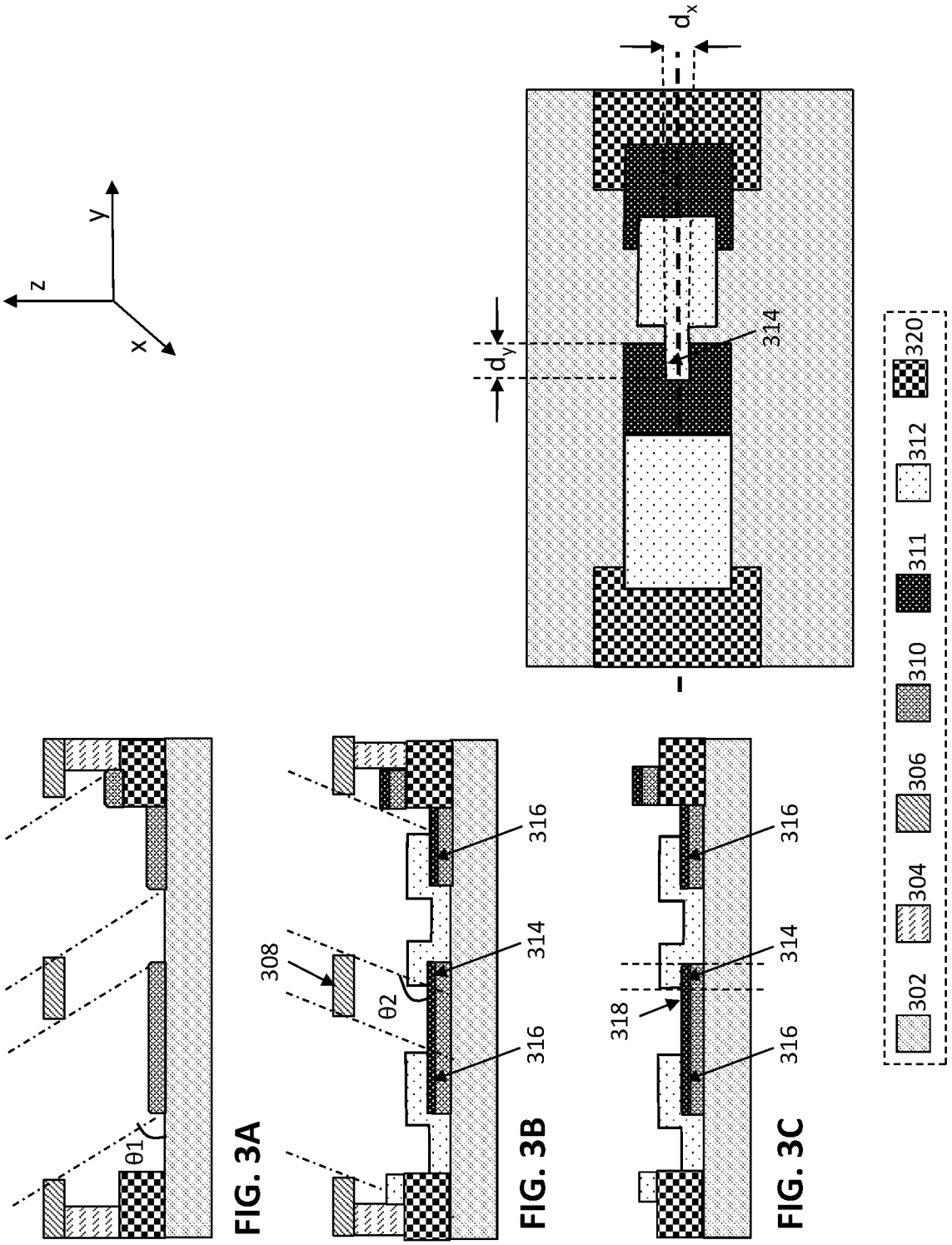

FIG. 3A

FIG. 3B

FIG. 3C

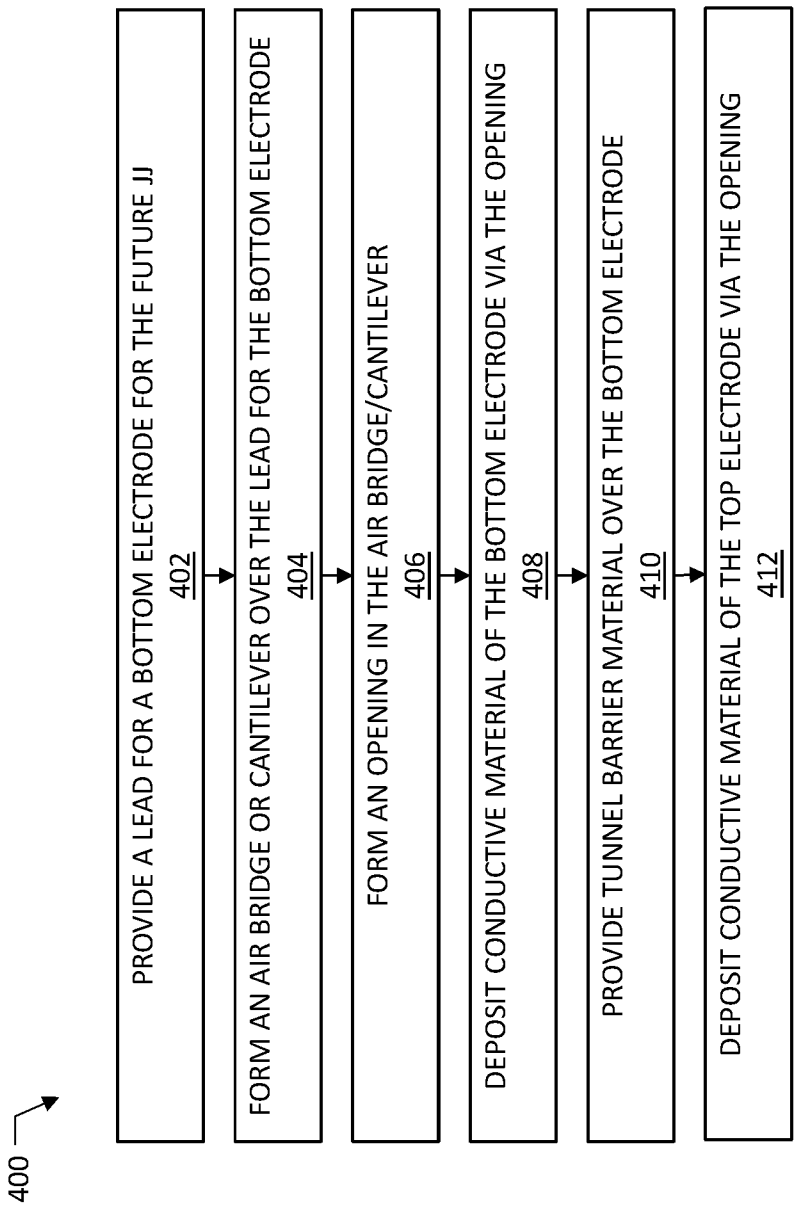
400
PROVIDE A LEAD FOR A BOTTOM ELECTRODE FOR THE FUTURE JJ
402
FORM AN AIR BRIDGE OR CANTILEVER OVER THE LEAD FOR THE BOTTOM ELECTRODE
404
FORM AN OPENING IN THE AIR BRIDGE/CANTILEVER
406
DEPOSIT CONDUCTIVE MATERIAL OF THE BOTTOM ELECTRODE VIA THE OPENING
408
PROVIDE TUNNEL BARRIER MATERIAL OVER THE BOTTOM ELECTRODE
410
DEPOSIT CONDUCTIVE MATERIAL OF THE TOP ELECTRODE VIA THE OPENING
412

FIG. 4

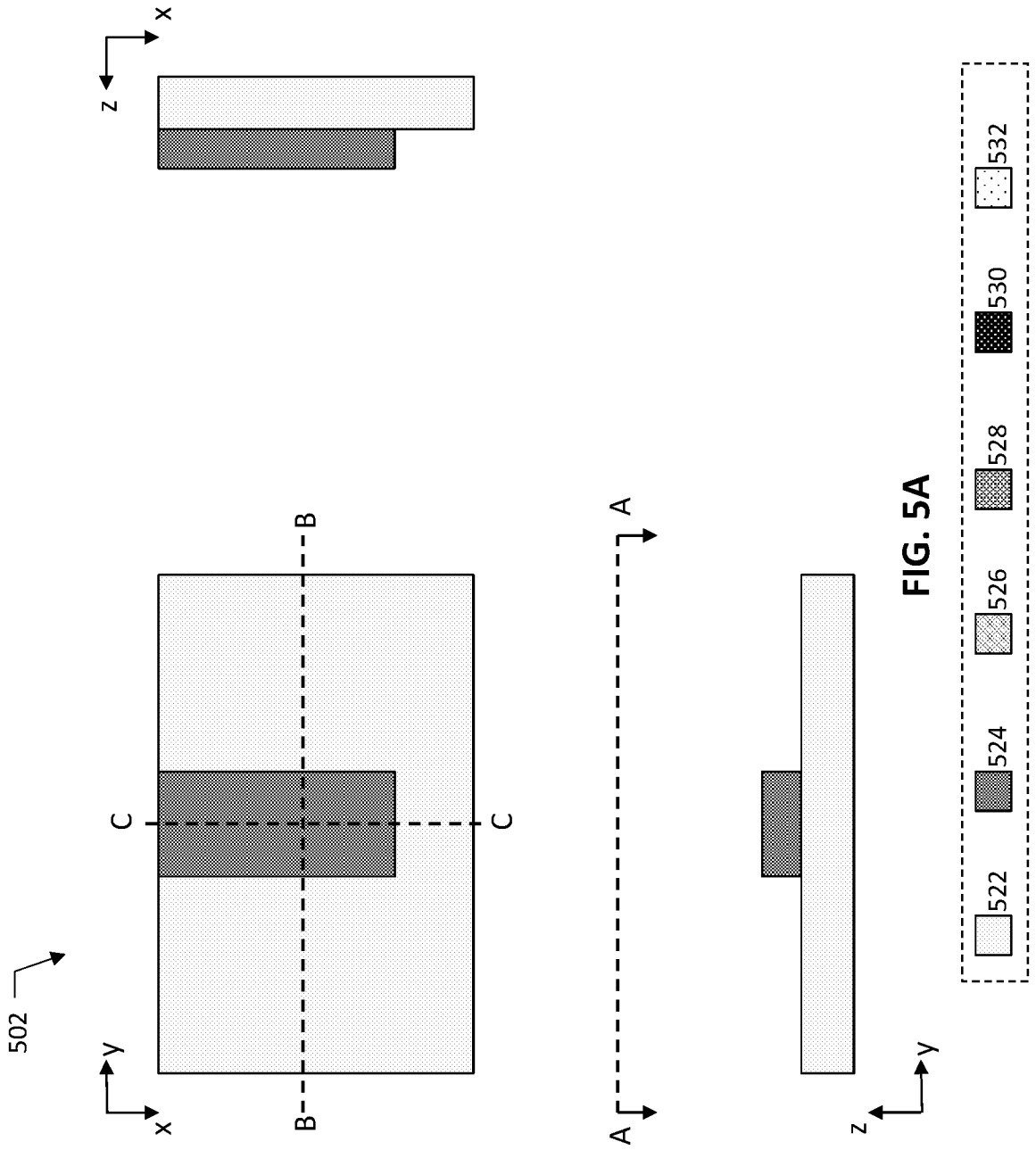

FIG. 5A

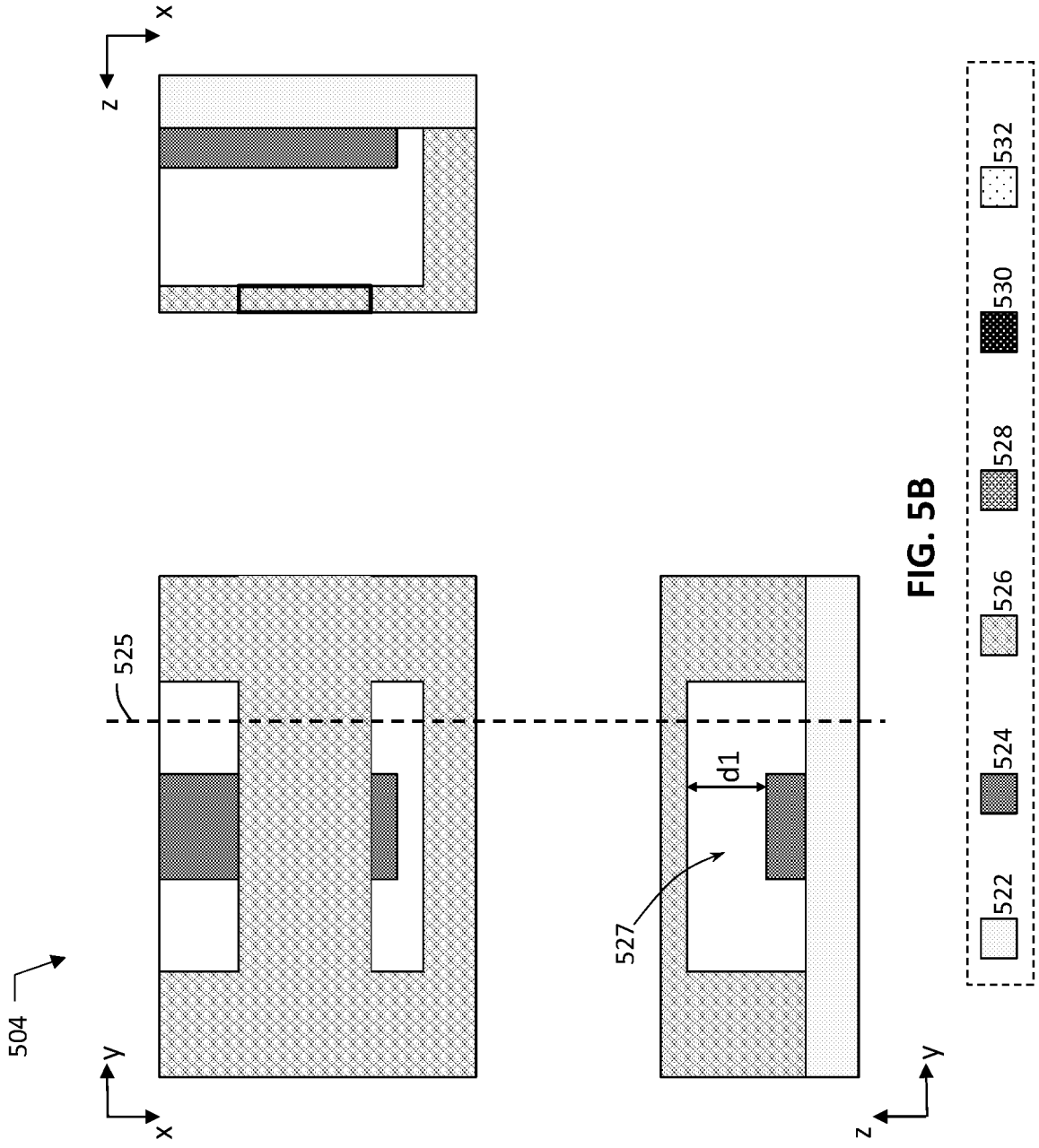

FIG. 5B

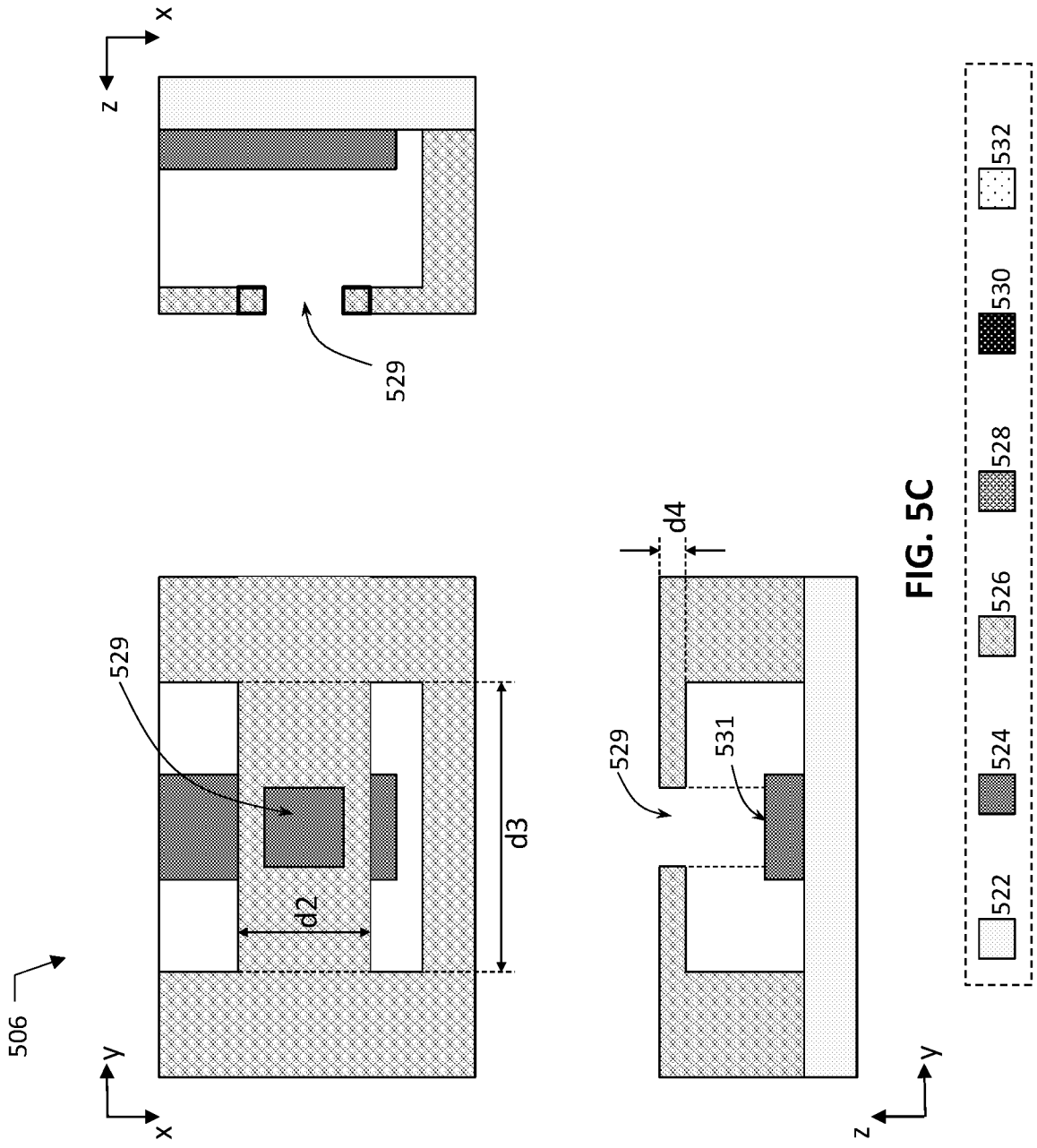

FIG. 5C

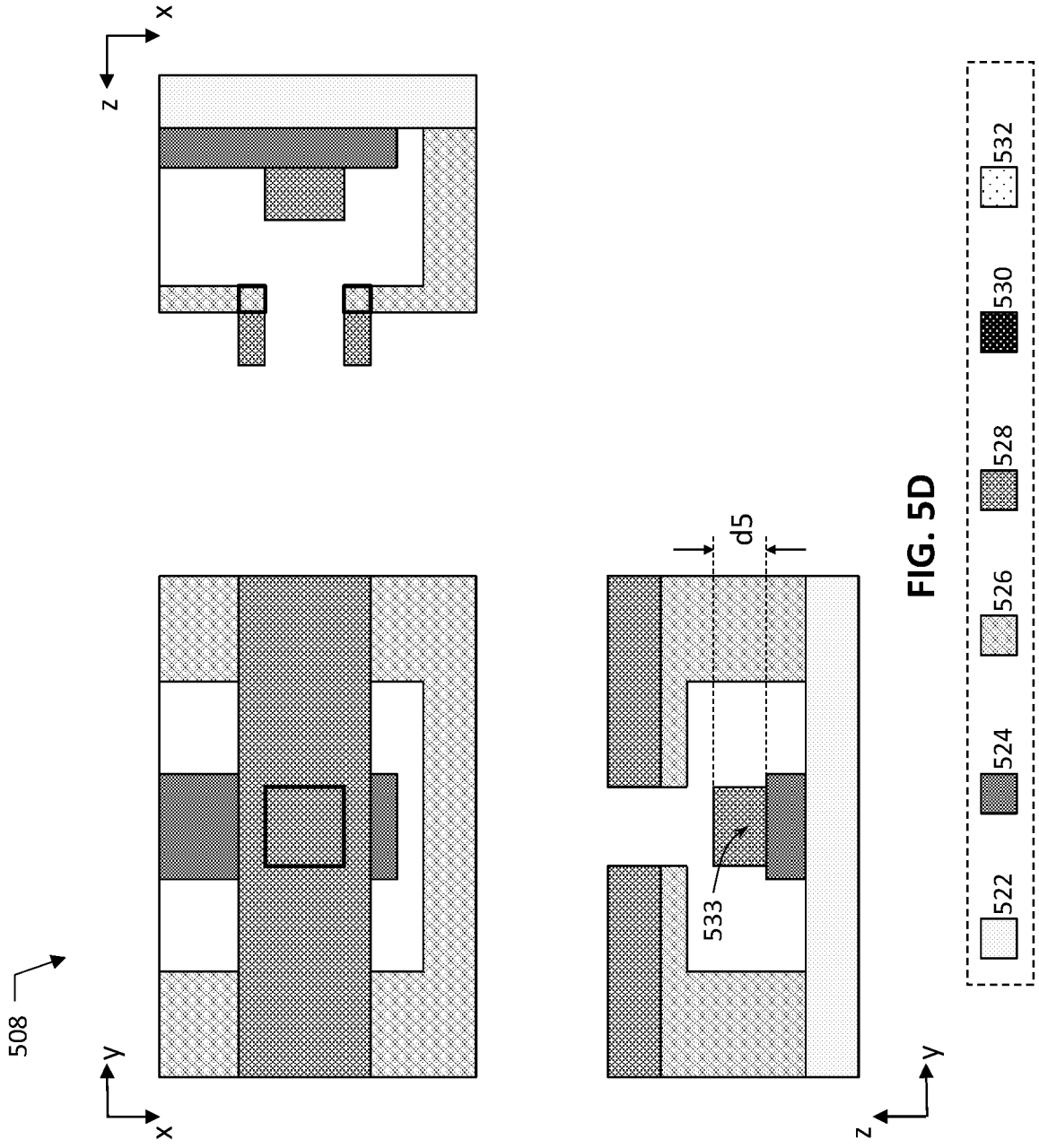

FIG. 5D

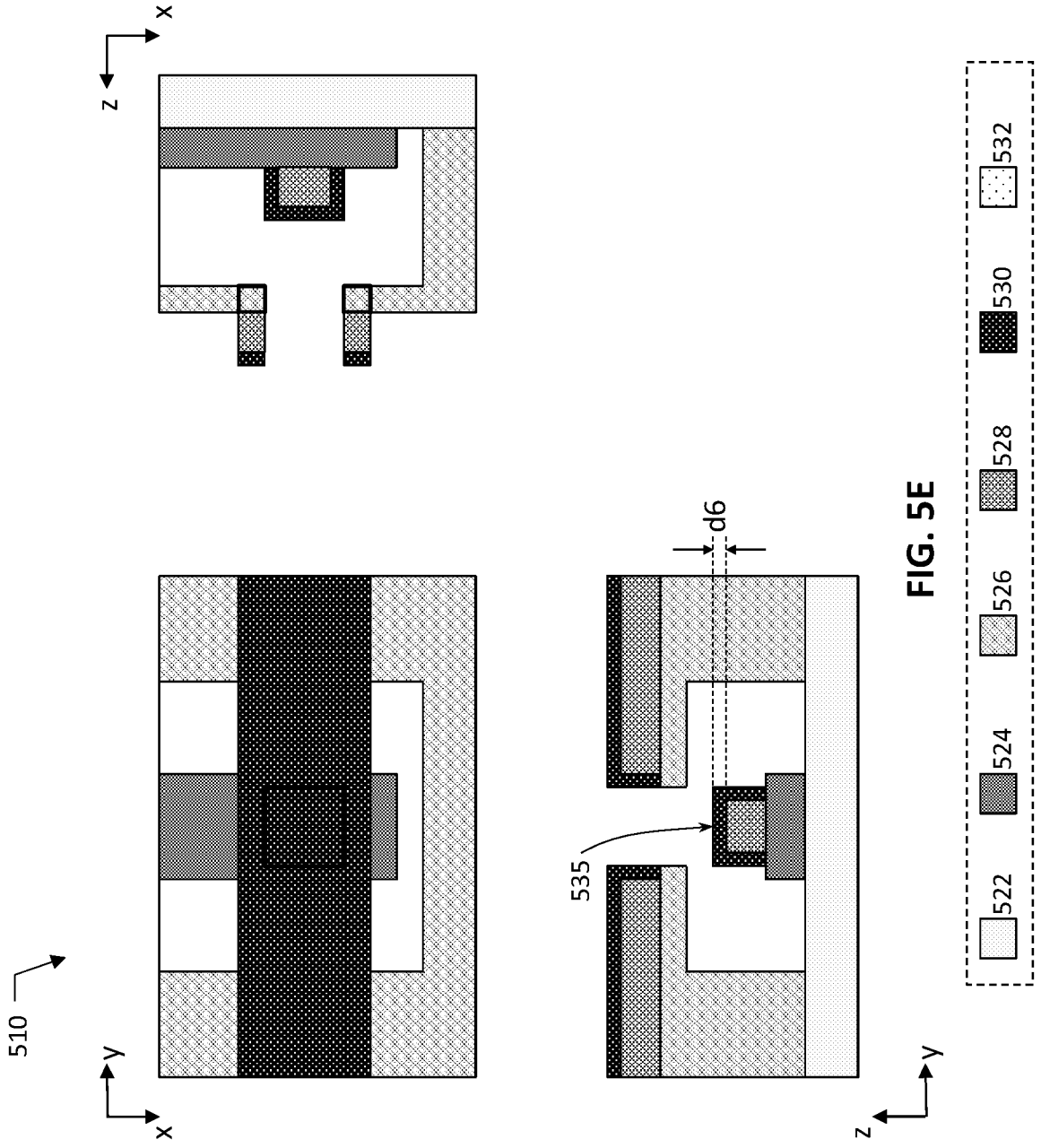

FIG. 5E

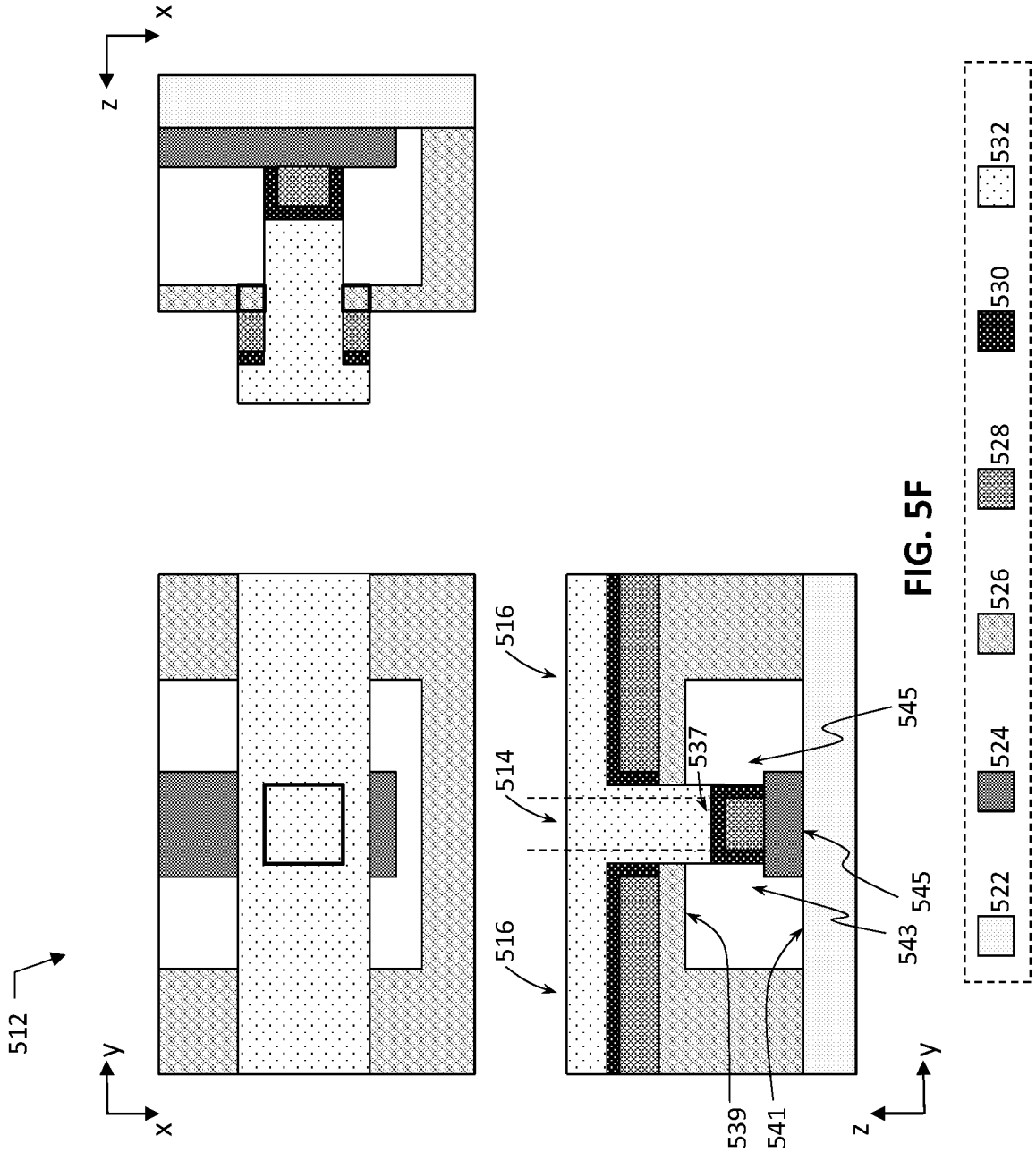
x
z
512
y
x
516
514
516
537
545
545
543
539
541
z
y
532
530
528
526
524
522

FIG. 5F

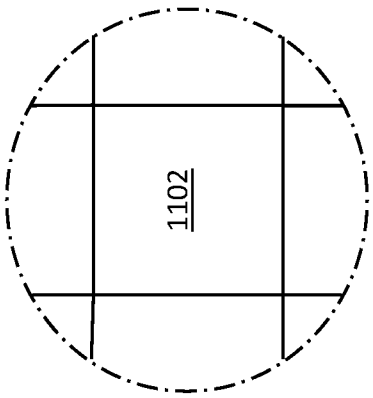

FIG. 6B

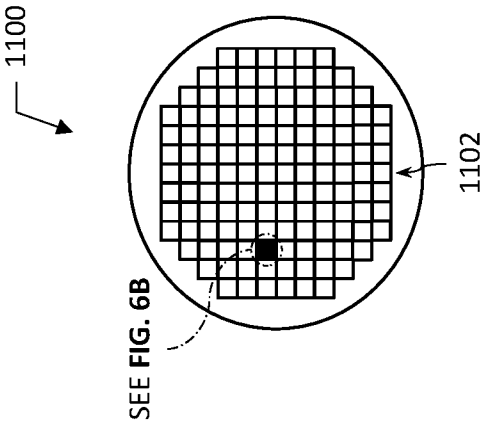

FIG. 6A

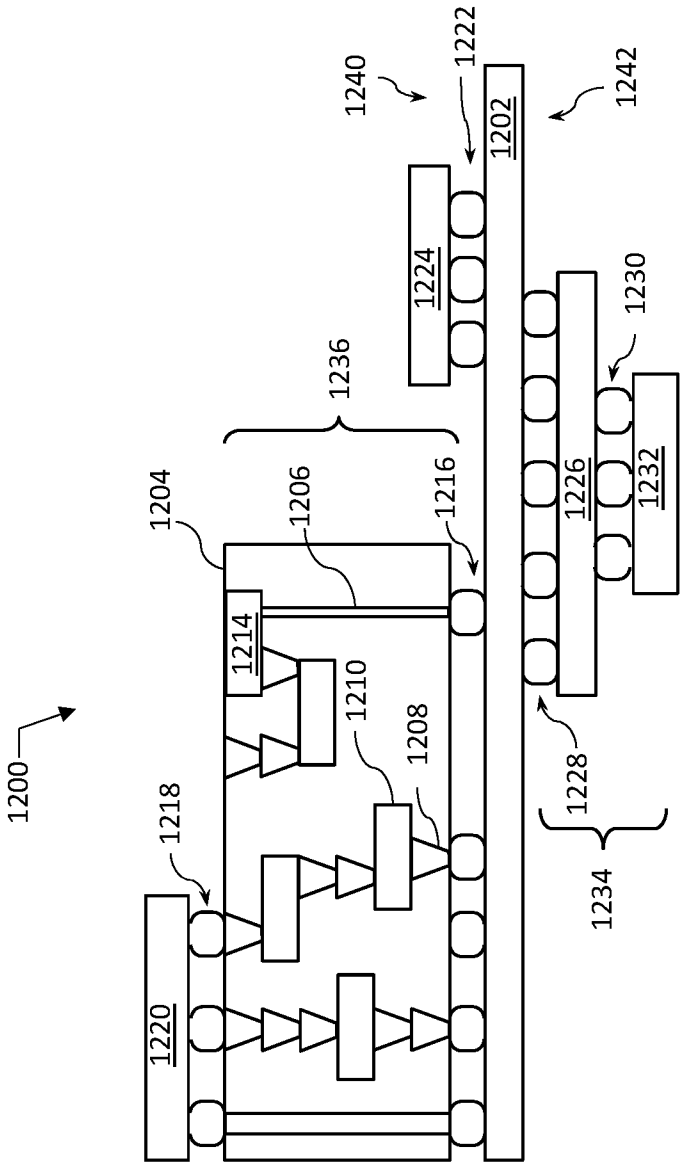
1200
1202
1204
1206
1208
1210
1214
1216
1218
1220
1222
1224
1226
1228
1230
1232
1234
1236
1240
1242

FIG. 7

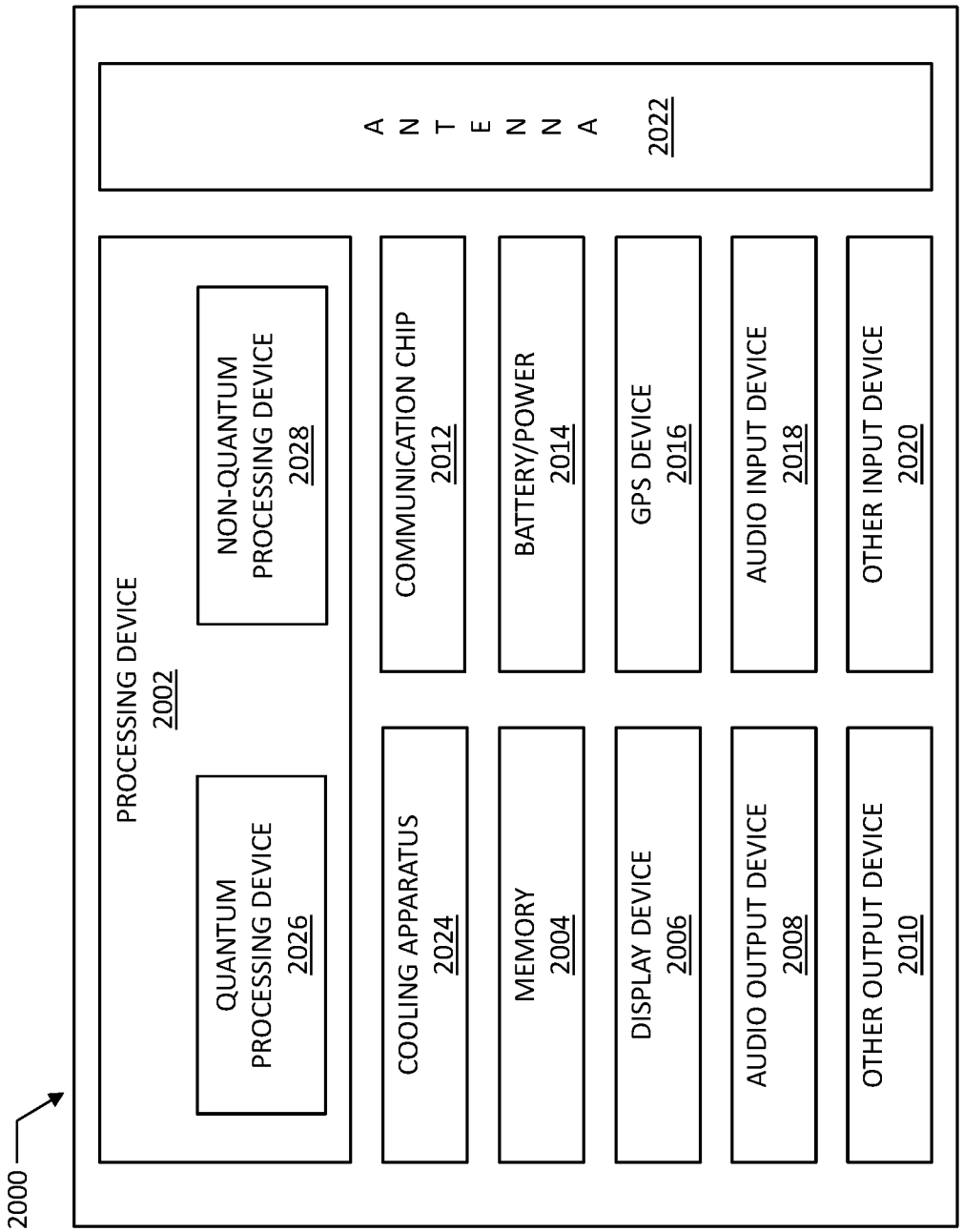
2000
PROCESSING DEVICE
2002
QUANTUM PROCESSING DEVICE
2026
NON-QUANTUM PROCESSING DEVICE
2028
COOLING APPARATUS
2024
MEMORY
2004
DISPLAY DEVICE
2006
AUDIO OUTPUT DEVICE
2008
OTHER OUTPUT DEVICE
2010
COMMUNICATION CHIP
2012
BATTERY/POWER
2014
GPS DEVICE
2016
AUDIO INPUT DEVICE
2018
OTHER INPUT DEVICE
2020
ANTENNA
2022

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/065932

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/15(2006.01)i, H01L 29/66(2006.01)i, H01L 39/02(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/15; H01L 39/02; H01L 39/24; G06N 99/00; H01L 29/06; H01L 39/22; H01L 29/66; H01L 31/0256

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: qubit, Josephson Junction, electrode lead, bridge, cantilever

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2017-0077383 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 16 March 2017 See paragraphs [0004], [0035]-[0047], claim 5 and figures 1B-1L.	1-4,6,8-9,11,17,23,25
Y		5,7,10,12-16,18-22,24
Y	US 2016-0093790 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION et al.) 31 March 2016 See paragraphs [0023]-[0025], [0035], [0045] and figures 1A-1B, 4.	5,7,10,12-16,18-22,24
A	US 2014-0264286 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 18 September 2014 See paragraphs [0019]-[0021] and figures 1A-1D.	1-25
A	US 2016-0148112 A1 (SAMSUNG ELECTRONICS CO., LTD.) 26 May 2016 See paragraphs [0039]-[0059] and figure 2.	1-25
A	US 2003-0042481 A1 (ALEXANDER YA TZALENCHUK et al.) 06 March 2003 See paragraphs [0053]-[0081] and figures 1A-1C.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 September 2018 (11.09.2018)	**11 September 2018 (11.09.2018)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
KANG, Sung Chul
Telephone No. +82-42-481-8405

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/065932

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2017-0077383 A1	16/03/2017	CN 106098926 A	09/11/2016
		US 2017-0033273 A1	02/02/2017
		US 2017-0084813 A1	23/03/2017
		US 9564573 B1	07/02/2017
US 2016-0093790 A1	31/03/2016	US 9385294 B2	05/07/2016
US 2014-0264286 A1	18/09/2014	US 2015-0311422 A1	29/10/2015
		US 2015-0340584 A1	26/11/2015
		US 9177814 B2	03/11/2015
		US 9716219 B2	25/07/2017
US 2016-0148112 A1	26/05/2016	KR 10-2016-0062569 A	02/06/2016
		US 9633314 B2	25/04/2017
US 2003-0042481 A1	06/03/2003	AU 2002-322942 A1	10/03/2003
		US 2003-0071258 A1	17/04/2003
		US 2003-0107033 A1	12/06/2003
		US 6753546 B2	22/06/2004
		US 6979836 B2	27/12/2005
		WO 2003-019683 A2	06/03/2003
		WO 2003-019683 A3	25/03/2004