(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
12 September 2013 (12.09.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/134561 A1

(51) International Patent Classification:
G01R 1/067 (2006.01) *H01L 21/66* (2006.01)

(21) International Application Number:
PCT/US2013/029712

(22) International Filing Date:
7 March 2013 (07.03.2013)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/607,893 7 March 2012 (07.03.2012) US

(71) Applicant *(for all designated States except US)*: **ADVANTEST CORPORATION** [JP/JP]; 1-32-1 Asahi-Cho, Nerima-Ku, Tokyo 179-0071 (JP).

(72) Inventor; and
(71) Applicant *(for US only)*: **NAMBURI, Lakshmikanth** [IN/US]; 747 West Camino Real Avenue, Arcadia, CA 91007 (US).

(74) Agent: **MURABITO, Anthony, C.**; Murabito Hao & Barnes LLP, Two North Market Street, Third Floor, San Jose, CA 95113 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: FINE PITCH PROBE ARRAY FROM BULK MATERIAL

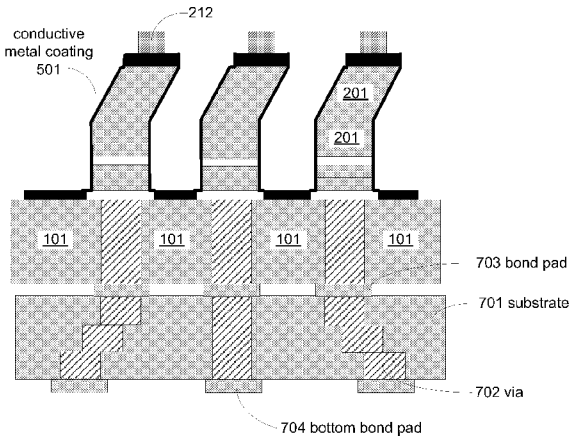

Figure 7

(57) **Abstract**: Fine pitch probe array from bulk material. In accordance with a first method embodiment, an article of manufacture includes an array of probes. Each probe includes a probe tip, suitable for contacting an integrated circuit test point. Each probe tip is mounted on a probe finger structure. All of the probe finger structures of the array have the same material grain structure. The probe fingers may have a non-linear profile and/or be configured to act as a spring.

WO 2013/134561 A1

FINE PITCH PROBE ARRAY FROM BULK MATERIAL

RELATED APPLICATION

[0001] This application claims priority to United States Provisional Patent Application 61/607,893 entitled, "A Method to Fabricate Fine Pitch Probe Arrays Using Silicon," filed 7 March 2012, to Namburi, which is hereby incorporated herein by reference in its entirety.

FIELD OF INVENTION

[0002] Embodiments of the present invention relate to the field of integrated circuit design, manufacture and test. More specifically, embodiments of the present invention relate to systems and methods for fine pitch probe arrays from bulk material.

BACKGROUND

[0003] Integrated circuit testing generally utilizes fine probes to make contact with test points of an integrated circuit in order to inject electrical signals and/or measure electrical parameters of the integrated circuit. Conventional circuit probes are produced singly, and manually assembled into an array corresponding to some or all of the test points on an integrated circuit.

[0004] Unfortunately, due to the constraints of producing the probes individually, and assembling them into an array, conventional integrated circuit probe arrays are generally unable to achieve a pitch, e.g., probe to probe spacing, of less than about 50 μm. In addition, conventional probes often have an undesirable high inductance, which may limit the frequency of test signals. Further, conventional integrated circuit probe arrays are typically unable to achieve necessary alignment accuracies in all three dimensions. Still further, such alignment and co-planarity deficiencies of

conventional probes deleteriously limit the number of probes and the total area of a probe array, and hence the total area of an integrated circuit that may be tested at a single time. For example, a single conventional integrated circuit probe array assembled at a fine pitch may not be capable of contacting all test points on a large integrated circuit, e.g., an advanced microprocessor.

SUMMARY OF THE INVENTION

[0005] Therefore, what is needed are systems and methods for fine pitch probe arrays from bulk material. What is additionally needed are systems and methods for fine pitch probe arrays from bulk material with fine pitches and high positional accuracy. A further need exists for systems and methods for fine pitch probe arrays from bulk material that are compatible and complementary with existing systems and methods of integrated circuit design, manufacturing and test. Embodiments of the present invention provide these advantages.

[0006] In contrast to the conventional art in which an array of electronic probes is constructed by adding individual probes to form an assembly, embodiments in accordance with the present invention form an array of electronic probes from a bulk material, removing material to render the basis of an array of electronic probes.

[0007] In accordance with a first method embodiment, an article of manufacture includes an array of probes. Each probe includes a probe tip, suitable for contacting an integrated circuit test point. Each probe tip is mounted on a probe finger structure. All of the probe finger structures of the array have the same material grain structure. The probe fingers may have a non-linear profile and/or be configured to act as a spring.

[0008] In accordance with a method embodiment, a bulk material with first and second substantially parallel faces is accessed. A probe base is formed on the first face. A probe tip suitable for contacting an integrated circuit test point is formed on the probe base. The second face is mounted to a carrier wafer. Portions of the bulk material are removed to form a probe finger structure coupled to the probe base and the probe tip. The probe finger structure is coated with a conductive metal electrically coupled to the probe tip. Formation of the probe tip and probe base may include photolithography.

[0009] In accordance with another embodiment of the present invention, an electronic probe array for testing integrated circuits includes a plurality of individual probes, mechanically coupled and electrically isolated. Each individual probe includes a probe tip functionally coupled to a probe finger structure. The probe tip is of a different material from the probe finger structure. The probe tip is configured for contacting an integrated circuit test point. Each probe finger structure is formed from a same piece of bulk material. Each individual probe is coated with conductive metal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. Unless otherwise noted, the drawings are not drawn to scale.

[0011] Figure 1 illustrates a portion of an exemplary "through-silicon via" (TSV) carrier wafer, in accordance with embodiments of the present invention.

[0012] Figure 2A illustrates formation of a probe block, in accordance with embodiments of the present invention.

[0013] Figure 2B illustrates a formation of slots between rows of probes along one axis to form a probe block, in accordance with embodiments of the present invention.

[0014] Figure 2C illustrates a plan view of a portion of a substrate after the formation of slots, in accordance with embodiments of the present invention.

[0015] Figure 3 illustrates a die bonding of a probe block to a carrier wafer, in accordance with embodiments of the present invention.

[0016] Figure 4 illustrates a sectional view of an array of individual probes, in accordance with embodiments of the present invention.

[0017] Figure 5 illustrates application of a conductive metal coating to an array, in accordance with embodiments of the present invention.

[0018] Figure 6 illustrates removal of the masking layer, exposing the probe tip, in accordance with embodiments of the present invention.

[0019] Figure 7 illustrates a typical application of an array of probes, in accordance with embodiments of the present invention.

DETAILED DESCRIPTION

[0020] Reference will now be made in detail to various embodiments of the present invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with these embodiments, it is understood that they are not intended to limit the invention to these embodiments. On the contrary, the

invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the invention, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be recognized by one of ordinary skill in the art that the invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the invention.

NOTATION AND NOMENCLATURE

[0021] Some portions of the detailed descriptions which follow (e.g., Figures 1-7) are presented in terms of procedures, steps, logic blocks, processing, and other symbolic representations of operations on data bits that may be performed on computer memory. These descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. A procedure, computer executed step, logic block, process, etc., is here, and generally, conceived to be a self-consistent sequence of steps or instructions leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer system. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like.

[0022] It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following discussions, it is

appreciated that throughout the present invention, discussions utilizing terms such as "accessing" or "forming" or "mounting" or "removing" or "coating" or "attaching" or "processing" or "singulating" or "roughening" or "filling" or "performing" or "generating" or "adjusting" or "creating" or "executing" or "continuing" or "indexing" or "computing" or "translating" or "calculating" or "determining" or "measuring" or "gathering" or "running" or the like, refer to the action and processes of a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

FINE PITCH PROBE ARRAY FROM BULK MATERIAL

[0023] Figure 1 illustrates a portion of an exemplary "through-silicon via" (TSV) carrier wafer 100, in accordance with embodiments of the present invention. Wafer 100 is illustrated as being formed in silicon, although any suitable material may be utilized. Wafer 100 should generally have parallel top and bottom faces. Any suitable plan-view shape may be used. Wafer 100 comprises a silicon substrate 101 with oxide on sidewalls of the silicon via to insulate the metal via from the semiconducting silicon.

[0024] Carrier wafer 100 also comprises a sacrificial ground layer, formed of any suitable material. Sacrificial ground layer 102 will be utilized during wire electrical discharge machining (wire-EDM) processing, further described below, and should be suitable for such purpose. Carrier wafer 100 further comprises a plurality of solder pads 103. Solder pads 103 may comprise an alloy of gold (Au) and tin (Sn), at an exemplary thickness of 2 μm. Under laying solder pads 103 are a plurality of under-bump-metallurgy (UBM) thin film stacks 105. UBM thin film stacks 105 may comprise a film

of, for example, titanium (Ti), platinum (Pt) and gold (Au). It is appreciated that other suitable materials may also be used. An insulating layer 104, e.g., silicon dioxide (SiO_2), or other suitable material, separates the stacks of solder pads 103 and UBM 105.

[0025] Carrier wafer 100 further comprises a plurality of through-silicon vias (TSV) 106. Through silicon vias 106 provide electrical coupling from the solder pads 103 to the other side of the carrier wafer 100, and to sacrificial ground layer 102.

[0026] Figure 2A illustrates formation of a probe block 200, in accordance with embodiments of the present invention. Probe block 200 comprises a substrate 201 comprising silicon, although any suitable material may be utilized, for example, beryllium copper. Silicon substrate 201 may be similar to silicon substrate 101, illustrated in Figure 1. Silicon substrate 201 may comprise highly doped p-type silicon, doped with boron (B) to a concentration of about 10^{18} dopants/cm^3, for example, which may produce an electrical resistivity of 0.001 ohm-cm. The thickness of the substrate 201 determines the overall height of the probe array.

[0027] Probe block 200 additionally comprises a plurality of solder pads 203. Solder pads 203 may be similar to solder pads 103, illustrated in Figure 1. Solder pads 203 may comprise an alloy of gold (Au) and tin (Sn), at an exemplary thickness of 2 μm. Under laying solder pads 203 are a plurality of under-bump-metallurgy (UBM) thin film stacks 205. UBM films 205 may be similar to UBM films 105, illustrated in Figure 1. UBM films 205 may comprise a film of, for example, titanium (Ti), platinum (Pt) and gold (Au). It is appreciated that other suitable materials may be used.

[0028] Probe block 200 further comprises a plurality of probes 210. Probes 210 comprise a probe base 211 and a probe tip 212. Probe tip 212

may comprise any material suitable for the probing application, e.g., suitable to contact an integrated circuit test point, for example, a noble metal, e.g., ruthenium (Ru), rhodium (Rh), palladium (Pd), silver (Ag), osmium (Os), iridium (Ir) and/or, platinum (Pt). (It is appreciated that gold (Au) is often included in the noble metals, but is generally considered too soft for probing.) The probe tip 212 and the upper face of the probe base 211 are masked with a masking layer 213, e.g., a non-conductive polymer. The probe base 211 may be fabricated by sputtering a seed layer on one side of the wafer, and lithographically patterned and plated. Probe tips 212 may be fabricated on top of the probe base by lithographically patterning photoresist , plating the tip material and etching the seed layer between the tip bases. The probe tips 212 may be planarized if necessary for a smooth finish. The probe tips 212 should then coated to protect them from the rest of the process.

[0029] Figure 2B illustrates a formation of slots 251 between rows of probes 210 along one axis to form probe block 250, in accordance with embodiments of the present invention.. It is appreciated that slots 251 represent the absence of substrate material. In some embodiments, slots 251 may remove an entire thickness of substrate 201. It is appreciated that substrate 201 is not completely singulated; portions of substrate 201 remain coupled outside of the plane of Figure 2B. Slots 251 may be formed by any suitable process, including, for example, deep reactive ion etching (DRIE).

[0030] Figure 2C illustrates a plan view of a portion of substrate 201 after the formation of slots 251, in accordance with embodiments of the present invention.. Slots 251 are substantially parallel, and separate "rows" of probes 210 from one another. Mask 213 is not illustrated in Figure 2C for clarity.

[0031] Figure 3 illustrates a die bonding 300 of probe block 250 to carrier wafer 100, in accordance with embodiments of the present invention. Bond pads 103 (Figure 1) are bonded to bond pads 203 (Figures 2A, 2B) by any suitable process.

[0032] Figure 4 illustrates a sectional view of an array 400 of individual probes 401, in accordance with embodiments of the present invention. It is to be appreciated that the plane of Figure 4 is perpendicular to the plane of Figure 3. For example, the plane of Figure 4 is parallel to, but not coincident with, the slots 251, as illustrated in Figure 2C. Individual proves 401 comprise a probe tip 212, a probe base 211 and a probe finger structure 402. It is appreciated that all probe fingers 402 will have the same material grain structure, as they are formed from the same block of material, e.g., single crystal silicon.

[0033] It is to be appreciated that individual probes 401 may have a complex shape in at least one dimension, in accordance with embodiments of the present invention. For example, as illustrated in Figure 4, probe fingers 401 are not linear, e.g., they are "bent" to the right. Such a profile, in one or more dimensions, may allow each individual probe to function as a spring, allowing for compliance to slight irregularities in a surface of an integrated circuit, and providing a restorative force to keep the probe tip, e.g., 212, in contact with an integrated circuit test point.

[0034] In accordance with embodiments of the present invention, such "non-straight" or non-linear probe profiles may be accomplished by wire electrical discharge machining (wire-EDM). For example, a wire of about 12 μm in diameter may be used to machine probes at fine pitch geometries less than 40 μm. It is appreciated that a probe pitch may be different in X and Y dimensions, and it is not necessarily the same, even in the same dimension. Although the probe fingers 401 are illustrated as being "straight" in the

plane of Figure 2B, wire electrical discharge machining could be applied to that stage as well, e.g., replacing deep reactive ion etching, to produce a more complex shape in that dimension, as well, in accordance with embodiments of the present invention. It is further appreciated that embodiments in accordance with the present invention may form probes with a pitch greater than about 40 μm. For example, a wire of greater than about 12 μm in diameter may be used to machine probes at larger pitches. Probes formed in accordance with embodiments of the present invention at such larger pitches continue to enjoy significant advantages over the conventional art, including, for example, lower cost, less complexity and exceptional precision in probe tip positional accuracy in all three dimensions.

[0035] Figure 5 illustrates application of a conductive metal coating 501 to array 400, in accordance with embodiments of the present invention. The conductive metal coating 501 may comprise gold (Au) and/or copper (Cu), or other suitable materials, and may be applied by any suitable process, including, for example, immersion plating or electro-less plating processes. The thickness of the conductive metal coating 501 may be determined by the required current carrying capability of the probes. Conductive metal coating 501 may not be required in the case that material 201 is a metal such as berellium-copper (BeCu) since it is sufficiently conductive, unlike doped silicon.

[0036] In Figure 6, the masking layer 213 (Figure 2) is removed, exposing the probe tip 212, via any suitable process, for example, using a dry reactive ion etch process or by using suitable wet chemistry. In addition, the sacrificial ground layer 102 (Figure 1) is removed. In this manner, an array of electrical probes 600 is formed from a bulk material, in accordance with embodiments of the present invention.

[0037] Figure 7 illustrates a typical application of array of probes 600 (Figure 6), in accordance with embodiments of the present invention. As illustrated in Figure 7, the array of electrical probes 600 is bonded to a space transforming substrate 701. Space transforming substrate 701 serves to transform the spacing of the probe heads 712, which may be on a pitch suitable for probing integrated circuits, e.g., less than or equal to about 40 μm, to a pitch more suitable for printed circuit boards, e.g., about 1 mm.

[0038] Substrate 701 may be similar to substrate 101 (Figure 1), although that is not required. Space transforming substrate 701 is electrically and mechanically bonded to array of probes 600 via any suitable processes and materials, for example via solder bonding pads 703. Bottom bond pads 704 serve to couple space transforming substrate 701 to a higher level assembly, for example, a printed circuit board.

[0039] In accordance with embodiments of the present invention, the individual probes of the array 600 are formed from a bulk material, e.g., from single crystal silicon with a high modulus. Such material functions as a spring without any appreciable plastic deformation. The complex shape increases the spring characteristic of the probes, allowing for compliance to slight irregularities in a surface of an integrated circuit, and providing a restorative force to keep the probe tip, e.g., 212, in contact with an integrated circuit test point. The probe tips exhibit a fine pitch, e.g., less than 40 μm, with excellent planarity and tip positional accuracy, as the probe tips are lithographically defined. The probe array has a high current carrying capability due to the conductive metal coating. Further, probe arrays in accordance with the present invention may be produced with shorter lead times and at reduced cost in comparison with the conventional art, as there is no manually assembly, and the processes leverage the economics of integrated circuit manufacturing.

[0040] Embodiments in accordance with the present invention provide systems and methods for fine pitch probe arrays from bulk material. In addition, embodiments in accordance with the present invention provide systems and methods for fine pitch probe arrays from bulk material with fine pitches and high positional accuracy. Further, embodiments in accordance with the present invention provide systems and methods for fine pitch probe arrays from bulk material that are compatible and complementary with existing systems and methods of integrated circuit design, manufacturing and test.

[0041] Various embodiments of the invention are thus described. While the present invention has been described in particular embodiments, it should be appreciated that the invention should not be construed as limited by such embodiments, but rather construed according to the below claims.

CLAIMS

What is claimed is:

1. An article of manufacture comprising:
an array of probes, wherein each probe comprises:
a probe tip, suitable for contacting an integrated circuit test point;
said probe tip mounted on a probe finger structure,
wherein all said probe finger structures of said array have the same material grain structure.

2. The article of manufacture of Claim 1 wherein said probe finger structure has a non-linear profile.

3. The article of manufacture of Claim 2 wherein said probe finger structure is configured to act as a spring.

4. The article of manufacture of Claim 1 further comprising a conductive metal coating on said probe finger structure, wherein said coating is in electrical contact with said probe tip,

5. The article of manufacture of Claim 1 wherein said probe tip comprises a noble metal excluding gold.

6. The article of manufacture of Claim 1 wherein said probe tips of said array of probes are arranged on a grid of less than 50 μm.

7. The article of manufacture of Claim 1 wherein said array of probes is functionally coupled to a space transforming substrate, for transforming a pitch of said array of probes to a larger pitch.

8. A method comprising:

accessing a bulk material with first and second substantially parallel faces;

forming a probe base on said first face;

forming a probe tip suitable for contacting an integrated circuit test point on said probe base;

mounting said second face to a carrier wafer;

removing portions of said bulk material to form a probe finger structure coupled to said probe base and said probe tip; and

coating said probe finger structure with a conductive metal electrically coupled to said probe tip.

9. The method of Claim 8 wherein said forming a probe base and said forming a probe tip comprise photolithography.

10. The method of Claim 8 wherein said probe tip comprises rhodium (Rh).

11. The method of Claim 8 wherein said removing comprises deep reactive ion etching (DRIE).

12. The method of Claim 8 wherein said removing comprises wire electrical discharge machining (wire-EDM).

13. The method of Claim 8 further comprising masking said probe tip prior to said coating.

14. The method of Claim 8 wherein said removing forms a non-linear probe finger structure.

15. An electronic probe array for testing integrated circuits comprising:

a plurality of individual probes, mechanically coupled and electrically isolated,

wherein each said individual probe comprises a probe tip functionally coupled to a probe finger structure,

wherein said probe tip is of a different material from said probe finger structure,

wherein said probe tip is configured for contacting an integrated circuit test point,

wherein each probe finger structure is formed from a same piece of bulk material, and

wherein each said individual probe is coated with conductive metal.

16. The electronic probe array of Claim 15 wherein said probe finger structure has a non-linear profile.

17. The electronic probe array of Claim 15 wherein said probe finger structure is configured to act as a spring.

18. The electronic probe array of Claim 15 further comprising a space transforming substrate, for transforming a pitch of said plurality of individual probes to a larger pitch.

19. The electronic probe array of Claim 15 wherein said probe tip comprises a noble metal

20. The electronic probe array of Claim 15 wherein two of said plurality of individual probes are closer than 50 μm from one another.

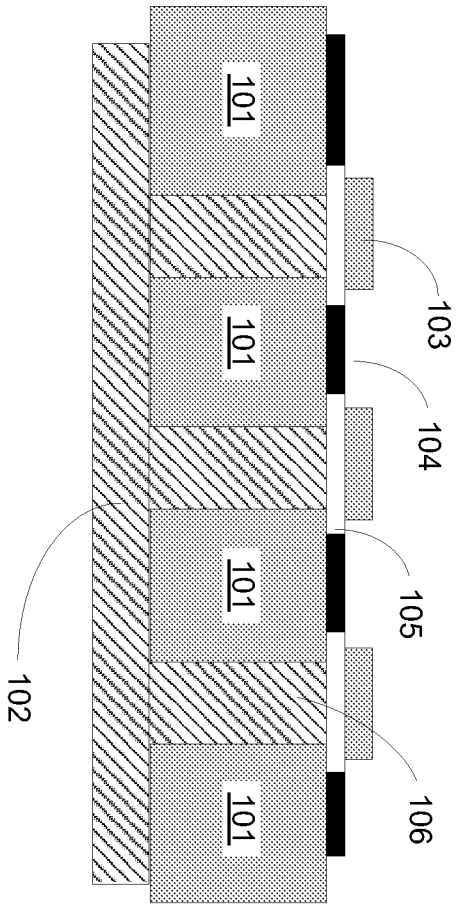

Figure 1

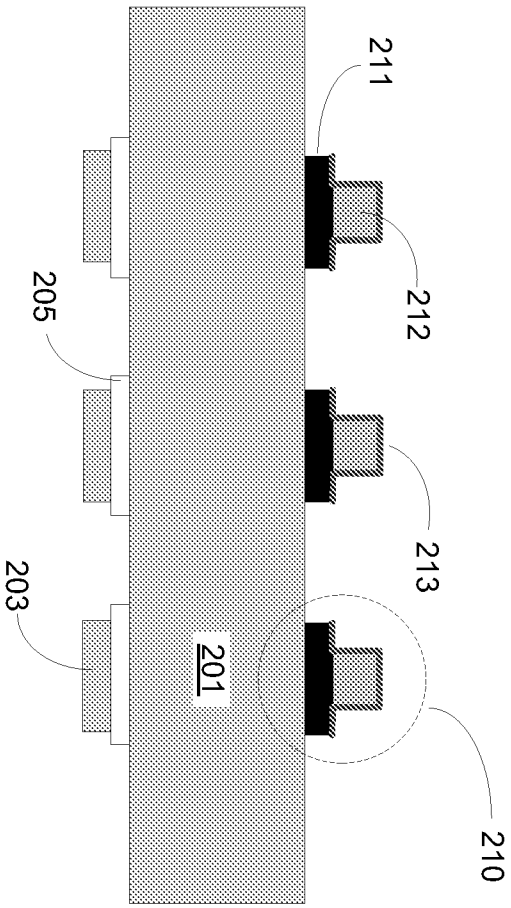

Figure 2A

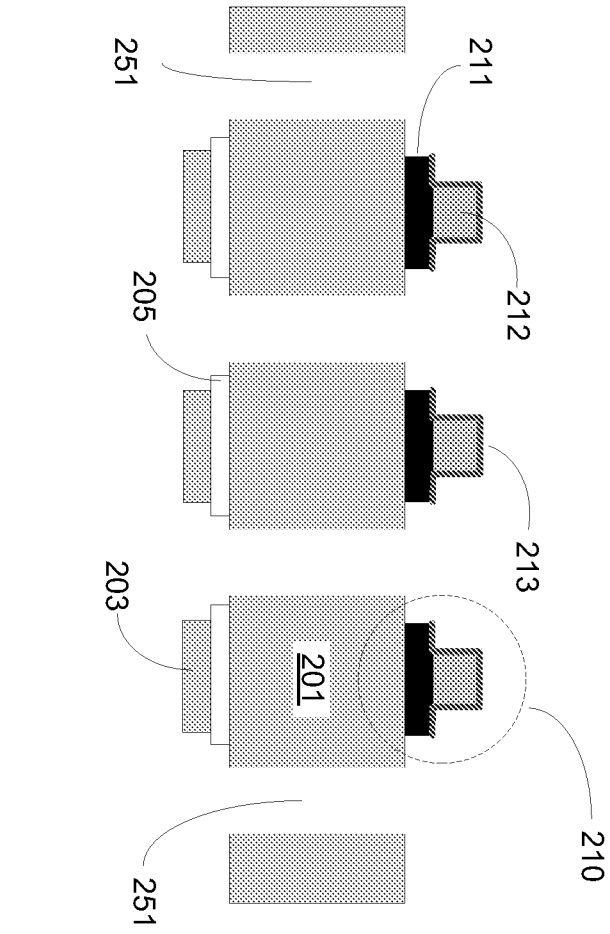

Figure 2B

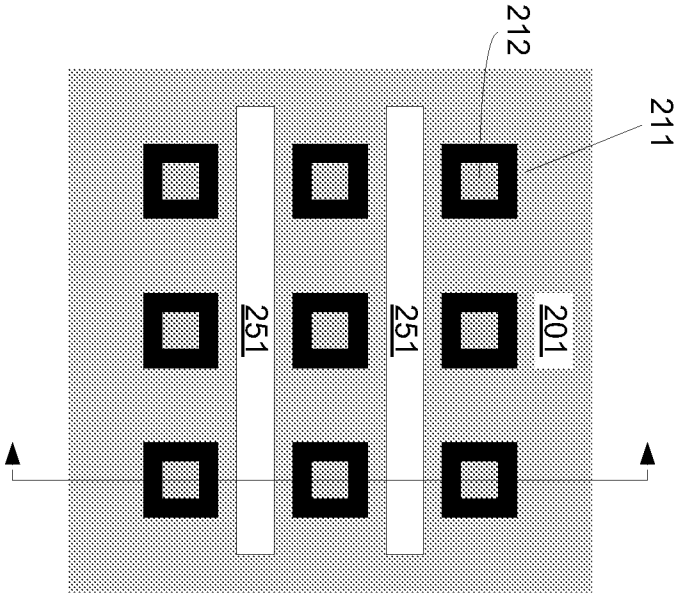

Figure 2C

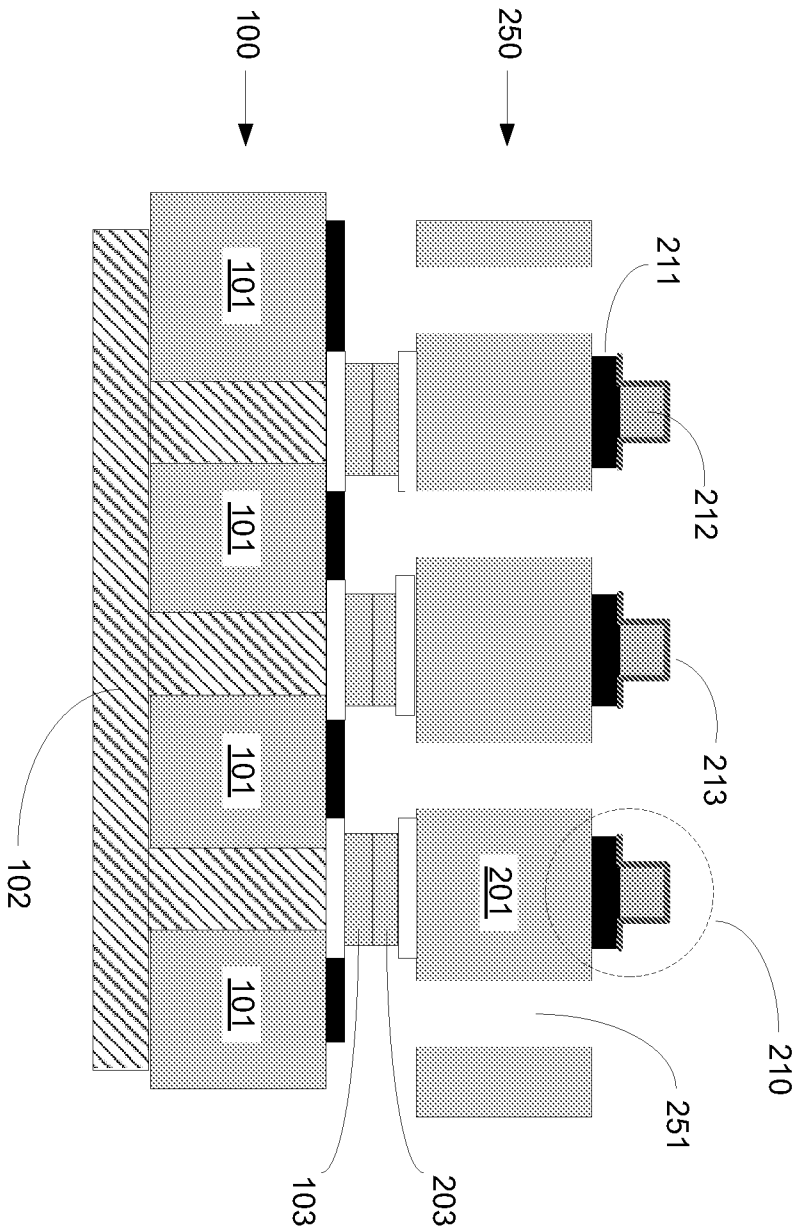

Figure 3

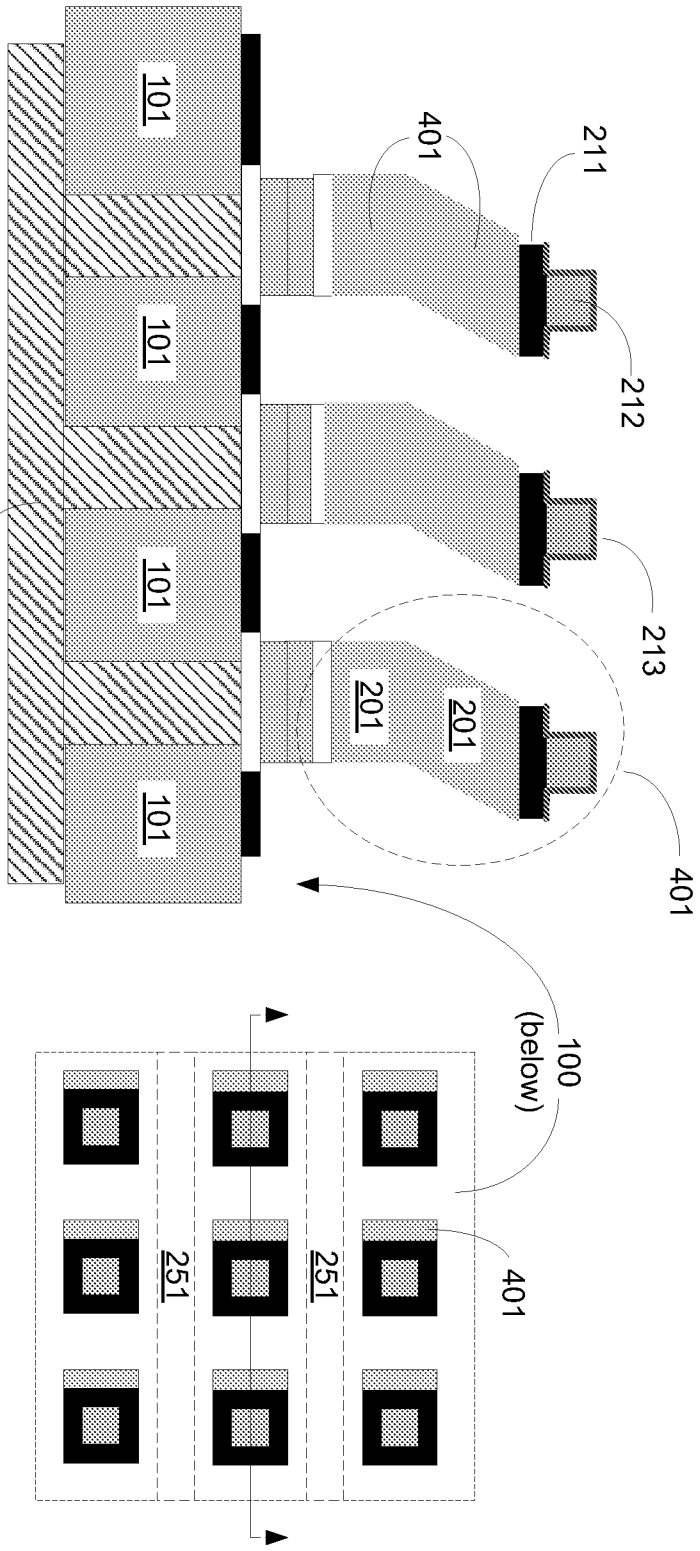
400
101
101
101
101
102
401
211
212
213
201
201
401
100
(below)
401
251
251

Figure 4

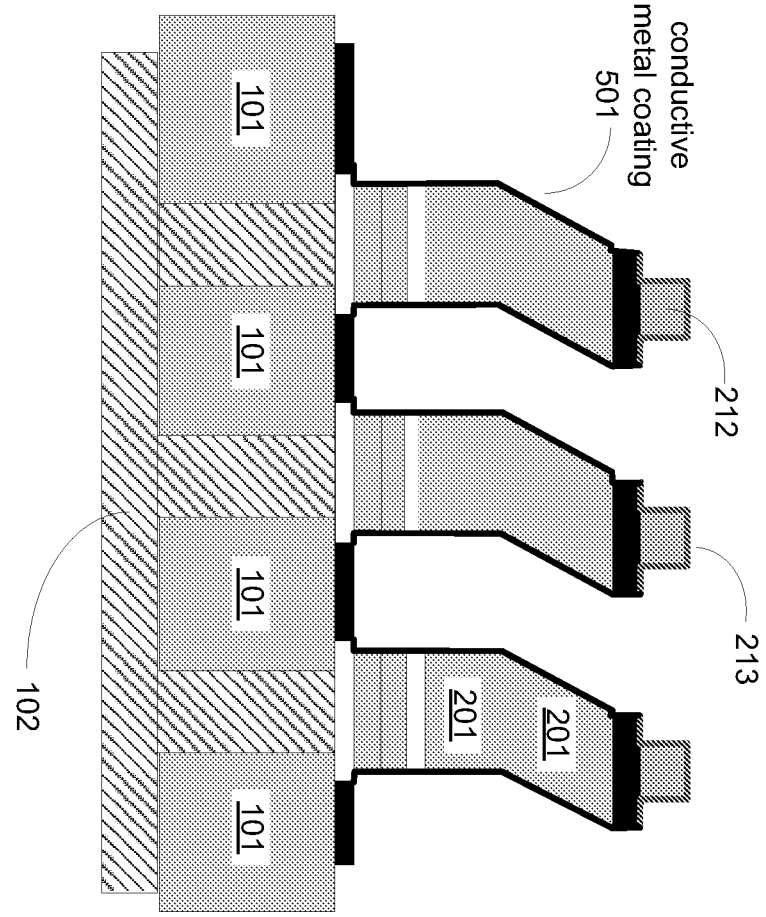
conductive metal coating
501
212
213
101
101
101
101
201
201
102

Figure 5

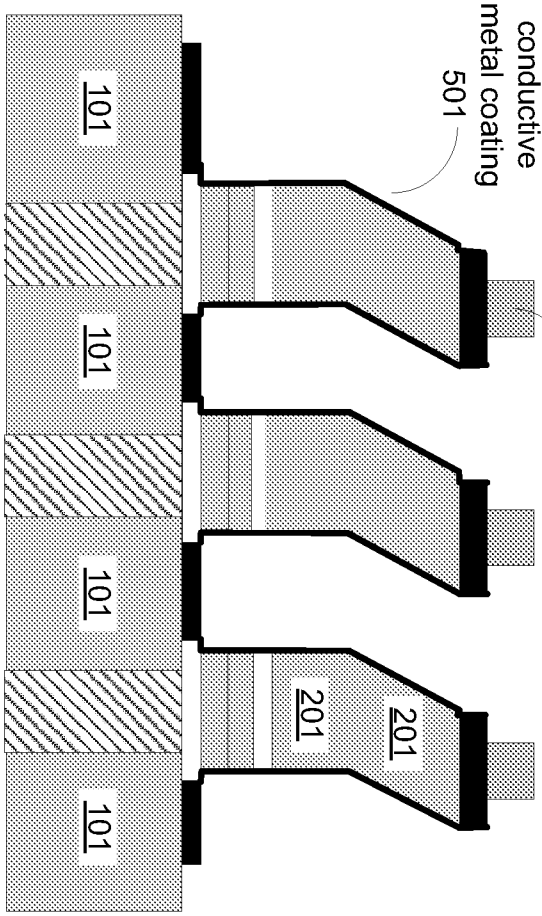

Figure 6

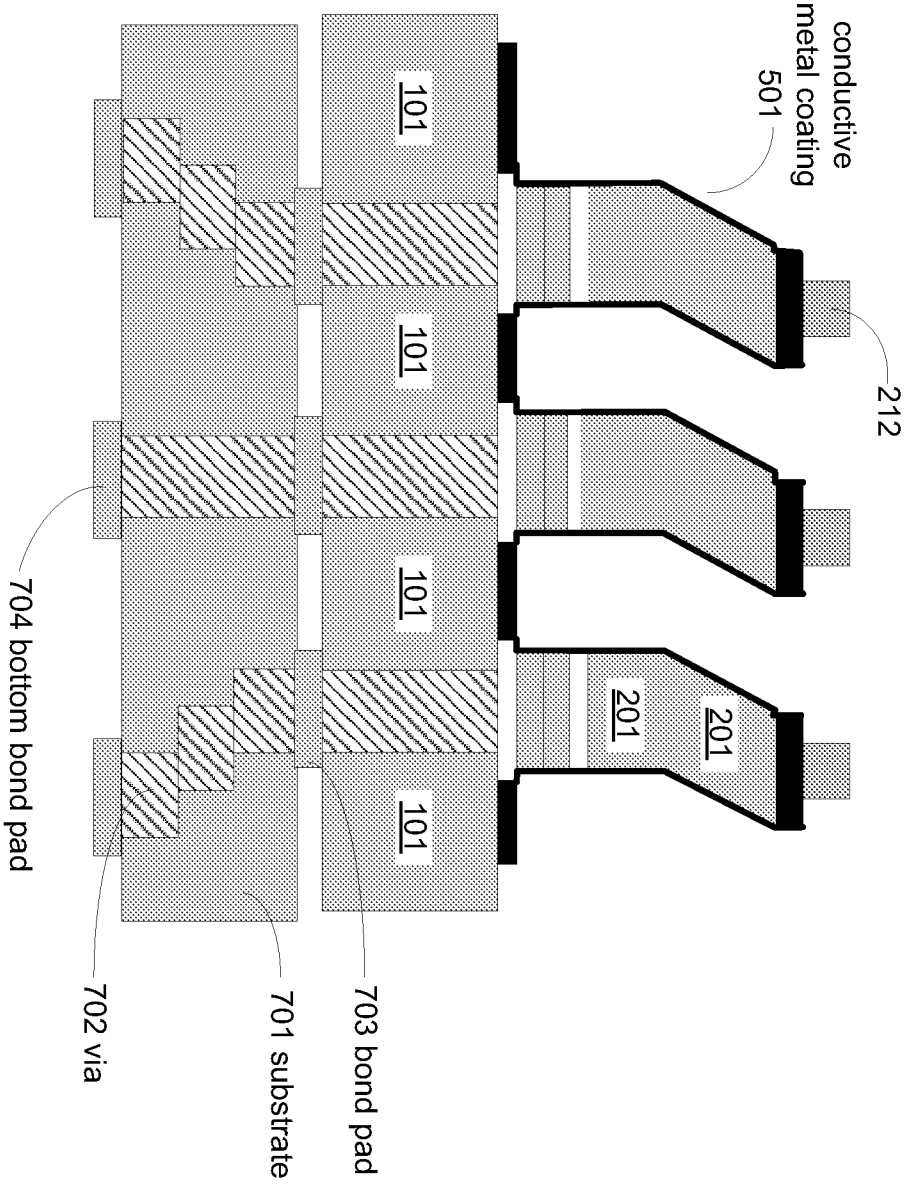
conductive metal coating
501
212
101
101
101
101
201
201
704 bottom bond pad
702 via
701 substrate
703 bond pad

Figure 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/029712

A. CLASSIFICATION OF SUBJECT MATTER

G01R 1/067(2006.01)i, H01L 21/66(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01R 1/067; G01R 31/00; C23F 1/00; H01L 21/336; H01R 43/00; G01R 1/06; G01R 31/02; G01R 1/073

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: fine pitch, probe, niddle, array

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 7385411 B2 (ELDRIDGE, BENJAMIN N.) 10 June 2008 See column 4, line 65 - column 5, lines 6, 38-40, 53-57, column 9, lines 16-20 and figures 3b, 3e, 4-5b.	1-20
Y	US 2002-0040884 A1 (HANTSCHEL, THOMAS et al.) 11 April 2002 See abstract paragraphs [0004], [0015]-[0016], [0030], [0041] claims 1, 10 and figures 2, 5.	1-20
A	US 2002-0127812 A1 (MATSUNAGA, NORIAKI et al.) 12 September 2002 See claims 1-2, 6 and figures 3a-3c.	1-20
A	US 2008-0180123 A1 (CHENG, HSU MING et al.) 31 July 2008 See abstract claims 1-2 and figures 2, 4.	1-20
A	US 2008-0164896 A1 (BEAMAN, BRIAN SAMUEL et al.) 10 July 2008 See paragraphs [0019], [0036], [0042], [0055] and figures 1, 11.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 June 2013 (20.06.2013)	**20 June 2013 (20.06.2013)**

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea
Facsimile No. 82-42-472-7140

Authorized officer
OH, Eung Gie
Telephone No. 82-42-481-8744

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/029712

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 7385411 B2	10.06.2008	CN 101036060 A	12.09.2007
		EP 1787133 A2	23.05.2007
		JP 2008-511840 A	17.04.2008
		KR 10-1207651 B1	03.12.2012
		KR 10-2007-0056099 A	31.05.2007
		US 2006-0043985 A1	02.03.2006
		US 2008-0238458 A1	02.10.2008
		US 7990164 B2	02.08.2011
		WO 2006-026733 A2	09.03.2006
US 2002-0040884 A1	11.04.2002	EP 0899538 A1	03.03.1999
		EP 0899538 B1	14.05.2003
		US 6328902 B1	11.12.2001
		US 6504152 B2	07.01.2003
US 2002-0127812 A1	12.09.2002	JP 2001-174482 A	29.06.2001
		US 2004-0196058 A1	07.10.2004
		US 6724208 B2	20.04.2004
		US 7032307 B2	25.04.2006
US 2008-0180123 A1	31.07.2008	CN 101275972 A	01.10.2008
		CN 101275972 B	16.02.2011
		TW 2008-46671 A	01.12.2008
		US 7696766 B2	13.04.2010
US 2008-0164896 A1	10.07.2008	EP 0593966 A1	27.04.1994
		EP 0593966 B1	30.12.1998
		EP 0925509 B1	07.09.2005
		JP 03578232 B2	20.10.2004
		JP 06-204399 A	22.07.1994
		JP 07-287031 A	31.10.1995
		JP 11-317476 A	16.11.1999
		JP 2000-502810 A	07.03.2000
		JP 2514305 B2	10.07.1996
		JP 3262531 B2	04.03.2002
		US 05371654 A	06.12.1994
		US 05531022 A	02.07.1996
		US 05635846 A	03.06.1997
		US 05811982 A	22.09.1998
		US 05821763 A	13.10.1998
		US 05838160 A	17.11.1998
		US 05914614 A	22.06.1999
		US 06054651 A	25.04.2000
		US 06104201 A	15.08.2000
		US 06151701 A	21.11.2000
		US 2001-0045012 A1	29.11.2001
		US 2001-0054907 A1	27.12.2001
		US 2002-0014004 A1	07.02.2002
		US 2002-0089344 A1	11.07.2002

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/029712

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 2002-0190738 A1	19.12.2002
		US 2003-0048108 A1	13.03.2003
		US 2003-0106213 A1	12.06.2003
		US 2004-0130343 A1	08.07.2004
		US 2004-0148773 A1	05.08.2004
		US 2005-0062492 A1	24.03.2005
		US 2005-0179456 A1	18.08.2005
		US 2007-0271781 A9	29.11.2007
		US 2008-0024154 A1	31.01.2008
		US 2008-0024155 A1	31.01.2008
		US 2008-0030215 A1	07.02.2008
		US 2008-0047741 A1	28.02.2008
		US 2008-0048690 A1	28.02.2008
		US 2008-0048691 A1	28.02.2008
		US 2008-0048697 A1	28.02.2008
		US 2008-0088332 A1	17.04.2008
		US 2008-0100316 A1	01.05.2008
		US 2008-0100317 A1	01.05.2008
		US 2008-0100318 A1	01.05.2008
		US 2008-0100324 A1	01.05.2008
		US 2008-0106281 A1	08.05.2008
		US 2008-0106282 A1	08.05.2008
		US 2008-0106283 A1	08.05.2008
		US 2008-0106284 A1	08.05.2008
		US 2008-0106285 A1	08.05.2008
		US 2008-0106291 A1	08.05.2008
		US 2008-0106872 A1	08.05.2008
		US 2008-0111568 A1	15.05.2008
		US 2008-0111569 A1	15.05.2008
		US 2008-0111570 A1	15.05.2008
		US 2008-0112144 A1	15.05.2008
		US 2008-0112145 A1	15.05.2008
		US 2008-0112146 A1	15.05.2008
		US 2008-0112147 A1	15.05.2008
		US 2008-0112148 A1	15.05.2008
		US 2008-0112149 A1	15.05.2008
		US 2008-0116912 A1	22.05.2008
		US 2008-0116913 A1	22.05.2008
		US 2008-0116914 A1	22.05.2008
		US 2008-0116915 A1	22.05.2008
		US 2008-0116916 A1	22.05.2008
		US 2008-0117611 A1	22.05.2008
		US 2008-0117612 A1	22.05.2008
		US 2008-0117613 A1	22.05.2008
		US 2008-0121879 A1	29.05.2008
		US 2008-0123310 A1	29.05.2008
		US 2008-0129319 A1	05.06.2008
		US 2008-0129320 A1	05.06.2008
		US 2008-0132094 A1	05.06.2008
		US 2009-0128176 A1	21.05.2009

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/029712

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 2009-0189288 A1	30.07.2009
		US 2009-0308756 A1	17.12.2009
		US 2009-0315579 A1	24.12.2009
		US 2010-0045266 A1	25.02.2010
		US 2010-0045317 A1	25.02.2010
		US 2010-0045318 A1	25.02.2010
		US 2010-0045320 A1	25.02.2010
		US 2010-0045321 A1	25.02.2010
		US 2010-0045324 A1	25.02.2010
		US 2010-0052715 A1	04.03.2010
		US 6295729 B1	02.10.2001
		US 6300780 B1	09.10.2001
		US 6329827 B1	11.12.2001
		US 6334247 B1	01.01.2002
		US 6452406 B1	17.09.2002
		US 6526655 B2	04.03.2003
		US 6708403 B2	23.03.2004
		US 6722032 B2	20.04.2004
		US 6880245 B2	19.04.2005
		US 7276919 B1	02.10.2007
		US 7332922 B2	19.02.2008
		US 7368924 B2	06.05.2008
		US 7495342 B2	24.02.2009
		US 7538565 B1	26.05.2009
		WO 98-11445 A1	19.03.1998