(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
13 July 2017 (13.07.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/119922 A1

(51) International Patent Classification:
H04L 1/00 (2006.01)

(21) International Application Number:
PCT/US2016/032931

(22) International Filing Date:
17 May 2016 (17.05.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/274,545 4 January 2016 (04.01.2016) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to the identity of the inventor (Rule 4.17(i))*

Published:

— *with international search report (Art. 21(3))*

(54) Title: ENCODING AND DECODING USING LOW-DENSITY PARITY-CHECK MATRICES

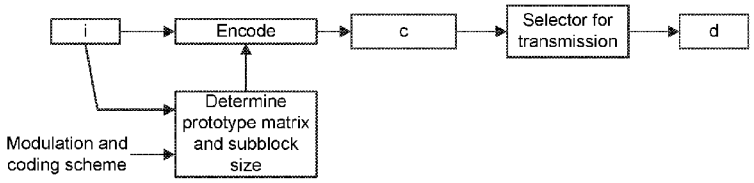

FIG. 2

(57) Abstract: Technology for a user equipment (UE) operable to encode information for transmission to an eNodeB is disclosed. The UE can acquire a block of information bits. The UE can select a modulation and coding scheme. The UE can determine a matrix prototype and a code word sub-block size based on a size of the block of information bits and the modulation and coding scheme. The UE can encode at least a portion of the block of information bits to obtain an encoded code word block. At least the portion of the block of information bits can be encoded based on the matrix prototype and the code word sub-block size. The UE can select a subset of bits from the encoded code word block. The UE can generate the subset of bits for transmission to an eNodeB.

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ENCODING AND DECODING USING LOW-DENSITY PARITY-CHECK MATRICES

BACKGROUND

[0001] Wireless mobile communication technology uses various standards and protocols to transmit data between a node (e.g., a transmission station) and a wireless device (e.g., a mobile device). Some wireless devices communicate using orthogonal frequency-division multiple access (OFDMA) in a downlink (DL) transmission and single carrier frequency division multiple access (SC-FDMA) in uplink (UL). Standards and protocols that use orthogonal frequency-division multiplexing (OFDM) for signal transmission include the third generation partnership project (3GPP) long term evolution (LTE), the Institute of Electrical and Electronics Engineers (IEEE) 702.16 standard (e.g., 702.16e, 702.16m), which is commonly known to industry groups as WiMAX (Worldwide interoperability for Microwave Access), and the IEEE 702.11 standard, which is commonly known to industry groups as WiFi.

[0002] In 3GPP radio access network (RAN) LTE systems, the node can be a combination of Evolved Universal Terrestrial Radio Access Network (E-UTRAN) Node Bs (also commonly denoted as evolved Node Bs, enhanced Node Bs, eNodeBs, or eNBs) and Radio Network Controllers (RNCs), which communicates with the wireless device, known as a user equipment (UE). The downlink (DL) transmission can be a communication from the node (e.g., eNodeB) to the wireless device (e.g., UE), and the uplink (UL) transmission can be a communication from the wireless device to the node.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Features and advantages of the disclosure will be apparent from the detailed description which follows, taken in conjunction with the accompanying drawings, which together illustrate, by way of example, features of the disclosure; and, wherein:

[0004] FIGS. 1A to 1H illustrate matrix prototypes corresponding to a coding rate of 8/9 and sub-block sizes of 12, 24, 36, 48, 60, 72, 84 and 96, respectively, in accordance with an example;

[0005] FIG. 2 illustrates a technique for encoding information using a selected matrix prototype in accordance with an example;

[0006] FIG. 3 illustrates a technique for decoding information using a selected matrix prototype in accordance with an example;

[0007] FIG. 4 depicts functionality of a user equipment (UE) operable to encode information for transmission to an eNodeB in accordance with an example;

[0008] FIG. 5 depicts functionality of a user equipment (UE) operable to decode information received from an eNodeB in accordance with an example;

[0009] FIG. 6 depicts a flowchart of a machine readable storage medium having instructions embodied thereon for encoding and decoding information at an eNodeB in accordance with an example;

[0010] FIG. 7 illustrates a diagram of a wireless device (e.g., UE) and a node (e.g., eNodeB) in accordance with an example; and

[0011] FIG. 8 illustrates a diagram of a wireless device (e.g., UE) in accordance with an example.

[0012] Reference will now be made to the exemplary embodiments illustrated, and specific language will be used herein to describe the same. It will nevertheless be understood that no limitation of the scope of the technology is thereby intended.

DETAILED DESCRIPTION

[0013] Before the present technology is disclosed and described, it is to be understood that this technology is not limited to the particular structures, process actions, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular examples only and is not intended to be limiting. The same reference numerals in different drawings represent the same element. Numbers provided in flow charts and processes are provided for clarity in illustrating actions and operations and do not necessarily indicate a particular order or sequence.

EXAMPLE EMBODIMENTS

[0014] An initial overview of technology embodiments is provided below and then specific technology embodiments are described in further detail later. This initial summary is intended to aid readers in understanding the technology more quickly but is not intended to identify key features or essential features of the technology nor is it intended to limit the scope of the claimed subject matter.

[0015] Information can be transmitted from a transmitter to a receiver over a communication channel. Noise inherent in the communication channel can produce errors in transmitted information. To mitigate the effect of noise in the communication channel, redundancy can be included in the transmission, and the redundancy can enable the receiver to accurately reconstruct original information despite the noise in the communication channel. The redundancy allows the receiver to detect a limited number of errors that can occur during transmission, and often to correct these errors without retransmission.

[0016] A number of possible coding schemes can be used for determining an amount and nature of the redundancy to include in the transmitted information. The redundancy can be in the form of redundant bits, which are added to the transmitted information. The coding schemes can vary depending on the desired level of error correction, decoding complexity, the ability to locate/correct or recover from the errors, the ability to correct burst errors, and other various characteristics. In addition, a number of codes can be available for a particular coding scheme, wherein the codes can vary in terms of the number of information bits and the number of redundant bits (or sometimes also known as parity bits). The codes can be systematic or non-systematic. With respect to systematic codes, redundant bits can be added to, for example, the end of a stream of information bits. With respect to non-systematic codes, some or all of the information bits may not be present in a transmitted bit stream.

[0017] The coding scheme and actual codes can be selected for use based on various criteria. For example, these criteria include an expected block error rate (BLER) of the transmission system, a desired BLER, an amount of transmission overhead associated with a particular code, an amount of processing to process the code, etc. In addition, a maximum fraction of errors (or missing bits that can be corrected) can be determined

based on the coding scheme used, so different coding schemes can be suitable for different conditions.

[0018] One exemplary code that can be used for encoding and decoding information in a noisy communication channel is a low-density parity-check (LDPC) code. LDPC codes are error correcting codes (i.e., codes that can be used for forward error correction or channel coding). In other words, the transmitter can encode data in a redundant manner using an LDPC code, and the receiver can decode the data using the LDPC decoding algorithm (e.g., belief propagation) such that any errors in the transmission are corrected. LDPC codes are parity check codes with a parity check matrix containing binary 0s and 1s. The parity check matrix can be defined in terms of a matrix dimension (e.g., information block length and number of parity-checks), a number of 1s per column, and a number of 1s per row. The 1s in the parity check matrix can be randomly distributed within the parity check matrix. For efficient encoding/decoding, the parity check matrix can be formed using submatrices having only a single 1 per column and per row. Therefore, for a given code, a number of parity check matrixes can be formed with varying block lengths by selecting different dimensions for the submatrices.

[0019] In the present technology, LDPC codes can be used for 3GPP systems, such as fifth generation (5G) cellular systems. The LDPC codes can include parity check matrices that support a defined coding rate. The defined code rate can indicate a proportion of a data-stream that is useful (non-redundant). For example, if the code rate is k/n, for every k bits of useful information, the coder generates n bits of total codeword, of which n-k are redundancy bits or parity bits. In a specific example, the present technology describes LDPC codes with parity check matrices that offer a coding rate of 8/9 and can support a data rate of 5 gigabits per second (Gbps). The parity check matrices can be used for supporting different block sizes. In addition, these parity check matrices can be specifically targeted for 5G applications, and therefore, superior to simply reusing 802.11n LDPC parity check matrices.

[0020] In one example, the 3GPP LTE standard supports adaptive modulation and coding schemes. For example, the 3GPP LTE standard supports a granular set of resource allocations, modulation and coding schemes, packet sizes (or transport block sizes), and rate-compatible channel coding. The adaptive modulation and coding schemes can be

based on turbo codes with circular buffer rate-matching for incremental redundancy (IR) hybrid automatic repeat request (HARQ) support.

[0021] The supported set of spectral efficiencies can range from 0.1 bits per second per Hertz (bps/Hz) to 7.6 bps/Hz for 256 quadrature amplitude modulation (QAM). Modulation and coding scheme (MCS) levels can be defined to correspond to approximately 1 decibel (dB) step sizes. Rate-compatible channel coding can be used to encode a packet or transport block (TB) at an arbitrary coding rate according to a selected MCS level, and multiple redundancy versions can be defined to support HARQ operation.

[0022] In one example, 802.11n/11ac LDPC code design is based on a limited set of code rates and block sizes. PHY protocol data unit (PPDU) encoding rules can be used to encode and transmit a packet on available channel resources. The PPDU encoding rules can include mechanisms for shortening and puncturing with respect to encoding the transmitting the packet. In the shortening mechanism, a packet of small size can be zero-padded and encoded with a parity-check matrix, and the zero-padding can be removed after encoding to achieve an effective lower code rate. In the puncturing mechanism, a packet can be encoded with a parity-check matrix, and the parity bits after encoding can be punctured to increase the effective code rate.

[0023] In one example, structured LDPC codes have been adopted in wireless technology standards, such as IEEE802.11n, IEEE802.11ac, and IEEE802.11ad. Structured LDPC codes based on shifted identity matrices can allow for vectorized operations that facilitate high throughput encoding and decoding. In addition, structured LDPC codes provide a framework to support a wide range of block sizes and code rates.

[0024] In one example, a LDPC code can have a codeword length $n = z \cdot n_b$, an information block $k = z \cdot k_b$, and a shift size or subblock size z. The LDPC code can have a code rate $r = k/n = k_b/n_b$, where the matrix prototype (as defined below) for the LDPC code has dimensions n_b - k_b x n_b. An LDPC encoder can encode an information block $i = i_0, i_1, i_2 \ldots i_{k-1}$ into a codeword c, of size n, $c = (c_0, c_1, \ldots c_{k-1}, c_k \ldots c_{n-1})$. In systematic encoding, the first k bits of the codeword are typically the same as the information bits, i.e., $c_j = i_j$, for j = 0 to k-1. The codeword c satisfies the parity-check equation $H \cdot c^T = 0$, where H is an n-k x n parity-check matrix. In other words, the LDPC code can have a particular code rate, and for a given number of information bits, parity check bits can be

added to the information bits. The parity check bits can be obtained by solving the parity check equation ($H \cdot c^T = 0$).

[0025] In one example, in these structured LDPC codes, each parity check matrix can be partitioned into square blocks, or sub matrices, of size z x z, wherein z is an integer. These sub matrices can be cyclic permutations of an identity matrix (or shifted identity matrix) or null matrices. A cyclic permutation matrix P_i can be obtained from the zxz identity matrix by cyclically shifting the columns to the right by i elements.

[0026] Three different exemplary sub-matrices are shown below (P_0, P_4 and P_2). The matrix P_0 is a zxz identity matrix, wherein z=5. The matrix P_0 is shifted right by a value of 0. The matrix P_4 indicates an identity matrix that is shifted right by a value of 4. In other words, each row of matrix P_0 is rotated cyclically by 4 to yield P_0. Similarly, P_2 is shifted right by a value of 2. Thus, each row of matrix P_0 is rotated cyclically by 2 to yield P_2. In addition, a null matrix can be used when every element of the sub matrix is 0.

$$P_0 = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}, P_4 = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix}, P_2 = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix}$$

[0027] In one example, a matrix H_r89_z96 is shown below.

31 1 0 - 76 45 29 - - 20 45 90 2 - 29 24 23 13 43 38 1 74 10 70 18 14 48 16 5 65 90 88 1 0 - -

20 - 40 15 - 51 38 49 36 - 28 91 30 92 - 15 13 24 91 59 13 37 7 26 94 18 58 8 42 95 42 14 - 0 0 -

- 87 33 27 2 - 27 76 22 11 - 3 28 82 23 - - 37 62 40 77 55 18 78 22 37 95 48 71 9 87 36 0 - 0 0

0 34 - 18 23 8 - 61 87 30 17 - - 65 38 0 36 25 58 61 19 35 65 9 90 72 13 8 55 15 86 59 1 - - 0

[0028] The matrix H_r89_z96 is for a coding rate of 8/9 with a sub matrix dimension (or z) that is equal to 96 and a code word length equal to 3456. In the matrix H_r89_z96, each non-negative integer i denotes the cyclic permutation matrix P_i and negative integer entries (-1) or null entries (-) denote null or zero submatrices. The matrix H_r89_z96 has 4 rows and 36 columns. To achieve a code rate of 8/9, the parity-check matrix can encode an information size of 32*96 to get a codeword of 36*96 of which 32*96 are information bits, and 4*96 are codeword bits. In this case, $n_b = 36$, $k_b = 32$ and n_b-$k_b = 4$. The first entry in the matrix H_r89_z96 is 31. The 31 is akin to P_{31}. In other words, a 96x96

identity matrix is rotated to the right by a value of 31, and this sub matrix corresponds to the 31 in the matrix H_r89_z96. Similarly, the second entry in the matrix H_r89_z96 is 1, which indicates that the 96x96 identity matrix is rotated to the right by a value of 1, and this sub matrix corresponds to the 1 in the matrix H_r89_z96. The matrix H_r89_z96 can be referred to as a matrix prototype. The matrix prototype is essentially used as a short hand notation.

[0029] For 5G cellular systems, for a coding rate of 8/9, supported codeword sizes can be defined for different shift sizes. For example, the supported shift sizes (z) can include 12, 24, 36, 48, 60, 72, 84 and 96. Assuming a matrix prototype of dimensions 4 x 36 (i.e., n_b = 36 and k_b= 32), this corresponds to codeword block sizes of z x 36, which are equal to 432, 864, 1296, 1728, 2160, 2592, 3024 and 3456, respectively. The 4 x 36 matrix yields a coding rate of (36 – 4) / 36 or 8/9. For each codeword block size, a matrix prototype can be provided. To decode each of these matrix prototypes, each row can be processed as a parity check equation. Dashed entries in the matrix prototype row can participate in the parity check equation (i.e., $H \cdot c^T = 0$), whereas non-dashed entries in the matrix prototype row do not participate in the parity check equation.

[0030] FIGS. 1A to 1H illustrate matrix prototypes corresponding to a coding rate of 8/9 and sub-block sizes of 12, 24, 36, 48, 60, 72, 84 and 96, respectively.

[0031] As shown in FIG 1A, the matrix H_r89_z12 with a sub block size or shift size (z) of 12 is a 4x36 matrix as follows:

5 3 5 - 8 6 6 - - 8 10 11 3 - 10 2 11 9 6 11 11 10 2 2 1 5 7 3 7 11 9 5 1 0 - -
7 - 6 5 - 11 5 2 11 - 4 8 0 10 - 7 4 8 2 1 7 4 2 8 4 7 11 4 3 3 7 6 - 0 0 -
- 10 1 6 9 - 1 7 11 11 - 5 2 6 4 - - 11 6 10 2 3 6 5 5 2 5 11 8 7 11 5 0 - 0 0
8 0 - 0 0 10 - 0 8 0 5 - - 4 7 9 4 2 5 5 11 11 10 1 11 10 10 6 4 1 10 7 1 - - 0.

[0032] As shown in FIG 1B, the matrix H_r89_z24 with a sub block size or shift size (z) of 24 is a 4x36 matrix as follows:

20 5 6 - 21 8 20 - - 13 12 6 12 - 15 13 1 18 13 15 9 9 3 8 9 21 22 5 10 16 14 2 1 0 - -
4 - 2 21 - 13 9 1 10 - 10 10 0 16 - 16 7 12 4 1 7 3 19 3 6 0 14 14 15 23 7 4 - 0 0 -
- 19 9 2 7 - 2 1 8 17 - 12 3 2 8 - - 13 3 17 1 16 4 2 2 1 22 1 7 0 11 20 0 - 0 0
23 18 - 15 17 21 - 10 16 14 21 - - 7 2 5 6 1 1 4 0 1 18 7 19 0 5 23 14 15 17 16 1 - - 0.

[0033] As shown in FIG 1C, the matrix H_r89_z36 with a sub block size or shift size (z) of 36 is a 4x36 matrix as follows:

2 35 31 - 18 15 3 - - 10 2 13 14 - 22 25 5 32 2 29 5 17 26 22 12 17 20 35 30 29 3 15 1 0 - -

29 - 20 10 - 5 5 15 21 - 12 28 30 18 - 19 30 4 16 2 18 4 22 22 22 24 21 30 19 15 7 14 - 0 0 -
- 11 19 20 1 - 33 17 0 11 - 31 31 1 25 - - 15 11 24 7 25 3 18 23 4 25 21 28 7 21 22 0 - 0 0
12 7 - 12 8 9 - 27 32 24 1 - - 6 18 26 8 12 25 30 11 5 24 20 1 1 1 15 6 31 31 3 1 - - 0.

[0034] As shown in FIG 1D, the matrix H_r89_z48 with a sub block size or shift size (z) of 48 is a 4x36 matrix as follows:

13 20 26 - 6 35 42 - - 22 17 4 14 - 13 29 38 15 34 22 7 28 23 26 0 41 13 45 20 42 27 7 1 0 - -
8 - 28 46 - 25 41 30 11 - 13 22 41 26 - 29 25 15 3 11 12 27 8 11 42 47 35 26 8 5 15 21 - 0 0 -
- 18 45 21 12 - 44 4 47 17 - 33 44 24 14 - - 23 31 10 3 20 26 42 39 26 12 23 15 18 47 27 0 - 0 0
44 27 - 10 38 31 - 10 12 40 16 - - 21 24 5 23 9 36 25 5 37 38 0 5 21 44 22 9 0 39 15 1 - - 0.

[0035] As shown in FIG 1E, the matrix H_r89_z60 with a sub block size or shift size (z) of 60 is a 4x36 matrix as follows:

38 55 54 - 25 54 19 - - 18 47 55 2 - 10 55 52 20 5 55 17 36 28 4 59 6 31 6 22 21 33 14 1 0 - -
38 - 35 44 - 28 11 3 19 - 11 8 58 59 - 44 4 29 47 41 54 37 47 46 14 17 50 2 24 18 40 59 - 0 0 -
- 47 59 34 2 - 8 49 8 2 - 48 6 53 19 - - 59 32 9 0 53 10 4 53 19 59 6 29 44 16 55 0 - 0 0
47 52 - 33 16 36 - 5 31 4 36 - - 2 51 31 14 12 31 7 55 37 11 24 59 48 3 27 59 9 13 5 1 - - 0.

[0036] As shown in FIG 1F, the matrix H_r89_z72 with a sub block size or shift size (z) of 72 is a 4x36 matrix as follows:

8 65 69 - 6 7 0 - - 58 6 58 7 - 24 65 57 64 36 32 54 15 39 24 50 62 60 70 70 12 8 10 1 0 - -
68 - 8 34 - 34 53 28 6 - 37 14 51 12 - 34 7 22 42 25 31 41 12 29 58 32 60 14 22 62 18 56 - 0 0 -
- 51 70 33 4 - 15 13 62 17 - 27 39 20 0 - - 37 7 29 71 59 44 34 6 35 40 37 57 37 59 44 0 - 0 0
47 59 - 4 22 45 - 17 20 51 29 - - 16 49 67 1 71 47 3 13 62 0 13 0 47 7 49 44 48 57 25 1 - - 0.

[0037] As shown in FIG 1G, the matrix H_r89_z84 with a sub block size or shift size (z) of 84 is a 4x36 matrix as follows:

27 27 7 - 23 40 76 - - 5 49 16 37 - 49 80 54 28 33 46 70 78 70 82 35 80 83 79 9 27 5 16 1 0 - -
51 - 45 5 - 53 83 46 27 - 48 42 0 15 - 24 74 13 50 58 63 48 53 22 46 76 40 40 51 18 11 10 - 0 0 -
- 36 5 53 65 - 65 66 64 52 - 68 16 22 43 - - 40 8 82 64 13 72 74 40 53 29 80 57 13 36 24 0 - 0 0
10 3 - 82 76 37 - 37 73 73 38 - - 46 0 61 70 32 27 38 30 76 27 49 50 76 37 27 64 35 1 49 1 - - 0.

[0038] As shown in FIG 1H, the matrix H_r89_z96 with a sub block size or shift size (z) of 96 is a 4x36 matrix as follows:

31 1 0 - 76 45 29 - - 20 45 90 2 - 29 24 23 13 43 38 1 74 10 70 18 14 48 16 5 65 90 88 1 0 - -
20 - 40 15 - 51 38 49 36 - 28 91 30 92 - 15 13 24 91 59 13 37 7 26 94 18 58 8 42 95 42 14 - 0 0 -
- 87 33 27 2 - 27 76 22 11 - 3 28 82 23 - - 37 62 40 77 55 18 78 22 37 95 48 71 9 87 36 0 - 0 0
0 34 - 18 23 8 - 61 87 30 17 - - 65 38 0 36 25 58 61 19 35 65 9 90 72 13 8 55 15 86 59 1 - - 0.

[0039] In one example, the prototype matrices can be designed to reduce a number of length-4 and length-6 cycles in a Tanner graph corresponding to the prototype matrices. In the construction of the prototype matrix, when assigning a shift size for each entry, the

algorithm can run through different candidate values and select a suitable value that minimizes the number of cycles. In general, Tanner graphs are bipartite graphs used to state constraints or equations which specify error correcting codes. In coding theory, Tanner graphs can be used to construct longer codes from smaller codes, and both encoders and decoders can employ Tanner graphs. Since the prototype matrices reduce the number of length-4 and length-6 cycles in the Tanner graph corresponding to the prototype matrices, the LDPC codes corresponding to these prototype matrices have favorable block error rate performance and relatively low error floors.

[0040] FIG. 2 illustrates an exemplary technique for encoding information using a selected matrix prototype. A transmitting device can acquire an information block for transmission. The information block can include information bits (i). The transmitting device can identify a modulation and coding scheme associated with the transmission. The transmitting device can determine a matrix prototype and a sub block size based on a size of the information block and the modulation and coding scheme. In some cases, the matrix prototype and subblock sizes to be used may be explicitly indicated by the entity requesting the transmission. The matrix prototype and corresponding sub block size that is selected can be one of the matrix prototypes shown in FIGS. 1A-1H. The transmitting device can encode at least a portion of the information block based on the matrix prototype and the sub block size to obtain an encoded code word (c). The transmitting device can select a set of bits (d) from the encoded code word for transmission to a receiving device. As a non-limiting example, starting bits of the encoded code word can be selected for transmission.

[0041] As an example, the information block size can be 3072 bits, and the modulation and coding scheme can correspond to a spectral efficiency of 5.4 bits per symbol per Hertz, which at 64-QAM corresponds to a coding rate of 5.4/6 = 0.9. Since this coding rate can be supported using a parity-check matrix of coding rate 8/9, the transmitting device can determine a matrix prototype corresponding to a subblock size of 3072/32 = 96 (as shown in FIG. 1H). The matrix prototype and the subblock size can be used to encode the information block and obtain codeword bits. After obtaining the codeword bits, the transmitting device can select a set of bits (e.g., 3072/0.9 rounded off to a nearest multiple of 6, which is the modulation order for 64-QAM) from the codeword bits to obtain bits for transmission. The bits can correspond to an MCS of 5.4 bits per symbol per

Hertz. The transmitting device can transmit the set of bits to the receiving device.

[0042] FIG. 3 illustrates an exemplary technique for decoding information using a selected matrix prototype. A receiving device can acquire a received block of bits (y), a length of information block size, and an associated modulation and coding scheme. The receiving device can receive the block of bits (y) from the transmitting device. The receiving device can determine a matrix prototype and a subblock size based on the modulation and coding scheme and the information block size. The matrix prototype and corresponding sub block size that is selected can be one of the matrix prototypes shown in FIGS. 1A-1H. The receiving block can decode the received block of bits based on the matrix prototype and the subblock size to obtain an estimated information block (i).

[0043] In one example, the receiving device can decode the received block of bits using a layered belief propagation scheme or another decoding technique used to decode LDPC codes. For example, the layered belief propagation scheme can be used to decode the parity check matrices. If there are a defined number of rows in the parity check matrix, each row can be considered as a layer. The belief propagation can solve the parity check equation on a row-by-row basis. The first row can process its parity check equation, and results of the first row can be passed on to the second row. The second row can process its parity check equation using the previous results, and the second row can pass its results to the third row, and so on.

[0044] Another example provides functionality 400 of a user equipment (UE) operable to encode information for transmission to an eNodeB, as shown in FIG. 4. The UE can comprise one or more processors and memory configured to: acquire, at the UE, a block of information bits, as in block 410. The UE can comprise one or more processors and memory configured to: select, at the UE, a modulation and coding scheme, as in block 420. The UE can comprise one or more processors and memory configured to: determine, at the UE, a matrix prototype and a code word sub-block size based on a size of the block of information bits and the modulation and coding scheme, as in block 430. The UE can comprise one or more processors and memory configured to: encode, at the UE, at least a portion of the block of information bits to obtain an encoded code word block, wherein at least the portion of the block of information bits is encoded based on the matrix prototype and the code word sub-block size, as in block 440. The UE can comprise one or more

processors and memory configured to: select, at the UE, a subset of bits from the encoded code word block, as in block 450. The UE can comprise one or more processors and memory configured to: generate, at the UE, the subset of bits for transmission to an eNodeB, as in block 460.

[0045] Another example provides functionality 500 of a user equipment (UE) operable to decode information received from an eNodeB, as shown in FIG. 5. The UE can comprise one or more processors and memory configured to: identify, at the UE, a block of bits received from the eNodeB, wherein the block of bits is associated with a block size length and a modulation and coding scheme, as in block 510. The UE can comprise one or more processors and memory configured to: determine, at the UE, a matrix prototype and a code word sub-block size based on the block size length and the modulation and coding scheme, as in block 520. The UE can comprise one or more processors and memory configured to: decode, at the UE, the block of bits received from the eNodeB to obtain a decoded block of information bits, wherein the decoded block of information bits is obtained based on the matrix prototype and the code word sub-block size, as in block 530.

[0046] Another example provides at least one machine readable storage medium having instructions 600 embodied thereon for encoding and decoding information at an eNodeB, as shown in FIG. 6. The instructions can be executed on a machine, where the instructions are included on at least one computer readable medium or one non-transitory machine readable storage medium. The instructions when executed perform: identifying, using one or more processors of the eNodeB, a block of information bits for transmission from the eNodeB to a user equipment (UE), as in block 610. The instructions when executed perform: determining, using the one or more processors of the eNodeB, a low density parity check (LDPC) matrix and a code word sub-block size based on a size of the block of information bits and a modulation and coding scheme, as in block 620. The instructions when executed perform: encoding, using the one or more processors of the eNodeB, at least a portion of the block of information bits to obtain an encoded code word block, wherein at least the portion of the block of information bits is encoded based on the LDPC matrix and the code word sub-block size, as in block 630. The instructions when executed perform: selecting, using the one or more processors of the eNodeB, a subset of bits from the encoded code word block, as in block 640. The instructions when executed perform: formatting, using the one or more processors of the eNodeB, the subset

of bits for transmission to the UE in the E-UTRAN, as in block 650.

[0047] FIG. 7 provides an example illustration of a user equipment (UE) device 700 and a nose 720. The UE device 700 can include a wireless device, a mobile station (MS), a mobile wireless device, a mobile communication device, a tablet, a handset, or other type of wireless device. The UE device 700 can include one or more antennas configured to communicate with the node 720 or transmission station, such as a base station (BS), an evolved Node B (eNB), a baseband unit (BBU), a remote radio head (RRH), a remote radio equipment (RRE), a relay station (RS), a radio equipment (RE), a remote radio unit (RRU), a central processing module (CPM), or other type of wireless wide area network (WWAN) access point. The node 720 can include one or more processors 722 and memory 724. The UE device 700 can be configured to communicate using at least one wireless communication standard including 3GPP LTE, WiMAX, High Speed Packet Access (HSPA), Bluetooth, and WiFi. The UE device 700 can communicate using separate antennas for each wireless communication standard or shared antennas for multiple wireless communication standards. The UE device 700 can communicate in a wireless local area network (WLAN), a wireless personal area network (WPAN), and/or a WWAN.

[0048] In some embodiments, the UE device 700 may include application circuitry 702, baseband circuitry 704, Radio Frequency (RF) circuitry 706, front-end module (FEM) circuitry 708 and one or more antennas 710, coupled together at least as shown.

[0049] The application circuitry 702 may include one or more application processors. For example, the application circuitry 702 may include circuitry such as, but not limited to, one or more single-core or multi-core processors. The processor(s) may include any combination of general-purpose processors and dedicated processors (e.g., graphics processors, application processors, etc.). The processors may be coupled with and/or may include a storage medium, and may be configured to execute instructions stored in the storage medium to enable various applications and/or operating systems to run on the system.

[0050] The baseband circuitry 704 may include circuitry such as, but not limited to, one or more single-core or multi-core processors. The baseband circuitry 704 may include one or more baseband processors and/or control logic to process baseband signals

received from a receive signal path of the RF circuitry 706 and to generate baseband signals for a transmit signal path of the RF circuitry 706. Baseband processing circuity 704 may interface with the application circuitry 702 for generation and processing of the baseband signals and for controlling operations of the RF circuitry 706. For example, in some embodiments, the baseband circuitry 704 may include a second generation (2G) baseband processor 704a, third generation (3G) baseband processor 704b, fourth generation (4G) baseband processor 704c, and/or other baseband processor(s) 704d for other existing generations, generations in development or to be developed in the future (e.g., fifth generation (5G), 6G, etc.). The baseband circuitry 704 (e.g., one or more of baseband processors 704a-d) may handle various radio control functions that enable communication with one or more radio networks via the RF circuitry 706. The radio control functions may include, but are not limited to, signal modulation/demodulation, encoding/decoding, radio frequency shifting, etc. In some embodiments, modulation/demodulation circuitry of the baseband circuitry 704 may include Fast-Fourier Transform (FFT), precoding, and/or constellation mapping/demapping functionality. In some embodiments, encoding/decoding circuitry of the baseband circuitry 704 may include convolution, tail-biting convolution, turbo, Viterbi, and/or Low Density Parity Check (LDPC) encoder/decoder functionality. Embodiments of modulation/demodulation and encoder/decoder functionality are not limited to these examples and may include other suitable functionality in other embodiments.

[0051] In some embodiments, the baseband circuitry 704 may include elements of a protocol stack such as, for example, elements of an evolved universal terrestrial radio access network (EUTRAN) protocol including, for example, physical (PHY), media access control (MAC), radio link control (RLC), packet data convergence protocol (PDCP), and/or radio resource control (RRC) elements. A central processing unit (CPU) 704e of the baseband circuitry 704 may be configured to run elements of the protocol stack for signaling of the PHY, MAC, RLC, PDCP and/or RRC layers. In some embodiments, the baseband circuitry may include one or more audio digital signal processor(s) (DSP) 704f. The audio DSP(s) 104f may be include elements for compression/decompression and echo cancellation and may include other suitable processing elements in other embodiments. Components of the baseband circuitry may

be suitably combined in a single chip, a single chipset, or disposed on a same circuit board in some embodiments. In some embodiments, some or all of the constituent components of the baseband circuitry 704 and the application circuitry 702 may be implemented together such as, for example, on a system on a chip (SOC).

[0052] In some embodiments, the baseband circuitry 704 may provide for communication compatible with one or more radio technologies. For example, in some embodiments, the baseband circuitry 704 may support communication with an evolved universal terrestrial radio access network (EUTRAN) and/or other wireless metropolitan area networks (WMAN), a wireless local area network (WLAN), a wireless personal area network (WPAN). Embodiments in which the baseband circuitry 704 is configured to support radio communications of more than one wireless protocol may be referred to as multi-mode baseband circuitry.

[0053] The RF circuitry 706 may enable communication with wireless networks using modulated electromagnetic radiation through a non-solid medium. In various embodiments, the RF circuitry 706 may include switches, filters, amplifiers, etc. to facilitate the communication with the wireless network. RF circuitry 706 may include a receive signal path which may include circuitry to down-convert RF signals received from the FEM circuitry 708 and provide baseband signals to the baseband circuitry 704. RF circuitry 706 may also include a transmit signal path which may include circuitry to up-convert baseband signals provided by the baseband circuitry 704 and provide RF output signals to the FEM circuitry 708 for transmission.

[0054] In some embodiments, the RF circuitry 706 may include a receive signal path and a transmit signal path. The receive signal path of the RF circuitry 706 may include mixer circuitry 706a, amplifier circuitry 706b and filter circuitry 706c. The transmit signal path of the RF circuitry 706 may include filter circuitry 706c and mixer circuitry 706a. RF circuitry 706 may also include synthesizer circuitry 706d for synthesizing a frequency for use by the mixer circuitry 706a of the receive signal path and the transmit signal path. In some embodiments, the mixer circuitry 706a of the receive signal path may be configured to down-convert RF signals received from the FEM circuitry 708 based on the synthesized frequency provided by synthesizer circuitry 706d. The amplifier circuitry 706b may be configured to amplify the down-converted signals and the filter circuitry

706c may be a low-pass filter (LPF) or band-pass filter (BPF) configured to remove unwanted signals from the down-converted signals to generate output baseband signals. Output baseband signals may be provided to the baseband circuitry 704 for further processing. In some embodiments, the output baseband signals may be zero-frequency baseband signals, although this is not a necessity. In some embodiments, mixer circuitry 706a of the receive signal path may comprise passive mixers, although the scope of the embodiments is not limited in this respect.

[0055] In some embodiments, the mixer circuitry 706a of the transmit signal path may be configured to up-convert input baseband signals based on the synthesized frequency provided by the synthesizer circuitry 706d to generate RF output signals for the FEM circuitry 708. The baseband signals may be provided by the baseband circuitry 704 and may be filtered by filter circuitry 706c. The filter circuitry 706c may include a low-pass filter (LPF), although the scope of the embodiments is not limited in this respect.

[0056] In some embodiments, the mixer circuitry 706a of the receive signal path and the mixer circuitry 706a of the transmit signal path may include two or more mixers and may be arranged for quadrature down-conversion and/or up-conversion respectively. In some embodiments, the mixer circuitry 706a of the receive signal path and the mixer circuitry 706a of the transmit signal path may include two or more mixers and may be arranged for image rejection (e.g., Hartley image rejection). In some embodiments, the mixer circuitry 706a of the receive signal path and the mixer circuitry 706a may be arranged for direct down-conversion and/or direct up-conversion, respectively. In some embodiments, the mixer circuitry 706a of the receive signal path and the mixer circuitry 706a of the transmit signal path may be configured for super-heterodyne operation.

[0057] In some embodiments, the output baseband signals and the input baseband signals may be analog baseband signals, although the scope of the embodiments is not limited in this respect. In some alternate embodiments, the output baseband signals and the input baseband signals may be digital baseband signals. In these alternate embodiments, the RF circuitry 706 may include analog-to-digital converter (ADC) and digital-to-analog converter (DAC) circuitry and the baseband circuitry 704 may include a digital baseband interface to communicate with the RF circuitry 706.

[0058] In some dual-mode embodiments, a separate radio IC circuitry may be provided

for processing signals for each spectrum, although the scope of the embodiments is not limited in this respect.

[0059] In some embodiments, the synthesizer circuitry 706d may be a fractional-N synthesizer or a fractional N/N+1 synthesizer, although the scope of the embodiments is not limited in this respect as other types of frequency synthesizers may be suitable. For example, synthesizer circuitry 706d may be a delta-sigma synthesizer, a frequency multiplier, or a synthesizer comprising a phase-locked loop with a frequency divider.

[0060] The synthesizer circuitry 706d may be configured to synthesize an output frequency for use by the mixer circuitry 706a of the RF circuitry 706 based on a frequency input and a divider control input. In some embodiments, the synthesizer circuitry 706d may be a fractional N/N+1 synthesizer.

[0061] In some embodiments, frequency input may be provided by a voltage controlled oscillator (VCO), although that is not a necessity. Divider control input may be provided by either the baseband circuitry 704 or the applications processor 702 depending on the desired output frequency. In some embodiments, a divider control input (e.g., N) may be determined from a look-up table based on a channel indicated by the applications processor 702.

[0062] Synthesizer circuitry 706d of the RF circuitry 706 may include a divider, a delay-locked loop (DLL), a multiplexer and a phase accumulator. In some embodiments, the divider may be a dual modulus divider (DMD) and the phase accumulator may be a digital phase accumulator (DPA). In some embodiments, the DMD may be configured to divide the input signal by either N or N+1 (e.g., based on a carry out) to provide a fractional division ratio. In some example embodiments, the DLL may include a set of cascaded, tunable, delay elements, a phase detector, a charge pump and a D-type flip-flop. In these embodiments, the delay elements may be configured to break a VCO period up into Nd equal packets of phase, where Nd is the number of delay elements in the delay line. In this way, the DLL provides negative feedback to help ensure that the total delay through the delay line is one VCO cycle.

[0063] In some embodiments, synthesizer circuitry 706d may be configured to generate a carrier frequency as the output frequency, while in other embodiments, the output frequency may be a multiple of the carrier frequency (e.g., twice the carrier frequency,

four times the carrier frequency) and used in conjunction with quadrature generator and divider circuitry to generate multiple signals at the carrier frequency with multiple different phases with respect to each other. In some embodiments, the output frequency may be a LO frequency (fLO). In some embodiments, the RF circuitry 706 may include an IQ/polar converter.

[0064] FEM circuitry 708 may include a receive signal path which may include circuitry configured to operate on RF signals received from one or more antennas 710, amplify the received signals and provide the amplified versions of the received signals to the RF circuitry 706 for further processing. FEM circuitry 708 may also include a transmit signal path which may include circuitry configured to amplify signals for transmission provided by the RF circuitry 706 for transmission by one or more of the one or more antennas 710.

[0065] In some embodiments, the FEM circuitry 708 may include a TX/RX switch to switch between transmit mode and receive mode operation. The FEM circuitry may include a receive signal path and a transmit signal path. The receive signal path of the FEM circuitry may include a low-noise amplifier (LNA) to amplify received RF signals and provide the amplified received RF signals as an output (e.g., to the RF circuitry 706). The transmit signal path of the FEM circuitry 708 may include a power amplifier (PA) to amplify input RF signals (e.g., provided by RF circuitry 706), and one or more filters to generate RF signals for subsequent transmission (e.g., by one or more of the one or more antennas 710.

[0066] FIG. 8 provides an example illustration of the wireless device, such as a user equipment (UE), a mobile station (MS), a mobile wireless device, a mobile communication device, a tablet, a handset, or other type of wireless device. The wireless device can include one or more antennas configured to communicate with a node, macro node, low power node (LPN), or, transmission station, such as a base station (BS), an evolved Node B (eNB), a baseband processing unit (BBU), a remote radio head (RRH), a remote radio equipment (RRE), a relay station (RS), a radio equipment (RE), or other type of wireless wide area network (WWAN) access point. The wireless device can be configured to communicate using at least one wireless communication standard such as, but not limited to, 3GPP LTE, WiMAX, High Speed Packet Access (HSPA), Bluetooth, and WiFi. The wireless device can communicate using separate antennas for each wireless

communication standard or shared antennas for multiple wireless communication standards. The wireless device can communicate in a wireless local area network (WLAN), a wireless personal area network (WPAN), and/or a WWAN. The wireless device can also comprise a wireless modem. The wireless modem can comprise, for example, a wireless radio transceiver and baseband circuitry (e.g., a baseband processor). The wireless modem can, in one example, modulate signals that the wireless device transmits via the one or more antennas and demodulate signals that the wireless device receives via the one or more antennas.

[0067] FIG. 8 also provides an illustration of a microphone and one or more speakers that can be used for audio input and output from the wireless device. The display screen can be a liquid crystal display (LCD) screen, or other type of display screen such as an organic light emitting diode (OLED) display. The display screen can be configured as a touch screen. The touch screen can use capacitive, resistive, or another type of touch screen technology. An application processor and a graphics processor can be coupled to internal memory to provide processing and display capabilities. A non-volatile memory port can also be used to provide data input/output options to a user. The non-volatile memory port can also be used to expand the memory capabilities of the wireless device. A keyboard can be integrated with the wireless device or wirelessly connected to the wireless device to provide additional user input. A virtual keyboard can also be provided using the touch screen.

Examples

[0068] The following examples pertain to specific technology embodiments and point out specific features, elements, or actions that can be used or otherwise combined in achieving such embodiments.

[0069] Example 1 includes an apparatus of a user equipment (UE) operable to encode information for transmission to an eNodeB, the apparatus comprising one or more processors and memory configured to: acquire, at the UE, a block of information bits; select, at the UE, a modulation and coding scheme; determine, at the UE, a matrix prototype and a code word sub-block size based on a size of the block of information bits and the modulation and coding scheme; encode, at the UE, at least a portion of the block of information bits to obtain an encoded code word block, wherein at least the portion of

the block of information bits is encoded based on the matrix prototype and the code word sub-block size; select, at the UE, a subset of bits from the encoded code word block; and generate, at the UE, the subset of bits for transmission to an eNodeB.

[0070] Example 2 includes the apparatus of Example 1, further comprising a baseband processor operable to: determine the matrix prototype and the code word sub-block size based on the size of the block of information bits and the modulation and coding scheme; and encode at least the portion of the block of information bits to obtain the encoded code word block; and a transceiver operable to transmit the subset of bits from the UE to the eNodeB.

[0071] Example 3 includes the apparatus of any of Examples 1 to 2, wherein the matrix prototype corresponds to a defined code rate, wherein the defined code rate is a coding rate of 8/9.

[0072] Example 4 includes the apparatus of any of Examples 1 to 3, wherein the modulation and coding scheme corresponds to a spectral efficiency of approximately 5.4 bits per symbol per Hertz.

[0073] Example 5 includes the apparatus of any of Examples 1 to 4, wherein the code word sub-block size is 84 and the matrix prototype is:

27 27 7 - 23 40 76 - - 5 49 16 37 - 49 80 54 28 33 46 70 78 70 82 35 80 83 79 9 27 5 16 1 0 - -

51 - 45 5 - 53 83 46 27 - 48 42 0 15 - 24 74 13 50 58 63 48 53 22 46 76 40 40 51 18 11 10 - 0 0 -

- 36 5 53 65 - 65 66 64 52 - 68 16 22 43 - - 40 8 82 64 13 72 74 40 53 29 80 57 13 36 24 0 - 0 0

10 3 - 82 76 37 - 37 73 73 38 - - 46 0 61 70 32 27 38 30 76 27 49 50 76 37 27 64 35 1 49 1 - - 0.

[0074] Example 6 includes the apparatus of any of Examples 1 to 5, wherein the code word sub-block size is 72 and the matrix prototype is:

8 65 69 - 6 7 0 - - 58 6 58 7 - 24 65 57 64 36 32 54 15 39 24 50 62 60 70 70 12 8 10 1 0 - -

68 - 8 34 - 34 53 28 6 - 37 14 51 12 - 34 7 22 42 25 31 41 12 29 58 32 60 14 22 62 18 56 - 0 0 -

- 51 70 33 4 - 15 13 62 17 - 27 39 20 0 - - 37 7 29 71 59 44 34 6 35 40 37 57 37 59 44 0 - 0 0

47 59 - 4 22 45 - 17 20 51 29 - - 16 49 67 1 71 47 3 13 62 0 13 0 47 7 49 44 48 57 25 1 - - 0.

[0075] Example 7 includes the apparatus of any of Examples 1 to 6, wherein the code word sub-block size is 60 and the matrix prototype is:

38 55 54 - 25 54 19 - - 18 47 55 2 - 10 55 52 20 5 55 17 36 28 4 59 6 31 6 22 21 33 14 1 0 - -

38 - 35 44 - 28 11 3 19 - 11 8 58 59 - 44 4 29 47 41 54 37 47 46 14 17 50 2 24 18 40 59 - 0 0 -
- 47 59 34 2 - 8 49 8 2 - 48 6 53 19 - - 59 32 9 0 53 10 4 53 19 59 6 29 44 16 55 0 - 0 0
47 52 - 33 16 36 - 5 31 4 36 - - 2 51 31 14 12 31 7 55 37 11 24 59 48 3 27 59 9 13 5 1 - - 0.

[0076] Example 8 includes the apparatus of any of Examples 1 to 7, wherein the code word sub-block size is 48 and the matrix prototype is:

13 20 26 - 6 35 42 - - 22 17 4 14 - 13 29 38 15 34 22 7 28 23 26 0 41 13 45 20 42 27 7 1 0 - -
8 - 28 46 - 25 41 30 11 - 13 22 41 26 - 29 25 15 3 11 12 27 8 11 42 47 35 26 8 5 15 21 - 0 0 -
- 18 45 21 12 - 44 4 47 17 - 33 44 24 14 - - 23 31 10 3 20 26 42 39 26 12 23 15 18 47 27 0 - 0 0
44 27 - 10 38 31 - 10 12 40 16 - - 21 24 5 23 9 36 25 5 37 38 0 5 21 44 22 9 0 39 15 1 - - 0.

[0077] Example 9 includes the apparatus of any of Examples 1 to 8, wherein the code word sub-block size is 36 and the matrix prototype is:

2 35 31 - 18 15 3 - - 10 2 13 14 - 22 25 5 32 2 29 5 17 26 22 12 17 20 35 30 29 3 15 1 0 - -
29 - 20 10 - 5 5 15 21 - 12 28 30 18 - 19 30 4 16 2 18 4 22 22 22 24 21 30 19 15 7 14 - 0 0 -
- 11 19 20 1 - 33 17 0 11 - 31 31 1 25 - - 15 11 24 7 25 3 18 23 4 25 21 28 7 21 22 0 - 0 0
12 7 - 12 8 9 - 27 32 24 1 - - 6 18 26 8 12 25 30 11 5 24 20 1 1 1 15 6 31 31 3 1 - - 0.

[0078] Example 10 includes the apparatus of any of Examples 1 to 9, wherein the code word sub-block size is 24 and the matrix prototype is:

20 5 6 - 21 8 20 - - 13 12 6 12 - 15 13 1 18 13 15 9 9 3 8 9 21 22 5 10 16 14 2 1 0 - -
4 - 2 21 - 13 9 1 10 - 10 10 0 16 - 16 7 12 4 1 7 3 19 3 6 0 14 14 15 23 7 4 - 0 0 -
- 19 9 2 7 - 2 1 8 17 - 12 3 2 8 - - 13 3 17 1 16 4 2 2 1 22 1 7 0 11 20 0 - 0 0
23 18 - 15 17 21 - 10 16 14 21 - - 7 2 5 6 1 1 4 0 1 18 7 19 0 5 23 14 15 17 16 1 - - 0.

[0079] Example 11 includes the apparatus of any of Examples 1 to 10, wherein the code word sub-block size is 12 and the matrix prototype is:

5 3 5 - 8 6 6 - - 8 10 11 3 - 10 2 11 9 6 11 11 10 2 2 1 5 7 3 7 11 9 5 1 0 - -
7 - 6 5 - 11 5 2 11 - 4 8 0 10 - 7 4 8 2 1 7 4 2 8 4 7 11 4 3 3 7 6 - 0 0 -
- 10 1 6 9 - 1 7 11 11 - 5 2 6 4 - - 11 6 10 2 3 6 5 5 2 5 11 8 7 11 5 0 - 0 0
8 0 - 0 0 10 - 0 8 0 5 - - 4 7 9 4 2 5 5 11 11 10 1 11 10 10 6 4 1 10 7 1 - - 0.

[0080] Example 12 includes an apparatus of a user equipment (UE) operable to decode information received from an eNodeB, the apparatus comprising one or more processors and memory configured to: identify, at the UE, a block of bits received from the eNodeB,

wherein the block of bits is associated with a block size length and a modulation and coding scheme; determine, at the UE, a matrix prototype and a code word sub-block size based on the block size length and the modulation and coding scheme; and decode, at the UE, the block of bits received from the eNodeB to obtain a decoded block of information bits, wherein the decoded block of information bits is obtained based on the matrix prototype and the code word sub-block size.

[0081] Example 13 includes the apparatus of Example 12, wherein the matrix prototype corresponds to a defined code rate, wherein the defined code rate is a coding rate of 8/9.

[0082] Example 14 includes the apparatus of any of Examples 12 to 13, wherein the modulation and coding scheme corresponds to a spectral efficiency of approximately 5.4 bits per symbol per Hertz.

[0083] Example 15 includes the apparatus of any of Examples 12 to 14, wherein the code word sub-block size is 84 and the matrix prototype is:

27 27 7 - 23 40 76 - - 5 49 16 37 - 49 80 54 28 33 46 70 78 70 82 35 80 83 79 9 27 5 16 1 0 - -
51 - 45 5 - 53 83 46 27 - 48 42 0 15 - 24 74 13 50 58 63 48 53 22 46 76 40 40 51 18 11 10 - 0 0 -
- 36 5 53 65 - 65 66 64 52 - 68 16 22 43 - - 40 8 82 64 13 72 74 40 53 29 80 57 13 36 24 0 - 0 0
10 3 - 82 76 37 - 37 73 73 38 - - 46 0 61 70 32 27 38 30 76 27 49 50 76 37 27 64 35 1 49 1 - - 0.

[0084] Example 16 includes the apparatus of any of Examples 12 to 15, wherein the code word sub-block size is 72 and the matrix prototype is:

8 65 69 - 6 7 0 - - 58 6 58 7 - 24 65 57 64 36 32 54 15 39 24 50 62 60 70 70 12 8 10 1 0 - -
68 - 8 34 - 34 53 28 6 - 37 14 51 12 - 34 7 22 42 25 31 41 12 29 58 32 60 14 22 62 18 56 - 0 0 -
- 51 70 33 4 - 15 13 62 17 - 27 39 20 0 - - 37 7 29 71 59 44 34 6 35 40 37 57 37 59 44 0 - 0 0
47 59 - 4 22 45 - 17 20 51 29 - - 16 49 67 1 71 47 3 13 62 0 13 0 47 7 49 44 48 57 25 1 - - 0.

[0085] Example 17 includes the apparatus of any of Examples 12 to 16, wherein the code word sub-block size is 60 and the matrix prototype is:

38 55 54 - 25 54 19 - - 18 47 55 2 - 10 55 52 20 5 55 17 36 28 4 59 6 31 6 22 21 33 14 1 0 - -
38 - 35 44 - 28 11 3 19 - 11 8 58 59 - 44 4 29 47 41 54 37 47 46 14 17 50 2 24 18 40 59 - 0 0 -
- 47 59 34 2 - 8 49 8 2 - 48 6 53 19 - - 59 32 9 0 53 10 4 53 19 59 6 29 44 16 55 0 - 0 0
47 52 - 33 16 36 - 5 31 4 36 - - 2 51 31 14 12 31 7 55 37 11 24 59 48 3 27 59 9 13 5 1 - - 0.

[0086] Example 18 includes the apparatus of any of Examples 12 to 17, wherein the code

word sub-block size is 48 and the matrix prototype is:

13 20 26 - 6 35 42 - - 22 17 4 14 - 13 29 38 15 34 22 7 28 23 26 0 41 13 45 20 42 27 7 1 0 - -

8 - 28 46 - 25 41 30 11 - 13 22 41 26 - 29 25 15 3 11 12 27 8 11 42 47 35 26 8 5 15 21 - 0 0 -

- 18 45 21 12 - 44 4 47 17 - 33 44 24 14 - - 23 31 10 3 20 26 42 39 26 12 23 15 18 47 27 0 - 0 0

44 27 - 10 38 31 - 10 12 40 16 - - 21 24 5 23 9 36 25 5 37 38 0 5 21 44 22 9 0 39 15 1 - - 0.

[0087] Example 19 includes the apparatus of any of Examples 12 to 18, wherein the code word sub-block size is 36 and the matrix prototype is:

2 35 31 - 18 15 3 - - 10 2 13 14 - 22 25 5 32 2 29 5 17 26 22 12 17 20 35 30 29 3 15 1 0 - -

29 - 20 10 - 5 5 15 21 - 12 28 30 18 - 19 30 4 16 2 18 4 22 22 22 24 21 30 19 15 7 14 - 0 0 -

- 11 19 20 1 - 33 17 0 11 - 31 31 1 25 - - 15 11 24 7 25 3 18 23 4 25 21 28 7 21 22 0 - 0 0

12 7 - 12 8 9 - 27 32 24 1 - - 6 18 26 8 12 25 30 11 5 24 20 1 1 1 15 6 31 31 3 1 - - 0.

[0088] Example 20 includes the apparatus of any of Examples 12 to 19, wherein the code word sub-block size is 24 and the matrix prototype is:

20 5 6 - 21 8 20 - - 13 12 6 12 - 15 13 1 18 13 15 9 9 3 8 9 21 22 5 10 16 14 2 1 0 - -

4 - 2 21 - 13 9 1 10 - 10 10 0 16 - 16 7 12 4 1 7 3 19 3 6 0 14 14 15 23 7 4 - 0 0 -

- 19 9 2 7 - 2 1 8 17 - 12 3 2 8 - - 13 3 17 1 16 4 2 2 1 22 1 7 0 11 20 0 - 0 0

23 18 - 15 17 21 - 10 16 14 21 - - 7 2 5 6 1 1 4 0 1 18 7 19 0 5 23 14 15 17 16 1 - - 0.

[0089] Example 21 includes the apparatus of any of Examples 12 to 20, wherein the code word sub-block size is 12 and the matrix prototype is:

5 3 5 - 8 6 6 - - 8 10 11 3 - 10 2 11 9 6 11 11 10 2 2 1 5 7 3 7 11 9 5 1 0 - -

7 - 6 5 - 11 5 2 11 - 4 8 0 10 - 7 4 8 2 1 7 4 2 8 4 7 11 4 3 3 7 6 - 0 0 -

- 10 1 6 9 - 1 7 11 11 - 5 2 6 4 - - 11 6 10 2 3 6 5 5 2 5 11 8 7 11 5 0 - 0 0

8 0 - 0 0 10 - 0 8 0 5 - - 4 7 9 4 2 5 5 11 11 10 1 11 10 10 6 4 1 10 7 1 - - 0.

[0090] Example 22 includes at least one machine readable storage medium having instructions embodied thereon for encoding and decoding information at an eNodeB, the instructions when executed perform the following: identifying, using one or more processors of the eNodeB, a block of information bits for transmission from the eNodeB to a user equipment (UE); determining, using the one or more processors of the eNodeB, a low density parity check (LDPC) matrix and a code word sub-block size based on a size of the block of information bits and a modulation and coding scheme; encoding, using the

one or more processors of the eNodeB, at least a portion of the block of information bits to obtain an encoded code word block, wherein at least the portion of the block of information bits is encoded based on the LDPC matrix and the code word sub-block size; selecting, using the one or more processors of the eNodeB, a subset of bits from the encoded code word block; and formatting, using the one or more processors of the eNodeB, the subset of bits for transmission to the UE.

[0091] Example 23 includes the at least one machine readable storage medium of Example 22, further comprising instructions when executed perform the following: identifying a block of bits received from the UE, wherein the block of bits is associated with a second block size length and a second modulation and coding scheme; determining a second matrix prototype and a second code word sub-block size based on the second block size length and the second modulation and coding scheme; and decoding the block of bits to obtain a decoded block of information bits, wherein the decoded block of information bits is obtained based on the second matrix prototype and the second code word sub-block size.

[0092] Example 24 includes the at least one machine readable storage medium of any of Examples 22-23, wherein: the matrix prototype corresponds to a coding rate of 8/9; and the modulation and coding scheme corresponds to a spectral efficiency of approximately 5.4 bits per symbol per Hertz.

[0093] Example 25 includes the at least one machine readable storage medium of any of Examples 22-24, wherein:

the code word sub-block size is 84 and the matrix prototype is:

27 27 7 - 23 40 76 - - 5 49 16 37 - 49 80 54 28 33 46 70 78 70 82 35 80 83 79 9 27 5 16 1 0 - -
51 - 45 5 - 53 83 46 27 - 48 42 0 15 - 24 74 13 50 58 63 48 53 22 46 76 40 40 51 18 11 10 - 0 0 -
- 36 5 53 65 - 65 66 64 52 - 68 16 22 43 - - 40 8 82 64 13 72 74 40 53 29 80 57 13 36 24 0 - 0 0
10 3 - 82 76 37 - 37 73 73 38 - - 46 0 61 70 32 27 38 30 76 27 49 50 76 37 27 64 35 1 49 1 - - 0; or

the code word sub-block size is 72 and the matrix prototype is:

8 65 69 - 6 7 0 - - 58 6 58 7 - 24 65 57 64 36 32 54 15 39 24 50 62 60 70 70 12 8 10 1 0 - -
68 - 8 34 - 34 53 28 6 - 37 14 51 12 - 34 7 22 42 25 31 41 12 29 58 32 60 14 22 62 18 56 - 0 0 -
- 51 70 33 4 - 15 13 62 17 - 27 39 20 0 - - 37 7 29 71 59 44 34 6 35 40 37 57 37 59 44 0 - 0 0

47 59 - 4 22 45 - 17 20 51 29 - - 16 49 67 1 71 47 3 13 62 0 13 0 47 7 49 44 48 57 25 1 - - 0; or

the code word sub-block size is 60 and the matrix prototype is:

38 55 54 - 25 54 19 - - 18 47 55 2 - 10 55 52 20 5 55 17 36 28 4 59 6 31 6 22 21 33 14 1 0 - -

38 - 35 44 - 28 11 3 19 - 11 8 58 59 - 44 4 29 47 41 54 37 47 46 14 17 50 2 24 18 40 59 - 0 0 -

- 47 59 34 2 - 8 49 8 2 - 48 6 53 19 - - 59 32 9 0 53 10 4 53 19 59 6 29 44 16 55 0 - 0 0

47 52 - 33 16 36 - 5 31 4 36 - - 2 51 31 14 12 31 7 55 37 11 24 59 48 3 27 59 9 13 5 1 - - 0; or

the code word sub-block size is 48 and the matrix prototype is:

13 20 26 - 6 35 42 - - 22 17 4 14 - 13 29 38 15 34 22 7 28 23 26 0 41 13 45 20 42 27 7 1 0 - -

8 - 28 46 - 25 41 30 11 - 13 22 41 26 - 29 25 15 3 11 12 27 8 11 42 47 35 26 8 5 15 21 - 0 0 -

- 18 45 21 12 - 44 4 47 17 - 33 44 24 14 - - 23 31 10 3 20 26 42 39 26 12 23 15 18 47 27 0 - 0 0

44 27 - 10 38 31 - 10 12 40 16 - - 21 24 5 23 9 36 25 5 37 38 0 5 21 44 22 9 0 39 15 1 - - 0; or

the code word sub-block size is 36 and the matrix prototype is:

2 35 31 - 18 15 3 - - 10 2 13 14 - 22 25 5 32 2 29 5 17 26 22 12 17 20 35 30 29 3 15 1 0 - -

29 - 20 10 - 5 5 15 21 - 12 28 30 18 - 19 30 4 16 2 18 4 22 22 22 24 21 30 19 15 7 14 - 0 0 -

- 11 19 20 1 - 33 17 0 11 - 31 31 1 25 - - 15 11 24 7 25 3 18 23 4 25 21 28 7 21 22 0 - 0 0

12 7 - 12 8 9 - 27 32 24 1 - - 6 18 26 8 12 25 30 11 5 24 20 1 1 1 15 6 31 31 3 1 - - 0; or

the code word sub-block size is 24 and the matrix prototype is:

20 5 6 - 21 8 20 - - 13 12 6 12 - 15 13 1 18 13 15 9 9 3 8 9 21 22 5 10 16 14 2 1 0 - -

4 - 2 21 - 13 9 1 10 - 10 10 0 16 - 16 7 12 4 1 7 3 19 3 6 0 14 14 15 23 7 4 - 0 0 -

- 19 9 2 7 - 2 1 8 17 - 12 3 2 8 - - 13 3 17 1 16 4 2 2 1 22 1 7 0 11 20 0 - 0 0

23 18 - 15 17 21 - 10 16 14 21 - - 7 2 5 6 1 1 4 0 1 18 7 19 0 5 23 14 15 17 16 1 - - 0; or

the code word sub-block size is 12 and the matrix prototype is:

5 3 5 - 8 6 6 - - 8 10 11 3 - 10 2 11 9 6 11 11 10 2 2 1 5 7 3 7 11 9 5 1 0 - -

7 - 6 5 - 11 5 2 11 - 4 8 0 10 - 7 4 8 2 1 7 4 2 8 4 7 11 4 3 3 7 6 - 0 0 -

- 10 1 6 9 - 1 7 11 11 - 5 2 6 4 - - 11 6 10 2 3 6 5 5 2 5 11 8 7 11 5 0 - 0 0

8 0 - 0 0 10 - 0 8 0 5 - - 4 7 9 4 2 5 5 11 11 10 1 11 10 10 6 4 1 10 7 1 - - 0.

[0094] Example 26 includes an apparatus of a user equipment (UE) operable to encode information for transmission to an eNodeB, the apparatus comprising one or more processors and memory configured to: acquire, at the UE, a block of information bits;

select, at the UE, a modulation and coding scheme; determine, at the UE, a matrix prototype and a code word sub-block size based on a size of the block of information bits and the modulation and coding scheme; encode, at the UE, at least a portion of the block of information bits to obtain an encoded code word block, wherein at least the portion of the block of information bits is encoded based on the matrix prototype and the code word sub-block size; select, at the UE, a subset of bits from the encoded code word block; and generate, at the UE, the subset of bits for transmission to an eNodeB.

[0095] Example 27 includes the apparatus of Example 26, further comprising: a baseband processor operable to: determine the matrix prototype and the code word sub-block size based on the size of the block of information bits and the modulation and coding scheme; and encode at least the portion of the block of information bits to obtain the encoded code word block; and a transceiver operable to transmit the subset of bits from the UE to the eNodeB.

[0096] Example 28 includes the apparatus of any of Examples 26 to 27, wherein the matrix prototype corresponds to a defined code rate, wherein the defined code rate is a coding rate of 8/9.

[0097] Example 29 includes the apparatus of any of Examples 26 to 28, wherein the modulation and coding scheme corresponds to a spectral efficiency of approximately 5.4 bits per symbol per Hertz.

[0098] Example 30 includes the apparatus of any of Examples 26 to 29, wherein:

the code word sub-block size is 84 and the matrix prototype is:

27 27 7 - 23 40 76 - - 5 49 16 37 - 49 80 54 28 33 46 70 78 70 82 35 80 83 79 9 27 5 16 1 0 - -

51 - 45 5 - 53 83 46 27 - 48 42 0 15 - 24 74 13 50 58 63 48 53 22 46 76 40 40 51 18 11 10 - 0 0 -

- 36 5 53 65 - 65 66 64 52 - 68 16 22 43 - - 40 8 82 64 13 72 74 40 53 29 80 57 13 36 24 0 - 0 0

10 3 - 82 76 37 - 37 73 73 38 - - 46 0 61 70 32 27 38 30 76 27 49 50 76 37 27 64 35 1 49 1 - - 0; or

the code word sub-block size is 72 and the matrix prototype is:

8 65 69 - 6 7 0 - - 58 6 58 7 - 24 65 57 64 36 32 54 15 39 24 50 62 60 70 70 12 8 10 1 0 - -

68 - 8 34 - 34 53 28 6 - 37 14 51 12 - 34 7 22 42 25 31 41 12 29 58 32 60 14 22 62 18 56 - 0 0 -

- 51 70 33 4 - 15 13 62 17 - 27 39 20 0 - - 37 7 29 71 59 44 34 6 35 40 37 57 37 59 44 0 - 0 0

47 59 - 4 22 45 - 17 20 51 29 - - 16 49 67 1 71 47 3 13 62 0 13 0 47 7 49 44 48 57 25 1 - - 0; or

wherein the code word sub-block size is 60 and the matrix prototype is:

38 55 54 - 25 54 19 - - 18 47 55 2 - 10 55 52 20 5 55 17 36 28 4 59 6 31 6 22 21 33 14 1 0 - -

38 - 35 44 - 28 11 3 19 - 11 8 58 59 - 44 4 29 47 41 54 37 47 46 14 17 50 2 24 18 40 59 - 0 0 -

- 47 59 34 2 - 8 49 8 2 - 48 6 53 19 - - 59 32 9 0 53 10 4 53 19 59 6 29 44 16 55 0 - 0 0

47 52 - 33 16 36 - 5 31 4 36 - - 2 51 31 14 12 31 7 55 37 11 24 59 48 3 27 59 9 13 5 1 - - 0; or

the code word sub-block size is 48 and the matrix prototype is:

13 20 26 - 6 35 42 - - 22 17 4 14 - 13 29 38 15 34 22 7 28 23 26 0 41 13 45 20 42 27 7 1 0 - -

8 - 28 46 - 25 41 30 11 - 13 22 41 26 - 29 25 15 3 11 12 27 8 11 42 47 35 26 8 5 15 21 - 0 0 -

- 18 45 21 12 - 44 4 47 17 - 33 44 24 14 - - 23 31 10 3 20 26 42 39 26 12 23 15 18 47 27 0 - 0 0

44 27 - 10 38 31 - 10 12 40 16 - - 21 24 5 23 9 36 25 5 37 38 0 5 21 44 22 9 0 39 15 1 - - 0; or

the code word sub-block size is 36 and the matrix prototype is:

2 35 31 - 18 15 3 - - 10 2 13 14 - 22 25 5 32 2 29 5 17 26 22 12 17 20 35 30 29 3 15 1 0 - -

29 - 20 10 - 5 5 15 21 - 12 28 30 18 - 19 30 4 16 2 18 4 22 22 22 24 21 30 19 15 7 14 - 0 0 -

- 11 19 20 1 - 33 17 0 11 - 31 31 1 25 - - 15 11 24 7 25 3 18 23 4 25 21 28 7 21 22 0 - 0 0

12 7 - 12 8 9 - 27 32 24 1 - - 6 18 26 8 12 25 30 11 5 24 20 1 1 1 15 6 31 31 3 1 - - 0; or

the code word sub-block size is 24 and the matrix prototype is:

20 5 6 - 21 8 20 - - 13 12 6 12 - 15 13 1 18 13 15 9 9 3 8 9 21 22 5 10 16 14 2 1 0 - -

4 - 2 21 - 13 9 1 10 - 10 10 0 16 - 16 7 12 4 1 7 3 19 3 6 0 14 14 15 23 7 4 - 0 0 -

- 19 9 2 7 - 2 1 8 17 - 12 3 2 8 - - 13 3 17 1 16 4 2 2 1 22 1 7 0 11 20 0 - 0 0

23 18 - 15 17 21 - 10 16 14 21 - - 7 2 5 6 1 1 4 0 1 18 7 19 0 5 23 14 15 17 16 1 - - 0; or

the code word sub-block size is 12 and the matrix prototype is:

5 3 5 - 8 6 6 - - 8 10 11 3 - 10 2 11 9 6 11 11 10 2 2 1 5 7 3 7 11 9 5 1 0 - -

7 - 6 5 - 11 5 2 11 - 4 8 0 10 - 7 4 8 2 1 7 4 2 8 4 7 11 4 3 3 7 6 - 0 0 -

- 10 1 6 9 - 1 7 11 11 - 5 2 6 4 - - 11 6 10 2 3 6 5 5 2 5 11 8 7 11 5 0 - 0 0

8 0 - 0 0 10 - 0 8 0 5 - - 4 7 9 4 2 5 5 11 11 10 1 11 10 10 6 4 1 10 7 1 - - 0.

[0099] Example 31 includes an apparatus of a user equipment (UE) operable to decode information received from an eNodeB, the apparatus comprising one or more processors and memory configured to: identify, at the UE, a block of bits received from the eNodeB, wherein the block of bits is associated with a block size length and a modulation and

coding scheme; determine, at the UE, a matrix prototype and a code word sub-block size based on the block size length and the modulation and coding scheme; and decode, at the UE, the block of bits received from the eNodeB to obtain a decoded block of information bits, wherein the decoded block of information bits is obtained based on the matrix prototype and the code word sub-block size.

[00100] Example 32 includes the apparatus of Example 31, wherein the matrix prototype corresponds to a defined code rate, wherein the defined code rate is a coding rate of 8/9.

[00101] Example 33 includes the apparatus of any of Examples 31 to 32, wherein the modulation and coding scheme corresponds to a spectral efficiency of approximately 5.4 bits per symbol per Hertz.

[00102] Example 34 includes the apparatus of any of Examples 31 to 33, wherein:

the code word sub-block size is 84 and the matrix prototype is:

27 27 7 - 23 40 76 - - 5 49 16 37 - 49 80 54 28 33 46 70 78 70 82 35 80 83 79 9 27 5 16 1 0 - -

51 - 45 5 - 53 83 46 27 - 48 42 0 15 - 24 74 13 50 58 63 48 53 22 46 76 40 40 51 18 11 10 - 0 0 -

- 36 5 53 65 - 65 66 64 52 - 68 16 22 43 - - 40 8 82 64 13 72 74 40 53 29 80 57 13 36 24 0 - 0 0

10 3 - 82 76 37 - 37 73 73 38 - - 46 0 61 70 32 27 38 30 76 27 49 50 76 37 27 64 35 1 49 1 - - 0; or

the code word sub-block size is 72 and the matrix prototype is:

8 65 69 - 6 7 0 - - 58 6 58 7 - 24 65 57 64 36 32 54 15 39 24 50 62 60 70 70 12 8 10 1 0 - -

68 - 8 34 - 34 53 28 6 - 37 14 51 12 - 34 7 22 42 25 31 41 12 29 58 32 60 14 22 62 18 56 - 0 0 -

- 51 70 33 4 - 15 13 62 17 - 27 39 20 0 - - 37 7 29 71 59 44 34 6 35 40 37 57 37 59 44 0 - 0 0

47 59 - 4 22 45 - 17 20 51 29 - - 16 49 67 1 71 47 3 13 62 0 13 0 47 7 49 44 48 57 25 1 - - 0; or

wherein the code word sub-block size is 60 and the matrix prototype is:

38 55 54 - 25 54 19 - - 18 47 55 2 - 10 55 52 20 5 55 17 36 28 4 59 6 31 6 22 21 33 14 1 0 - -

38 - 35 44 - 28 11 3 19 - 11 8 58 59 - 44 4 29 47 41 54 37 47 46 14 17 50 2 24 18 40 59 - 0 0 -

- 47 59 34 2 - 8 49 8 2 - 48 6 53 19 - - 59 32 9 0 53 10 4 53 19 59 6 29 44 16 55 0 - 0 0

47 52 - 33 16 36 - 5 31 4 36 - - 2 51 31 14 12 31 7 55 37 11 24 59 48 3 27 59 9 13 5 1 - - 0; or

the code word sub-block size is 48 and the matrix prototype is:

13 20 26 - 6 35 42 - - 22 17 4 14 - 13 29 38 15 34 22 7 28 23 26 0 41 13 45 20 42 27 7 1 0 - -

8 - 28 46 - 25 41 30 11 - 13 22 41 26 - 29 25 15 3 11 12 27 8 11 42 47 35 26 8 5 15 21 - 0 0 -

- 18 45 21 12 - 44 4 47 17 - 33 44 24 14 - - 23 31 10 3 20 26 42 39 26 12 23 15 18 47 27 0 - 0 0

44 27 - 10 38 31 - 10 12 40 16 - - 21 24 5 23 9 36 25 5 37 38 0 5 21 44 22 9 0 39 15 1 - - 0; or

the code word sub-block size is 36 and the matrix prototype is:

2 35 31 - 18 15 3 - - 10 2 13 14 - 22 25 5 32 2 29 5 17 26 22 12 17 20 35 30 29 3 15 1 0 - -

29 - 20 10 - 5 5 15 21 - 12 28 30 18 - 19 30 4 16 2 18 4 22 22 22 24 21 30 19 15 7 14 - 0 0 -

- 11 19 20 1 - 33 17 0 11 - 31 31 1 25 - - 15 11 24 7 25 3 18 23 4 25 21 28 7 21 22 0 - 0 0

12 7 - 12 8 9 - 27 32 24 1 - - 6 18 26 8 12 25 30 11 5 24 20 1 1 1 15 6 31 31 3 1 - - 0; or

the code word sub-block size is 24 and the matrix prototype is:

20 5 6 - 21 8 20 - - 13 12 6 12 - 15 13 1 18 13 15 9 9 3 8 9 21 22 5 10 16 14 2 1 0 - -

4 - 2 21 - 13 9 1 10 - 10 10 0 16 - 16 7 12 4 1 7 3 19 3 6 0 14 14 15 23 7 4 - 0 0 -

- 19 9 2 7 - 2 1 8 17 - 12 3 2 8 - - 13 3 17 1 16 4 2 2 1 22 1 7 0 11 20 0 - 0 0

23 18 - 15 17 21 - 10 16 14 21 - - 7 2 5 6 1 1 4 0 1 18 7 19 0 5 23 14 15 17 16 1 - - 0; or

the code word sub-block size is 12 and the matrix prototype is:

5 3 5 - 8 6 6 - - 8 10 11 3 - 10 2 11 9 6 11 11 10 2 2 1 5 7 3 7 11 9 5 1 0 - -

7 - 6 5 - 11 5 2 11 - 4 8 0 10 - 7 4 8 2 1 7 4 2 8 4 7 11 4 3 3 7 6 - 0 0 -

- 10 1 6 9 - 1 7 11 11 - 5 2 6 4 - - 11 6 10 2 3 6 5 5 2 5 11 8 7 11 5 0 - 0 0

8 0 - 0 0 10 - 0 8 0 5 - - 4 7 9 4 2 5 5 11 11 10 1 11 10 10 6 4 1 10 7 1 - - 0.

[00103] Example 35 includes at least one machine readable storage medium having instructions embodied thereon for encoding and decoding information at an eNodeB, the instructions when executed perform the following: identifying, using one or more processors of the eNodeB, a block of information bits for transmission from the eNodeB to a user equipment (UE); determining, using the one or more processors of the eNodeB, a low density parity check (LDPC) matrix and a code word sub-block size based on a size of the block of information bits and a modulation and coding scheme; encoding, using the one or more processors of the eNodeB, at least a portion of the block of information bits to obtain an encoded code word block, wherein at least the portion of the block of information bits is encoded based on the LDPC matrix and the code word sub-block size; selecting, using the one or more processors of the eNodeB, a subset of bits from the encoded code word block; and formatting, using the one or more processors of the eNodeB, the subset of bits for transmission to the UE.

[00104] Example 36 includes the at least one machine readable storage medium of Example 35, further comprising instructions when executed perform the following: identifying a block of bits received from the UE, wherein the block of bits is associated with a second block size length and a second modulation and coding scheme; determining a second matrix prototype and a second code word sub-block size based on the second block size length and the second modulation and coding scheme; and decoding the block of bits to obtain a decoded block of information bits, wherein the decoded block of information bits is obtained based on the second matrix prototype and the second code word sub-block size.

[00105] Example 37 includes the at least one machine readable storage medium of any of Examples 35 to 36, wherein: the matrix prototype corresponds to a coding rate of 8/9; and the modulation and coding scheme corresponds to a spectral efficiency of approximately 5.4 bits per symbol per Hertz.

[00106] Example 38 includes the at least one machine readable storage medium of any of Examples 35 to 37, wherein:

the code word sub-block size is 84 and the matrix prototype is:

27 27 7 - 23 40 76 - - 5 49 16 37 - 49 80 54 28 33 46 70 78 70 82 35 80 83 79 9 27 5 16 1 0 - -
51 - 45 5 - 53 83 46 27 - 48 42 0 15 - 24 74 13 50 58 63 48 53 22 46 76 40 40 51 18 11 10 - 0 0 -
- 36 5 53 65 - 65 66 64 52 - 68 16 22 43 - - 40 8 82 64 13 72 74 40 53 29 80 57 13 36 24 0 - 0 0
10 3 - 82 76 37 - 37 73 73 38 - - 46 0 61 70 32 27 38 30 76 27 49 50 76 37 27 64 35 1 49 1 - - 0; or

the code word sub-block size is 72 and the matrix prototype is:

8 65 69 - 6 7 0 - - 58 6 58 7 - 24 65 57 64 36 32 54 15 39 24 50 62 60 70 70 12 8 10 1 0 - -
68 - 8 34 - 34 53 28 6 - 37 14 51 12 - 34 7 22 42 25 31 41 12 29 58 32 60 14 22 62 18 56 - 0 0 -
- 51 70 33 4 - 15 13 62 17 - 27 39 20 0 - - 37 7 29 71 59 44 34 6 35 40 37 57 37 59 44 0 - 0 0
47 59 - 4 22 45 - 17 20 51 29 - - 16 49 67 1 71 47 3 13 62 0 13 0 47 7 49 44 48 57 25 1 - - 0; or

the code word sub-block size is 60 and the matrix prototype is:

38 55 54 - 25 54 19 - - 18 47 55 2 - 10 55 52 20 5 55 17 36 28 4 59 6 31 6 22 21 33 14 1 0 - -
38 - 35 44 - 28 11 3 19 - 11 8 58 59 - 44 4 29 47 41 54 37 47 46 14 17 50 2 24 18 40 59 - 0 0 -
- 47 59 34 2 - 8 49 8 2 - 48 6 53 19 - - 59 32 9 0 53 10 4 53 19 59 6 29 44 16 55 0 - 0 0
47 52 - 33 16 36 - 5 31 4 36 - - 2 51 31 14 12 31 7 55 37 11 24 59 48 3 27 59 9 13 5 1 - - 0; or

the code word sub-block size is 48 and the matrix prototype is:

13 20 26 - 6 35 42 - - 22 17 4 14 - 13 29 38 15 34 22 7 28 23 26 0 41 13 45 20 42 27 7 1 0 - -
8 - 28 46 - 25 41 30 11 - 13 22 41 26 - 29 25 15 3 11 12 27 8 11 42 47 35 26 8 5 15 21 - 0 0 -
- 18 45 21 12 - 44 4 47 17 - 33 44 24 14 - - 23 31 10 3 20 26 42 39 26 12 23 15 18 47 27 0 - 0 0
44 27 - 10 38 31 - 10 12 40 16 - - 21 24 5 23 9 36 25 5 37 38 0 5 21 44 22 9 0 39 15 1 - - 0; or

the code word sub-block size is 36 and the matrix prototype is:

2 35 31 - 18 15 3 - - 10 2 13 14 - 22 25 5 32 2 29 5 17 26 22 12 17 20 35 30 29 3 15 1 0 - -
29 - 20 10 - 5 5 15 21 - 12 28 30 18 - 19 30 4 16 2 18 4 22 22 22 24 21 30 19 15 7 14 - 0 0 -
- 11 19 20 1 - 33 17 0 11 - 31 31 1 25 - - 15 11 24 7 25 3 18 23 4 25 21 28 7 21 22 0 - 0 0
12 7 - 12 8 9 - 27 32 24 1 - - 6 18 26 8 12 25 30 11 5 24 20 1 1 1 15 6 31 31 3 1 - - 0; or

the code word sub-block size is 24 and the matrix prototype is:

20 5 6 - 21 8 20 - - 13 12 6 12 - 15 13 1 18 13 15 9 9 3 8 9 21 22 5 10 16 14 2 1 0 - -
4 - 2 21 - 13 9 1 10 - 10 10 0 16 - 16 7 12 4 1 7 3 19 3 6 0 14 14 15 23 7 4 - 0 0 -
- 19 9 2 7 - 2 1 8 17 - 12 3 2 8 - - 13 3 17 1 16 4 2 2 1 22 1 7 0 11 20 0 - 0 0
23 18 - 15 17 21 - 10 16 14 21 - - 7 2 5 6 1 1 4 0 1 18 7 19 0 5 23 14 15 17 16 1 - - 0; or

the code word sub-block size is 12 and the matrix prototype is:

5 3 5 - 8 6 6 - - 8 10 11 3 - 10 2 11 9 6 11 11 10 2 2 1 5 7 3 7 11 9 5 1 0 - -
7 - 6 5 - 11 5 2 11 - 4 8 0 10 - 7 4 8 2 1 7 4 2 8 4 7 11 4 3 3 7 6 - 0 0 -
- 10 1 6 9 - 1 7 11 11 - 5 2 6 4 - - 11 6 10 2 3 6 5 5 2 5 11 8 7 11 5 0 - 0 0
8 0 - 0 0 10 - 0 8 0 5 - - 4 7 9 4 2 5 5 11 11 10 1 11 10 10 6 4 1 10 7 1 - - 0.

[00107] Example 39 includes an eNodeB operable to encode and decode information, the eNodeB comprising: means for identifying a block of information bits for transmission from the eNodeB to a user equipment (UE); means for determining a low density parity check (LDPC) matrix and a code word sub-block size based on a size of the block of information bits and a modulation and coding scheme; means for encoding at least a portion of the block of information bits to obtain an encoded code word block, wherein at least the portion of the block of information bits is encoded based on the LDPC matrix and the code word sub-block size; means for selecting a subset of bits from the encoded code word block; and means for formatting the subset of bits for transmission to the UE.

[00108] Example 40 includes the eNodeB of Example 39, further comprising: means for identifying a block of bits received from the UE, wherein the block of bits is associated with a second block size length and a second modulation and coding scheme; means for determining a second matrix prototype and a second code word sub-block size based on the second block size length and the second modulation and coding scheme; and means for decoding the block of bits to obtain a decoded block of information bits, wherein the decoded block of information bits is obtained based on the second matrix prototype and the second code word sub-block size.

[00109] Example 41 includes the eNodeB of any of Examples 39 to 40, wherein: the matrix prototype corresponds to a coding rate of 8/9; and the modulation and coding scheme corresponds to a spectral efficiency of approximately 5.4 bits per symbol per Hertz.

[00110] Example 42 includes the eNodeB of any of Examples 39 to 41, wherein:

the code word sub-block size is 84 and the matrix prototype is:

27 27 7 - 23 40 76 - - 5 49 16 37 - 49 80 54 28 33 46 70 78 70 82 35 80 83 79 9 27 5 16 1 0 - -
51 - 45 5 - 53 83 46 27 - 48 42 0 15 - 24 74 13 50 58 63 48 53 22 46 76 40 40 51 18 11 10 - 0 0 -
- 36 5 53 65 - 65 66 64 52 - 68 16 22 43 - - 40 8 82 64 13 72 74 40 53 29 80 57 13 36 24 0 - 0 0
10 3 - 82 76 37 - 37 73 73 38 - - 46 0 61 70 32 27 38 30 76 27 49 50 76 37 27 64 35 1 49 1 - - 0; or

the code word sub-block size is 72 and the matrix prototype is:

8 65 69 - 6 7 0 - - 58 6 58 7 - 24 65 57 64 36 32 54 15 39 24 50 62 60 70 70 12 8 10 1 0 - -
68 - 8 34 - 34 53 28 6 - 37 14 51 12 - 34 7 22 42 25 31 41 12 29 58 32 60 14 22 62 18 56 - 0 0 -
- 51 70 33 4 - 15 13 62 17 - 27 39 20 0 - - 37 7 29 71 59 44 34 6 35 40 37 57 37 59 44 0 - 0 0
47 59 - 4 22 45 - 17 20 51 29 - - 16 49 67 1 71 47 3 13 62 0 13 0 47 7 49 44 48 57 25 1 - - 0; or

the code word sub-block size is 60 and the matrix prototype is:

38 55 54 - 25 54 19 - - 18 47 55 2 - 10 55 52 20 5 55 17 36 28 4 59 6 31 6 22 21 33 14 1 0 - -
38 - 35 44 - 28 11 3 19 - 11 8 58 59 - 44 4 29 47 41 54 37 47 46 14 17 50 2 24 18 40 59 - 0 0 -
- 47 59 34 2 - 8 49 8 2 - 48 6 53 19 - - 59 32 9 0 53 10 4 53 19 59 6 29 44 16 55 0 - 0 0
47 52 - 33 16 36 - 5 31 4 36 - - 2 51 31 14 12 31 7 55 37 11 24 59 48 3 27 59 9 13 5 1 - - 0; or

the code word sub-block size is 48 and the matrix prototype is:

13 20 26 - 6 35 42 - - 22 17 4 14 - 13 29 38 15 34 22 7 28 23 26 0 41 13 45 20 42 27 7 1 0 - -

8 - 28 46 - 25 41 30 11 - 13 22 41 26 - 29 25 15 3 11 12 27 8 11 42 47 35 26 8 5 15 21 - 0 0 -

- 18 45 21 12 - 44 4 47 17 - 33 44 24 14 - - 23 31 10 3 20 26 42 39 26 12 23 15 18 47 27 0 - 0 0

44 27 - 10 38 31 - 10 12 40 16 - - 21 24 5 23 9 36 25 5 37 38 0 5 21 44 22 9 0 39 15 1 - - 0; or

the code word sub-block size is 36 and the matrix prototype is:

2 35 31 - 18 15 3 - - 10 2 13 14 - 22 25 5 32 2 29 5 17 26 22 12 17 20 35 30 29 3 15 1 0 - -

29 - 20 10 - 5 5 15 21 - 12 28 30 18 - 19 30 4 16 2 18 4 22 22 22 24 21 30 19 15 7 14 - 0 0 -

- 11 19 20 1 - 33 17 0 11 - 31 31 1 25 - - 15 11 24 7 25 3 18 23 4 25 21 28 7 21 22 0 - 0 0

12 7 - 12 8 9 - 27 32 24 1 - - 6 18 26 8 12 25 30 11 5 24 20 1 1 1 15 6 31 31 3 1 - - 0; or

the code word sub-block size is 24 and the matrix prototype is:

20 5 6 - 21 8 20 - - 13 12 6 12 - 15 13 1 18 13 15 9 9 3 8 9 21 22 5 10 16 14 2 1 0 - -

4 - 2 21 - 13 9 1 10 - 10 10 0 16 - 16 7 12 4 1 7 3 19 3 6 0 14 14 15 23 7 4 - 0 0 -

- 19 9 2 7 - 2 1 8 17 - 12 3 2 8 - - 13 3 17 1 16 4 2 2 1 22 1 7 0 11 20 0 - 0 0

23 18 - 15 17 21 - 10 16 14 21 - - 7 2 5 6 1 1 4 0 1 18 7 19 0 5 23 14 15 17 16 1 - - 0; or

the code word sub-block size is 12 and the matrix prototype is:

5 3 5 - 8 6 6 - - 8 10 11 3 - 10 2 11 9 6 11 11 10 2 2 1 5 7 3 7 11 9 5 1 0 - -

7 - 6 5 - 11 5 2 11 - 4 8 0 10 - 7 4 8 2 1 7 4 2 8 4 7 11 4 3 3 7 6 - 0 0 -

- 10 1 6 9 - 1 7 11 11 - 5 2 6 4 - - 11 6 10 2 3 6 5 5 2 5 11 8 7 11 5 0 - 0 0

8 0 - 0 0 10 - 0 8 0 5 - - 4 7 9 4 2 5 5 11 11 10 1 11 10 10 6 4 1 10 7 1 - - 0.

[00111] Various techniques, or certain aspects or portions thereof, may take the form of program code (i.e., instructions) embodied in tangible media, such as floppy diskettes, compact disc-read-only memory (CD-ROMs), hard drives, non-transitory computer readable storage medium, or any other machine-readable storage medium wherein, when the program code is loaded into and executed by a machine, such as a computer, the machine becomes an apparatus for practicing the various techniques. A non-transitory computer readable storage medium can be a computer readable storage medium that does not include signal. In the case of program code execution on programmable computers, the computing device may include a processor, a storage medium readable by the processor (including volatile and non-volatile memory and/or storage elements), at least one input device, and at least one output device. The volatile and non-volatile memory

and/or storage elements may be a random-access memory (RAM), erasable programmable read only memory (EPROM), flash drive, optical drive, magnetic hard drive, solid state drive, or other medium for storing electronic data. The node and wireless device may also include a transceiver module (i.e., transceiver), a counter module (i.e., counter), a processing module (i.e., processor), and/or a clock module (i.e., clock) or timer module (i.e., timer). In one example, selected components of the transceiver module can be located in a cloud radio access network (C-RAN). One or more programs that may implement or utilize the various techniques described herein may use an application programming interface (API), reusable controls, and the like. Such programs may be implemented in a high level procedural or object oriented programming language to communicate with a computer system. However, the program(s) may be implemented in assembly or machine language, if desired. In any case, the language may be a compiled or interpreted language, and combined with hardware implementations.

[00112] As used herein, the term "circuitry" may refer to, be part of, or include an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor (shared, dedicated, or group), and/or memory (shared, dedicated, or group) that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable hardware components that provide the described functionality. In some embodiments, the circuitry may be implemented in, or functions associated with the circuitry may be implemented by, one or more software or firmware modules. In some embodiments, circuitry may include logic, at least partially operable in hardware.

[00113] It should be understood that many of the functional units described in this specification have been labeled as modules, in order to more particularly emphasize their implementation independence. For example, a module may be implemented as a hardware circuit comprising custom very-large-scale integration (VLSI) circuits or gate arrays, off-the-shelf semiconductors such as logic chips, transistors, or other discrete components. A module may also be implemented in programmable hardware devices such as field programmable gate arrays, programmable array logic, programmable logic devices or the like.

[00114] Modules may also be implemented in software for execution by various types of processors. An identified module of executable code may, for instance, comprise one or

more physical or logical blocks of computer instructions, which may, for instance, be organized as an object, procedure, or function. Nevertheless, the executables of an identified module may not be physically located together, but may comprise disparate instructions stored in different locations which, when joined logically together, comprise the module and achieve the stated purpose for the module.

[00115] Indeed, a module of executable code may be a single instruction, or many instructions, and may even be distributed over several different code segments, among different programs, and across several memory devices. Similarly, operational data may be identified and illustrated herein within modules, and may be embodied in any suitable form and organized within any suitable type of data structure. The operational data may be collected as a single data set, or may be distributed over different locations including over different storage devices, and may exist, at least partially, merely as electronic signals on a system or network. The modules may be passive or active, including agents operable to perform desired functions.

[00116] Reference throughout this specification to "an example" or “exemplary” means that a particular feature, structure, or characteristic described in connection with the example is included in at least one embodiment of the present technology. Thus, appearances of the phrases "in an example" or the word “exemplary” in various places throughout this specification are not necessarily all referring to the same embodiment.

[00117] As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary. In addition, various embodiments and example of the present technology may be referred to herein along with alternatives for the various components thereof. It is understood that such embodiments, examples, and alternatives are not to be construed as defacto equivalents of one another, but are to be considered as separate and autonomous representations of the present technology.

[00118] Furthermore, the described features, structures, or characteristics may be

combined in any suitable manner in one or more embodiments. In the following description, numerous specific details are provided, such as examples of layouts, distances, network examples, etc., to provide a thorough understanding of embodiments of the technology. One skilled in the relevant art will recognize, however, that the technology can be practiced without one or more of the specific details, or with other methods, components, layouts, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the technology.

[00119] While the forgoing examples are illustrative of the principles of the present technology in one or more particular applications, it will be apparent to those of ordinary skill in the art that numerous modifications in form, usage and details of implementation can be made without the exercise of inventive faculty, and without departing from the principles and concepts of the technology. Accordingly, it is not intended that the technology be limited, except as by the claims set forth below.

CLAIMS

What is claimed is:

1. An apparatus of a user equipment (UE) operable to encode information for transmission to an eNodeB, the apparatus comprising one or more processors and memory configured to:

acquire, at the UE, a block of information bits;

select, at the UE, a modulation and coding scheme;

determine, at the UE, a matrix prototype and a code word sub-block size based on a size of the block of information bits and the modulation and coding scheme;

encode, at the UE, at least a portion of the block of information bits to obtain an encoded code word block, wherein at least the portion of the block of information bits is encoded based on the matrix prototype and the code word sub-block size;

select, at the UE, a subset of bits from the encoded code word block; and

generate, at the UE, the subset of bits for transmission to an eNodeB.

2. The apparatus of claim 1, further comprising:

a baseband processor operable to:

determine the matrix prototype and the code word sub-block size based on the size of the block of information bits and the modulation and coding scheme; and

encode at least the portion of the block of information bits to obtain the encoded code word block; and

a transceiver operable to transmit the subset of bits from the UE to the eNodeB.

3. The apparatus of claim 1, wherein the matrix prototype corresponds to a defined code rate, wherein the defined code rate is a coding rate of 8/9.

4. The apparatus of claim 1, wherein the modulation and coding scheme corresponds to a spectral efficiency of approximately 5.4 bits per symbol per Hertz.

5. The apparatus of any of claims 1 to 4, wherein the code word sub-block size is 84 and the matrix prototype is:

27 27 7 - 23 40 76 - - 5 49 16 37 - 49 80 54 28 33 46 70 78 70 82 35 80 83 79 9 27 5 16 1 0 - -
51 - 45 5 - 53 83 46 27 - 48 42 0 15 - 24 74 13 50 58 63 48 53 22 46 76 40 40 51 18 11 10 - 0 0 -
- 36 5 53 65 - 65 66 64 52 - 68 16 22 43 - - 40 8 82 64 13 72 74 40 53 29 80 57 13 36 24 0 - 0 0
10 3 - 82 76 37 - 37 73 73 38 - - 46 0 61 70 32 27 38 30 76 27 49 50 76 37 27 64 35 1 49 1 - - 0.

6. The apparatus of claim 1, wherein the code word sub-block size is 72 and the matrix prototype is:

8 65 69 - 6 7 0 - - 58 6 58 7 - 24 65 57 64 36 32 54 15 39 24 50 62 60 70 70 12 8 10 1 0 - -
68 - 8 34 - 34 53 28 6 - 37 14 51 12 - 34 7 22 42 25 31 41 12 29 58 32 60 14 22 62 18 56 - 0 0 -
- 51 70 33 4 - 15 13 62 17 - 27 39 20 0 - - 37 7 29 71 59 44 34 6 35 40 37 57 37 59 44 0 - 0 0
47 59 - 4 22 45 - 17 20 51 29 - - 16 49 67 1 71 47 3 13 62 0 13 0 47 7 49 44 48 57 25 1 - - 0.

7. The apparatus of claim 1, wherein the code word sub-block size is 60 and the matrix prototype is:

38 55 54 - 25 54 19 - - 18 47 55 2 - 10 55 52 20 5 55 17 36 28 4 59 6 31 6 22 21 33 14 1 0 - -
38 - 35 44 - 28 11 3 19 - 11 8 58 59 - 44 4 29 47 41 54 37 47 46 14 17 50 2 24 18 40 59 - 0 0 -
- 47 59 34 2 - 8 49 8 2 - 48 6 53 19 - - 59 32 9 0 53 10 4 53 19 59 6 29 44 16 55 0 - 0 0
47 52 - 33 16 36 - 5 31 4 36 - - 2 51 31 14 12 31 7 55 37 11 24 59 48 3 27 59 9 13 5 1 - - 0.

8. The apparatus of claim 1, wherein the code word sub-block size is 48 and the matrix prototype is:

13 20 26 - 6 35 42 - - 22 17 4 14 - 13 29 38 15 34 22 7 28 23 26 0 41 13 45 20 42 27 7 1 0 - -
8 - 28 46 - 25 41 30 11 - 13 22 41 26 - 29 25 15 3 11 12 27 8 11 42 47 35 26 8 5 15 21 - 0 0 -
- 18 45 21 12 - 44 4 47 17 - 33 44 24 14 - - 23 31 10 3 20 26 42 39 26 12 23 15 18 47 27 0 - 0 0
44 27 - 10 38 31 - 10 12 40 16 - - 21 24 5 23 9 36 25 5 37 38 0 5 21 44 22 9 0 39 15 1 - - 0.

9. The apparatus of claim 1, wherein the code word sub-block size is 36 and the matrix prototype is:

2 35 31 - 18 15 3 - - 10 2 13 14 - 22 25 5 32 2 29 5 17 26 22 12 17 20 35 30 29 3 15 1 0 - -
29 - 20 10 - 5 5 15 21 - 12 28 30 18 - 19 30 4 16 2 18 4 22 22 22 24 21 30 19 15 7 14 - 0 0 -
- 11 19 20 1 - 33 17 0 11 - 31 31 1 25 - - 15 11 24 7 25 3 18 23 4 25 21 28 7 21 22 0 - 0 0
12 7 - 12 8 9 - 27 32 24 1 - - 6 18 26 8 12 25 30 11 5 24 20 1 1 1 15 6 31 31 3 1 - - 0.

10. The apparatus of claim 1, wherein the code word sub-block size is 24 and the matrix prototype is:

20 5 6 - 21 8 20 - - 13 12 6 12 - 15 13 1 18 13 15 9 9 3 8 9 21 22 5 10 16 14 2 1 0 - -
4 - 2 21 - 13 9 1 10 - 10 10 0 16 - 16 7 12 4 1 7 3 19 3 6 0 14 14 15 23 7 4 - 0 0 -
- 19 9 2 7 - 2 1 8 17 - 12 3 2 8 - - 13 3 17 1 16 4 2 2 1 22 1 7 0 11 20 0 - 0 0
23 18 - 15 17 21 - 10 16 14 21 - - 7 2 5 6 1 1 4 0 1 18 7 19 0 5 23 14 15 17 16 1 - - 0.

11. The apparatus of claim 1, wherein the code word sub-block size is 12 and the matrix prototype is:

5 3 5 - 8 6 6 - - 8 10 11 3 - 10 2 11 9 6 11 11 10 2 2 1 5 7 3 7 11 9 5 1 0 - -
7 - 6 5 - 11 5 2 11 - 4 8 0 10 - 7 4 8 2 1 7 4 2 8 4 7 11 4 3 3 7 6 - 0 0 -
- 10 1 6 9 - 1 7 11 11 - 5 2 6 4 - - 11 6 10 2 3 6 5 5 2 5 11 8 7 11 5 0 - 0 0
8 0 - 0 0 10 - 0 8 0 5 - - 4 7 9 4 2 5 5 11 11 10 1 11 10 10 6 4 1 10 7 1 - - 0.

12. An apparatus of a user equipment (UE) operable to decode information received from an eNodeB, the apparatus comprising one or more processors and memory configured to:

identify, at the UE, a block of bits received from the eNodeB, wherein the block of bits is associated with a block size length and a modulation and coding scheme;

determine, at the UE, a matrix prototype and a code word sub-block size based on the block size length and the modulation and coding scheme; and

decode, at the UE, the block of bits received from the eNodeB to obtain a decoded block of information bits, wherein the decoded block of information bits is obtained based on the matrix prototype and the code word sub-block size.

13. The apparatus of claim 12, wherein the matrix prototype corresponds to a defined code rate, wherein the defined code rate is a coding rate of 8/9.

14. The apparatus of claim 12, wherein the modulation and coding scheme corresponds to a spectral efficiency of approximately 5.4 bits per symbol per Hertz.

15. The apparatus of any of claims 12 to 14, wherein the code word sub-block size is 84 and the matrix prototype is:

27 27 7 - 23 40 76 - - 5 49 16 37 - 49 80 54 28 33 46 70 78 70 82 35 80 83 79 9 27 5 16 1 0 - -
51 - 45 5 - 53 83 46 27 - 48 42 0 15 - 24 74 13 50 58 63 48 53 22 46 76 40 40 51 18 11 10 - 0 0 -
- 36 5 53 65 - 65 66 64 52 - 68 16 22 43 - - 40 8 82 64 13 72 74 40 53 29 80 57 13 36 24 0 - 0 0
10 3 - 82 76 37 - 37 73 73 38 - - 46 0 61 70 32 27 38 30 76 27 49 50 76 37 27 64 35 1 49 1 - - 0.

16. The apparatus of claim 12, wherein the code word sub-block size is 72 and the matrix prototype is:

8 65 69 - 6 7 0 - - 58 6 58 7 - 24 65 57 64 36 32 54 15 39 24 50 62 60 70 70 12 8 10 1 0 - -
68 - 8 34 - 34 53 28 6 - 37 14 51 12 - 34 7 22 42 25 31 41 12 29 58 32 60 14 22 62 18 56 - 0 0 -
- 51 70 33 4 - 15 13 62 17 - 27 39 20 0 - - 37 7 29 71 59 44 34 6 35 40 37 57 37 59 44 0 - 0 0
47 59 - 4 22 45 - 17 20 51 29 - - 16 49 67 1 71 47 3 13 62 0 13 0 47 7 49 44 48 57 25 1 - - 0.

17. The apparatus of claim 12, wherein the code word sub-block size is 60 and the matrix prototype is:

38 55 54 - 25 54 19 - - 18 47 55 2 - 10 55 52 20 5 55 17 36 28 4 59 6 31 6 22 21 33 14 1 0 - -
38 - 35 44 - 28 11 3 19 - 11 8 58 59 - 44 4 29 47 41 54 37 47 46 14 17 50 2 24 18 40 59 - 0 0 -
- 47 59 34 2 - 8 49 8 2 - 48 6 53 19 - - 59 32 9 0 53 10 4 53 19 59 6 29 44 16 55 0 - 0 0
47 52 - 33 16 36 - 5 31 4 36 - - 2 51 31 14 12 31 7 55 37 11 24 59 48 3 27 59 9 13 5 1 - - 0.

18. The apparatus of claim 12, wherein the code word sub-block size is 48 and the matrix prototype is:

13 20 26 - 6 35 42 - - 22 17 4 14 - 13 29 38 15 34 22 7 28 23 26 0 41 13 45 20 42 27 7 1 0 - -
8 - 28 46 - 25 41 30 11 - 13 22 41 26 - 29 25 15 3 11 12 27 8 11 42 47 35 26 8 5 15 21 - 0 0 -
- 18 45 21 12 - 44 4 47 17 - 33 44 24 14 - - 23 31 10 3 20 26 42 39 26 12 23 15 18 47 27 0 - 0 0
44 27 - 10 38 31 - 10 12 40 16 - - 21 24 5 23 9 36 25 5 37 38 0 5 21 44 22 9 0 39 15 1 - - 0.

19. The apparatus of claim 12, wherein the code word sub-block size is 36 and the matrix prototype is:

2 35 31 - 18 15 3 - - 10 2 13 14 - 22 25 5 32 2 29 5 17 26 22 12 17 20 35 30 29 3 15 1 0 - -
29 - 20 10 - 5 5 15 21 - 12 28 30 18 - 19 30 4 16 2 18 4 22 22 22 24 21 30 19 15 7 14 - 0 0 -
- 11 19 20 1 - 33 17 0 11 - 31 31 1 25 - - 15 11 24 7 25 3 18 23 4 25 21 28 7 21 22 0 - 0 0
12 7 - 12 8 9 - 27 32 24 1 - - 6 18 26 8 12 25 30 11 5 24 20 1 1 1 15 6 31 31 3 1 - - 0.

20. The apparatus of claim 12, wherein the code word sub-block size is 24 and the matrix prototype is:

20 5 6 - 21 8 20 - - 13 12 6 12 - 15 13 1 18 13 15 9 9 3 8 9 21 22 5 10 16 14 2 1 0 - -
4 - 2 21 - 13 9 1 10 - 10 10 0 16 - 16 7 12 4 1 7 3 19 3 6 0 14 14 15 23 7 4 - 0 0 -
- 19 9 2 7 - 2 1 8 17 - 12 3 2 8 - - 13 3 17 1 16 4 2 2 1 22 1 7 0 11 20 0 - 0 0
23 18 - 15 17 21 - 10 16 14 21 - - 7 2 5 6 1 1 4 0 1 18 7 19 0 5 23 14 15 17 16 1 - - 0.

21. The apparatus of claim 12, wherein the code word sub-block size is 12 and the matrix prototype is:

5 3 5 - 8 6 6 - - 8 10 11 3 - 10 2 11 9 6 11 11 10 2 2 1 5 7 3 7 11 9 5 1 0 - -
7 - 6 5 - 11 5 2 11 - 4 8 0 10 - 7 4 8 2 1 7 4 2 8 4 7 11 4 3 3 7 6 - 0 0 -
- 10 1 6 9 - 1 7 11 11 - 5 2 6 4 - - 11 6 10 2 3 6 5 5 2 5 11 8 7 11 5 0 - 0 0
8 0 - 0 0 10 - 0 8 0 5 - - 4 7 9 4 2 5 5 11 11 10 1 11 10 10 6 4 1 10 7 1 - - 0.

22. At least one machine readable storage medium having instructions embodied thereon for encoding and decoding information at an eNodeB, the instructions when executed perform the following:

identifying, using one or more processors of the eNodeB, a block of information bits for transmission from the eNodeB to a user equipment (UE);

determining, using the one or more processors of the eNodeB, a low density parity check (LDPC) matrix and a code word sub-block size based on a size of the block of information bits and a modulation and coding scheme;

encoding, using the one or more processors of the eNodeB, at least a portion of the block of information bits to obtain an encoded code word block, wherein at least the portion of the block of information bits is encoded based on the LDPC matrix and the code word sub-block size;

selecting, using the one or more processors of the eNodeB, a subset of bits from the encoded code word block; and

formatting, using the one or more processors of the eNodeB, the subset of bits for transmission to the UE.

23. The at least one machine readable storage medium of claim 22, further comprising instructions when executed perform the following:

identifying a block of bits received from the UE, wherein the block of bits is associated with a second block size length and a second modulation and coding scheme;

determining a second matrix prototype and a second code word sub-block size based on the second block size length and the second modulation and coding scheme; and

decoding the block of bits to obtain a decoded block of information bits, wherein the decoded block of information bits is obtained based on the second matrix prototype and the second code word sub-block size.

24. The at least one machine readable storage medium of claim 22, wherein:

the matrix prototype corresponds to a coding rate of 8/9; and

the modulation and coding scheme corresponds to a spectral efficiency of approximately 5.4 bits per symbol per Hertz.

25. The at least one machine readable storage medium of any of claims 22 to 24, wherein:

the code word sub-block size is 84 and the matrix prototype is:

27 27 7 - 23 40 76 - - 5 49 16 37 - 49 80 54 28 33 46 70 78 70 82 35 80 83 79 9 27 5 16 1 0 - -
51 - 45 5 - 53 83 46 27 - 48 42 0 15 - 24 74 13 50 58 63 48 53 22 46 76 40 40 51 18 11 10 - 0 0 -
- 36 5 53 65 - 65 66 64 52 - 68 16 22 43 - - 40 8 82 64 13 72 74 40 53 29 80 57 13 36 24 0 - 0 0
10 3 - 82 76 37 - 37 73 73 38 - - 46 0 61 70 32 27 38 30 76 27 49 50 76 37 27 64 35 1 49 1 - - 0; or

the code word sub-block size is 72 and the matrix prototype is:

8 65 69 - 6 7 0 - - 58 6 58 7 - 24 65 57 64 36 32 54 15 39 24 50 62 60 70 70 12 8 10 1 0 - -
68 - 8 34 - 34 53 28 6 - 37 14 51 12 - 34 7 22 42 25 31 41 12 29 58 32 60 14 22 62 18 56 - 0 0 -
- 51 70 33 4 - 15 13 62 17 - 27 39 20 0 - - 37 7 29 71 59 44 34 6 35 40 37 57 37 59 44 0 - 0 0
47 59 - 4 22 45 - 17 20 51 29 - - 16 49 67 1 71 47 3 13 62 0 13 0 47 7 49 44 48 57 25 1 - - 0; or

the code word sub-block size is 60 and the matrix prototype is:

38 55 54 - 25 54 19 - - 18 47 55 2 - 10 55 52 20 5 55 17 36 28 4 59 6 31 6 22 21 33 14 1 0 - -
38 - 35 44 - 28 11 3 19 - 11 8 58 59 - 44 4 29 47 41 54 37 47 46 14 17 50 2 24 18 40 59 - 0 0 -
- 47 59 34 2 - 8 49 8 2 - 48 6 53 19 - - 59 32 9 0 53 10 4 53 19 59 6 29 44 16 55 0 - 0 0
47 52 - 33 16 36 - 5 31 4 36 - - 2 51 31 14 12 31 7 55 37 11 24 59 48 3 27 59 9 13 5 1 - - 0; or

the code word sub-block size is 48 and the matrix prototype is:

13 20 26 - 6 35 42 - - 22 17 4 14 - 13 29 38 15 34 22 7 28 23 26 0 41 13 45 20 42 27 7 1 0 - -
8 - 28 46 - 25 41 30 11 - 13 22 41 26 - 29 25 15 3 11 12 27 8 11 42 47 35 26 8 5 15 21 - 0 0 -
- 18 45 21 12 - 44 4 47 17 - 33 44 24 14 - - 23 31 10 3 20 26 42 39 26 12 23 15 18 47 27 0 - 0 0
44 27 - 10 38 31 - 10 12 40 16 - - 21 24 5 23 9 36 25 5 37 38 0 5 21 44 22 9 0 39 15 1 - - 0; or

the code word sub-block size is 36 and the matrix prototype is:

2 35 31 - 18 15 3 - - 10 2 13 14 - 22 25 5 32 2 29 5 17 26 22 12 17 20 35 30 29 3 15 1 0 - -
29 - 20 10 - 5 5 15 21 - 12 28 30 18 - 19 30 4 16 2 18 4 22 22 22 24 21 30 19 15 7 14 - 0 0 -
- 11 19 20 1 - 33 17 0 11 - 31 31 1 25 - - 15 11 24 7 25 3 18 23 4 25 21 28 7 21 22 0 - 0 0
12 7 - 12 8 9 - 27 32 24 1 - - 6 18 26 8 12 25 30 11 5 24 20 1 1 1 15 6 31 31 3 1 - - 0; or

the code word sub-block size is 24 and the matrix prototype is:

20 5 6 - 21 8 20 - - 13 12 6 12 - 15 13 1 18 13 15 9 9 3 8 9 21 22 5 10 16 14 2 1 0 - -
4 - 2 21 - 13 9 1 10 - 10 10 0 16 - 16 7 12 4 1 7 3 19 3 6 0 14 14 15 23 7 4 - 0 0 -
- 19 9 2 7 - 2 1 8 17 - 12 3 2 8 - - 13 3 17 1 16 4 2 2 1 22 1 7 0 11 20 0 - 0 0
23 18 - 15 17 21 - 10 16 14 21 - - 7 2 5 6 1 1 4 0 1 18 7 19 0 5 23 14 15 17 16 1 - - 0; or

the code word sub-block size is 12 and the matrix prototype is:

5 3 5 - 8 6 6 - - 8 10 11 3 - 10 2 11 9 6 11 11 10 2 2 1 5 7 3 7 11 9 5 1 0 - -
7 - 6 5 - 11 5 2 11 - 4 8 0 10 - 7 4 8 2 1 7 4 2 8 4 7 11 4 3 3 7 6 - 0 0 -
- 10 1 6 9 - 1 7 11 11 - 5 2 6 4 - - 11 6 10 2 3 6 5 5 2 5 11 8 7 11 5 0 - 0 0
8 0 - 0 0 10 - 0 8 0 5 - - 4 7 9 4 2 5 5 11 11 10 1 11 10 10 6 4 1 10 7 1 - - 0.

H_r89_z12 (z = 12):

```
5  3  5  -  8  6  6  -  -  8 10 11  3  - 10  2 11  9  6 11 11 10  2  2  1  5  7  3  7 11  9  5  1  0  -  -
7  -  6  5  - 11  5  2 11  -  4  8  0 10  -  7  4  8  2  1  7  4  2  8  4  7 11  4  3  3  7  6  -  0  0  -
- 10  1  6  9  -  1  7 11 11  -  5  2  6  4  -  - 11  6 10  2  3  6  5  5  2  5 11  8  7 11  5  0  -  0  0
8  0  -  0  0 10  -  0  8  0  5  -  -  4  7  9  4  2  5  5 11 11 10  1 11 10 10  6  4  1 10  7  1  -  -  0
```

FIG. 1A

H_r89_z24 (z = 24):

```
20  5  6  - 21  8 20  -  - 13 12  6 12  - 15 13  1 18 13 15  9  9  3  8  9 21 22  5 10 16 14  2  1  0  -  -
 4  -  2 21  - 13  9  1 10  - 10 10  0 16  - 16  7 12  4  1  7  3 19  3  6  0 14 14 15 23  7  4  -  0  0  -
 - 19  9  2  7  -  2  1  8 17  - 12  3  2  8  -  - 13  3 17  1 16  4  2  2  1 22  1  7  0 11 20  0  -  0  0
23 18  - 15 17 21  - 10 16 14 21  -  -  7  2  5  6  1  1  4  0  1 18  7 19  0  5 23 14 15 17 16  1  -  -  0
```

FIG. 1B

H_r89_z36 (z = 36):

```
 2 35 31  - 18 15  3  -  - 10  2 13 14  - 22 25  5 32  2 29  5 17 26 22 12 17 20 35 30 29  3 15  1  0  -  -
29  - 20 10  -  5  5 15 21  - 12 28 30 18  - 19 30  4 16  2 18  4 22 22 22 24 21 30 19 15  7 14  -  0  0  -
 - 11 19 20  1  - 33 17  0 11  - 31 31  1 25  -  - 15 11 24  7 25  3 18 23  4 25 21 28  7 21 22  0  -  0  0
12  7  - 12  8  9  - 27 32 24  1  -  -  6 18 26  8 12 25 30 11  5 24 20  1  1  1 15  6 31 31  3  1  -  -  0
```

FIG. 1C

H_r89_z48 (z = 48):

```
13 20 26  -  6 35 42  -  - 22 17  4 14  - 13 29 38 15 34 22  7 28 23 26  0 41 13 45 20 42 27  7  1  0  -  -
 8  - 28 46  - 25 41 30 11  - 13 22 41 26  - 29 25 15  3 11 12 27  8 11 42 47 35 26  8  5 15 21  -  0  0  -
 - 18 45 21 12  - 44  4 47 17  - 33 44 24 14  -  - 23 31 10  3 20 26 42 39 26 12 23 15 18 47 27  0  -  0  0
44 27  - 10 38 31  - 10 12 40 16  -  - 21 24  5 23  9 36 25  5 37 38  0  5 21 44 22  9  0 39 15  1  -  -  0
```

FIG. 1D

H_r89_z60 (z = 60):

```
38 55 54  - 25 54 19  -  - 18 47 55  2  - 10 55 52 20  5 55 17 36 28  4 59  6 31  6 22 21 33 14  1  0  -  -
38  - 35 44  - 28 11  3 19  - 11  8 58 59  - 44  4 29 47 41 54 37 47 46 14 17 50  2 24 18 40 59  -  0  0  -
 - 47 59 34  2  -  8 49  8  2  - 48  6 53 19  -  - 59 32  9  0 53 10  4 53 19 59  6 29 44 16 55  0  -  0  0
47 52  - 33 16 36  -  5 31  4 36  -  -  2 51 31 14 12 31  7 55 37 11 24 59 48  3 27 59  9 13  5  1  -  -  0
```

FIG. 1E

H_r89_z72 (z = 72):

```
8 65 69  -  6  7  0  -  - 58  6 58  7  - 24 65 57 64 36 32 54 15 39 24 50 62 60 70 70 12  8 10  1  0  -  -
68  -  8 34  - 34 53 28  6  - 37 14 51 12  - 34  7 22 42 25 31 41 12 29 58 32 60 14 22 62 18 56  -  0  0  -
 - 51 70 33  4  - 15 13 62 17  - 27 39 20  0  -  - 37  7 29 71 59 44 34  6 35 40 37 57 37 59 44  0  -  0  0
47 59  -  4 22 45  - 17 20 51 29  -  - 16 49 67  1 71 47  3 13 62  0 13  0 47  7 49 44 48 57 25  1  -  -  0
```

FIG. 1F

H_r89_z84 (z = 84):

```
27 27  7  - 23 40 76  -  -  5 49 16 37  - 49 80 54 28 33 46 70 78 70 82 35 80 83 79  9 27  5 16  1  0  -  -
51  - 45  5  - 53 83 46 27  - 48 42  0 15  - 24 74 13 50 58 63 48 53 22 46 76 40 40 51 18 11 10  -  0  0  -
 - 36  5 53 65  - 65 66 64 52  - 68 16 22 43  -  - 40  8 82 64 13 72 74 40 53 29 80 57 13 36 24  0  -  0  0
10  3  - 82 76 37  - 37 73 73 38  -  - 46  0 61 70 32 27 38 30 76 27 49 50 76 37 27 64 35  1 49  1  -  -  0
```

FIG. 1G

H_r89_z96 (z = 96):

```
31  1  0  - 76 45 29  -  - 20 45 90  2  - 29 24 23 13 43 38  1 74 10 70 18 14 48 16  5 65 90 88  1  0  -  -
20  - 40 15  - 51 38 49 36  - 28 91 30 92  - 15 13 24 91 59 13 37  7 26 94 18 58  8 42 95 42 14  -  0  0  -
 - 87 33 27  2  - 27 76 22 11  -  3 28 82 23  -  - 37 62 40 77 55 18 78 22 37 95 48 71  9 87 36  0  -  0  0
 0 34  - 18 23  8  - 61 87 30 17  -  - 65 38  0 36 25 58 61 19 35 65  9 90 72 13  8 55 15 86 59  1  -  -  0
```

FIG. 1H

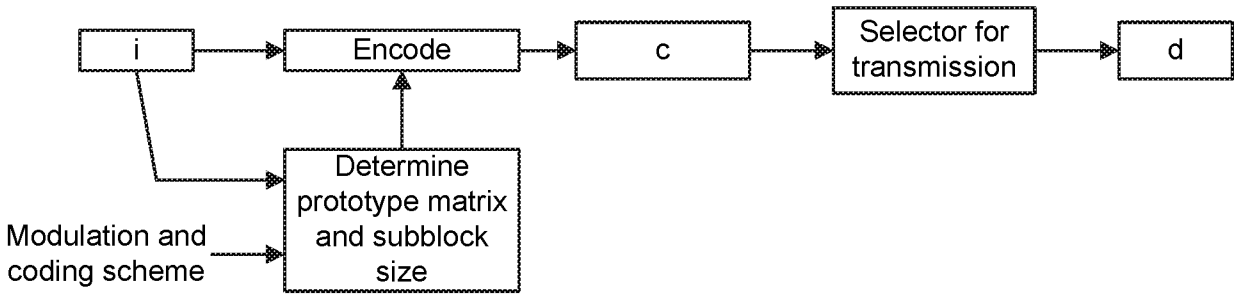
i
Encode
c
Selector for transmission
d
Determine prototype matrix and subblock size
Modulation and coding scheme

FIG. 2

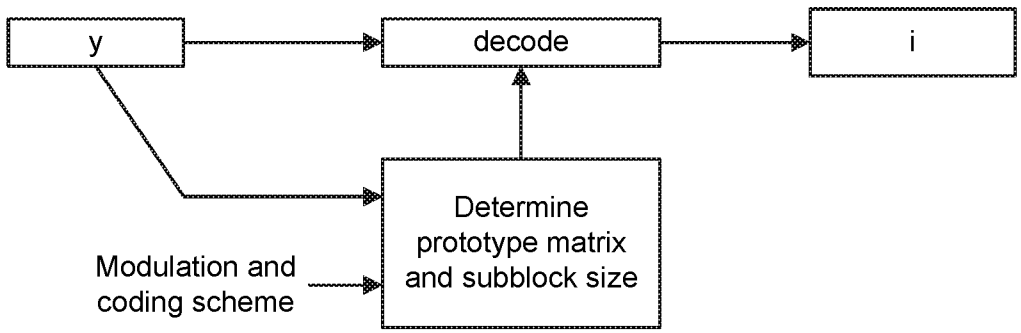
y
decode
i
Determine prototype matrix and subblock size
Modulation and coding scheme

FIG. 3

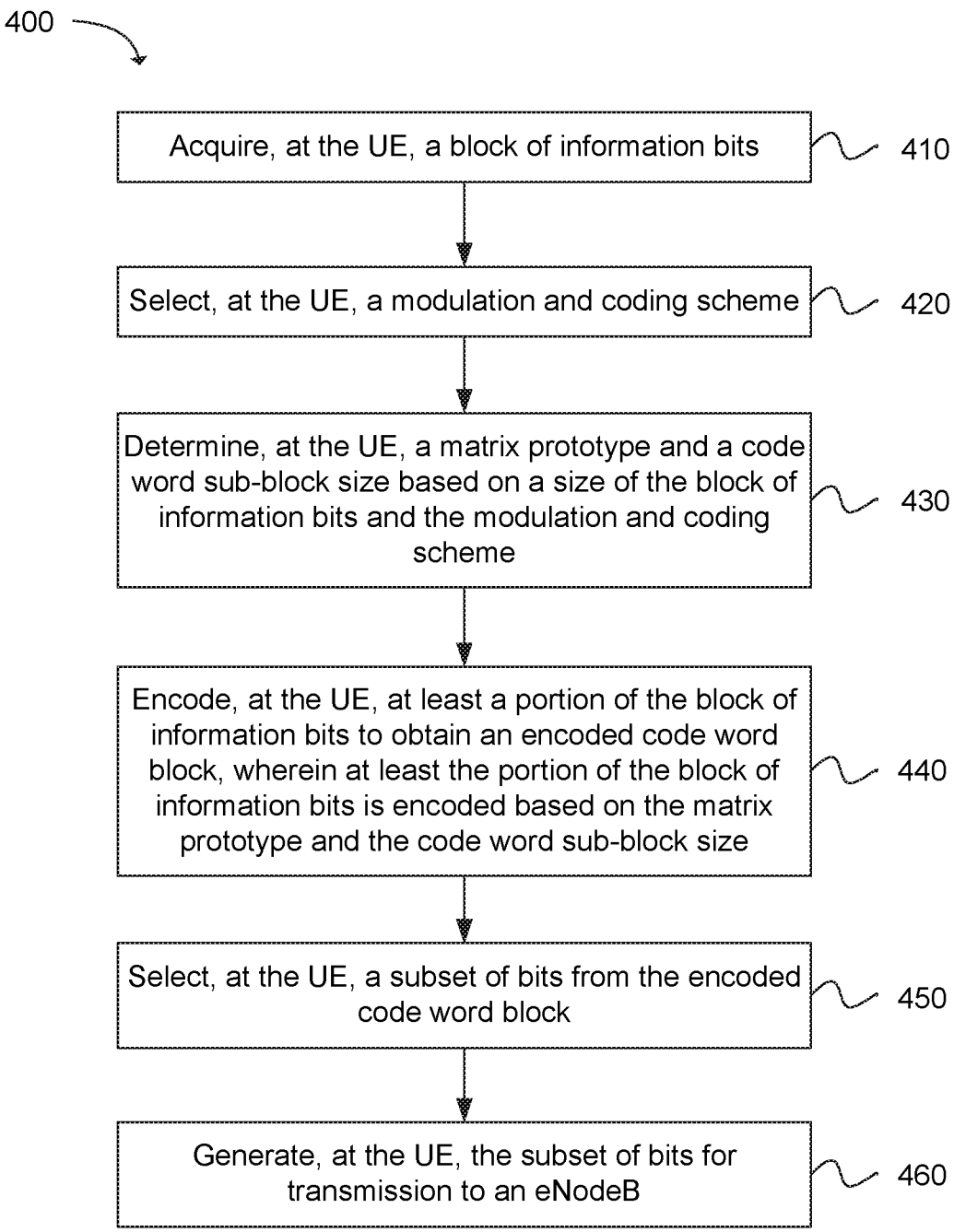
400
Acquire, at the UE, a block of information bits
410
Select, at the UE, a modulation and coding scheme
420
Determine, at the UE, a matrix prototype and a code word sub-block size based on a size of the block of information bits and the modulation and coding scheme
430
Encode, at the UE, at least a portion of the block of information bits to obtain an encoded code word block, wherein at least the portion of the block of information bits is encoded based on the matrix prototype and the code word sub-block size
440
Select, at the UE, a subset of bits from the encoded code word block
450
Generate, at the UE, the subset of bits for transmission to an eNodeB
460

FIG. 4

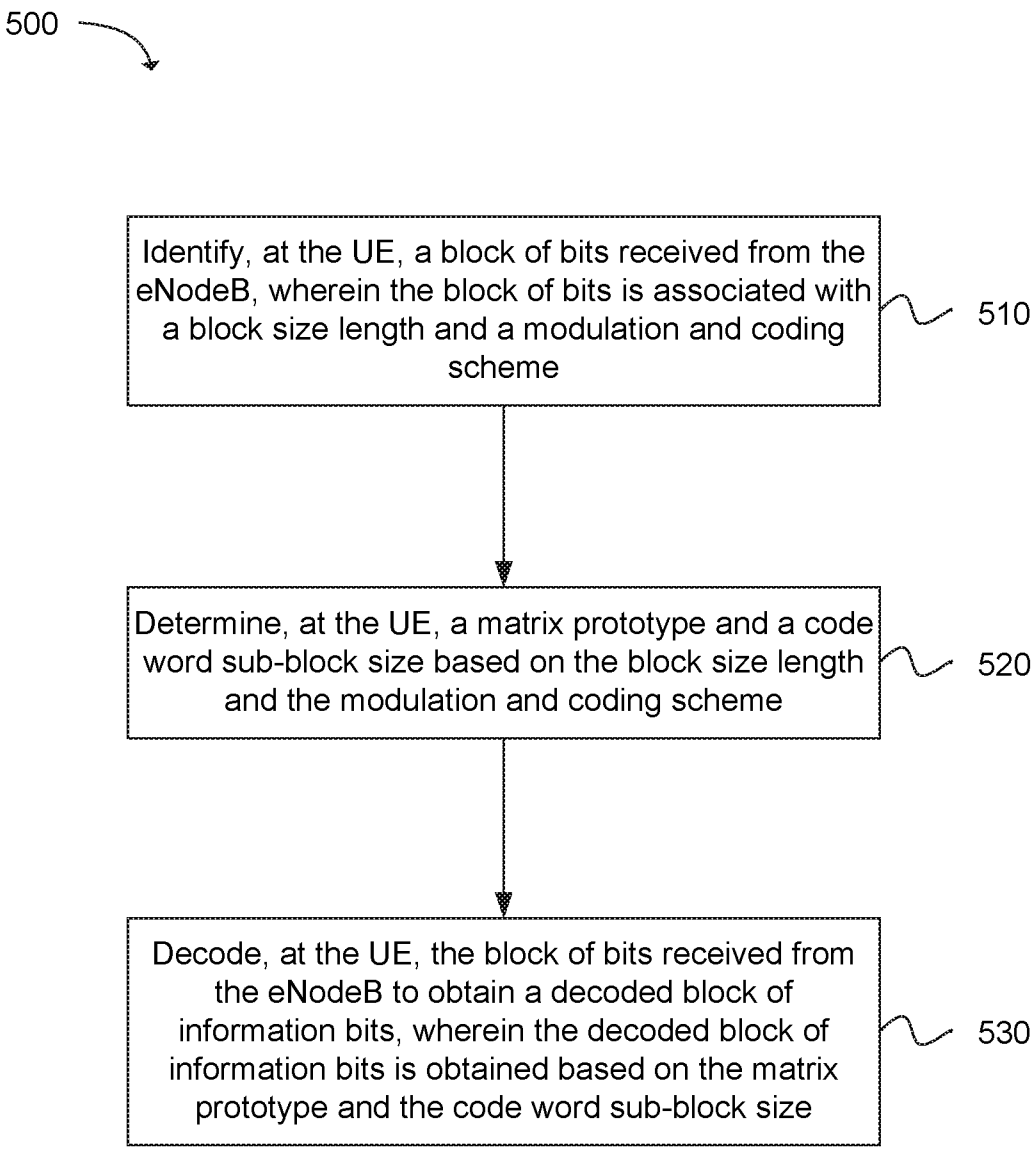
500
Identify, at the UE, a block of bits received from the eNodeB, wherein the block of bits is associated with a block size length and a modulation and coding scheme
510
Determine, at the UE, a matrix prototype and a code word sub-block size based on the block size length and the modulation and coding scheme
520
Decode, at the UE, the block of bits received from the eNodeB to obtain a decoded block of information bits, wherein the decoded block of information bits is obtained based on the matrix prototype and the code word sub-block size
530

FIG. 5

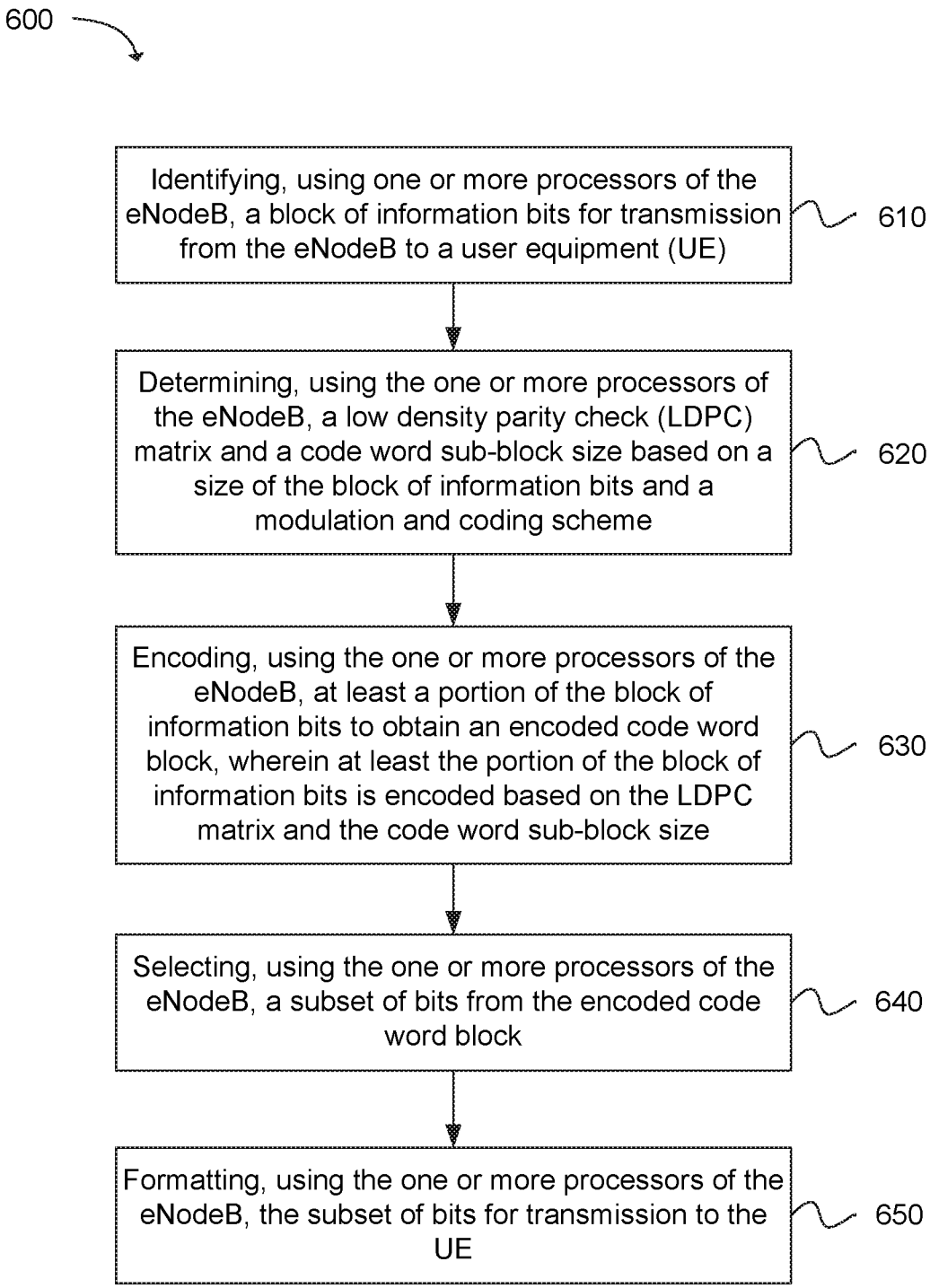
600
Identifying, using one or more processors of the eNodeB, a block of information bits for transmission from the eNodeB to a user equipment (UE)
610
Determining, using the one or more processors of the eNodeB, a low density parity check (LDPC) matrix and a code word sub-block size based on a size of the block of information bits and a modulation and coding scheme
620
Encoding, using the one or more processors of the eNodeB, at least a portion of the block of information bits to obtain an encoded code word block, wherein at least the portion of the block of information bits is encoded based on the LDPC matrix and the code word sub-block size
630
Selecting, using the one or more processors of the eNodeB, a subset of bits from the encoded code word block
640
Formatting, using the one or more processors of the eNodeB, the subset of bits for transmission to the UE
650

FIG. 6

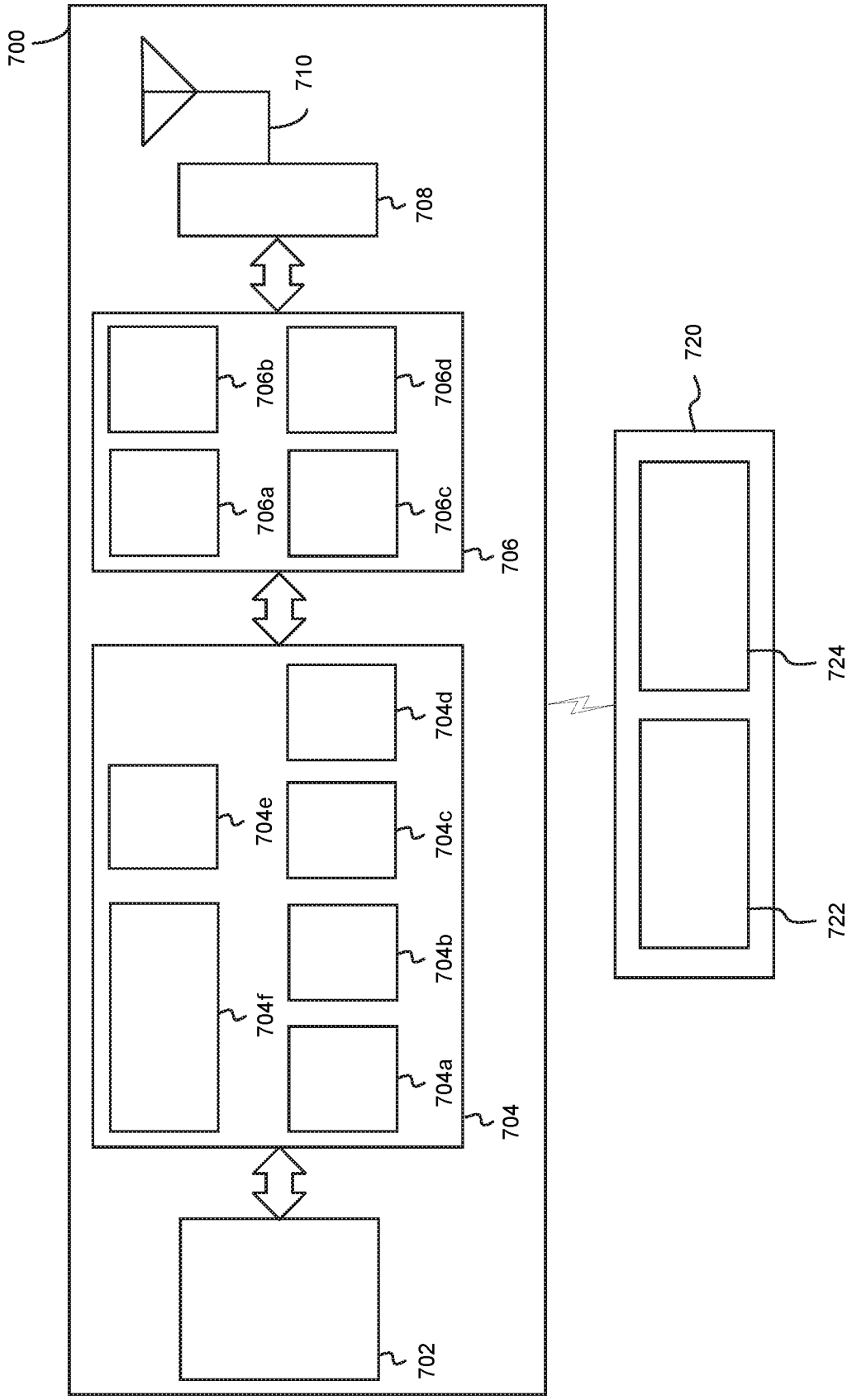
700
710
708
706b
706d
706a
706c
706
720
704d
704e
704c
704f
704b
704a
704
724
722
702

FIG. 7

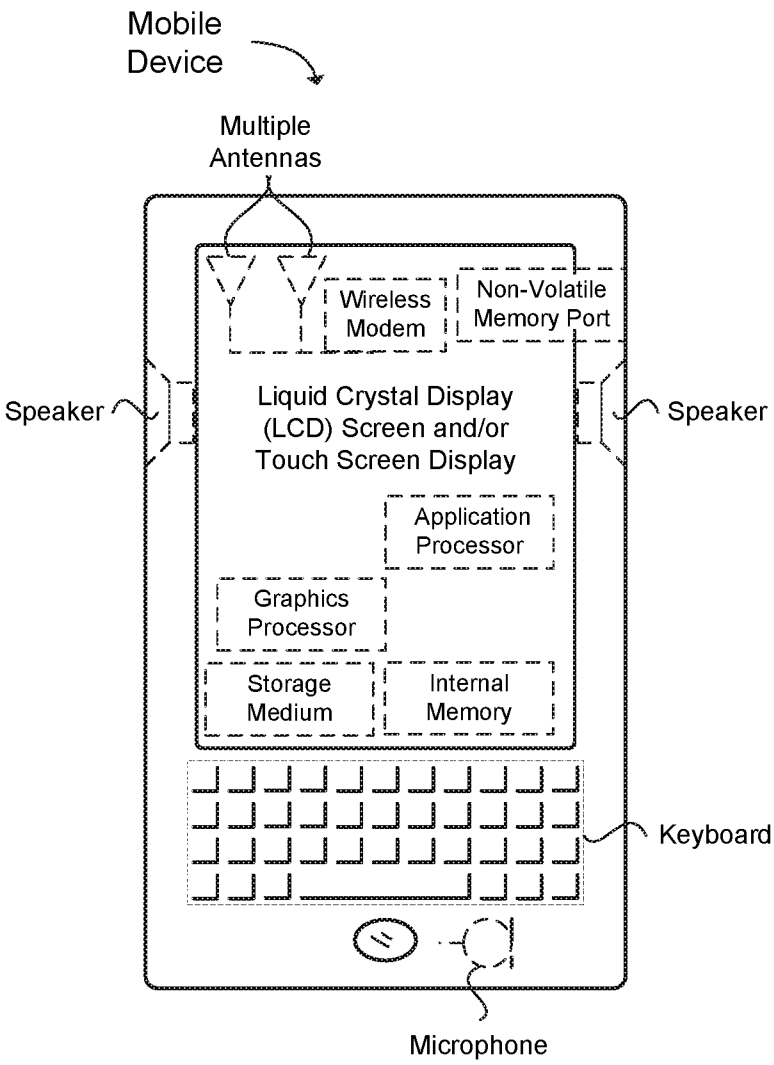
Mobile Device
Multiple Antennas
Wireless Modem
Non-Volatile Memory Port
Speaker
Liquid Crystal Display (LCD) Screen and/or Touch Screen Display
Speaker
Application Processor
Graphics Processor
Storage Medium
Internal Memory
Keyboard
Microphone

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/032931

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04L1/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/289437 A1 (OH MIN S [KR] ET AL) 29 December 2005 (2005-12-29) paragraphs [0030] - [0035] paragraphs [0072] - [0097]; figure 1 paragraphs [0111], [0112] paragraphs [0121] - [0124] paragraphs [0159] - [0162] figures 14-27 -----	1-25
X	US 2008/109699 A1 (STOLPMAN VICTOR [US]) 8 May 2008 (2008-05-08) paragraphs [0023] - [0030] paragraph [0044]; figure 2a paragraphs [0050] - [0056]; figures 3-5 paragraphs [0067] - [0070]; figures 7,8 claims 3-5 ----- -/--	1-25

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 September 2016	16/09/2016

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Kreppel, Jan

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/032931

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2010/023838 A1 (SHEN BA-ZHONG [US] ET AL) 28 January 2010 (2010-01-28) paragraphs [0136] - [0152]; figures 8-11	1-25
A	US 2004/221223 A1 (YU NAM-YUL [KR] ET AL) 4 November 2004 (2004-11-04) paragraphs [0052] - [0073]; figures 5,6	1-25

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INTERNATIONAL SEARCH REPORT

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