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(54) Abstract Title
 Solid state image sensor

(57) A solid state image sensor comprises a semiconductor substrate 32 of a first conductivity type having one or more photosensistive pixels formed therein, the photosensitive area 20 of the or each pixel being formed by the semiconductor substrate and one or more impurity layers 33,34 of a second conductivity type formed within an active area of the semiconductor substrate. The photosensitive area has one or more edge portions defined by isolation 31 separating the active area of the semiconductor substrate from other active areas thereof, and the doping density of the impurity at the edge portion(s) of the photosensitive area is substantially restricted. A preferred embodiment is a CMOS photodiode sensor in which each pixel thereof includes a photodiode 20 formed by two N-type layers 33,34 in a P-type substrate. The lower N-type layer 33 is more heavily doped than the upper layer 34 and the edges of the lower layer 33 are set back from the edges of the upper layer 34. Alternatively, the lower layer 33 may be absent altogether. The layers 33, 34 are formed by the use of two or more different masks in the impurity doping process during manufacture of the sensor. Such a construction reduces dark-current leakage.
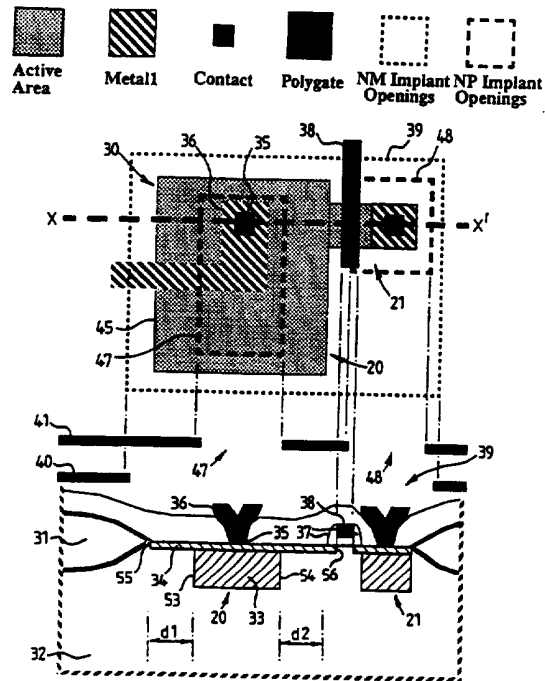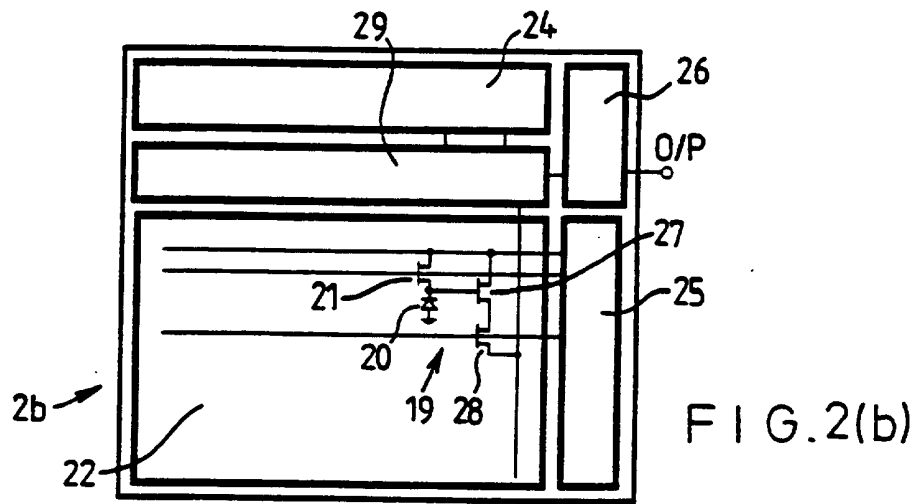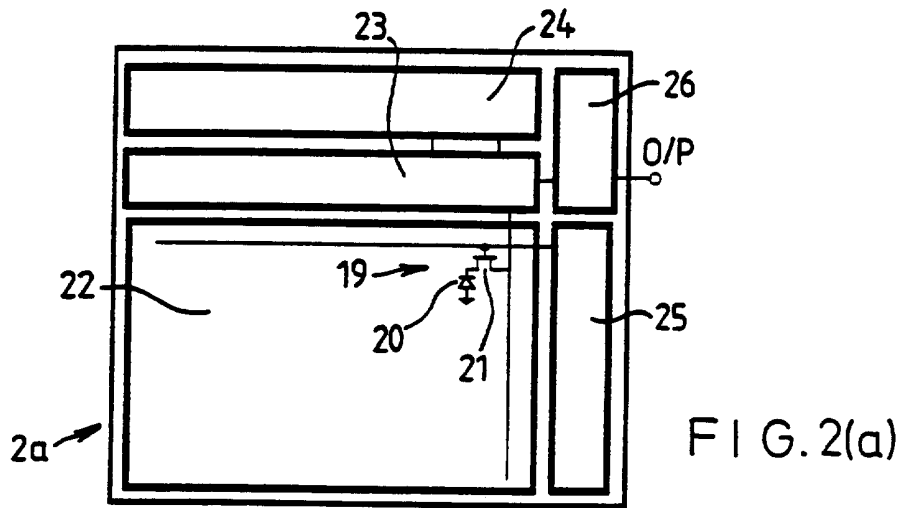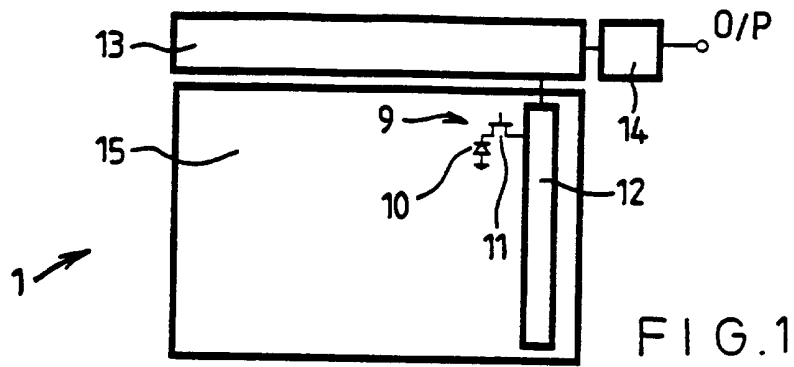
Active Area   Metal1   Contact   Polygate   NM Implant Openings   NP Implant Openings

FIG.4

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

This print takes account of replacement documents submitted after the date of filing to enable the application to comply with the formal requirements of the Patents Rules 1995

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FIG.1

FIG.2(a)

FIG.2(b)

Active
Area

Metal1

Contact

Polygate

N Implants
Mask Openings

F I G . 3

Active Area   Metal1   Contact   Polygate   NM Implant Openings   NP Implant Openings

F I G. 4

Active Area   Metal1   Contact   Polygate   NM Implant Openings   NP Implant Openings

FIG.5

Active Area

Metal1

Contact

Polygate

NM Implant Openings

NP Implant Openings

FIG.6

| Active Area | Metal1 | Contact | Polygate | NM Implant Openings | NP Implant Openings |

30 36 35 38

45 20 48 21

X — — — — — — — — — — — X'

41 39 40

31 36 37 35 38 34 20 21 32 48

F I G .7

Active Area   Metal   Contact   Polygate   N- Implant Openings   N+ Implant Openings

FIG.8

Active Area Metal1 Contact Polygate NM Implant Openings NP Implant Openings

FIG.9

Active Area   Metal1   Contact   Polygate   NM Implant Openings   NP Implant Openings

FIG.10

FIG.11

IMPROVED SOLID STATE IMAGE SENSOR

The present invention relates to improved solid state image
sensors and methods of manufacturing such improved sensors.
5 More specifically, the invention is concerned with solid
state image sensors which utilise photodiode structures as
the light-sensing elements of the sensor, and in
particular, but not exclusively, to Complementary Metal
Oxide Semiconductor (CMOS) image sensors of the photodiode
10 type.

Solid state image sensors dominate electronic imaging
applications such as Closed Circuit Television (CCTV),
video cameras and camcorders, scanners, and newly developed
15 markets such as PC(Personal Computer)-cameras for video
conferencing and Digital Stills Cameras. One popular form
of solid state image sensor is the Charge Coupled Device
(CCD) image sensor, while sensors built entirely in
standard CMOS technology are also becoming popular. Such
20 CCD and CMOS image sensors commonly comprise an array of
pixels formed in a semiconductor substrate, each pixel
comprising a photosensitive element which is normally in
the form of a photodiode, or alternatively a polysilicon
electrode (photogate), for responding to incident light.
25

In CCD and CMOS "photodiode" sensors, each pixel contains a
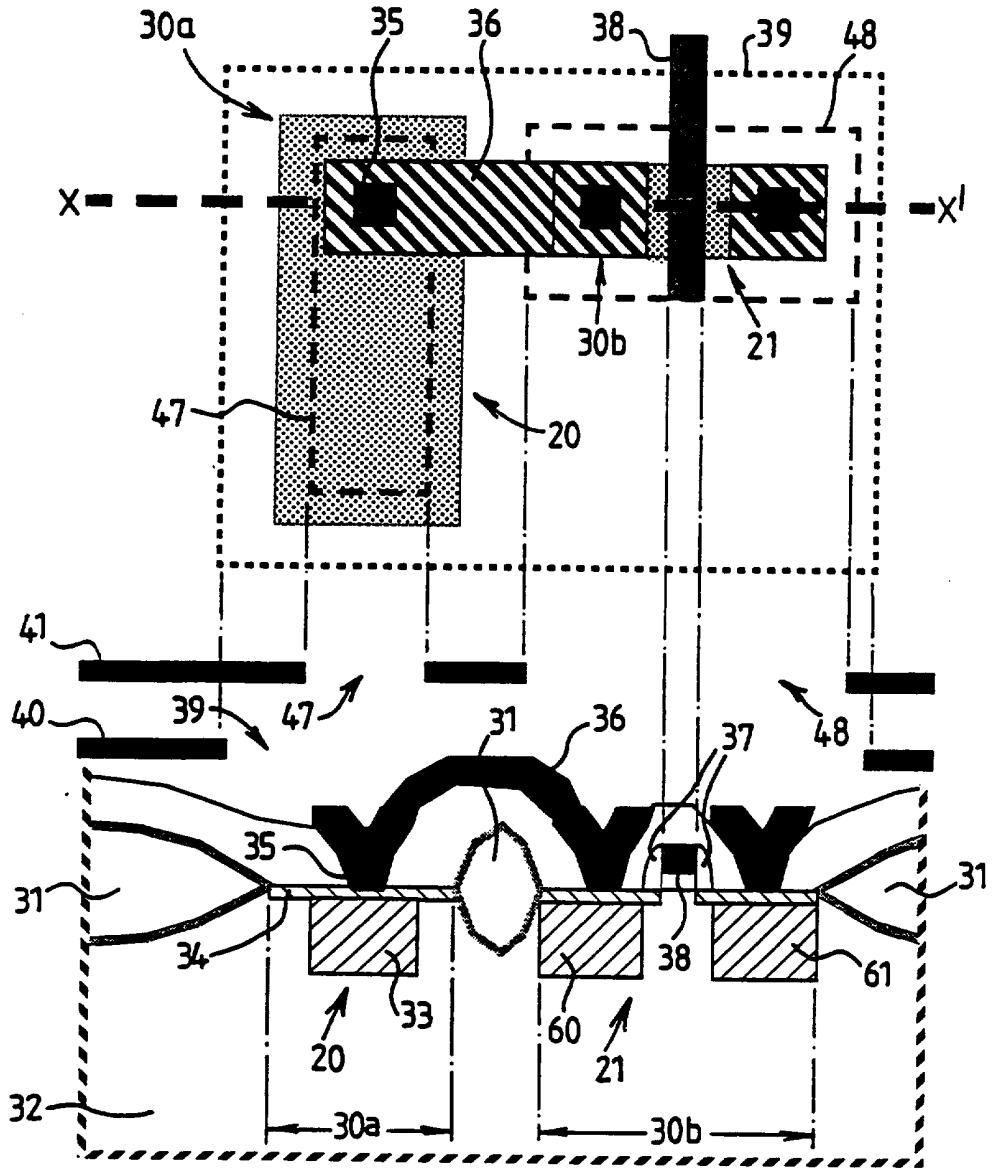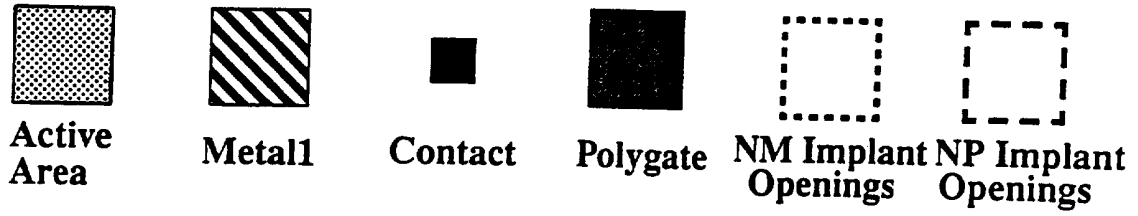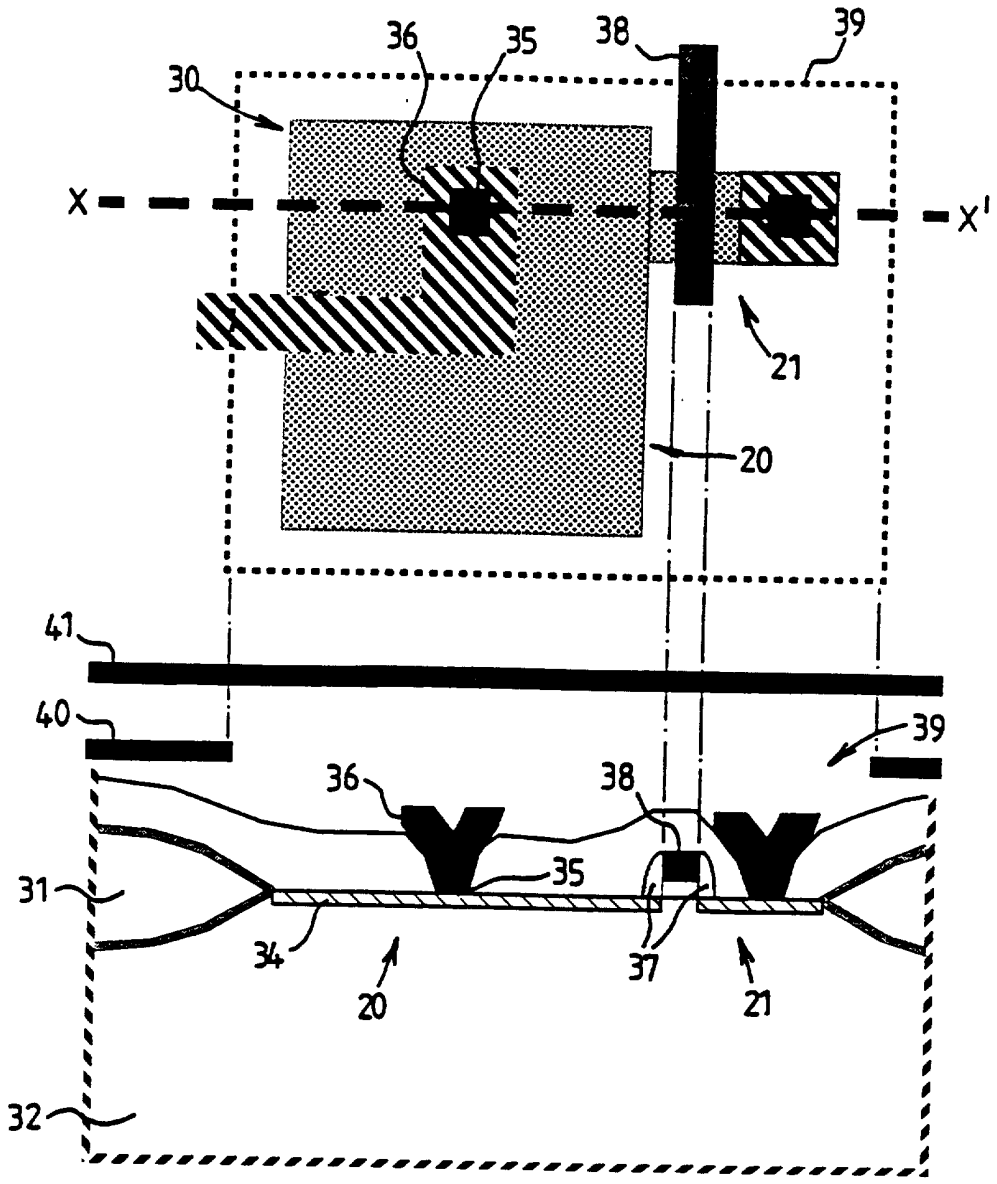photodiode and at least one MOS (access) transistor which
photodiode and transistor(s) are often, but not
necessarily, made in the same "active area" of the
30 semiconductor substrate in order to improve packing
density. ``Active area'' is a common term in the field, the
"active areas" being the areas at the surface of the
semiconductor substrate in which the photodiodes and
transistors can be manufactured. The active areas are
35 defined by isolation means commonly in the form of Field
Oxide generated using a LOCOS(Local Oxidation of Silicon)
technique, which separates out the active areas. In the
most predominantly used types of CCD and CMOS photodiode

sensors (hereinafter referred to as "conventional" photodiode sensors) the photodiode is made from at least two layers of n-type material in a p-type substrate of silicon, the n-type layers being formed by implantation

5 and/or diffusion of one or more dopants into the p-type silicon substrate. The n-type layers are of different doping densities and depths and will include a low-density layer doped to a relatively shallow depth and at least one high-density layer immediately thereunder which has a

10 doping density at least an order of magnitude greater than the low-density layer and is doped to a depth greater by a factor of at least two than the depth of the low-density layer.

15 The standard technique for creating the n-type layers is to implant or diffuse dopants (in the form of impurity ions) through an opening, or openings, in a mask at the surface of the p-type substrate. The mask is made of a material which prevents the passage of such dopants therethrough and

20 is often in the form of photoresist laid onto the surface of the semiconductor substrate. The or each implant opening in the mask generally encompasses one or more of the active areas of the substrate. Where the access transistor is formed in the same active area as the photodiode, a

25 polysilicon gate element or "polygate" is formed on the substrate, crossing at least a portion of the active area, and a "spacer" in the form of an oxide material may also be formed at two opposite edges of the polygate. Only regions of the "active areas" of the substrate which are not

30 covered by a blocking layer of sufficient thickness to prevent the passage of dopants (in the form of implant ions) will receive the dose(s) of dopant(s) being used to create the n-type layers. Thus areas below the Field Oxide, the polygate and the spacer (where present) do not receive

35 dopants. In sensors of this type the low-density and high density n-type layers are thus generally defined by the edges of the Field Oxide (isolation) and the edges of the polygate and/or spacer.

It has been found that yields in practically implemented
sensors of the afore-described type can be adversely
affected by a random leakage phenomenon which manifests
5   itself in any number of pixels in a given sensor array as a
dark-current leakage one or more orders of magnitude
greater than the mean of the dark current for all the
pixels in the array (where the "dark current" is the
residual current present in a pixel when there is no
10   illumination incident thereon). These "leaky" pixels appear
whiter than their neighbours, as a function of pixel
exposure and gain. They appear to the user of the camera,
or other product in which the image sensor is incorporated,
as "white", or artificially bright, pixels or spots on the
15   final image.

According to the exact pixel arrangement, and the process
conditions prevailing at the time of manufacture, as many
as 0.1% or more of the pixels in the array may appear
20   "white". This gives an unacceptable spotty appearance to
the image, and the effect may be so severe as to make the
device unusable unless some form of post-processing
correction of these sites is applied. Such correction may
be costly in terms of video-rate, calibration time, and
25   hardware. In demanding applications the cosmetically
acceptable limits of the number of corrected white pixels
may be small. The number of "white" pixels occurring,
beyond the blemish specification of the end-user, results
in poor overall product yield for the image sensor
30   manufacturer.

It is an object of the present invention to avoid or
minimise one or more of the foregoing disadvantages.

35   Without in any way restricting the scope of the present
invention it is believed that the above problems arise due
to degradation of the semiconductor at the outer edges of
the photosensistive areas (i.e. of the photodiode) due to

high physical and electrical stresses induced at these
edges in the course of heavy doping processes. We have now
found that by substantially restricting doping levels in
the vicinity of these edges such problems can be
5   substantially avoided.

According to a first aspect of the present invention, a
solid state image sensor comprises a semiconductor
substrate of a first conductivity type having at least one
10 pixel formed therein for sensing incident light energy,
said at least one pixel comprising photosensitive means,
said photosensitive means comprising said semiconductor
substrate and at least one impurity region formed within an
active area of the surface of said semiconductor substrate,
15 and said photosensitive means having at least one edge
portion defined by isolation means which isolation means
separates said active area of the semiconductor substrate
from other active areas thereof, said at least one impurity
region comprising at least one impurity layer of a second
20 conductivity type, wherein the doping density of said
impurity in an edge region of said at least one impurity
region at said at least one edge portion of said
photosensitive means is substantially restricted.

25 One advantage of the image sensor according to the
invention is that degradation of the semiconductor at the
edge portion(s) of the photosensitive means defined by the
isolation means is substantially avoided since the doping
density in the impurity region is restricted in the
30 vicinity of this, or at least one such, edge portion.

Said photosensitive means is most preferably a photodiode.
It is conceivable, although generally less preferred, that
said photosensitive means may alternatively be a bipolar
35 transistor.

The doping density in said edge region of the impurity
region may be restricted by substantially avoiding any

impurity doping in this region, or at least any high
density impurity doping in this region. In one preferred
embodiment said at least one impurity region in the
photosensitive means may simply comprise a single lightly
5   doped impurity layer. Generally though it is desirable to
have at least one second, more heavily doped, impurity
layer which is at least partially disposed below a first,
more lightly doped, impurity layer. Said more heavily doped
layer is commonly provided to protect against contact
10   junction spiking and also beneficially increases pixel
capacitance. Said more heavily doped layer or layers
generally have a doping density which is at least an order
of magnitude greater than said more lightly doped layer. In
accordance with the present invention any such second more
15   heavily doped impurity layer should have its outer edge set
back from said at least one edge portion of the
photosensitive means so that the doping density of said
impurity at said edge portion is substantially restricted.
Said more lightly doped impurity layer preferably comprises
20   greater than 10% of the surface of said photosensitive
means. Said at least one second, more heavily doped, layer
is preferably deeper than said first, more lightly doped,
layer by a factor of at least 1.5. The depth of said at
least one more heavily doped layer is preferably greater
25   than 0.1μm (measured from the surface of the photosensitive
means).

It will of course be appreciated that the outermost edge of
the photosensitive means is not sharply defined insofar as
30   there is a degree of intermixing of the isolation means,
substrate, and the impurity layer dopant at the atomic
level so that the edge is somewhat fuzzy across a finite
width. In accordance with the present invention said edge
region (of said at least one impurity region) having said
35   substantially restricted doping density desirably has a
width of at least $\lambda/4$, preferably at least $\lambda/2$, most
preferably at least λ, in order to substantially avoid the

afore-mentioned random leakage problem, where λ is the minimum process feature size of the solid state image sensor.(The minimum process feature size is a commonly used term in the field and is defined as the minimum size of any

5   feature within a component formed on or in the semiconductor substrate.) The width of the somewhat fuzzy region which is the outermost edge of the photosensitive means may commonly be an order of magnitude smaller than the minimum process feature size,λ. It will further be

10   appreciated that the edge of the impurity region can also not be exactly defined, there being a manufacturing tolerance of the order of, commonly, at least $\lambda/10$ in defining the edge of the impurity region. There will also usually be further tolerance factors associated with the

15   definition of the edges of the impurity regions arising from repeatability limitations in the implant/diffusion process. By ensuring that the edge region of the impurity region which has restricted doping density is at least $\lambda/4$ in width we seek to take all these tolerances into account

20   to ensure that heavy impurity doping does not take place in the vicinity of at least a portion of the edge of the photosensitive means during manufacture of the sensor.

Where, as afore-mentioned, said at least one impurity

25   region comprises a first, more lightly doped impurity layer and a second, more heavily doped, impurity layer, the outer edge of said at least one second, more heavily doped, layer is preferably set back from said at least one edge portion of the photosensitive means by at least $\lambda/4$.

30

It will be appreciated that as integrated sensor, particularly CMOS, geometries get smaller (as technology advances), λ will also get smaller. As this happens, the above-mentioned depths of the more lightly and more heavily

35   doped layers will also get smaller (though the relative depths are likely to be kept substantially the same).

In general, low density doping corresponds to doping
densities not greater than 1×10^{14} atoms/cm^3, usually from
1×10^{13} to 3×10^{13} atoms/cm^3, whilst heavy doping
corresponds to doping densities of at least 5×10^{14},
usually from 10^{15} to 10^{16} atoms/cm^3. Where there is only a
single, lightly doped layer in the photosensitive means the
doping density of this layer may be in the region of $1 \times$
10^{13} to 5×10^{14} atoms/cm^3. Where, as afore-described,
there is at least one second, more heavily doped, impurity
layer which is disposed at least partially below a first,
more lightly doped, impurity layer, said more heavily doped
layer or layers preferably have a heavy doping density of,
for example, at least 2×10^{15} atoms/cm^3 while said more
lightly doped layer preferably has a light doping density,
for example 2×10^{13} atoms/cm^3.

It will though be appreciated that the density of impurity
is not, in practice, constant throughout an impurity layer
in the semiconductor substrate, the distribution of
impurity dopant depending on many factors including inter
alia the energy with which the dopant is implanted into the
substrate, the angle at which the dopant is implanted, and
diffusion of the implanted dopant in the substrate.
Commonly, the density of dopant in the substrate may vary
to a greater or lesser extent with depth from the surface
of the substrate.

Moreover, it will be further appreciated that said first,
more lightly doped, layer and said at least one second,
more heavily doped, layer are not entirely separate layers.
These different layers are manufactured effectively by
implanting one dose of impurity dopant ``on top of'' another
dose of impurity dopant, and so on, until the desired
number of layers of different doping densities have been
formed. For example, commonly the first, more lightly
doped, layer will be created first by exposing at least one
said active area to a predetermined low dose of impurity

which will be implanted/diffused into the semiconductor
substrate to form said first layer. A second, more heavily
doped layer, will subsequently be formed by
implanting/diffusing a second, heavier dose of the same (or

5   a different) impurity through said first layer. Due to the
afore-mentioned distribution characteristics of the doping
process the end result will be that the first layer will
also contain some impurity from the second, high density,
dose, but most of the second dose of impurity will be

10   spacially disposed below the first, lightly doped, layer.
We therefore refer to the second layer being disposed ``at
least partially'' below the first layer.

In another aspect the present invention provides a solid

15   state image sensor comprising a semiconductor substrate of
a first conductivity type having at least one pixel formed
therein for sensing incident light energy, said at least
one pixel comprising photosensitive means, said
photosensitive means comprising said semiconductor

20   substrate and at least one impurity region of a second
conductivity type formed in an active area of the surface
region of said semiconductor substrate, and said
photosensitive means having at least one edge portion
defined by isolation means which separates said active area

25   of the semiconductor substrate surface from other active
areas thereof, said at least one impurity region comprising
a first impurity layer of said second conductivity type,
wherein the image sensor further includes at least one
further impurity layer of said second conductivity type

30   which is more heavily doped with impurity than said first
layer by a factor of at least substantially one order of
magnitude, and the or each said further, more heavily
doped, impurity layer is spaced apart from said at least
one edge portion of said photosensitive means defined by

35   said isolation means so as to restrict the doping density
of the impurity at said at least one edge portion.

In the image sensor according to either of the above aspects of the invention, said at least one pixel may further include at least one transistor which includes a polygate, and preferably also spacer means formed at least

5   partially therearound. Said at least one polygate and respective spacer means where provided, may be formed in the same active area of the semiconductor substrate surface as said photosensitive means and, where this is the case, said polygate and/or said spacer means may define a further

10   edge portion of said photosensitive means. Where said at least one pixel includes such a polygate and/or spacer defining a further edge portion of the photosensitive means, the doping density of said impurity in an edge region of said at least one impurity region at said further

15   one edge portion of said photosensitive means is preferably also substantially restricted. Each said more heavily doped impurity layer is preferably spaced apart from said further edge portion of said photosensitive means in order to further reduce any dark-current leakage exhibited by said

20   pixel.

We believe that the high stresses, physical and electrical, that the more highly doped impurity layer induces at the edge portions of the photosensitive means (in most cases a

25   photodiode made from n-type material in a p-type substrate) defined by the isolation means or the edge of the polygate and/or or spacer means causes the defects that result in the observed random leakage phenomenon problems of the "conventional" photodiode based sensors, in particular CMOS

30   photodiode sensors. By ensuring that the heavily doped impurity layers are spaced away from these edge regions we seek to avoid such problems. Image sensors according to the present invention has been shown to have an incidence of 'leaky' pixels at least an order of magnitude less than

35   similar image sensors using the afore-described "conventional" photodiode structure.

In addition to improving the product yield for the
manufacturer of these image sensors, the image sensors
according to the invention have been found to have an
improved response to ``blue'' light (i.e. light having

5   wavelengths associated with the blue region of the
spectrum). This is due to the fact that (in each pixel)
areas of the photodiode which have restricted doping
densities have improved response to blue light. Lightly
doped layers have wider depletion regions and in our

10 invention tend to be shallower than more heavily doped
layers: in such lightly doped, shallow layers the
associated depletion region that collects the photons of
light is closer to the surface. This improves the blue
light sensitivity of the photodiode.

15

Said solid state image sensor according to the first or
second aspect of the invention is preferably manufactured
in CMOS. Alternatively, the image sensor may be of the CCD
type. The or each said pixel may be of the "active pixel",

20 or alternatively the "passive pixel", type.

Said at least one pixel may comprise more than one said
active area and said at least one transistor, including
said polygate and respective spacer means (where provided),

25 may be formed in a different active area to said
photosensitive means.

Where said photosensitive means has a plurality of edge
portions defined by said isolation means, and/or any

30 polygate and/or spacer which may be present in said at
least one pixel, and the impurity region comprises at least
one more heavily doped impurity layer disposed at least
partially below a more lightly doped impurity layer, a
respective edge of the or each said more heavily doped

35 layer is preferably set back from each said edge portion of
the photosensitive means. In some cases though the edges of
the more heavily doped layer or layers may be set back from

only one or some of said edge portions of the
photosensitive means.

In one embodiment of the invention, where said at least one
pixel comprises said photosensitive means and at least one
transistor, which transistor may be formed in the same
active area as said photosensitive means or may be formed
in a different active area of the pixel, said impurity
region of said photosensitive means may consist of only a
single lightly doped impurity layer and said transistor may
have an impurity region also of said second conductivity
type and comprising a first, lightly doped, impurity layer
and a second, more heavily doped impurity layer, at least a
part of, preferably substantially all of, said second layer
being disposed under said first layer. Alternatively, said
at least one transistor may comprise an impurity region of
said second conductivity type which region consists of only
a single, lightly doped, impurity layer. Where both said
photosensitive element and said transistor comprise a
first, more lightly doped, impurity layer and a second,
more heavily doped, impurity layer, the depths of the
respective second impurity layers may be different.

Said impurity region may have one or more different
impurity dopants therein. Said semiconductor substrate of
said first conductivity type is preferably a p-type silicon
substrate, and said second conductivity type impurity or
impurities in said impurity region are n-type
impurity/impurities. Where said image sensor comprises at
least two impurity layers of said second conductivity type
each layer may be formed by implanting/diffusion of a
different impurity. For example, said lightly, or more
lightly, doped impurity layers may be formed from
Phosphorus (P31) and said heavy, or more heavily doped,
layers may be formed from Arsenic (As75) (both being
suitable n-type dopants).

Said solid state image sensor preferably comprises an array of pixels each comprising photosensitive means and having restricted doping densities at edge portions of the photosensitive means so as to reduce dark-current leakage
5 in the image sensor.

According to a third aspect of the invention we provide a method of reducing dark-current leakage in a solid state image sensor having at least one pixel for sensing incident
10 light energy, manufactured in a semiconductor substrate using generally known techniques, characterised by substantially restricting the doping density of impurity in an edge region of at least one impurity region at an edge portion of a photosensitive means formed in said at least
15 one pixel of said semiconductor substrate.

The method may include avoiding the creation of any heavily doped impurity layers within the or each pixel of the image sensor. Alternatively, the method may include avoiding the
20 creation of any heavily doped impurity layers within one or more photosensitive means formed in the image sensor, other components in the image sensor (within or without the pixels), for example one or more transistors, having heavily doped impurity regions therein .In the latter case,
25 the photosensitive means preferably comprises a single lightly doped impurity layer of one conductivity type implanted/diffused into an active surface region of the semiconductor substrate which is of another conductivity type, and separate masks are used for the
30 implantation/diffusion of the impurity dopant for the lightly doped and heavily doped layers.

According to a fourth aspect of the invention we provide a method of reducing dark-current leakage in a solid state
35 image sensor manufactured using generally known techniques, characterised by including in the manufacture of the image sensor the steps of:

a) defining active areas of the surface of a semiconductor substrate by using an isolation technique to isolate predetermined areas of the semiconductor substrate surface for impurity ion implantation/diffusion;

5   b) providing a first mask means having at least one aperture therein which encompasses at least one said active area;

c) implanting/diffusing an impurity dopant into said at least one active area via said at least one aperture in

10   said first mask means so as to create a first, relatively lightly doped impurity layer in the semiconductor substrate;

d) providing a second mask means having at least one aperture defined therein;

15   e) implanting/diffusing an impurity dopant into said active area via said at least one aperture in said second mask means, so as to create a second, relatively heavily doped impurity layer;

f) said second mask means being arranged relative to said

20   first mask means so that said second impurity layer is disposed at least partially under said first impurity layer and an outer edge of said second impurity layer is set back from a corresponding outer edge of said first impurity layer at at least one edge portion of a photosensitive

25   region of the image sensor.

The method may further include providing one or more further mask means each having at least one aperture defined therein, and implanting/diffusing an impurity

30   dopant into said active area via said at least one aperture in the or each said further mask means, so as to create a one or more further, relatively heavily doped impurity layer(s) in said active area, the masks being arranged relative to each other so that an outer edge of the or each

35   said further impurity layer is set back from a corresponding outer edge of said first impurity layer at said at least one edge portion of said photosensitive region.

The above described methods are primarily intended for use
in the manufacture of CMOS image sensors, but may also be
applicable in the manufacture of CCD-type image sensors. It
5   will be appreciated that the known techniques for
manufacturing such sensors will be well-known to the person
skilled in the art of solid state image sensor manufacture
and will include the conventional isolation techniques
(e.g. LOCOS, Modified LOCOS, Trench Isolation, and shallow
10   Trench Isolation), photolithography , impurity dopant
implantation/diffusion, etching etc., all of which involve
numerous steps and procedures which may be implemented in
various ways. By way of example only we would refer to one
recognised text on the manufacture of solid state devices
15   which details some of the conventional procedures which may
be carried out to create such an image sensor. This text is
"VLSI Technology", 2nd Edition, by S.M.Sze (Published by
McGraw-Hill International Editions, Electrical Engineering
Series).
20
Embodiments of the invention will now be described, by way
of example only, and with reference to the accompanying
drawings in which:
Fig.1 is a schematic, partial representation of a CCD
25   photodiode image sensor;
Fig.2(a) is a schematic, partial representation of a
passive pixel CMOS photodiode image sensor;
Fig.2(b) is a schematic, partial representation of an
active pixel CMOS photodiode image sensor;
30   Fig.3 comprises a schematic cross-sectional side view and a
plan view of one pixel of a conventional CMOS photodiode
image sensor;
Fig. 4 comprises a schematic cross-sectional side view and
a plan view of one pixel of a first embodiment of an
35   improved CMOS photodiode image sensor;
Fig.5 comprises a schematic cross-sectional side view and a
plan view of one pixel of a second embodiment of an
improved CMOS photodiode image sensor;

Fig.6 comprises a schematic cross-sectional side view and a plan view of one pixel of a third embodiment of an improved CMOS photodiode image sensor;

Fig.7 comprises a schematic cross-sectional side view and a
5 plan view of one pixel of a fourth embodiment of an improved CMOS photodiode image sensor;

Fig.8 comprises a schematic cross-sectional side view and a plan view of one pixel of a fifth embodiment of an improved CMOS photodiode image sensor;

10 Fig.9 comprises a schematic cross-sectional side view and a plan view of one pixel of a sixth embodiment of an improved CMOS photodiode image sensor;

Fig.10 comprises a schematic cross-sectional side view and a plan view of one pixel of a seventh embodiment of an
15 improved CMOS photodiode image sensor; and

Fig.11 comprises a schematic cross-sectional side view and a plan view of one pixel of an eighth embodiment of an improved CMOS photodiode image sensor.

20 Fig.1 illustrates schematically a CCD photodiode image sensor 1, where only one pixel 9 of the pixel array 15 is shown (for clarity). There are many possible configurations for the arrangement of the CCD shift elements, but the common items are a photodiode 10 and an access transistor
25 11. The charge accumulated in the photodiode is transferred to a vertical transfer unit 12 via the access transistor 11, then the charge packets are shifted through the vertical transfer unit to a horizontal transfer unit 13 where they are finally shifted out via an output buffer 14
30 to an output O/P. The array 15 of pixels can be linear or 2-dimensional.

Figs. 2(a) and 2(b) illustrate schematically two predominant types of CMOS photodiode image sensor. Fig.2(a)
35 illustrates a passive pixel sensor 2a, only one pixel 19 in a pixel array 22 of the sensor being shown (for clarity). In use of the sensor, charge accumulated in a photodiode 20 is read from the pixel 19 by an access transistor 21 via a

charge detector 23 at the end of each pixel column of the
array (the array comprising a number of rows and columns),
and the result is multiplexed under the control of the
horizontal access unit 24, to an output unit 26 having an
5   output O/P. The horizontal access unit 24 is commonly made
of either address decoding schemes or shift register
schemes. A vertical access unit 25 controls which rows are
being read or reset, and is also commonly made of either
address decoding schemes or shift register schemes.
10

Fig.2(b) illustrates an active pixel sensor 2b (like parts
to the sensor of Fig.2(a) being referenced by like
numerals), which includes a buffer within the pixel 19,
such that the charge accumulated on the photodiode 20 can
15   be read more easily as a voltage or a current. Each of the
active pixels in the pixel array 22 in Fig.2(b) uses a MOS
transistor 27 to form the top half of a voltage buffer
within the pixel. The resulting low-impedance voltage
signal can be read out relatively easily via a read
20   transistor 28 and a column buffer 29. The photodiode is
reset by an access transistor 21.

Variations of each of these types of CMOS sensor are
possible, including active pixel types which use fewer or
25   more transistors per pixel than the 3-transistor
architecture shown in Figure 2(b). There are also
variations of the passive pixels with extra transistors
added to improve blooming. For all CMOS sensors the array
22 of pixels can be linear or 2-dimensional.
30

The commonality between the passive pixel CMOS photodiode
sensor, the active pixel CMOS photodiode sensors and the
CCD photodiode sensor is that each pixel contains a
photodiode 10,20 and at least one MOS access transistor
35   11,21. Fig.3 shows schematically (much enlarged), both a
plan view (upper portion of Fig.3) and a cross-sectional
side view (taken along the line X-X' in the plan view), of
one pixel in a "conventional" photodiode image sensor in a

P-substrate CMOS process. The pixel includes a photodiode
20 and an access transistor 21. The photodiode 20 is made
by implanting and/or diffusing n-type, or ``N-type'' layers
33, 34 in a p-type or ``P-type'' silicon substrate 32. There
5   are two N-type layers 33,34 of different doping densities
and depths. The uppermost layer 34 is lightly doped to a
shallow depth, and lowermost layer 33 has a doping density
at least an order of magnitude greater than the uppermost
layer 34 and to a depth greater than a factor of one point
10 five of the depth of uppermost layer 33. These layers shall
henceforth be referred to as the NM (layer 34) and the NP
(layer 33) respectfully. The N-type dopants although of the
same conductivity type do not have to be made of the same
impurity ions, the two most commonly used ions being
15 Phosphorus, (P31), and Arsenic (As75).

The access transistor 21 comprises a polygate 38 (the
``gate'' element of the transistor) and may also include a
spacer 37. A spacer 37, in the form of an oxide, is often
20 used to allow an implant or "dopant" to be self aligned
with a sized version of the polygate 38. The drain/source
elements of the transistor comprise the photodiode 20 and
two further n-type impurity regions in the form of layers
21a,21b, as shown in Fig.3. These two n-type layers 21a,21b
25 are of different doping densities, similarly to the
photodiode 20. (The more heavily doped layer 21a is
commonly of the same depth as the heavily doped layer 33 in
the photodiode, but may be of a shallower or deeper depth.)

30 As shown in Fig.3, the photodiode 20 and the access
transistor 21 are normally made in the same "active area"
30, based on their implementation in a standard sub-micron
P-substrate CMOS process. Although it is possible to layout
the access transistor in a separate active area, this is
35 generally not done as it is less efficient spatially. The
"active areas" in a CMOS process are the areas of silicon
in which diodes and transistors can be manufactured, and
are at the surface of the semiconductor substrate. They are

defined by isolation means 31 that separates out different
"active areas". The isolation means 31, in the sensor
illustrated in Fig.3, is an area of Field Oxide 31 that has
been generated using a LOCOS (Local Oxidation of Silicon)
5   technique. (Other techniques exist, such as Modified LOCOS,
Trench isolation and shallow Trench Isolation.) The
photodiode 20 and the transistor 21 are each made of N-type
layers 33,34 in a P-type substrate 32 of silicon. There may
be one or more N-type layers within the photodiode. These
10   are generally achieved by implanting or diffusing dopants
through an opening 39 in a mask 40 that prevents the
passage of these ions. The mask is commonly photoresist, or
an insulator defined by photoresist (e.g. silicon oxide or
silicon nitride). Only surface areas which do not have a
15   blocking layer of sufficient thickness will receive the
dose of dopants. Hence the areas below the isolation means
31, the polygate 38 and the spacer 37, if present, do not
receive the dopants. The final position of the dopants will
depend on the subsequent processing of the silicon, as they
20   will diffuse laterally and vertically when given certain
heat treatments. The P-type silicon is often also graded in
the vertical direction by a P-type surface implant, "P-
FIELD" outside the "active area" 30, a P-type well implant
"PWELL" beneath the "active area" 30, and by using a P-type
25   "EPITAXIAL" layer grown on top of a heavily doped P-type
base substrate - these are not shown as they do not
directly influence the invention. The photodiode 20 can
contain a contact 35 to a connectivity layer, in this
diagram shown as METAL1 36, if connectivity is required to
30   other elements within the pixel, for example the buffer
transistor 10 in the active pixel sensor 1b previously
mentioned. The transistor 21 also has a metal contact 50
connecting the transistor to the same or a further
connectivity layer 52.

35

The standard technique for creating the N-type layers in a
standard CMOS process is to self align these layers to a
logical combination of the active area 30 AND the mask

opening 39 for the implant, NOT the polygate 38,
with/without a "spacer" 37. If a "spacer" is present then
the NP layer is generally aligned to its edge, while the NM
layer is aligned to the edge of the polygate 38. The
5   implant opening(s) 39 in the mask 40 in this case encompass
the active area(s) 30.

As afore-mentioned, we believe that the high stresses,
physical and electrical, that the highly doped NP layer
10   induces at the edge 48 of the photodiode 20 adjacent the
isolation (Field Oxide 31) and at the edge 49 of the
polygate/spacer 38/39 causes the defects that result in the
observed manufacturing problems of photodiode based
sensors, in particular CMOS sensors. The "modified" or
15   "improved" image sensors which will now be described with
reference to Figs. 4-11 have been shown to have an
incidence of 'leaky' pixels at least an order of magnitude
less than the "conventional" diode structure.

20   We have designed a new photodiode structure that moves the
highly doped NP layers away from at least some portion of
the photodiode edges 48,49 at the isolation 31 and the
polygate/spacer 38/37 edge. Figure 4 shows a plan and
cross-sectional cross-sectional views (similar to Fig.3) of
25   one pixel of an improved sensor according to one embodiment
of the invention (like parts to those of the sensor of
Fig.3 being referenced with like numerals). Each pixel in
the improved sensor includes a "modified" photodiode in a
P-substrate process, in which photodiode 20 the NP layer 33
30   has been brought back from all of the outer edge 45 of the
NM layer 34 at the isolation 31 and brought back from that
portion of the outer edge 45 of the NM layer at the spacer
37. The distance by which the NP layer is set back from the
outer edge 45 of the NM layer, at the isolation 31 and the
35   spacer 37, may vary over the perimeter of the NP layer.
This is achieved during the manufacture of the image sensor
by using separate masks 40,41 for the light and heavy
doping processes used to create the NM and NP layers

respectively. The NM layer is created by implanting/diffusing n-type impurity dopant into the active area 30 via the single aperture 39 in the first mask 40, similarly to the procedure used to create the NM layer in

5   the conventional photodiode structure of Fig.3. However, the NP layer is created by implanting/diffusing n-type impurity dopant into only two portions of the active area via two respective apertures 47,48 in a second mask 41 laid over the first mask 40, as indicated in Fig.4. One aperture

10   48 in the second mask 40 is for the NP layer of the transistor 21, while the other aperture 47 is for the NP layer in the photodiode 20. In the embodiment of Fig.4, the apertures 47,48 in the second mask 41 are substantially rectangular and the aperture 47 for the photodiode NP layer

15   is of a width in one direction (i.e. has a first diameter) such that two opposite (rectilinear) edges 53,54 of the NP layer in the photodiode 20 will be set back by distances d1 and d2 respectively from corresponding portions 55,56 of the outer edge 45 of the NM layer, at the isolation 31

20   and/or the spacer 37, as shown. The minimum distance recommended for d1 and d2 is $\lambda/4$, where λ is the minimum feature size of the CMOS process used. The distances d1 and d2 do not have to be equal. The aperture 47 for the photodiode NP layer is of a length in another direction

25   (i.e. has a second diameter) such that two further, opposite edges (not shown) of the NP layer in the photodiode 20 will be set back from corresponding portions of the outer edge of the NM layer, at the isolation 31, preferably being set back by at least $\lambda/4$.

30
It will be appreciated that in reality the various edges of the isolation 31, the photodiode 20, the NM and NP layers, the polygate and/or spacer are not precisely defined lines, as shown in the drawings, but tend to be somewhat fuzzy as

35   afore-described, over a region which may have a width of up to approximately $\lambda/10$, depending on manufacturing tolerances, impurity implantation/diffusion processes used,

and/or other reasons. It will further be appreciated that
the sensor fabrication engineer, familiar with CMOS
fabrication and tolerances involved, will be able to
control the formation of the n-type layers to an extent
5   which is such that the nominal position of these edges is
known, at least to within given tolerance(s).

The NM implant aperture or ``opening'' 39 in the first mask
40 ensures that the NM implant is over the whole photodiode
10   20, by encompassing the active area 30 completely. The NP
implant apertures or ``openings'' 47,48 can be completely or
only partially enclosed effectively within the opening 39
for the NM implant, in the area of the photodiode 20. The
amount of the enclosure alters the effectiveness of the
15   improvement in the performance of the pixel (with regard to
random dark current leakage). The masks may be made from
photoresist which is subsequently removed, or by the
deposition of material which is subsequently left on the
substrate or ``die''.
20
It will further be appreciated that the mask openings may
be of any shape, as may be the photodiode 20 and transistor
21.

25   In the following Figs.5-11, like parts to those in Figs.3
and 4 have been referenced by like numerals.

Figure 5 shows a plan view and a sectional view of a pixel
incorporating a "modified" photodiode in a P-substrate
30   process where the NP layer has been brought back from only
part (not all) of the outer edge 45 of the NM layer 33 of
the photodiode 20 (in the active area 30), that part
including the portion 56 at the spacer 37.

35   Figure 6 shows another "modified" photodiode in a P-
substrate process where the NP layer has been brought back
from only part of the outer edge 45 of the NM layer of the

photodiode 20 defined by the isolation 31, and has not been
brought back from the spacer 37.

Figure 7 shows a "modified" photodiode, where there is no
5   NP implant within the photodiode 20, but this implant
exists in the access transistor 21 in the pixel. Note the
contact 35 within the photodiode 20 is shown to be over
only the NM layer 34. This is possible providing the
contact method, within the CMOS process used, does not
10   cause a short or a reliability problem through the NM layer
to the substrate 32. One method to achieve this is to
deposit a barrier metal before putting down the contact. As
shown in Fig.7, the second mask 41 in this case has only
one opening 48 for the active area 30 of the pixel, for
15   each opening 39 of the first mask 40.

Figure 8 is the same as Figure 7, but without a contact 35
within the photodiode 20. In this case there is only the
contact 50 on the transistor 21, to the connectivity layer
20   52. This is to show that a "modified" pixel does not have
to have a contact within its the photosensitive region
(i.e. the photodiode 20), if further connectivity outside
the active area is not required e.g. in the case of a
passive pixel. This is applicable to any of the
25   configurations of "modified" photodiodes described.

Figure 9 shows a section of a "modified" photodiode similar
to the photodiode of Fig.4, but with an additional (second)
highly doped impurity layer 42, obtained by using a third
30   mask 43 having a mask opening 44 over the active area 30.
All the afore-described embodiments can be provided with a
plurality of high implant layers, if desired. The edges of
each such highly doped layer are preferably each set back
from a corresponding portion of the outer edge of the
35   photodiode 20 defined by the isolation 31, or the polygate
38 or spacer 37, but in some cases only some of the edges
may be set back in this manner. As shown in Fig. 9, the

edges of each highly doped layer may also be set back from
the edges of adjacent highly doped layers.

Figure 10 shows a section of a "modified" photodiode in a
5   P-substrate process where the photodiode 20 and the access
transistor 21 are in separate active areas 30a,30b. The
photodiode, having an NM layer and an NP layer, is shown
with the NP layer edges set back from all the outer edge of
the NM layer (defined by the isolation 31), in the active
10   area 30a which contains the photodiode 20a. The NP layer is
present in the access transistor 21 drain/source regions.
The NP implant mask 41 in this case has one opening 47 for
the photodiode and another opening 48 for the NP layer in
each of the two necessary N-type impurity regions 60,61
15   transistor 21. All configurations of NP implant are
applicable to this embodiment.

Figure 11 shows a section of a "modified" photodiode, where
there is no NP implant (i.e. heavily doped N-type region)
20   within the photodiode 20 or the access transistor 21, but
at least one heavily doped region or layer does exist
elsewhere in the solid state image sensor, for example in
the logic or readout circuitry, outside the pixel array.
There is therefore no opening in the second (NP implant)
25   mask 41 over the active area 30 of the pixel shown. The
mask 41 will have openings at the appropriate other active
areas in the sensor where the heavily doped regions are to
be created.

30   In addition to improving the product yield for the
manufacturer of these CMOS image sensors, the area of the
"modified" photodiode 20 that has only the NM layer has
improved response to blue light, as the associated
depletion layer that collects the photons of light is
35   closer to the surface. The greater the area of the
photodiode that contains only NM layer, the better the
response of the sensor towards light in the blue wavelength
region of the spectrum.

It will be appreciated that various modifications to the
described embodiments are possible without departing from
the scope of the invention. For example, the first 40,
5 second 41 and any further, masks may be deposited in any
preferred order, and the NM/NP impurity layers formed in
any desired order accordingly without departing from the
invention.

10 It will further be appreciated that in some device
fabrication processes, namely where all the diodes and
transistors on the substrate 32 which is of one
conductivity type (i.e. P-type or N-type) are to be of the
same conductivity type (i.e. all NMOS devices, or all PMOS
15 devices) it may be possible to create the NM layer 34
without using the first mask 40, by instead simply doping
all the active areas of the semiconductor substrate at the
same time. The second mask 41, and any further masks, would
be arranged relative to the appropriate ones of the various
20 active areas so that one or more edges of the NP layer(s)
are set back from the edge of the photodiode 20 defined by
the isolation means 31. Where the sensor is fabricated in
CMOS it will be necessary to use a first mask when creating
the NM layer so as to avoid doping all active areas of the
25 substrate (since the substrate will be designed to contain
both NMOS and PMOS transistors).

CLAIMS

1. A solid state image sensor comprising a semiconductor substrate of a first conductivity type having at least one
5   pixel formed therein for sensing incident light energy, said at least one pixel comprising photosensitive means, said photosensitive means comprising said semiconductor substrate and at least one impurity region formed within an active area of the surface of said semiconductor substrate,
10 and said photosensitive means having at least one edge portion defined by isolation means which isolation means separates said active area of the semiconductor substrate from other active areas thereof, said at least one impurity region comprising at least one impurity layer of a second
15 conductivity type, wherein the doping density of said impurity in an edge region of said at least one impurity region at said at least one edge portion of said photosensitive means is substantially restricted.

20 2. A solid state image sensor according to claim 1, wherein said photosensitive means is a photodiode.

3. A solid state image sensor according to claim 1 or claim 2, wherein the doping density in said edge region of said
25 at least one impurity region is restricted by substantially avoiding any high density impurity doping in said edge region.

4. A solid state image sensor according any of claims 1 to
30 3, wherein said at least one impurity region in said photosensitive means comprises a single, lightly doped impurity layer.

5. A solid state image sensor according to any of claims 1
35 to 3, wherein said at least one impurity region comprises at least one second, more heavily doped, impurity layer which is disposed at least partially below a first, more lightly doped, impurity layer, and an outer edge of said at

least one second, more heavily doped, impurity layer is set back from said at least one edge portion of the photosensitive means, whereby the doping density of impurity at said edge portion is substantially restricted.

5

6. A solid state image sensor according to claim 5, wherein said at least one second, more heavily doped, layer is deeper than said first, more lightly doped, layer by a factor of at least 1.5.

10

7. A solid state image sensor according to claim 6, wherein the depth of said at least one more heavily doped layer greater than 0.1μm, as measured from the surface of the photosensitive means.

15

8. A solid state image sensor according to any preceding claim, wherein said edge region of said at least one impurity region having said substantially restricted doping density has a width of at least $\lambda/4$, where λ is the minimum

20 process feature size of the solid state image sensor.

9. A solid state image sensor according to any of claims 5-7, wherein said outer edge of said at least one second, more heavily doped impurity layer is set back from said at

25 least one edge portion by at least $\lambda/4$, where λ is the minimum process feature size of the solid state image sensor.

10. A solid state image sensor according to claim 4,
30 wherein the doping density of said single, lightly doped impurity layer is in the range of 1×10^{13} to 5×10^{14} atoms/cm^3.

11. A solid state image sensor according to any of claim 5-
35 7, wherein said more lightly doped impurity layer has a doping density of at least 2×10^{13} atoms/cm^3 and said at

least one second, more heavily doped, impurity layer has a
doping density not greater than 2 x 10^{15} atoms/cm^3.

12. A solid state image sensor comprising a semiconductor
substrate of a first conductivity type having at least one
pixel formed therein for sensing incident light energy,
said at least one pixel comprising photosensitive means,
said photosensitive means comprising said semiconductor
substrate and at least one impurity region of a second
conductivity type formed in an active area of the surface
region of said semiconductor substrate, and said
photosensitive means having at least one edge portion
defined by isolation means which separates said active area
of the semiconductor substrate surface from other active
areas thereof, said at least one impurity region comprising
a first impurity layer of said second conductivity type,
wherein the image sensor further includes at least one
further impurity layer of said second conductivity type
which is more heavily doped with impurity than said first
layer by a factor of at least substantially one order of
magnitude, and the or each said further, more heavily
doped, impurity layer is spaced apart from said at least
one edge portion of said photosensitive means defined by
said isolation means so as to restrict the doping density
of the impurity at said at least one edge portion.

13. A solid state image sensor according to any preceding
claim, wherein said at least one pixel further includes at
least one transistor.

14. A solid state image sensor according to claim 13,
wherein said at least one transistor is formed in the same
active area as said photosensitive means and said at least
one transistor comprises a polygate and spacer means, said
spacer means defining a further edge portion of said
photosensitive means, and wherein the doping density of
said impurity in an edge region of said at least one

impurity region at said further one edge portion of said
photosensitive means is also substantially restricted.

15. A solid state image sensor according to claim 14, when
dependant from any of claims 5-7, wherein each said more
heavily doped impurity layer is spaced apart from said
further edge portion of said photosensitive means in order
to further reduce any dark-current leakage exhibited by
said pixel.

16. A solid state image sensor according any preceding
claim, wherein said sensor is manufactured in CMOS.

17. A solid state image sensor according any preceding
claim, wherein said sensor is a CCD photodiode image
sensor.

18. A solid state image sensor according to any preceding
claim, wherein said photosensitive means has a plurality of
edge portions defined by said isolation means, and the
impurity region comprises at least one more heavily doped
impurity layer disposed at least partially below a more
lightly doped impurity layer, and a respective edge of the
or each said more heavily doped layer is set back from each
said edge portion of the photosensitive means.

19. A solid state image sensor according to any preceding
claim wherein said impurity region comprises one or more
different impurities of said second conductivity type, said
semiconductor substrate of said first conductivity type is
a p-type silicon substrate, and said one or more impurities
of said second conductivity type are n-type
impurity/impurities.

20. A solid state image sensor according to any preceding
claim, wherein said sensor comprises an array of pixels
each comprising photosensitive means and having restricted
impurity doping densities at edge portions of the

photosensitive means so as to reduce dark-current leakage
in the image sensor.

21. A method of reducing dark-current leakage in a solid
state image sensor having at least one pixel for sensing
incident light energy, manufactured in a semiconductor
substrate using generally known techniques, characterised
by substantially restricting the doping density of impurity
in an edge region of at least one impurity region at an
edge portion of a photosensitive means formed in said at
least one pixel of said semiconductor substrate.

22. A method according to claim 21, wherein the method
includes avoiding the creation of any heavily doped
impurity layers within said at least one pixel of the image
sensor.

23. A method according to claim 21, wherein the method
includes avoiding the creation of any heavily doped
impurity layers within said photosensitive means formed in
said at least one pixel of the image sensor.

24. A method of reducing dark-current leakage in a solid
state image sensor manufactured using generally known
techniques, characterised by including in the manufacture
of the image sensor the steps of:
a) defining active areas of the surface of a semiconductor
substrate by using an isolation technique to isolate
predetermined areas of the semiconductor substrate surface
for impurity ion implantation/diffusion;
b) providing a first mask means having at least one
aperture therein which encompasses at least one said active
area;
c) implanting/diffusing an impurity dopant into said at
least one active area via said at least one aperture in
said first mask means so as to create a first, relatively
lightly doped impurity layer in the semiconductor
substrate;

d) providing a second mask means having at least one
aperture defined therein;

e) implanting/diffusing an impurity dopant into said active
area via said at least one aperture in said second mask

5   means, so as to create a second, relatively heavily doped
impurity layer;

f) said second mask means being arranged relative to said
first mask means so that said second impurity layer is
disposed at least partially under said first impurity layer

10   and an outer edge of said second impurity layer is set back
from a corresponding outer edge of said first impurity
layer at at least one edge portion of a photosensitive
region of the image sensor.

15   25. The method according to claim 24, wherein the method
further includes providing one or more further mask means
each having at least one aperture defined therein, and
implanting/diffusing an impurity dopant into said active
area via said at least one aperture in the or each said

20   further mask means, so as to create a one or more further,
relatively heavily doped impurity layer(s) in said active
area, the masks being arranged relative to each other so
that an outer edge of the or each said further impurity
layer is set back from a corresponding outer edge of said

25   first impurity layer at said at least one edge portion of
said photosensitive region.

26. A solid state image sensor as described herein and with
reference to any one of Figs. 4-11 of the drawings.

30

Application No: GB 9708574.0   **Examiner:** Martyn Dixon
Claims searched: all   **Date of search:** 9 July 1997

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Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H1K (KECCX,KECD,KECX)

Int Cl (Ed.6): H01L (27/14,27/146,27/148,31/0352)

Other: online: WPI, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	EP 0360595 A	(Matsushita) see heavily doped region 11 and spacing l_1 in fig 1	1,2,17, 20,21
X	EP 0240238 A	(Sony) see low impurity concentration region 23 in fig 2	1-3,12,16, 20,21
X	US 5514887 A	(NEC) see impurity layers 131,132 in fig 8	1-3,12, 13,16,17, 20,21