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(54) **FORMATION OF A DISPOSABLE SPACER TO POST DOPE A GATE CONDUCTOR**

(75) Inventors: **David V. Horak**, Essex Junction, NY (US); **Toshiharu Furukawa**, Essex Junction, VT (US); **Akihisa Sekiguchi**, Briarcliff Manor, NY (US)

Correspondence Address:
SCULLY, SCOTT, MURPHY & PRESSER, P.C.
400 GARDEN CITY PLAZA
Suite 300
GARDEN CITY, NY 11530 (US)

(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

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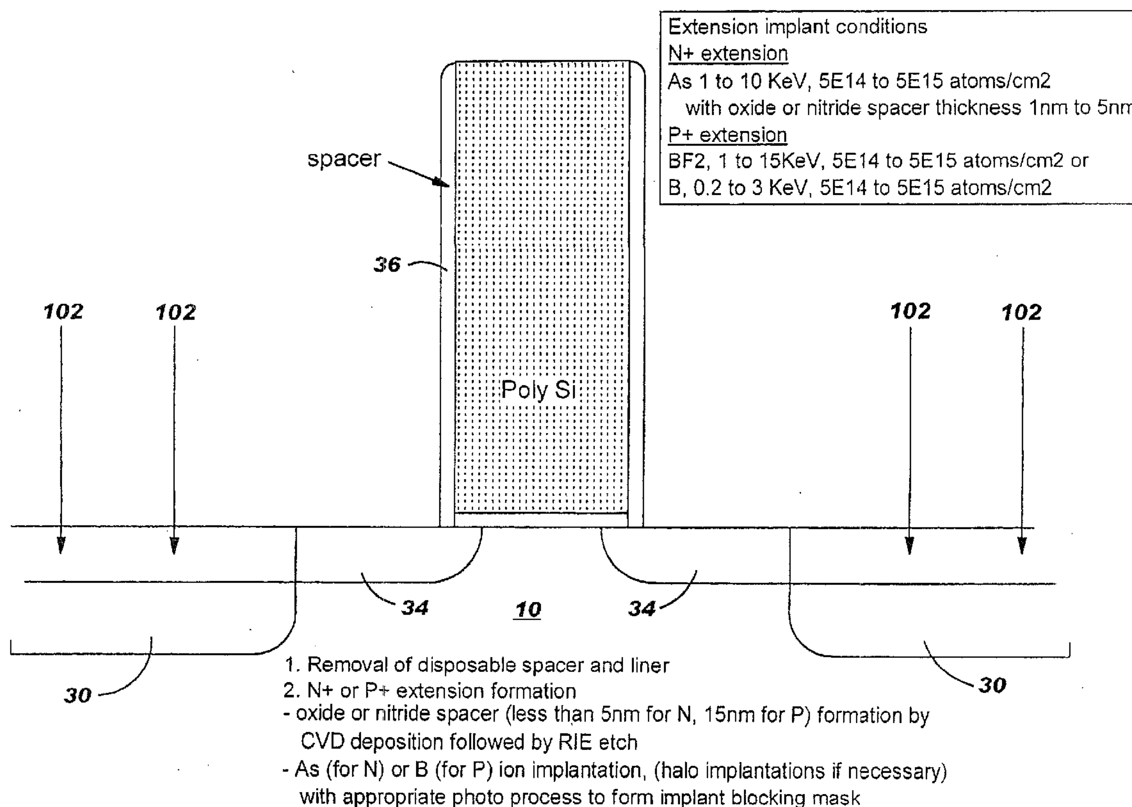
(57) **ABSTRACT**

A method of forming a doped gate structure on a semiconductor device and a semiconductor structure formed in that method are provided. The method comprises the steps of providing a semiconductor device including a gate dielectric layer, and forming a gate stack on said dielectric layer. This latter step, in turn, includes the steps of forming a first gate layer on the dielectric layer, and forming a second disposable layer on top of the first gate layer. A fat spacer is formed around the first gate layer and the second disposable layer. The second disposable layer is removed, and ions are implanted in the first gate layer to supply additional dopant into the gate above the gate dielectric layer, while the fat disposable spacer keeps the implanted ions away from the critical source and drain diffusion region.



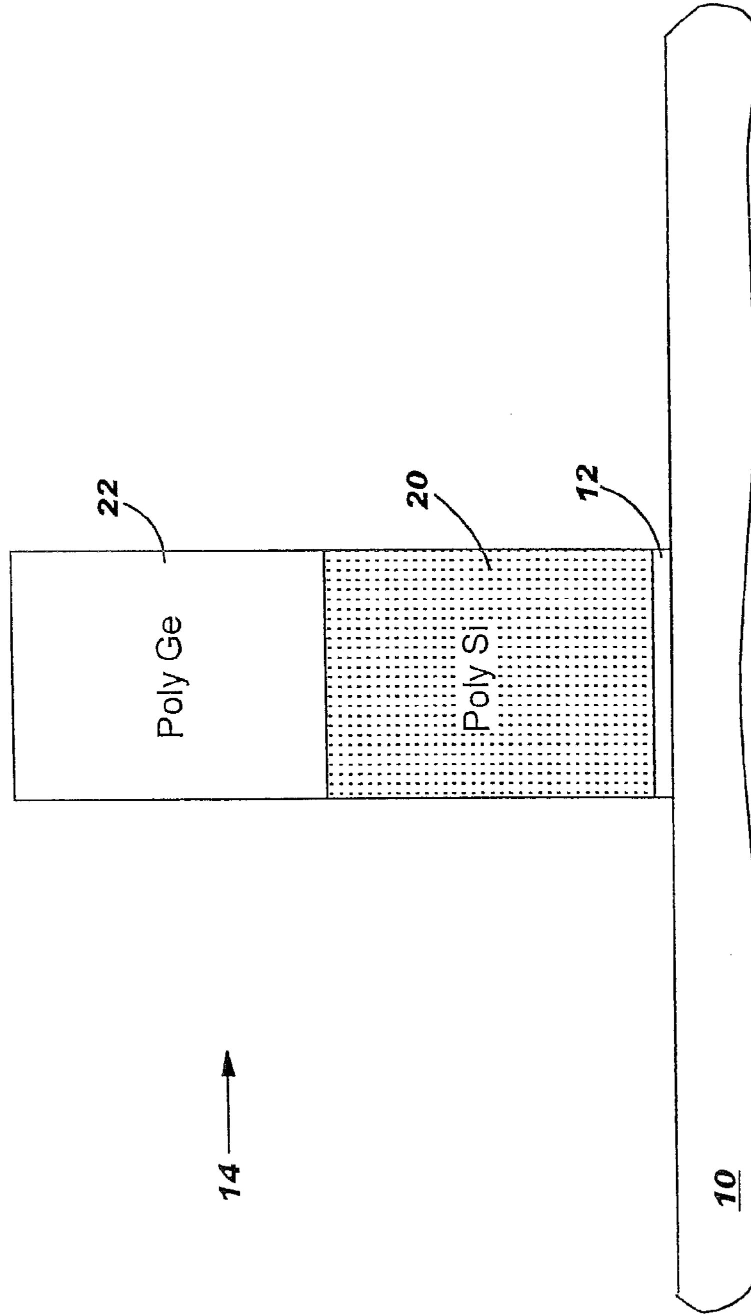
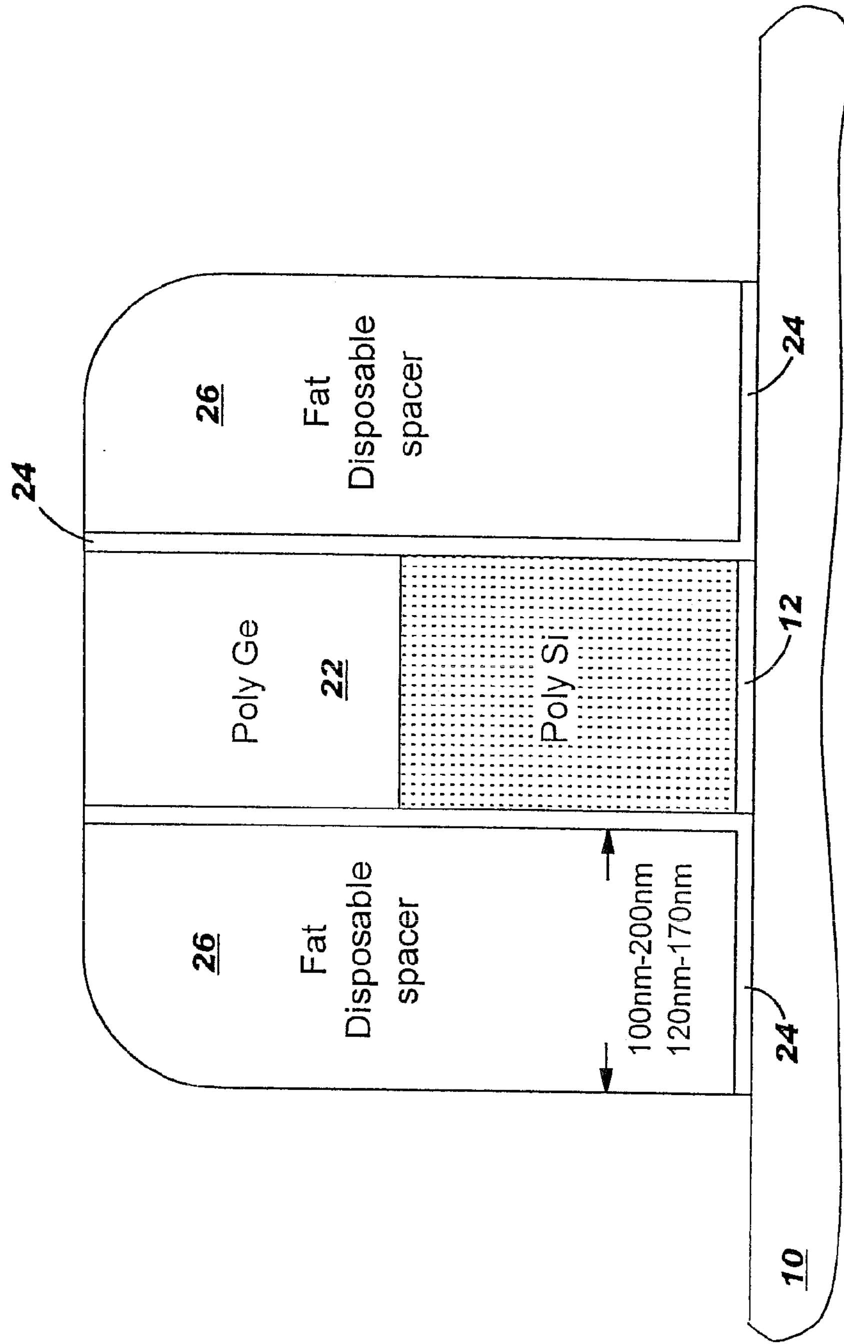


FIG. 1

FIG. 2



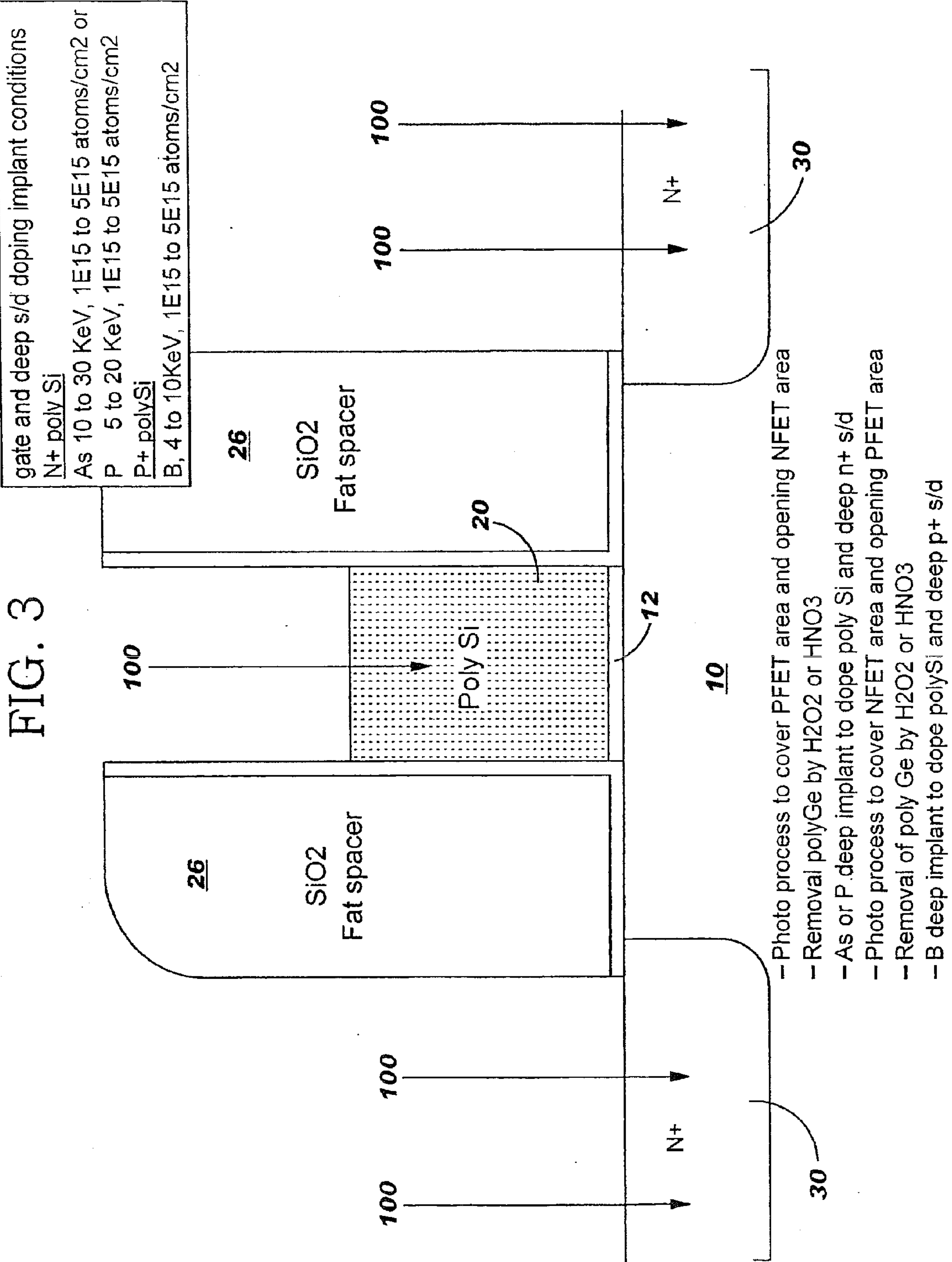


FIG. 3
gate and deep s/d doping implant conditions
N+ poly Si
As 10 to 30 KeV, 1E15 to 5E15 atoms/cm2 or
P 5 to 20 KeV, 1E15 to 5E15 atoms/cm2
P+ polySi
B, 4 to 10KeV, 1E15 to 5E15 atoms/cm2
100
100
100
100
100
26
SiO2
Fat spacer
26
SiO2
Fat spacer
20
Poly Si
12
10
N+
N+
30
30
– Photo process to cover PFET area and opening NFET area
– Removal polyGe by H2O2 or HNO3
– As or P deep implant to dope poly Si and deep n+ s/d
– Photo process to cover NFET area and opening PFET area
– Removal of poly Ge by H2O2 or HNO3
– B deep implant to dope polySi and deep p+ s/d

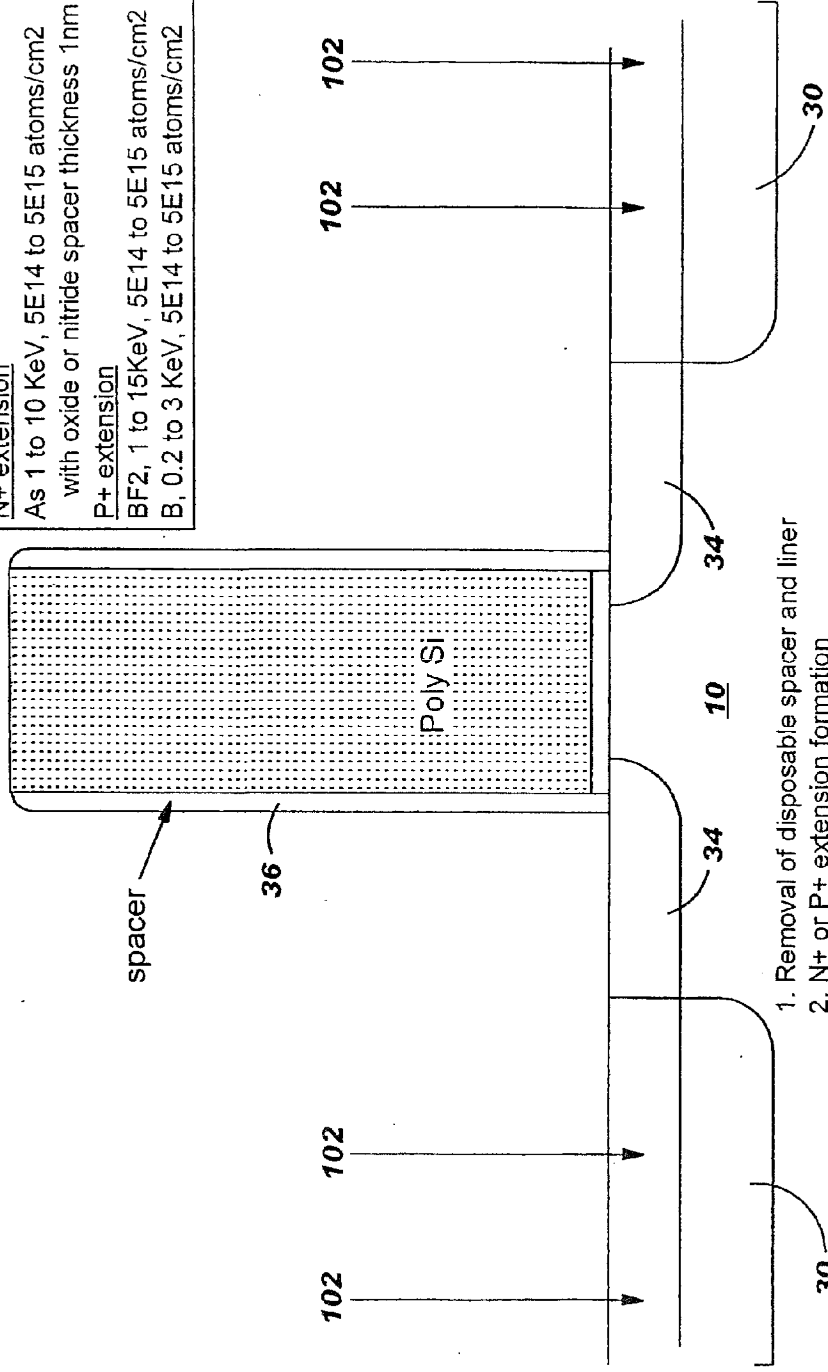


FIG. 4
Extension implant conditions
N+ extension
As 1 to 10 KeV, 5E14 to 5E15 atoms/cm2
with oxide or nitride spacer thickness 1nm to 5nm
P+ extension
BF2, 1 to 15KeV, 5E14 to 5E15 atoms/cm2 or
B, 0.2 to 3 KeV, 5E14 to 5E15 atoms/cm2
spacer
36
Poly Si
102
102
102
102
34
34
10
30
30
1. Removal of disposable spacer and liner
2. N+ or P+ extension formation
- oxide or nitride spacer (less than 5nm for N, 15nm for P) formation by
CVD deposition followed by RIE etch
- As (for N) or B (for P) ion implantation, (halo implantations if necessary)
with appropriate photo process to form implant blocking mask

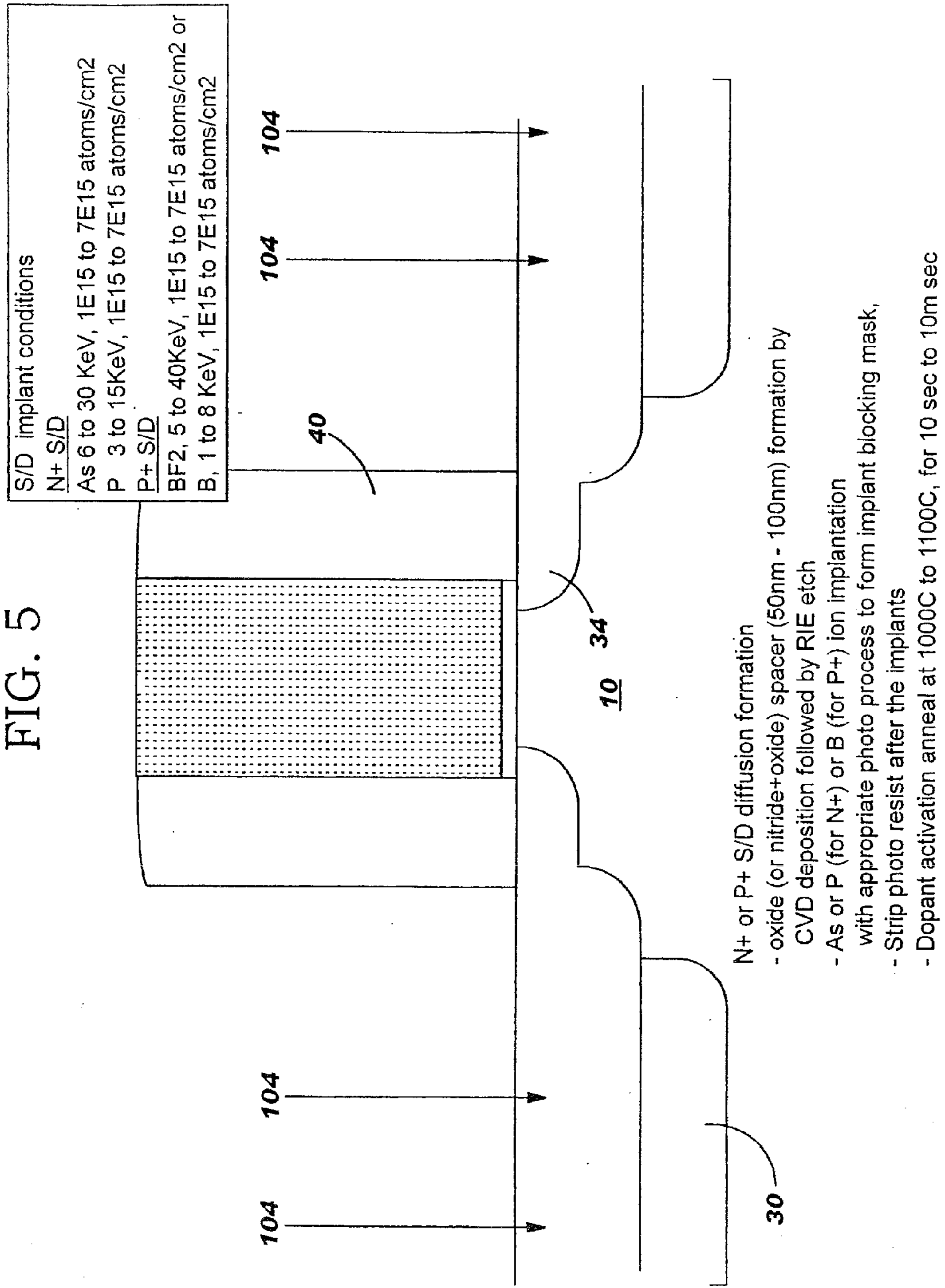


FIG. 5
S/D implant conditions
N+ S/D
As 6 to 30 KeV, 1E15 to 7E15 atoms/cm2
P 3 to 15KeV, 1E15 to 7E15 atoms/cm2
P+ S/D
BF2, 5 to 40KeV, 1E15 to 7E15 atoms/cm2 or
B, 1 to 8 KeV, 1E15 to 7E15 atoms/cm2
104
104
104
104
40
34
10
30
N+ or P+ S/D diffusion formation
- oxide (or nitride+oxide) spacer (50nm - 100nm) formation by
CVD deposition followed by RIE etch
- As or P (for N+) or B (for P+) ion implantation
with appropriate photo process to form implant blocking mask,
- Strip photo resist after the implants
- Dopant activation anneal at 1000C to 1100C, for 10 sec to 10m sec

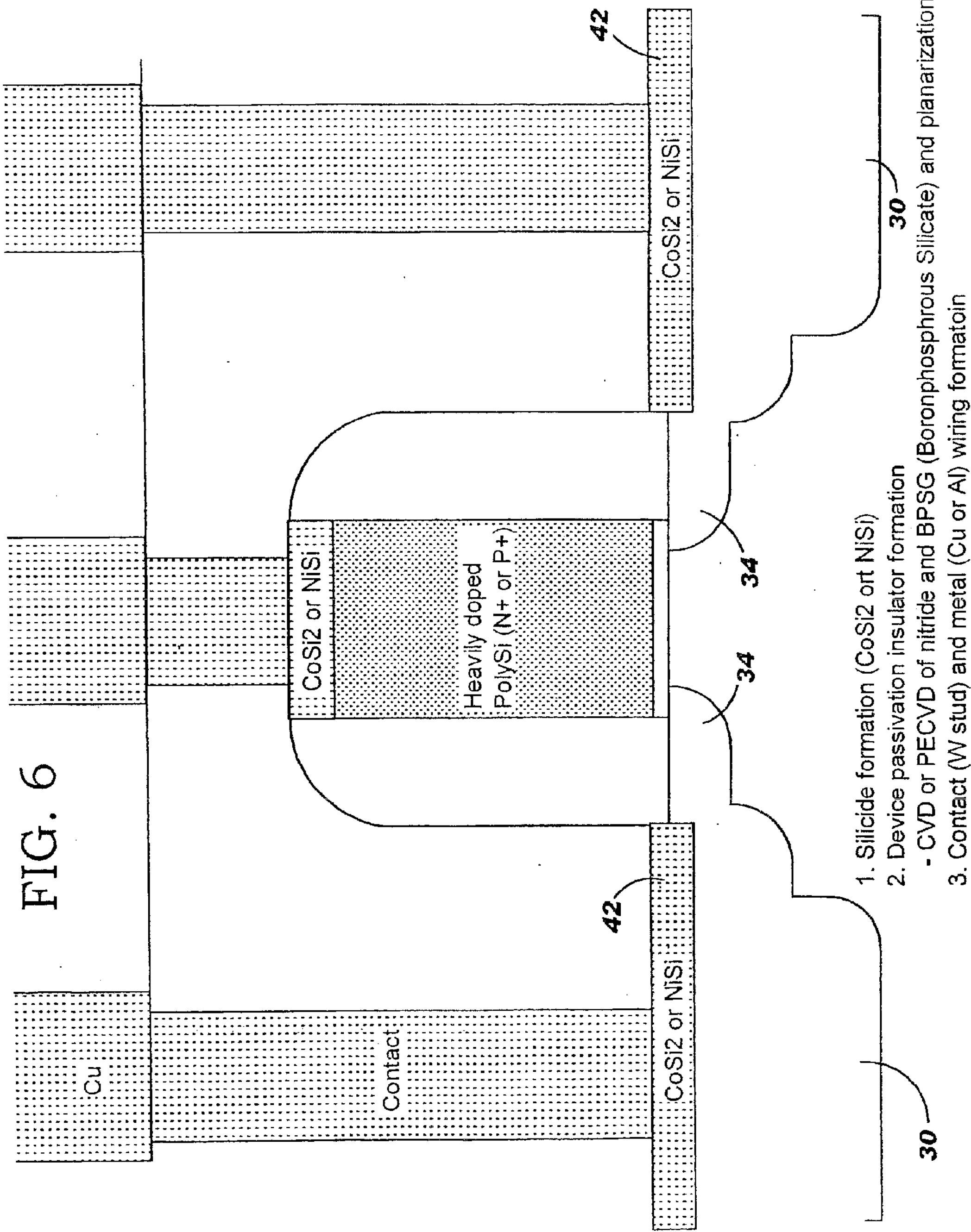


FIG. 6

FORMATION OF A DISPOSABLE SPACER TO POST DOPE A GATE CONDUCTOR

CROSS REFERENCE TO RELATED APPLICATION

[0001] The present application is a divisional application of application Ser. No. 10/752,386, filed Jan. 6, 2004.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention generally relates to semiconductor device manufacturing, and more particularly, the invention relates to a method of fabricating semiconductor devices having a reduced carrier-depletion effect of polysilicon (polySi) gate conductor. Even more specifically, the invention relates to the use of a fat disposable spacer, in such fabrication methods, to facilitate post-doping of the polySi gate conductor without disturbing the optimum source and drain doping profile for a high performance metal oxide semiconductor filed effect transistor (MOSFET).

[0004] 2. Background Art

[0005] With decreasing gate lengths in metal oxide semiconductor field effect transistors (MOSFETs), the effective gate dielectric thicknesses (Tinv) of the order of **2** nm or less are required to improve short-channel behavior and to increase the on-current without increasing the off-current. The contribution of carrier-depletion effect of the polySi gate conductor at the gate dielectric interface, the so called "polySi depletion effect," to the effective gate dielectric thickness becomes significantly large when the Tinv is of the order of 2 nm or less. It has been recognized that it is important to dope the polySi gate heavily, particularly near the gate dielectric interface, to reduce the polySi depletion effect. However, with the conventional manufacturing process, where the gate polySi and S/D diffusion are implanted at the same time, it is not possible to dope the polySi gate in such a way to minimize the polySi depletion effect without compromising the optimum source and drain (S/D) diffusion doping profile, because the polySi and S/D diffusion are doped by the same ion implantations. It is desirable to decouple the PolySi and S/D implantation so that they can be optimized separately.

[0006] One method to decouple the gate and S/D implant is known as "pre-doping" of PolySi. The polySi is implanted prior to PolySi etching to define the gate conductor to boost polySi-doping levels. The disadvantage of this method is that the PFET and NFET areas are doped using different species (e.g., boron and arsenic) which can cause these areas to etch differently during the PolySi etch. This is a serious concern for device length control of both NFET and PFET.

[0007] Another method to decouple the gate that has been used is known as post-doping with "anti-spacer." It is called post-doping because the additional doping to the gate is made after the gate PolySi etching to avoid the problems associated with etching of the dual doped PolySi. With the post-doping method with anti-spacer, a planarizing polymer layer such as an anti-reflective coating material (ARC) is spun onto the wafer after the PolySi has been etched. The ARC fills areas between the PolySi lines, which blocks the implant from going into the Si S/D regions while thin enough ARC is left on top of the PolySi. However, the most serious drawback of this technique is that enough ARC material actually stays on top of the PolySi of either a wide PolySi line or dense multiple PolySi lines, which blocks the implant from going into the PolySi, where it is needed.

SUMMARY OF THE INVENTION

[0008] An object of this invention is to fabricate a semiconductor device having a reduced carrier-depletion effect of a polysilicon (polysi) gate conductor.

[0009] Another object of the invention is to use a fat disposable spacer, in a semiconductor fabrication process, to facilitate post-doping of the polySi gate conductor without disturbing the optimum source and drain doping profile for a high performance metal oxide semiconductor field effect transistor (MOSFET).

[0010] These and other objectives are attained with a method of forming a doped gate structure on a semiconductor device, and a semiconductor structure formed in that method. The method comprises the steps of providing a semiconductor device including a gate dielectric layer, and forming a gate stack on said dielectric layer. This latter step, in turn, includes the steps of forming a first gate layer on the dielectric layer, and forming a second layer on top of the first gate layer. A disposable spacer is formed around the first and second gate layers. The increased stack height by addition of the second layer enables to form a wide disposable spacer. The second layer is removed, and ions are implanted in the first gate layer to supply additional dopant to the polySi gate above the gate dielectric layer. The wide disposable spacer keeps the implant away from the critical regions of S/D diffusion.

[0011] Further benefits and advantages of the invention will become apparent from a consideration of the following detailed description, given with reference to the accompanying drawings, which specify and show preferred embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. **1** shows portions of a semiconductor wafer with a poly Si gate and disposable poly Ge stack.

[0013] FIG. **2** shows a disposable spacer around the poly Si gate and disposable Poly Ge stack.

[0014] FIG. **3** illustrates an ion implantation process applied to the semiconductor wafer.

[0015] FIGS. **4** and **5** illustrate further ion implantation processes applied to the semiconductor wafer.

[0016] FIG. **6** shows the semiconductor wafer after further processing.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] The present invention, which provides a method of fabricating a MOSFET device in which additional doping of the polySi gate without disturbing the critical region of the source/drain regions of the extensions is achieved, will now be described in greater detail by referring to the drawings that accompany the present application. It is noted that in the accompanying drawings, like and/or corresponding elements are referred to by like reference numerals.

[0018] Reference is first made to FIG. **1** which illustrates portions of an initial structure that may be employed in the present invention. Specifically, the initial structure shown in FIG. **1** comprises semiconductor substrate **10**, a layer of gate dielectric **12** formed on a surface of semiconductor substrate **10**, and a patterned gate stack **14** formed on portions of gate dielectric **12**. It should be noted that preferably a multitude of stacks **14** are formed on dielectric **12**, however for the sake of simplicity, only one stack is shown in the drawings.

[0019] The structure shown in FIG. **1** is comprised of conventional materials well know in the art and it is fabricated utilizing processing steps that are also well known in the art. For example, semiconductor substrate **10** comprises any semiconducting material including, but not limited to: Si, Ge, SiGe, GaAs, InAs, InP and all other III/V semiconductor compounds. Semiconductor substrate **10** may also include a layered substrate comprising the same or different semiconducting materials, e.g., Si/Si or Si/SiGe, as well as a silicon-on-insulator (SOI) substrate. The substrate may be of the n- or p-type depending on the desired device to be fabricated.

[0020] Additionally, semiconductor substrate **10** may contain active device regions, wiring regions, isolation regions or other like regions that are typically present in MOSFET-containing devices. For clarity, these regions are not shown in the drawings, but are nevertheless meant to be included within substrate **10**. In one highly preferred embodiment of the present invention, semiconductor substrate **10** is comprised of Si.

[0021] Next, a layer of gate dielectric material **12** such as a silicon oxide, silicon nitride, silicon oxynitride, high k material such as Al_2O_3, HfO_2, ZrO_2, or any combination and multilayers thereof, is then formed on a surface of semiconductor substrate **10** utilizing a conventional process well known in the art. For example, the layer of gate dielectric material may be formed by a thermal growing process such as oxidation, nitridation or oxynitridation or, alternatively, by utilizing a chemical vapor deposition (CVD), plasma-assisted CVD, evaporation or chemical solution deposition.

[0022] The thickness of the layer of the gate dielectric material formed at this point of the present invention is not critical to the present invention, but typically, gate dielectric **12** has a thickness of from about 1 to about 20 nm after deposition, with a thickness of from about one to about three nm being more highly preferred. It is noted that the gate dielectric material employed in the present invention may be a conventional dielectric material such as SiO_2 or Si_3N_4, SiO_xN_y, or alternatively, high-k dielectrics such as oxides of Ta, Zr, Hf, Al or combinations thereof may be employed. In one highly preferred embodiment of the present invention, gate dielectric **12** is comprised of an oxide such as SiO_2, or oxynitride SiO_xN_y, Al_2O_3 (aluminum oxide)or $HfSi_xO_y$ (hafnium silicate).

[0023] After forming gate dielectric **12** on a surface of semiconductor substrate **10**, a plurality of gate stacks **14** are formed atop the layer of gate dielectric. As shown in FIG. **1**, each gate stack is comprised of two layers **20** and **22**, one on top of the other. Preferably, the first layer **20** is comprised of intrinsic polycrystalline or so called poly silicon, and the second layer **22** is comprised of polycrystalline or so called poly germanium. Also, for example, each layer may be about 50 to 150 nm in height. The thicker the polySi layer, the more difficult it is to heavily dope the polySi near the gate dielectric **12** without degrading the S/D diffusion profile, since the higher energy implantation is required to heavily dope the polySi near the gate dielectric. The gate stack **14** is positioned by using conventional lithography and etching steps. The photoresist used is stripped after the etch to form the gate stack structure shown in FIG. **1**.

[0024] The term "gate material" as used herein denotes a conductive material, a material that can be made conductive via a subsequent process such as ion implantation, or any combination thereof. Illustrative examples of suitable gate materials that can be employed in the present invention include, but are not limited to: polysilicon, amorphous silicon or polysilicon germanium.

[0025] The gate material is formed on the surface of gate dielectric **12** utilizing conventional deposition processes well known in the art including, but not limited to: CVD, or plasma-assisted CVD.

[0026] With reference to FIG. **2**, after gate stack **14** is formed, an oxide/nitride line **24** is deposited on the stack and on the semiconductor substrate **10** immediately around the gate stack. After this, an oxide, disposable space **26** is formed around the gate stack **14** by conformally depositing the oxide and directionally etching the oxide by reactive ion etching (RIE). The RIE removes the liner **24** and spacer **26** from the top of the gate stack **14** and the exposed Si substrate area. The disposable layer **22**, of at least the same thickness as, or thicker than, that of polySi layer **20**, was added and the at least 2× fatter space **26** was formed so that the deep polySi doping implantation (discussed below) is kept away from the critical region of S/D diffusion near the extension.

[0027] With reference to FIGS. **2** and **3**, the disposable poly Ge layer **22** is removed from gate stack **14**; and this may be done, for example, by a H_2O_2 or HNO_3 etching process, while the PFET area is covered by a photo resist. After the poly Ge layer is removed, an As or P deep ion implantation process **100** is employed to dope the N+ polySi layer **20**. The implant goes into the substrate **10**, forming extension regions **30**, but it is kept sufficiently away from the active device area by the fat spacer **26**.

[0028] With reference to FIGS. **3** and **4**, after the deep implant **100** to dope the poly Si layer, spacer **26** and the liner **24** may be removed and second n+ and p+ extensions **34** are formed by ion implantation **102** with using blocking photoresist mask (not shown in the figure) and spacers **36**. This second spacer **36** may be formed using any suitable procedure, and, for instance, the spacer may be formed using a CVD oxide deposition and directional etch process.

[0029] With reference to FIG. **5**, after the n+ and p+ extension implantation, n+ and p+ source/drain diffusion regions **30** are doped by ion implantation **104** with the third spacer **40** formed over spacer **36** and with using blocking photoresist mask (not shown in the Figure).

[0030] Further processing steps may then be used to complete the fabrication of the semiconductor device. With reference to FIG. **6**, $CoSi_2$ or NiSi layer **42** may be formed on top of the semiconductor substrate **10** and the top of PolySi gate conductor. Conventional semiconductor fabrication techniques may be used to form silicide layer **42**. Passivation insulator is formed over the device, and then contacts and metal wiring are formed to make working CMOS circuits.

[0031] The process described here is one of the preferred embodiments and the process sequence may be varied to achieve the same results. For example, the S/D extension implantations can be made right after the deposition of the liner layer **24** as a spacer before the formation of the fat disposable spacer **26**. Also, hollow implantations, which are not an essential part of the present invention, may be made at the same process step as the extension ion implantations.

[0032] While it is apparent that the invention herein disclosed is well calculated to fulfill the objects stated above, it will be appreciated that numerous modifications and embodiments may be devised by those skilled in the art, and it is intended that the appended claims cover all such modifications and embodiments as fall within the true spirit and scope of the present invention.

1-12. (canceled)

13. A semiconductor structure, comprising:

a substrate including a gate dielectric layer;

a gate stack on the gate dielectric layer, said gate stack including a first gate layer on the dielectric layer and comprised of a first material, and a second layer on top of the first gate layer and comprised of a second material different than the first material; and

a disposable spacer extending around the gate stack, and extending upward above the substrate to a level higher than the top of the first gate layer.

14. A semiconductor structure according to claim 13, wherein the disposable spacer thickness is equal or thicker than the first gate layer so that at least 2× fatter spacer is formed.

15. A semiconductor structure according to claim 13, wherein the spacer extends upward substantially to the top of the gate stack.

16. A semiconductor structure according to claim 13, further comprising a liner deposited on the gate stack between the gate stack and the spacer.

17. A semiconductor structure according to claim 16, wherein said liner is also deposited on the semiconductor substrate, between said substrate and the spacer.

* * * * *