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(54) **SEMICONDUCTOR PHOTOMULTIPLIER**

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(57) **ABSTRACT**

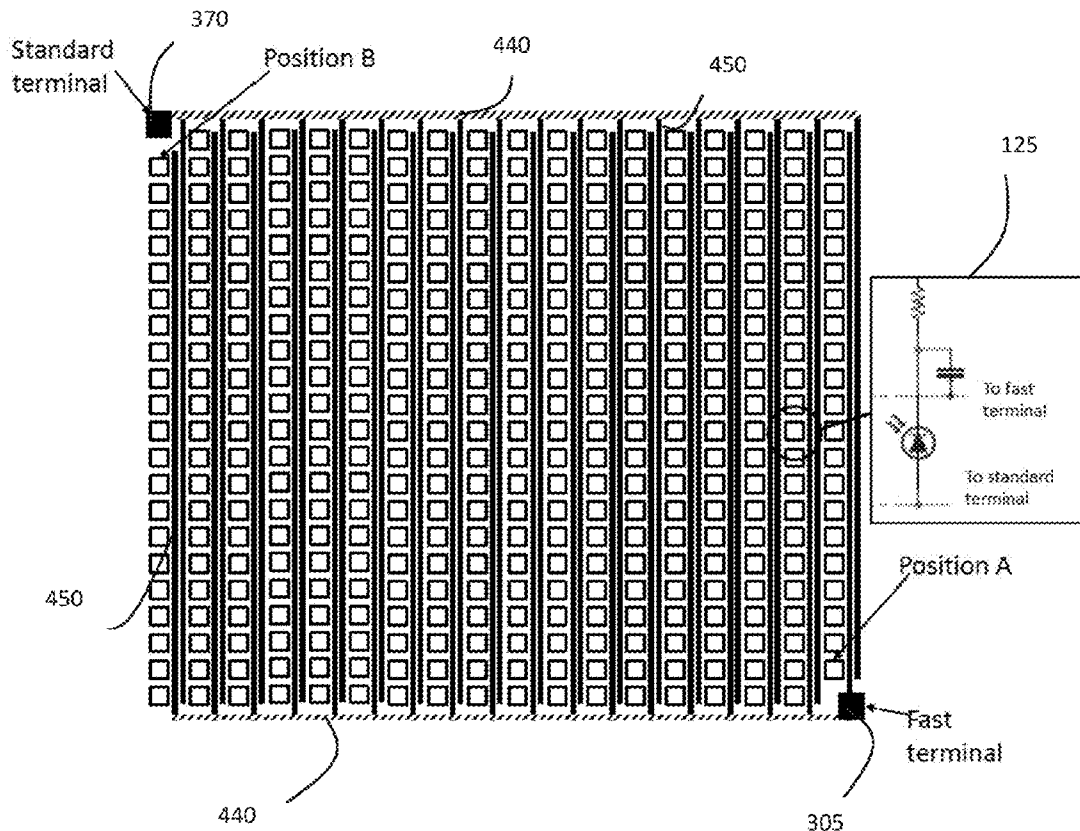The present disclosure relates to a semiconductor photomultiplier comprising a a substrate; an array of photosensitive elements formed on a first major surface of the substrate; a plurality of primary bus lines interconnecting the photosensitive elements; at least one segmented secondary bus line provided on a second major surface of the substrate which is operably coupled to one or more terminals; and multiple vertical interconnect access (via) extending through the substrate operably coulping the primary bus lines to the at least one segmented secondary bus line.

Fig. 1

Fig. 2

Fig. 3

Fig. 4

a   b   c   d

Direction of minor rows

Fig. 5

Fig. 6

Fig. 7

Fig. 8

Fig. 9

Fig. 10

Fig. 11

TSVs positioned along the major row (standard terminal)

TSVs positioned along the major row (fast terminal)
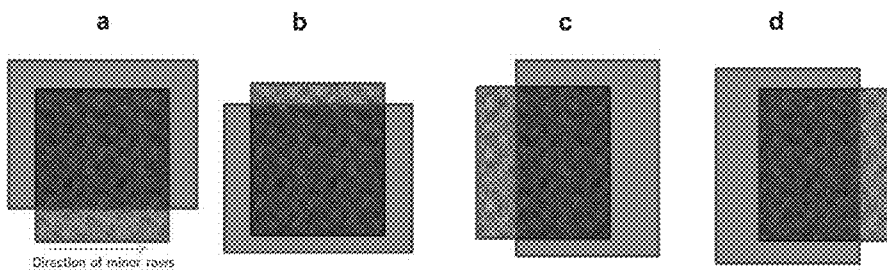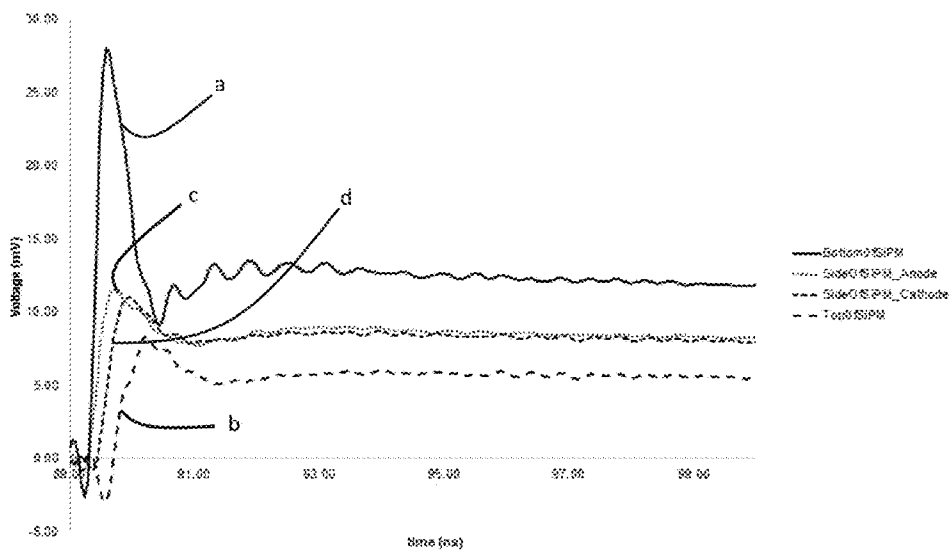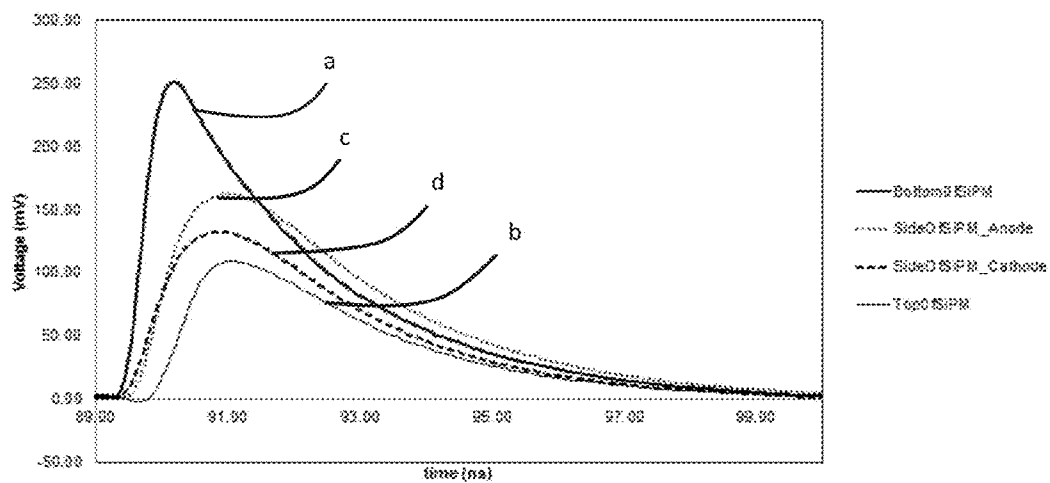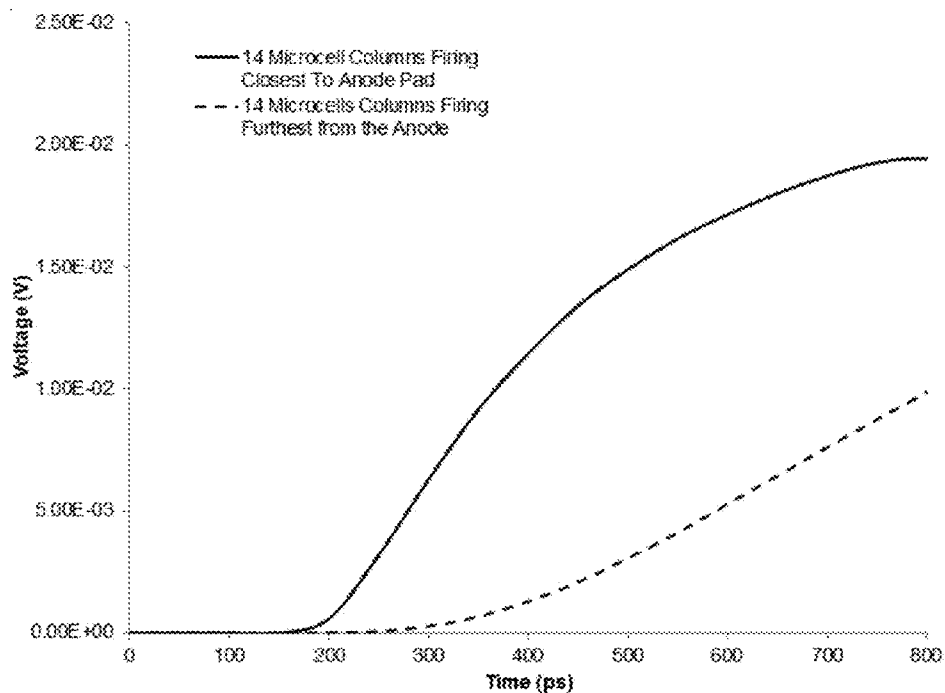
Fig. 12

Fig. 13

Fig. 14

SEMICONDUCTOR PHOTOMULTIPLIER

FIELD OF THE INVENTION

[0001] The present disclosure relates to photon detectors. In particular, the present disclosure relates to high sensitivity photon detectors such as semiconductor photomultipliers. In particular, but not exclusively, the present disclosure relates to semiconductor photomultipliers (SiPMs or SPMs) in such areas as Positron Emission Tomography [PET], including Time-Of-Flight PET [TOF-PET], Laser Ranging [LIDAR] applications, bio luminescence, High Energy Physics [HEP] detectors.

BACKGROUND

[0002] SiPMs are semiconductor photon sensitive devices made up of an array of very small Geiger-mode avalanche photodiode (APD) cells on a substrate such as silicon. APD cells vary in dimension from several micron to 100 microns depending on the mask used, and can have a typical density of up to 3000 microcells/sq. mm. Avalanche diodes can also be made from other semiconductors besides silicon, depending on the properties that are desirable. Silicon detects in the visible and near infrared range, with low multiplication noise (excess noise). Germanium (Ge) detects infrared to 1.7 μm wavelength, but has high multiplication noise. InGaAs (Indium Gallium Arsenide) detects to a maximum wavelength of 1.6 μm, and has less multiplication noise than Ge. InGaAs is generally used for the multiplication region of a heterostructure diode, is compatible with high speed telecommunications using optical fibres, and can reach speeds of greater than Gbit/s. Gallium nitride operates with UV light. HgCdTe (Mercury Cadmium Telluride) operates in the infrared, to a maximum wavelength of about 14 μm, requires cooling to reduce dark currents, and can achieve a very low level of excess noise.

[0003] Silicon avalanche diodes can function with breakdown voltages of 100 to >1000V, typically. APDs exhibit internal current gain effect of about 100-1000 due to impact ionization, or avalanche effect, when a high reverse bias voltage is applied (approximately 100->200 V in silicon, depending on the doping profile in the junction). Silicon Photomultipliers or SiPMs can achieve a gain of 10^5 to 10^6 by using Geiger mode APDs also known as Single Photon Avalanche Diodes (SPADs) which operate with a reverse voltage that is greater than the breakdown voltage, and by maintaining the dark count event rate at a sufficiently low level. The current generated by an avalanche event must be quenched by an appropriate current limited scheme so that the device can recover and reset after an avalanche event. SiPM sensors have lower operating voltages than APDs and have a breakdown voltage from 10-100 Volts.

[0004] Silicon Photomultipliers typically include a matrix of major and minor bus lines. The minor bus lines connect directly to the microcells. The minor bus lines are then joined to bond pads by a major bus line. The minor bus lines are loaded with the inductance, capacitance and resistance of the microcells. The major bus lines are then loaded with the inductance, capacitance and resistance of the minor bus lines. The rise time, delay and recovery time of signal from a microcell on the SiPM will therefore depend strongly on its position in the SiPM. The variation in rise time and delay across the array will give rise to increased jitter and therefore increased coincidence resolving time (CRT) or timing jitter.

[0005] There is therefore a need to provide a semiconductor photomultiplier which addresses at least some of the drawbacks of the prior art.

SUMMARY

[0006] In one aspect, there is provided a semiconductor photomultiplier comprising:
[0007] a substrate;
[0008] an array of photosensitive elements formed on a first major surface of the substrate;
[0009] a plurality of primary bus lines interconnecting the photosensitive elements;
[0010] at least one segmented secondary bus line provided on a second major surface of the substrate which is operably coupled to one or more terminals; and
[0011] multiple vertical interconnect access (vias) extending through the substrate operably coulping the primary bus lines to the at least one segmented secondary bus line.
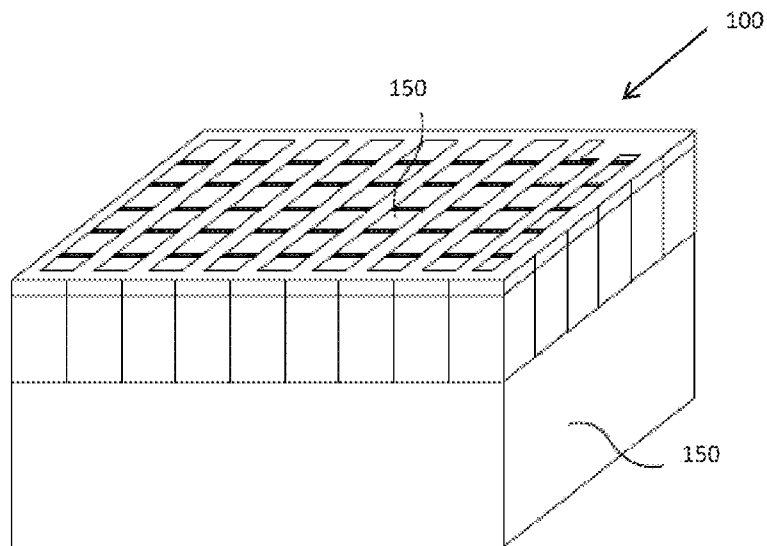
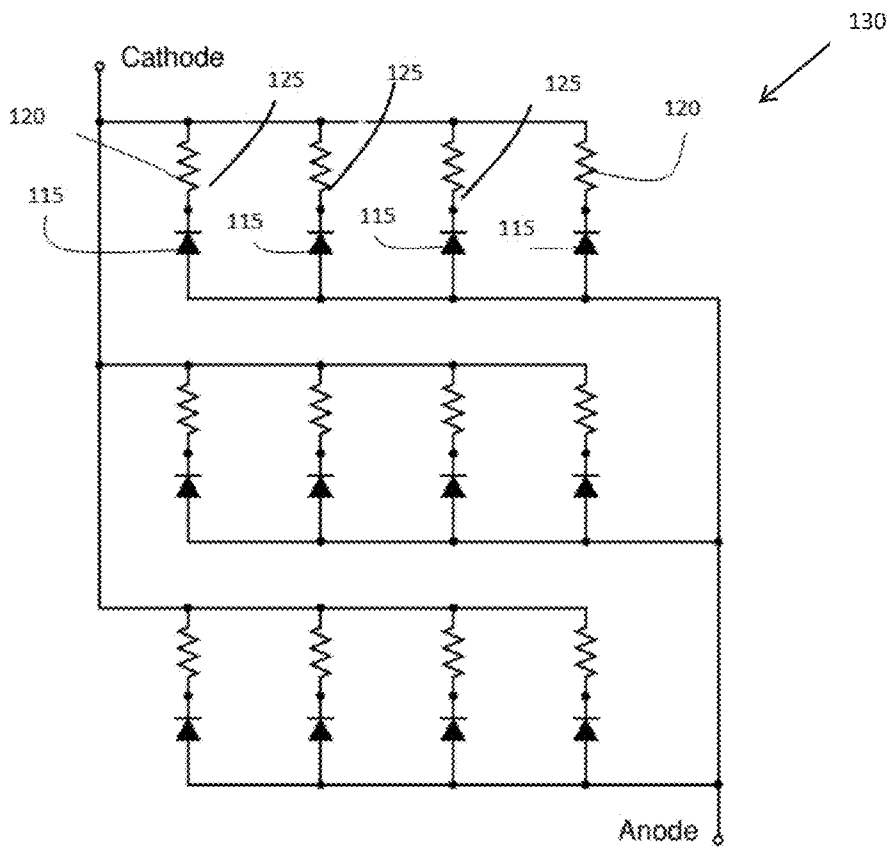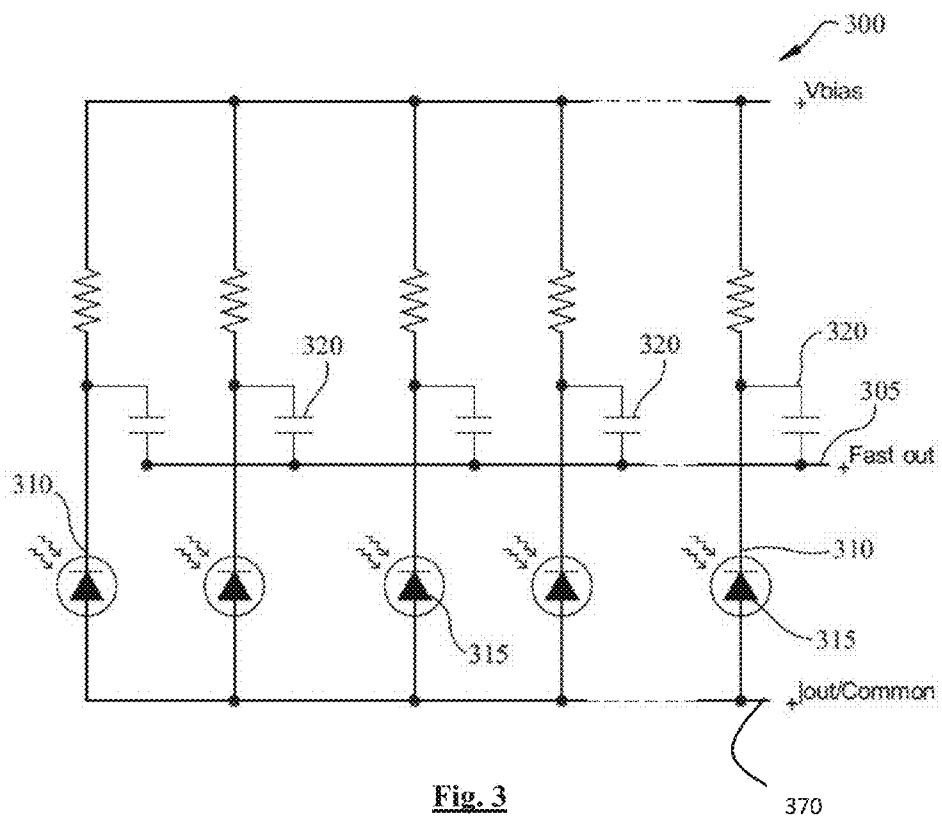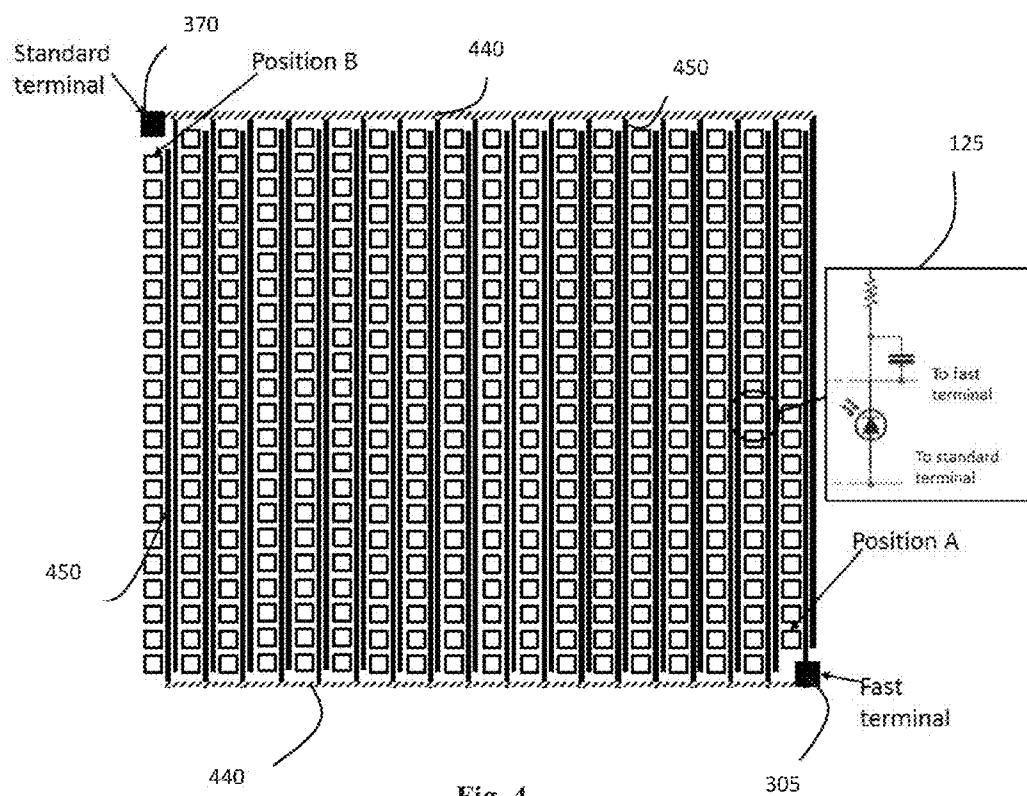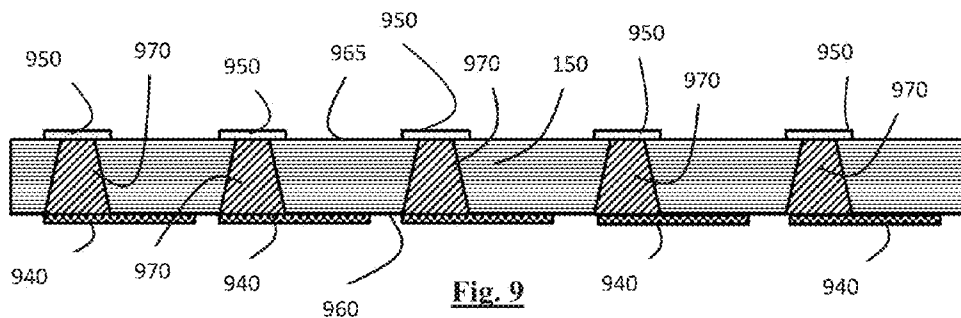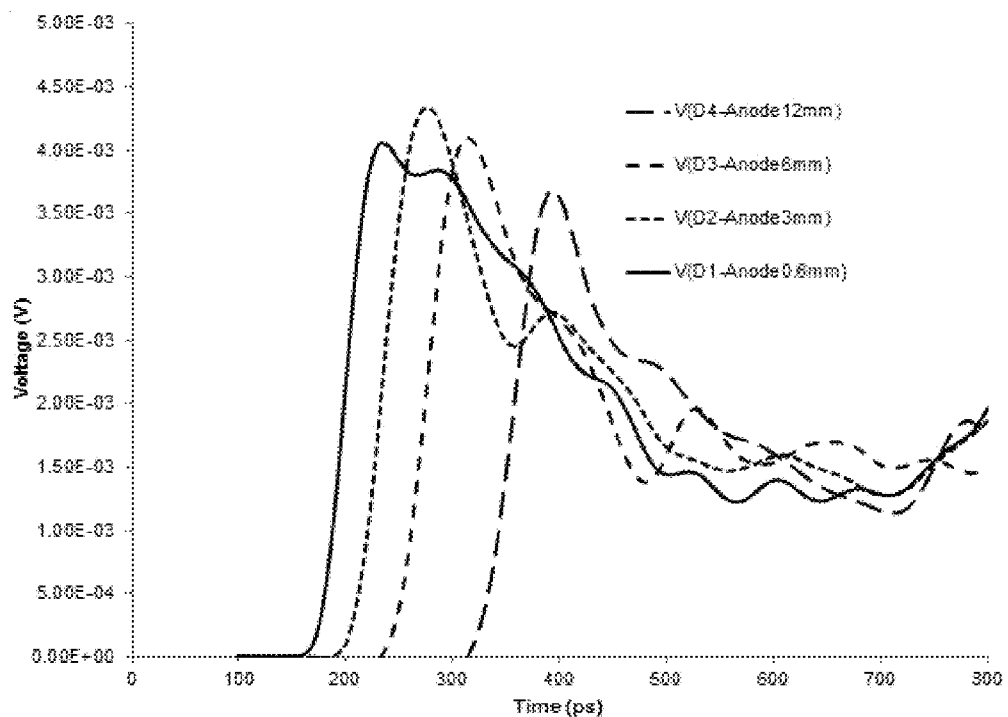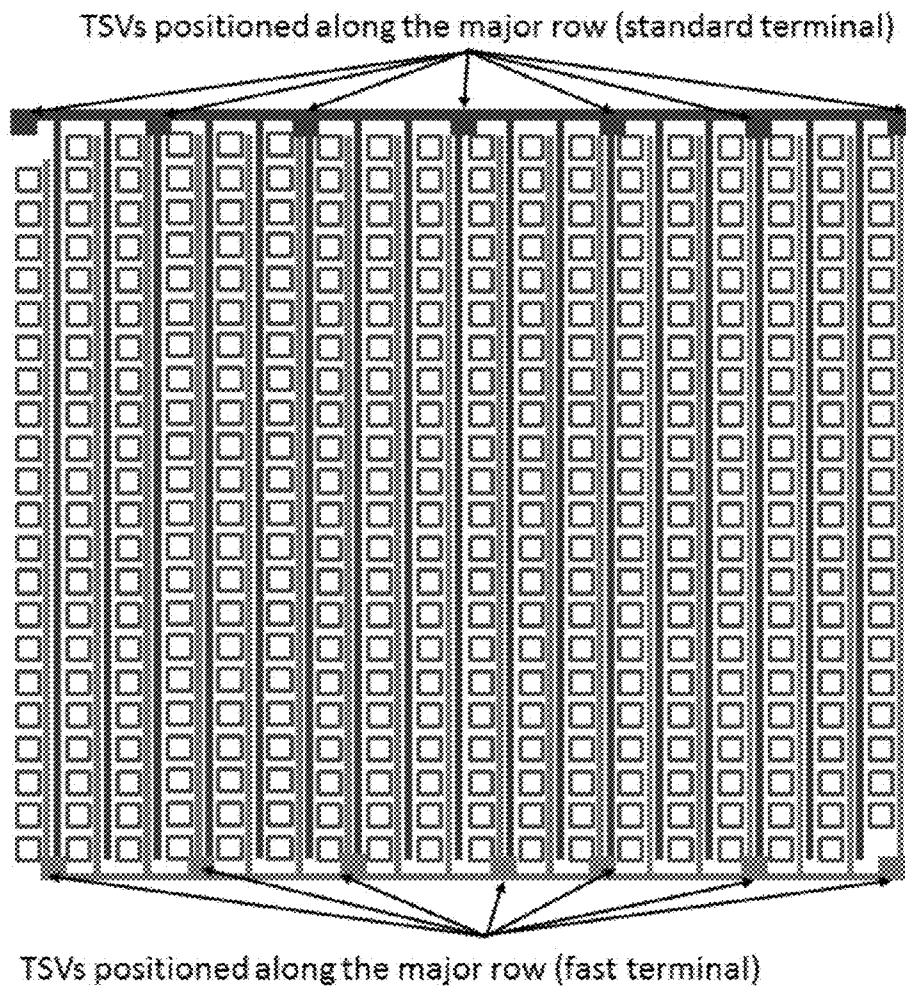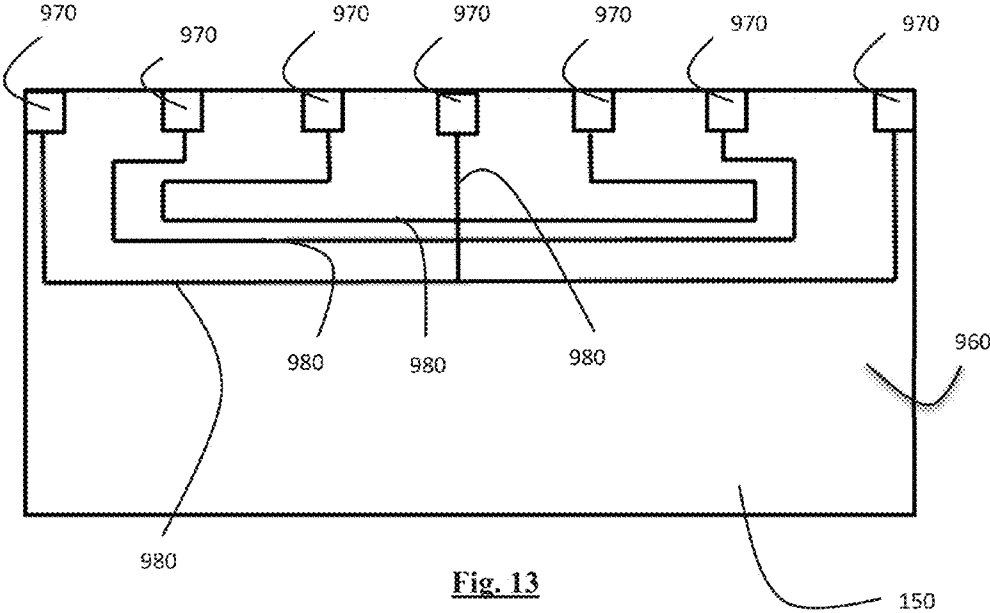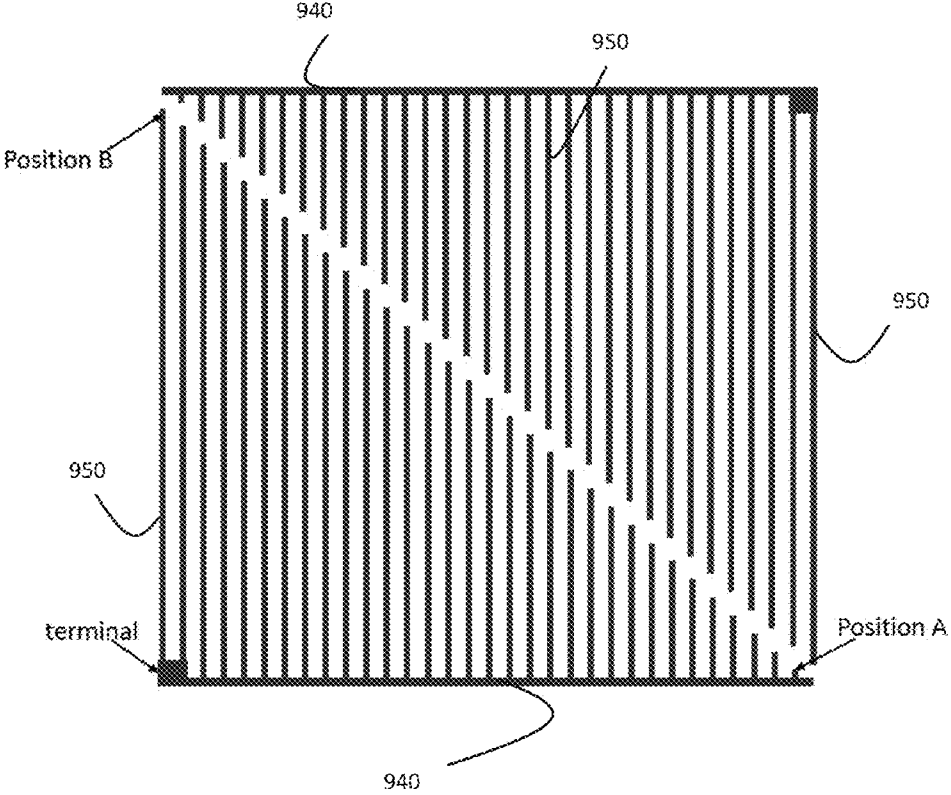[0012] In another aspect, the photosensitive element comprises a single photon avalanche diode (SPAD).

[0013] In a further aspect, a quench element is associated with each SPAD. Advantageously, the quench element is a passive component resistor. Preferably, the quench element is an active component transistor.

[0014] In one aspect, each segment of the segmented secondary bus line has an associated via coupled to a corresponding primary bus line.

[0015] In a further aspect, each photosensitive element is part of a microcell.

[0016] In another aspect, at least some of the segments of the segmented secondary bus line are of equal length in order to equalise the signal delays from the microcells to the one or more terminals.

[0017] In a further aspect, the length of at least some of the primary bus lines are of equal length in order to equalise the signal delays from the microcells to the one or more terminals.

[0018] In one aspect, each microcell comprises a photodiode. Advantageously, each microcell comprises a resistor coupled in series to the photodiode. Preferably, a capacitive element is provided.

[0019] In another aspect, the interconnected photosensitive elements are arranged in a grid configuration.

[0020] In a further aspect, the primary buses lines are parallel to columns in the grid configuration. Advantageously, at least some of the primary bus lines extend between the columns.

[0021] In another aspect, the primary and secondary bus lines are perpendicular to each other. Advantageously, each photosensitive element comprises an avalanche photodiode or a single photon avalanche diode.

[0022] In one aspect, each interconnected photosensitive element comprises a quench resistor coupled in series to the avalanche photodiode or a single photon avalanche diode.

[0023] The present disclosure relates to a substrate comprising:
[0024] an array of photosensitive elements formed on a first major surface of the substrate;
[0025] a plurality of primary bus lines interconnecting the photosensitive elements;
[0026] at least one segmented secondary bus line provided on a second major surface of the substrate which is operably coupled to one or more terminals; and

[0027] multiple vertical interconnect access (vias) extending through the substrate operably coulping the primary bus lines to the at least one segmented secondary bus line.

[0028] The present disclosure also relates to a method of fabricating a semiconductor photomultiplier; the method comprising:

[0029] forming an array of photosensitive elements on a first major surface of a substrate;

[0030] providing a plurality of primary bus lines interconnecting the photosensitive elements;

[0031] providing at least one segmented secondary bus line on a second major surface of the substrate which is operably coupled to one or more terminals; and

[0032] providing multiple vertical interconnect access (vias) extending through the substrate operably coulping the primary bus lines to the at least one segmented secondary bus line.

[0033] These and other problems are addressed by providing a semiconductor photomultiplier having primary and secondary bus lines on respective opposite sides of the substrate interconnected by vertical interconnect access (via).

[0034] These and other features will be better understood with reference to the followings Figures which are provided to assist in an understanding of the present teaching.

BRIEF DESCRIPTION OF THE DRAWINGS

[0035] The present teaching will now be described with reference to the accompanying drawings in which:

[0036] FIG. 1 illustrates an exemplary structure of a silicon photomultiplier.

[0037] FIG. 2 is a schematic circuit diagram of an exemplary silicon photomultiplier.

[0038] FIG. 3 is a schematic circuit diagram of an exemplary silicon photomultiplier.

[0039] FIG. 4 is a top plan view of an exemplary silicon photomultiplier.

[0040] FIG. 5 is a diagrammatic view of four microcells.

[0041] FIG. 6 is a graph showing that signal delay, rise time and overall shape depend on the position of the microcell.

[0042] FIG. 7 is a graph showing that signal delay, rise time and overall shape depend on the position of the microcell.

[0043] FIG. 8 is a graph which shows the signal from the microcells furthest from the major row (furthest from terminal) compared with the signal from those closest to it.

[0044] FIG. 9 shows a cross sectional view of a photomultiplier in accordance with the present teaching.

[0045] FIG. 10 is a plan view of a bottom surface of the photomultiplier of FIG. 9.

[0046] FIG. 11 is a simulated graph of the signals on a segmented bus line on the bottom surface of the photomultiplier of FIG. 9.

[0047] FIG. 12 is a diagrammatic illustration of primary and secondary bus lines of the photomultiplier in accordance with the present teaching.

[0048] FIG. 13 is a plan view of a bottom surface of the photomultiplier in accordance with the present teaching.

[0049] FIG. 14 is a diagrammatic illustration of primary and secondary bus lines of the photomultiplier in accordance with the present teaching.

DETAILED DESCRIPTION OF THE DRAWINGS

[0050] The present disclosure will now be described with reference to some exemplary semiconductor photomultipliers. It will be understood that the exemplary semiconductor photomultipliers are provided to assist in an understanding of the teaching and is not to be construed as limiting in any fashion. Furthermore, circuit elements or components that are described with reference to any one Figure may be interchanged with those of other Figures or other equivalent circuit elements without departing from the spirit of the present teaching. It will be appreciated that for simplicity and clarity of illustration, where considered appropriate, reference numerals may be repeated among the figures to indicate corresponding or analogous elements.

[0051] Referring initially to FIG. 1, a silicon photomultiplier 100 comprising an array of Geiger mode photodiodes is shown. The array is formed on a semiconductor substrate 150 using semiconductor processes which will be known to one skilled in the art and may include for example, but not limited to, deposition, implantation, diffusion, patterning, doping, and etching. Patterned layers of conducting material, insulating material and doped areas of semiconductor form the structure of the photodiode. A quench resistor is provided adjacent to each photodiode which may be used to limit the avalanche current. The photodiodes are electrically connected to common biasing and ground electrodes by aluminium or similar conductive tracking.

[0052] The Silicon Photomultiplier 100 integrates a dense array of small, electrically and optically isolated Geigermode photodiodes 115. Each photodiode 115 is coupled in series to a quench resistor 120. Each photodiode 115 and its associated quench resistor 120 are referred to as a microcell 125. The number of microcells 125 typically number between 100 and 3000 per mm². The signals of all microcells 125 are then summed to form the output of the SiPM 100. A simplified electrical circuit 130 is provided to illustrate the concept in FIG. 2. Each microcell 125 detects photons identically and independently. The sum of the discharge currents from each of these individual binary detectors combines to form a quasi-analog output, and is thus capable of giving information on the magnitude of an incident photon flux.

[0053] Each microcell 125 generates a highly uniform and quantized amount of charge every time the microcell 125 undergoes a Geiger breakdown. The gain of a microcell 125 (and hence the detector) is defined as the ratio of the output charge to the charge on an electron. The output charge can be calculated from the over-voltage and the microcell capacitance.

$$G = \frac{C \cdot \Delta V}{q}$$

Where:

[0054] G is the gain of the microcell;

[0055] C is the capacitance of the microcell;

[0056] ΔV is the over-voltage; and

[0057] q is the charge of an electron.

[0058] Referring now to FIG. 3 which illustrates a silicon photomultiplier 300 described in PCT Patent Application no. WO 2011/117309 of which the present assignee is the applicant, the contents are incorporated herein by reference. The

SPM 300 has a third electrode 305 which is capacitively coupled to each photodiode cathode 310 in order to provide a fast readout of the avalanche signals from the photodiodes 315. When the photodiode 315 emits a current pulse, part of the resulting change in voltage at the cathode 310 will be coupled via mutual capacitance 320 into the third (fast) electrode 305. Using the third electrode 305 for readout avoids the compromised transient performance resulting from the relatively large RC time constant associated with the biasing circuit.

[0059] It will be appreciated by thoses skilled in the art that silicon photomultipliers comprise major bus lines 440 and minor bus lines 450 as illustrated in FIG. 4. In silicon photomultipliers know heretofore the minor bus lines 450 connect directly to the microcells 125. The minor bus lines 450 are then coupled to major bus line 440 which connect to the bond pads associated with the terminals 370 and 305. Typically, the minor bus lines 450 extend vertically between the columns of microcells 125; while the major bus lines 440 extend horizontally adjacent the outer row of the microcells 125. The minor bus lines 450 are loaded with the inductance, capacitance and resistance of the microcells 125. The major bus lines 440 are then loaded with the inductance, capacitance and resistance of the minor bus lines 450. The rise time, delay and recovery time of signal from a microcell 125 on the SiPM will therefore depend significantly on its position in the SiPM. The variation in rise time and delay across the array will give rise to increased jitter and therefore increased coincidence resolving time (CRT). It will be appreciated by those skilled in the art that a microcell 125 firing at position A will have a very different signal path to microcell 125 firing at position B. The rise time and delay of the signal will be different as the signal path is not uniform. The range of these parameters impacts coincidence resolving time (CRT) significantly.

[0060] Referring now to FIGS. 5 and 6, which shows experimental data to quantify the range of delays and rise times seen across a SiPM. Pulses coming from different areas of the SiPM were compared by partially (85%) blacking out areas as indicated by labels a, b, c, and d in FIG. 5.

[0061] a) The minor rows closest to the anode were exposed. The signal path along the major row is short.

[0062] b) The minor rows at the end of the major rows were exposed. This is the opposite of (a). The signal path along the major row will be long.

[0063] c) The microcells on the minor bus closest to the major bus are exposed. The signal path along the minor rows will be short.

[0064] d) The micro cells on the minor bus furthest from the major row are exposed. The signal path along the minor rows will be long.

[0065] It is clear from the graphs in FIGS. 6 and 7 that the standard terminal 370 and fast output terminal 305 signal delay, rise time and overall shape depend strongly on position on the major row. FIG. 6 illustrates the signals measured at the standard terminal 370, while FIG. 7 illustrates the signals measured at the fast terminal 305. The delay from difference between 'a' and 'b' is approximately 400 ps. The graph of FIG. 8 shows the signal from fourteen microcells furthest from the major row (anode terminal) compared with the signal from fourtheen microcells closest to major row (anode terminal). It is clear that there is significant time delay between the two signals. It is desirable to segment the major bus line in order to reduce the load on the signal. If the

segments were joined together on top of the substrate 150, the area taken up by the additional bus lines would be subtracted from the optically active area, significantly reducing the photo-detection efficiency (PDE).

[0066] Referring now to FIGS. 9 and 10 which illustrates an exemplary layout of minor bus lines 950 and major bus lines 940 in accordance with the present teaching. The minor bus lines 950 extend vertically between the columns of microcells 125 similar as previously described with reference to FIG. 4. The major bus lines 940 are provided on a lower surface 960 of the subtrate 150 and are operably coupled to the minor bus lines 950 via true silicon vias (TSVs) 970. The minor bus lines 950 interconnect the microcells 125 which are formed on an upper surface 965 of the substrate 150. The TSVs 970 are vertical connections which pass completely through the subtrate 150. The number of major bus lines 940 which may be used is significantly increased compared to the arrangement of FIG. 4 because the area for accommodating the major bus lines 940 is not limited to the periphery of the upper major surface of the substrate 150. The full area of the bottom surface 960 of the substrate 150 is available to accommodate the major bus lines 940. The major bus line 940 is segmented into multiple segments 980 as illustrated in FIG. 10. In the exemplary, six segments 980 extend horizontally on the bottom surface 960 of the substrate 150. It is will be appreciated by thoses skilled in the art that the major bus line 940 may be segmented into any desirable number of segments 980. Routing the major bus lines 940 under the silicon substrate 150 minimises the impact on the optically active area of the SiPM. It will be clear to those skilled in the art that CRT is strongly dependant on the range of delay seen across the array of microcells in the SiPM. Reducing the range of delay by segmenting the major bus lines 940 will reduce CRT.

[0067] Referring now to the graph of FIG. 11 which is a simulated graph of the SiPM of FIG. 10 showing the signal delay, rise time and overall shape of the signal of four different segments connected to different major bus lengths (980). The signal delay between the fastest and slowest signal is approximately 150 ps. Thus making the major bus lengths equal under the silicon will reduce the delay range further, thereby reducing CRT. Such a scheme is illustrated in FIG. 13.

[0068] Referring now to FIG. 12 which shows TSVs positioned along the major row associated with the standard terminal 370 and TSVs positioned along the major row associated with the fast terminal 305. Using TSVs allows the arrays of microcells 125 on top surface 965 of the substrate 150 to be segmented so that the major rows are shorted. The major and minor rows may be connected to the under side of the substrate at various positions in the area of the die and shorted via copper tracks. This will effectively reduce the load on each segment of microcells 125. The reduced load will lead to a reduced range of delays (jitter and CRT). Further reductions in jitter can be achieved by using minor rows of various lengths so that the minor row load seen by a microcell furthest from the terminal is smallest and that seen by a microcell closes to the terminal is largest.

[0069] Referring now to FIG. 13 there illustrated a segmented major bus line on the bottom surface 960 of the substrate 150. The major bus line is similar to the arrangement described in FIG. 10 with the exception that track length is increased in order to equalise the signal delays from the

microcells **125** to the terminals. This is possible because due to the extra space under the substrate **150** to route the metal lines.

[0070] Referring now to FIG. **14** there is illustrated an exemplary arrangement of the minor bus lines where the signal paths from the microcells to the terminals are equalised. For example, the signal path from position A to the terminal is approximately equal to signal path from position B. Such a scheme can be incorporated with the arrangement illustrated in FIGS. **9, 10, 12, 13** in order to further reduce the delay range.

[0071] It will be appreciated by those of ordinary skill in the art that the silicon photomultiplier of the present teaching may be fabricated on the substrate **150** using conventional semiconductor processing techniques and may include for example, but not limited to, deposition, implantation, diffusion, patterning, doping, and etching. Patterned layers of conducting material, insulating material and doped areas of semiconductor form the structure of the microcells.

[0072] It will be appreciated by the person of skill in the art that various modifications may be made to the above described embodiments without departing from the scope of the present invention. In this way it will be understood that the teaching is to be limited only insofar as is deemed necessary in the light of the appended claims. The term semiconductor photomultiplier is intended to cover any solid state photomultiplier device such as Silicon Photomultiplier [SiPM], MicroPixel Photon Counters [MPPC], MicroPixel Avalanche Photodiodes [MAPD] but not limited to.

[0073] Similarly the words comprises/comprising when used in the specification are used to specify the presence of stated features, integers, steps or components but do not preclude the presence or addition of one or more additional features, integers, steps, components or groups thereof.

I claim:

1. A semiconductor photomultiplier comprising:
a substrate;
an array of photosensitive elements formed on a first major surface of the substrate;
a plurality of primary bus lines interconnecting the photosensitive elements;
at least one segmented secondary bus line provided on a second major surface of the substrate which is operably coupled to one or more terminals; and
multiple vertical interconnect access (vias) extending through the substrate operably coulping the primary bus lines to the at least one segmented secondary bus line.

2. A semiconductor photomultiplier as claimed in claim **1**, wherein the photosensitive element comprises a single photon avalanche diode (SPAD).

3. A semiconductor photomultiplier as claimed in claim **2**, wherein a quench element is associated with each SPAD.

4. A semiconductor photomultiplier as claimed in claim **3**, wherein the quench element is a passive component resistor.

5. A semiconductor photomultiplier as claimed in claim **3**, wherein the quench element is an active component transistor.

6. A semiconductor photomultiplier as claimed in claim **1**, wherein each segment of the segmented secondary bus line has an associated via coupled to a corresponding primary bus line.

7. A semiconductor photomultiplier as claimed in claim **1**, wherein each photosensitive element is part of a microcell.

8. A semiconductor photomultiplier as claimed in claim **7**, wherein at least some of the segments of the segmented secondary bus line are of equal length in order to equalise the signal delays from the microcells to the one or more terminals.

9. A semiconductor photomultiplier as claimed in claim **7**, wherein the length of at least some of the primary bus lines are of equal length in order to equalise the signal delays from the microcells to the one or more terminals.

10. A semiconductor photomultiplier as claimed in claim **7**, wherein each microcell comprises a photodiode.

11. A semiconductor photomultiplier as claimed in claim **10**, wherein each microcell comprises a resistor coupled in series to the photodiode.

12. A semiconductor photomultiplier as claimed in claim **11**, further comprising a capacitive element.

13. A semiconductor photomultiplier as claimed in claim **1**, wherein the interconnected photosensitive elements are arranged in a grid configuration.

14. A semiconductor photomultiplier as claimed in claim **13**, wherein the primary buses lines are parallel to columns in the grid configuration.

15. A semiconductor photomultiplier as claimed in claim **14**, wherein at least some of the primary bus lines extend between the columns.

16. A semiconductor photomultiplier as claimed claim **1**, wherein the primary and secondary bus lines are perpendicular to each other.

17. A semiconductor photomultiplier as claimed in claim **1**, wherein each photosensitive element comprises an avalanche photodiode or a single photon avalanche diode.

18. A semiconductor photomultiplier as claimed in claim **13**, wherein each interconnected photosensitive element comprises a quench resistor coupled in series to the avalanche photodiode or a single photon avalanche diode.

19. A substrate comprising:
an array of photosensitive elements formed on a first major surface of the substrate;
a plurality of primary bus lines interconnecting the photosensitive elements;
at least one segmented secondary bus line provided on a second major surface of the substrate which is operably coupled to one or more terminals; and
multiple vertical interconnect access (vias) extending through the substrate operably coulping the primary bus lines to the at least one segmented secondary bus line.

20. A method of fabricating a semiconductor photomultiplier; the method comprising:
forming an array of photosensitive elements on a first major surface of a substrate;
providing a plurality of primary bus lines interconnecting the photosensitive elements;
providing at least one segmented secondary bus line on a second major surface of the substrate which is operably coupled to one or more terminals; and
providing multiple vertical interconnect access (vias) extending through the substrate operably coulping the primary bus lines to the at least one segmented secondary bus line.

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