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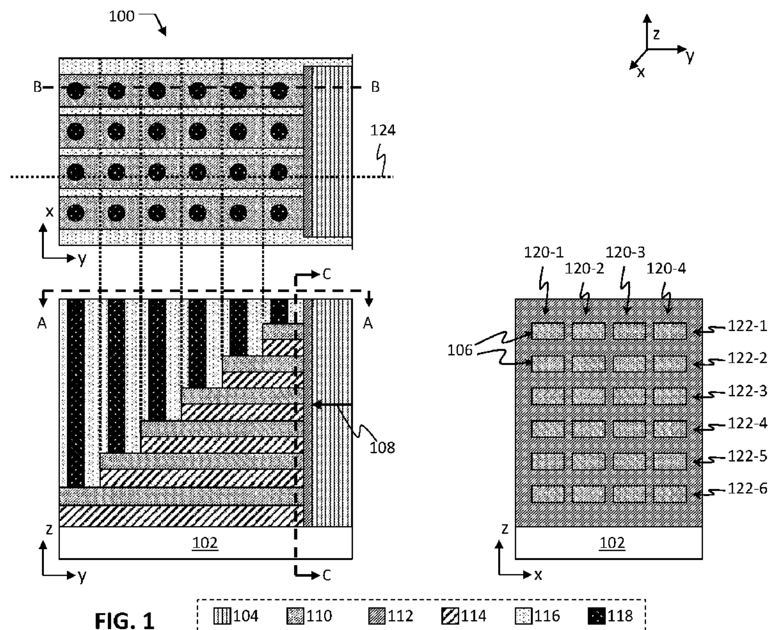
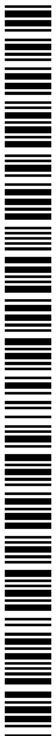


FIG. 1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(57) Abstract: Quantum dot devices, and related systems and methods, are disclosed herein. An exemplary quantum dot device may include a substrate housing a quantum well stack having a plurality of layers, and a plurality of gate stacks adjacent to different portions of a first layer of the quantum well stack. The quantum well layers are stacked in a direction parallel to the substrate so that each of the layers is substantially perpendicular to the substrate, i.e. the layers are vertical. Consequently, quantum dots which form in the quantum well stack during operation of the device may be seen as arranged in a vertical array. Quantum dot devices disclosed herein provide strong spatial localization of the quantum dots, good scalability in the number of quantum dots included in the device, and/or design flexibility in making electrical connections to the quantum dot devices.

[Continued on next page]

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QUANTUM DOT DEVICES WITH VERTICAL QUANTUM DOT ARRAYS

Technical field

[0001] This disclosure relates generally to the field of quantum computing, and more specifically, to quantum dot devices for use in quantum circuits.

Background

[0002] Quantum computing refers to the field of research related to computation systems that use quantum-mechanical phenomena to manipulate data. These quantum-mechanical phenomena, such as superposition (in which a quantum variable can simultaneously exist in multiple different states) and entanglement (in which multiple quantum variables have related states irrespective of the distance between them in space or time), do not have analogs in the world of classical computing, and thus cannot be implemented with classical computing devices.

[0003] Quantum computers use so-called quantum bits, referred to as qubits (both terms “bits” and “qubits” often interchangeably refer to the values that they hold as well as to the actual devices that store the values). Similar to a bit of a classical computer, at any given time, a qubit can be either 0 or 1. However, in contrast to a bit of a classical computer, a qubit can also be 0 and 1 at the same time, which is a result of superposition of quantum states – a uniquely quantum-mechanical phenomenon. Entanglement also contributes to the unique nature of qubits in that input data to a quantum processor can be spread out among entangled qubits, allowing manipulation of that data to be spread out as well: providing input data to one qubit results in that data being shared to other qubits with which the first qubit is entangled.

[0004] Compared to well-established and thoroughly researched classical computers, quantum computing is still in its infancy, with the highest number of qubits in a solid-state quantum processor currently being below 100. One of the main challenges resides in protecting qubits from decoherence so that they can stay in their information-holding states long enough to perform the necessary calculations and read out the results.

Brief Description of the Drawings

[0005] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0006] FIG. 1 provides various views of a single-sided quantum dot device, in accordance with some embodiments of the present disclosure.

[0007] FIGS. 2A-2B illustrate various exemplary biasing schemes for a quantum dot device in accordance with various embodiments of the present disclosure.

[0008] FIG. 3 provides various views of a double-sided quantum dot device, in accordance with some embodiments of the present disclosure.

[0009] FIGS. 4A-4E illustrate various embodiments of a quantum well stack that may be included in a quantum dot device, in accordance with various embodiments.

[0010] FIGS. 5A-5B provide a flow chart of a method for fabricating quantum dot devices as described herein, according to some embodiments of the present disclosure.

[0011] FIGS. 6A-6K are cross-sections illustrating various exemplary stages in the manufacture of a quantum dot device using the method of FIGS. 5A-5B, in accordance with some embodiments of the present disclosure.

[0012] FIGS. 7A and 7B are top views of a wafer and dies that may include any of the quantum dot devices disclosed herein.

[0013] FIG. 8 is a cross-sectional side view of a device assembly that may include any of the quantum dot devices disclosed herein.

[0014] FIG. 9 is a block diagram of an example quantum computing device that may include any of the quantum dot devices disclosed herein, in accordance with various embodiments.

Detailed Description

Overview

[0015] As briefly described above, quantum computing, or quantum information processing, refers to the field of research related to computation systems that use quantum-mechanical phenomena to manipulate data. One example of quantum-mechanical phenomena is the principle of quantum superposition, which asserts that any two or more quantum states can be added together, i.e. superposed, to produce another valid quantum state, and that any quantum state can be represented as a sum of two or more other distinct states. Quantum entanglement is another example of quantum-mechanical phenomena. Entanglement refers to groups of particles being generated or interacting in such a way that the state of one particle becomes intertwined with that of the others. Furthermore, the quantum state of each particle cannot be described independently. Instead, the quantum state is given for the group of entangled particles as a whole. Yet another example of quantum-mechanical phenomena is sometimes described as a “collapse” because it asserts that when we observe (measure) particles, we unavoidably change their properties in that, once observed, the particles cease to be in a state of superposition or entanglement (i.e. by trying to ascertain anything about the particles, we collapse their state).

[0016] Put simply, superposition postulates that a given particle can be simultaneously in two states, entanglement postulates that two particles can be related in that they are able to instantly coordinate their states irrespective of the distance between them in space and time, and collapse

postulates that when one observes a particle, one unavoidably changes the state of the particle and its' entanglement with other particles. These unique phenomena make manipulation of data in quantum computers significantly different from that of classical computers (i.e. computers that use phenomena of classical physics). Therefore, both the industry and the academics continue to focus on a search for new and improved physical systems whose functionality could approach that expected of theoretically designed qubits.

[0017] Physical systems for implementing qubits that have been explored until now include e.g. quantum dot qubits, superconducting qubits, single trapped ion qubits, photon polarization qubits, etc. Out of the various physical implementations of qubits, quantum dot qubit devices are promising candidates for building a quantum computer.

[0018] Embodiments of the present disclosure provide improved layout designs for quantum dot devices employing quantum dot qubits. To that end, various quantum dot devices, and related systems and methods, are disclosed herein. The quantum dot devices disclosed herein may enable the formation of quantum dots to serve as quantum bits ("qubits") in a quantum computing device, as well as the control of these quantum dots to perform quantum logic operations. In some embodiments, a quantum dot device may include a substrate, a quantum well stack provided over the substrate, and at least one gate stack, but preferably a plurality of gate stacks. The quantum well stack may include a plurality of planar layers, wherein planes of the quantum well layers are substantially perpendicular to the substrate (i.e., if the substrate is considered to be horizontal, then the quantum well layers are vertical). In other words, the layers of the quantum well stack are stacked in a direction substantially parallel to the substrate, or, phrased differently, a normal to the planes of the layers of the quantum well stack is substantially parallel to the substrate. The at least one gate stack is adjacent to a portion of first layer of the quantum well layers. When multiple gate stacks are employed, such gate stacks are adjacent to different portions of the first layer of the quantum well layers, where some of the different portions could be at different distances from the substrate. Since the planes of the layers of the quantum well stack are substantially perpendicular to the substrate, when a plurality of gate stacks are used to form gates over different portions of the first layer of the quantum well stack, quantum dots which will form during operation of the quantum dot device will be in a plane perpendicular to the substrate, i.e. the array of the resulting quantum dots will be vertical (i.e. the plane of the array of such quantum dots will be perpendicular to the plane of the substrate). This is in sharp contrast to conventional quantum dot arrays which are all horizontal (i.e. conventionally, the plane of the array of quantum dots is parallel to the plane of the substrate).

[0019] Unlike previous approaches to quantum dot formation and manipulation, various embodiments of the quantum dot devices disclosed herein may provide strong spatial localization of the quantum dots (and therefore good control over quantum dot interactions and manipulation), good scalability in the number of quantum dots included in the device, and/or design flexibility in making electrical connections to the quantum dot devices to integrate the quantum dot devices in larger computing devices.

[0020] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense. For ease of discussion, all of the lettered sub-figures associated with a particular numbered figure may be referred to by the number of that figure; for example, FIGS. 4A-4E may be referred to as "FIG. 3," etc.

[0021] In the drawings, some schematic illustrations of exemplary structures of various devices and assemblies described herein may be shown with precise right angles and straight lines, but it is to be understood that such schematic illustrations may not reflect real-life process limitations which may cause the features to not look so “ideal” when any of the structures described herein are examined using e.g. scanning electron microscopy (SEM) images or transmission electron microscope (TEM) images. In such images of real structures, possible processing defects could also be visible, such as e.g. not-perfectly straight edges of materials, tapered vias or other openings, inadvertent rounding of corners or variations in thicknesses of different material layers, occasional screw, edge, or combination dislocations within the crystalline region, and/or occasional dislocation defects of single atoms or clusters of atoms. There may be other defects not listed here but that are common within the field of device fabrication. Furthermore, the accompanying drawings are not necessarily drawn to scale.

[0022] Various operations may be described as multiple discrete actions or operations in turn in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0023] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and

B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges. As used herein, the notation "A/B/C" means (A), (B), and/or (C).

[0024] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. The accompanying drawings are not necessarily drawn to scale. Unless otherwise specified, the use of the ordinal adjectives “first,” “second,” and “third,” etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0025] The terms “over,” “under,” “between,” and “on” as used herein refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer “on” a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening layers.

[0026] While the disclosure may use the singular term "layer," the term "layer" should be understood to refer to assemblies that may include multiple different material layers.

[0027] In the following detailed description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. For example, the terms “oxide,” “carbide,” “nitride,” etc. refer to compounds containing, respectively, oxygen, carbon, nitrogen, etc. The terms “substantially,” “close,” “approximately,” “near,” and “about,” generally refer to being within +/- 20% of a target value based on the context of a particular value as described herein or as known in the art. Similarly, terms indicating orientation of various elements, such as e.g. “coplanar,” “perpendicular,” “orthogonal,” “parallel,” or any other angle between the elements, generally refer to being within +/- 5-10% of a target value based on the context of a particular value as described herein or as known in the art. Furthermore, as used herein, terms indicating what may be considered an idealized behavior, such as e.g. “superconducting” or “lossless”, are intended to cover functionality

that may not be exactly ideal but is within acceptable margins for a given application. For example, a certain level of loss, either in terms of non-zero electrical resistance or non-zero amount of spurious two-level systems may be acceptable such that the resulting materials and structures may still be referred to by these "idealized" terms. Specific values associated with an acceptable level of loss are expected to change over time as fabrication precision will improve and as fault-tolerant schemes may become more tolerant of higher losses, all of which are within the scope of the present disclosure.

[0028] Still further, while the present disclosure may include references to microwave signals, this is done only because current qubits are designed to work with such signals because the energy in the microwave range is higher than thermal excitations at the temperature at which the qubits are typically operated. In addition, techniques for the control and measurement of microwaves are well known. For these reasons, typical frequencies of qubits are in 1-10 GHz, e.g. in 3-8 GHz, range, in order to be higher than thermal excitations, but low enough for ease of microwave engineering. However, advantageously, because excitation energy of qubits is controlled by the circuit elements, qubits can be designed to have any frequency. Therefore, in general, qubits could be designed to operate with signals in other ranges of electromagnetic spectrum and embodiments of the present disclosure could be modified accordingly. All of these alternative implementations are within the scope of the present disclosure.

Quantum dot devices with vertical quantum well layers

[0029] FIG. 1 provides various views of a quantum dot device 100 with quantum well layers perpendicular to the substrate (i.e. vertical), in accordance with some embodiments of the present disclosure.

[0030] In particular, FIG. 1 illustrates a top down view (the view shown in the upper left portion of FIG. 1) of the y-x plane of the coordinate system illustrated in some of the present FIGS., a first cross-sectional view (the view shown in the lower left portion of FIG. 1) along the y-z plane, and a second cross-sectional view (the view shown in the lower right portion of FIG. 1) along the x-z plane. For example, the top down view shown in FIG. 1 may be the view looking down from a plane indicted in FIG. 1 as a plane AA, the first cross-sectional view may be a cross-section along a plane indicted in FIG. 1 as a plane BB, and the second cross-sectional view may be a cross-section along a plane indicted in FIG. 1 as a plane CC (each of the planes AA, BB, and CC is shown in FIG. 1 with a dashed line intended to illustrate a plane perpendicular to the page of the drawing and containing said dashed line). The top down view of a portion of the quantum dot device 100 is shown in FIG. 1 with some of the materials removed so that gate contact metal 118 to quantum dot (QD) gates and barrier gates, described below, are visible. Similarly, the second cross-sectional view of the quantum

dot device 100 is shown in FIG. 1 with the interlayer dielectric (ILD) 116 removed so that the gate dielectric 110 is visible below the gate metal portions 108 of each of the gate stacks 106. A legend provided within a dashed box at the bottom of FIG. 1 illustrates patterns used to indicate some of the elements shown in FIG. 1, so that FIG. 1 is not cluttered by too many reference numerals. These considerations are also applicable to FIGS. 2A-2B, FIG. 3, and FIGS. 6A-6K, showing views similar to those shown in FIG. 1, and using a similar/same notation. In all of the present FIGS., same reference numerals refer to the same or analogous elements/materials shown.

[0031] As shown in FIG. 1, the quantum dot device 100 may include a substrate 102, a quantum well stack 104 provided over the substrate 102, and a plurality of gate stacks 106 provided in contact with the quantum well stack 104.

[0032] The substrate 102 may be any substrate which may serve as a foundation for housing quantum circuits. In one implementation, the substrate 102 may be a crystalline substrate such as, but not limited to a silicon or a sapphire substrate, and may be provided as a wafer or a portion thereof. In other implementations, the substrate 102 may be non-crystalline. In general, any material that provides sufficient advantages (e.g. sufficiently good electrical isolation and/or ability to apply known fabrication and processing techniques) to outweigh the possible disadvantages (e.g. negative effects of various defects), and that may serve as a foundation upon which a quantum circuit may be built, falls within the spirit and scope of the present disclosure. Additional examples of substrates which may serve as the substrate 102 on which the quantum dot devices as described herein may be fabricated include silicon-on-insulator (SOI) substrates, III-V substrates, and quartz substrates.

[0033] The quantum well stack 104 may include a plurality of layers, each of which is provided substantially perpendicular to the substrate 102, i.e. if the substrate 102 is considered to be horizontal, then each of the layers of the quantum well stack 104 is a vertical layer, illustrated with exemplary vertical lines shown within the quantum well stack 104 in the upper left and lower left illustrations of FIG. 1. Thus, the individual layers of the quantum well stack 104 are stacked in a direction substantially parallel to the plane of the substrate 102 (which direction is illustrated in FIG. 1 with an arrow 108), or, phrased differently, a normal to the planes of the layers of the quantum well stack 104 (which normal is also in the direction 112) is substantially parallel to the substrate 102. A quantum well stack 104 may include at least one quantum well layer 152 (not specifically shown in FIG. 1, but discussed below) in which quantum dots may be localized during operation of the quantum dot device 100; examples of quantum well stacks 104 are discussed below with reference to FIG. 3.

[0034] Each of the gate stacks 106 is a stack of a gate metal 110 and a gate dielectric 112. Only two of the gate stacks 106 are specifically labeled in FIG. 1 in order to not clutter the drawing, but an exemplary 4x6 array of the gate stacks 106 (i.e. 24 gate stacks in total) is illustrated in the lower right portion view of FIG. 1. Of course, in various embodiments, the quantum dot device 100 may include any other number of such gate stacks 106. Furthermore, while FIG. 1 illustrates that the gate dielectric 112 of the different gate stacks 106 is provided as a continuous layer adjacent to the first layer of the gate stack 104, in other embodiments of the quantum dot device 100, each of the gate stacks 106 may include an individual gate dielectric 112, e.g. the gate dielectric 112 of each of the gate stacks 106 may include a dielectric material provided only between the gate metal 110 and the portion of the quantum well stack 104. In the quantum dot device 100 of FIG. 1, the gate dielectric 112 may be in contact with the quantum well stack 104, and, for each of the gate stacks 106, the gate dielectric 112 is between the respective gate metal 110 and the respective portion of the quantum well stack 104.

[0035] As shown in FIG. 1, each of the gate metals 110 may be provided as a strip of a suitable conductive or superconductive material. In various embodiments, such a strip of the gate metal 110 may have a width (i.e. a dimension measured along the x-axis shown in FIG. 1) between about 10 and 500 nanometers (nm), including all values and ranges therein, e.g. between about 20 and 100 nm, or between about 30 and 50 nm, and a thickness (i.e. a dimension measured along the z-axis shown in FIG. 1) between about 10 and 500 nm, including all values and ranges therein, e.g. between about 20 and 100 nm, or between about 30 and 50 nm.

[0036] The individual strips of the gate metal 110 may be stacked above one another in a step-like manner, as can be seen in the lower left illustration of FIG. 1, electrically insulated from one another with an insulating spacer 114, to form a column 120 of the gate metals 110 (4 such columns are shown in the exemplary embodiment of the quantum dot device 100 of FIG. 1, indicated as columns 120-1 through 120-4). In a given column 120, individual gate stacks of the plurality of gate stacks may be aligned along a single line substantially perpendicular to the substrate 102. During the operation of the quantum dot device 100, quantum dots may be formed in the portions of the quantum well stack 104 behind the gate metals 110 for the gate stacks biased to function as quantum dot gates, as described in greater detail below (i.e. the resulting quantum dots may also be arranged in columns, i.e. along a line perpendicular to the substrate, at a distance from one another). When multiple columns are used, then the individual strips of the gate metal 110 may further be arranged in rows (6 such rows are shown in the exemplary embodiment of the quantum dot device 100 of FIG. 1, indicated as rows 122-1 through 122-6).

[0037] Within a given column 120 of the gate metals 110, the individual strips of the gate metal 110 may have different lengths (i.e. dimensions measured along the y-axis shown in FIG. 1). In various embodiments, the lengths of the gate metals 110 may be between about 50 and 500,000 nm, including all values and ranges therein, e.g. between about 500 and 100,000 nm, or between about 1000 and 50,000. In a given column of the gate metals 110, the lengths of any pair of individual gate metals 110 closest to one another (i.e. one "step" of the gate metal 110 and the next "step" of the gate metal 110) may differ by anywhere between about 50 and 10,000 nm, including all values and ranges therein, e.g. between about 10 and 5000 nm, or between about 500 and 2000 nm.

[0038] As a result of arranging the strips of the gate metal 110 in columns 120, various gate stacks 106, e.g. some of the gate metals 110 in case a continuous shared gate dielectric 112 is used, are provided at different distances from the substrate. For example, the gate stacks 106 of the upper-most row 122-1 (i.e. the shortest "step" of the step-like arrangement shown in FIG. 1) of the vertical array of gate stacks are provided at a distance to the substrate 102 than the gate stacks 106 of the lowest row 122-6 (i.e. the longest "step" of the step-like arrangement shown in FIG. 1).

[0039] In various embodiments, the spacer 114 separating the different layers of the gate metals 110 may have a thickness (i.e. a dimension measured along the z-axis shown in FIG. 1) between about 1 and 500 nm, including all values and ranges therein, e.g. between about 5 and 100 nm, or between about 10 and 50 nm. The pairs of two closest different columns of the gate metals 110 (e.g. each pair of the two closest columns of the 4 columns shown in the exemplary embodiment of FIG. 1) may be separated by a distance (i.e. a dimension measured along the x-axis shown in FIG. 1) between about 5 and 500 nm, including all values and ranges therein, e.g. between about 10 and 100 nm, or between about 20 and 40 nm. Separation (i.e. electrical insulation) between the individual columns of the gate metals 110 may be provided using an insulating material, e.g. an ILD 116, as shown in FIG. 1. In various embodiments, the plurality of gate stacks 106 may have a pitch (i.e. center-to-center distance) between about 10 and 500 nm, including all values and ranges therein, e.g. between about 20 and 200 nm, or between about 35 and 50 nm.

[0040] Electrical connectivity to each of the gate stacks 106 may be provided by means of gate contact metal 118, e.g. provided in vias as shown in FIG. 1, electrically connected to the respective gate metal 110. As shown in FIG. 1, the gate contact metals 118 for the individual gate stacks 106 are electrically isolated from one another by the ILD 116. Because of the step-like arrangement of the gate metals 110 of different gate stacks 106 within each column 120, contacts 118 to individual gate metals 110 of a given column 120 may be seen as electrically conductive vias arranged along a single plane substantially perpendicular to the substrate 120, e.g. illustrated in the upper left view of FIG. 1 as a plane shown with a dotted line 124. The array of gate contacts 118 allows different ones

of the gates 106 to be separately electrically controlled. The vertical positioning of the quantum well stack 104, and the step-like arrangement of the gate metals 110 may be particularly advantageous for providing easier control of the individual gates 106, i.e. easier control of the individual quantum dots formed in the vicinity of those gates as a result of the gate operation.

[0041] During operation of the quantum dot device 100, some of the gate stacks 106 may form quantum dot gates, while other gate stacks 106 may form barrier gates, depending on the biases (e.g. voltages) applied to the individual gates 106. Still other gate stacks 106 may act as accumulation gates.

[0042] In general, the term "quantum dot gate" (also sometimes interchangeably referred to as a "plunger gate") is used to describe a gate under which an electrostatic quantum dot is formed during operation of the quantum dot device, e.g. the quantum dot device 100. By controlling the voltage applied to a quantum dot gate, e.g. using a suitable control logic included with or associated with the quantum dot device 100, the electric field in the quantum well stack adjacent to that gate can be modulated/changed to create an energy valley (assuming electron-based quantum dot qubits) between the tunnel barriers created by the barrier gates. Thus, in general, during operation of the quantum dot device 100 shown in FIG. 1, electrical signals (e.g., voltages, radio frequency (RF), and/or microwave signals) may be provided to a quantum dot gate (and neighboring gates) to cause a quantum dot (e.g., an electron spin-based quantum dot) to form in the portion of the quantum well stack 104 adjacent to the quantum dot gate.

[0043] In general, the term "barrier gate" is used to describe a gate used to set a tunnel barrier (i.e. a potential barrier) between either two quantum dot gates (i.e. controlling tunneling of charge carrier(s), e.g. electrons, from one quantum dot to an adjacent quantum dot) or a quantum dot gate and an accumulation gate. When the control logic of the quantum dot device changes the voltage applied to a barrier gate, it changes the height of the tunnel barrier. When a barrier gate is used to set a tunnel barrier between two quantum dot gates, the barrier gate may be used to transfer charge carriers between quantum dots that may be formed in areas of the quantum well adjacent to these quantum dot gates. When a barrier gate is used to set a tunnel barrier between a quantum dot gate and an accumulation gate, the barrier gate may be used to transfer charge carriers in and out of the quantum dot array via the accumulation gate. Thus, in general, during operation of the quantum dot device 100 shown in FIG. 1, electrical signals (e.g., voltages, RF, and/or microwave signals) may be provided to a barrier gate to control the potential energy barrier between adjacent quantum dots or between a quantum dot gate and an adjacent accumulation gate. For example, in some implementations, a barrier gate may be provided between each pair of quantum dot gates, as explained below.

[0044] In general, the term “accumulation gate” (also referred to as “accumulation region”) is used to describe a gate used to form a two-dimensional electron gas (2DEG) in an area that is between the area where the quantum dots may be formed and a charge carrier reservoir. Changing the voltage applied to the accumulation gate allows the control logic of the quantum dot device to control the number of charge carriers in the area under the accumulation gate. For example, changing the voltage applied to the accumulation gate allows reducing the number of charge carriers in the area under the gate so that single charge carriers can be transferred from the reservoir into the quantum dot array, and vice versa. Accumulation regions may be electrically coupled to the quantum well layer of the quantum well stack 104. The accumulation regions may be regions in which carriers accumulate (e.g., due to doping, or due to the presence of large electrodes that pull carriers into the quantum well layer), and may serve as reservoirs of carriers that can be selectively drawn into the areas of the quantum well layer under the quantum dot gates (e.g., by controlling the voltages on the quantum dot gates and the barrier gates) to form carrier-based quantum dots (e.g., electron or hole quantum dots). In some embodiments, a quantum dot device 100 may not include lateral accumulation regions, but may instead include doped layers within the quantum well stack 104. These doped layers may provide the carriers to the quantum well layer. Any combination of accumulation regions (e.g., doped or non-doped) or doped layers in a quantum well stack 104 may be used in any of the embodiments of the quantum dot devices 100 disclosed herein.

[0045] One exemplary biasing scheme which may be used to set which gate stacks 106 act as barrier gates and which act as quantum dot gates is shown in FIG. 2A, illustrating a view of a quantum dot device 200A similar to the quantum dot device 100 shown in the lower right portion of FIG. 1, but with a different number of rows and columns of the gate metals 110. In FIG. 2A, each of the squares 240 (only two of them labeled in order to not clutter the drawing) illustrate a different gate, e.g. a different gate stack 106. Out of those, the squares 240 shown in black illustrate gates biased to act as quantum dot gates (i.e., during operation, quantum dots would form in the portion of the quantum well stack 104 that is behind (in the view of FIG. 2A) the gate dielectric 112 behind the black squares), the squares 240 shown with a brick pattern illustrate gates biased to act as barrier gates, while the squares 240 shown in white illustrate gates biased to act as accumulation gates. This creates a two-dimensional rectangular, i.e. an array of quantum dots with each pair of quantum dots separated by a barrier gate.

[0046] Another exemplary biasing scheme which may be used to set which gate stacks 106 act as barrier gates and which act as quantum dot gates is shown in FIG. 2B, illustrating a view of a quantum dot device 200B similar to the quantum dot device 100 shown in the lower right portion of FIG. 1, but with a different number of rows and columns of the gate metals 110. Similar to FIG. 2A,

in FIG. 2B, the squares 240 shown in black illustrate gates biased to act as quantum dot gates, the squares 240 shown with a brick pattern illustrate gates biased to act as barrier gates, while the squares 240 shown in white illustrate gates biased to act as accumulation gate. The accumulation regions between neighboring accumulation gates can merge, creating a single accumulation region. This creates columns which each containing a single quantum dot with an accumulation region above and below.

[0047] Although some of the drawings and description herein may refer to a particular set of gates as "barrier" or "quantum dot" lines or gates, respectively, this is simply for ease of discussion, and in other embodiments, the role of "barrier" and "quantum dot" lines and gates may be switched (e.g., barrier gates may instead act as quantum dot gates, and vice versa).

[0048] Any suitable materials may be used in various ones of the embodiments disclosed herein. For example, in some embodiments, any of the gate metals 110 may be a superconductor, such as aluminum, titanium nitride (e.g., deposited via atomic layer deposition), or niobium titanium nitride. The gate dielectric 112 may be any suitable material. For example, in some embodiments, the gate dielectric 112 may be silicon oxide, aluminum oxide, or a high-k dielectric, such as hafnium oxide. More generally, the gate dielectric 112 may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of materials that may be used in the gate dielectric 112 may include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, tantalum oxide, tantalum silicon oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric 112 to improve the quality of the gate dielectric 112. In some embodiments, the gate dielectric 112 may be a multilayer gate dielectric, with the layers stacked up in the direction of the arrow 108 shown in FIG. 1. The spacer materials (e.g., the spacer material 114) may be any suitable material, such as a carbon-doped oxide, silicon nitride, silicon oxide, or other carbides or nitrides (e.g., silicon carbide, silicon nitride doped with carbon, and silicon oxynitride). The insulating materials 116 may include silicon oxide, silicon nitride, aluminum oxide, carbon-doped oxide, and/or silicon oxynitride, for example. The gate contact metal 118 may include any suitable conductive or superconductive material, such as e.g. copper, aluminum, titanium nitride, or niobium titanium nitride. Hardmasks, not specifically shown in FIG. 1, may be formed of silicon nitride, silicon carbide, or another suitable material.

[0049] Although not specifically shown in FIGS., in some embodiments, the quantum dot device 100 may include a set of magnets above some or all of the quantum dot gates such that the quantum dot gates are disposed between corresponding magnets and the quantum well stack 104. In one example arrangement of magnets in a quantum dot device 100, each magnet along a quantum dot gate may have a different associated frequency. This frequency may be engineered to take a particular value, or different magnets may have different frequencies due to process variations. Any suitable magnets may be used, and each magnet may thus act as an "antenna" for directing energy of a matching frequency to the quantum dot associated with the magnet. To perform a Pauli gate (or "NOT") operation on a particular quantum dot π, a microwave pulse (e.g., in the gigahertz range) may be applied to the quantum dot gate line that includes the quantum dot gate associated with the quantum dot π. The frequency of the microwave pulse may allow the quantum dot π to be selected by the field gradient of the associated magnet, and thus the microwave pulse may change only the state of the quantum dot π (and not other quantum dots disposed below the same quantum dot gate). The voltages on the other quantum dot gates may remain fixed, and the voltages on the barrier gates may also remain fixed to confine the Pauli gate operation to the quantum dot π.

[0050] Although FIG. 1 illustrates a particular number of gate stacks 106, columns 120, and rows 122, this is simply for illustrative purposes, and any number of gate stacks 106, columns 120, and rows 122 may be included in a quantum dot device 100. Electrical interconnects (e.g., vias and conductive lines) may make contact with the gate metals 110 and gate contacts 118 in any desired manner, all of which being within the scope of the present disclosure.

[0051] FIG. 3 is a cross-sectional view of a double-sided quantum dot device 300, in accordance with various embodiments. The quantum dot device 300 of FIG. 3 may be formed by fabricating the quantum dot device discussed with reference to FIG. 1 on both sides of the quantum well stack 104, e.g. as described below with reference to FIGS. 6A-6K. The quantum well stack 104 may itself include two quantum well layers, one in which quantum dots may be formed by the gates on the corresponding side of the quantum well stack 104, and the other in which quantum dots may be formed by the gates on the other, corresponding side of the quantum well stack 104. The two such quantum well layers are schematically illustrated in the example of FIG. 3 as quantum well layers 324-1 and 324-2 within each of which some exemplary quantum dots shown as white circles. Respective gate dielectrics 112 of the gate stacks on each side of the quantum well stack 104 are shown in FIG. 3 as a first gate dielectric 112-1 and a second gate dielectric 112-2. In some embodiments, the quantum dots formed in one of the quantum well layers may act as the "active" quantum dots in the quantum dot device 100, and the quantum dots formed in the other of the quantum well layers may act as the "read" quantum dots, sensing the state of the active quantum

dots for readout (e.g., through the corresponding gates and other interconnects). Similar double-sided quantum dot devices may be formed using the alternative arrangements of the quantum dot device as e.g. shown in FIGS. 2A-2B, all of which being within the scope of the present disclosure.

[0052] FIGS. 4A-4E illustrate various examples of quantum well stacks 104 that may provide the quantum well stacks 104 of any of the embodiments of the quantum dot devices 100, 200, and 300disclosed herein. FIGS. 4A-4E illustrate the quantum well stacks in a horizontal position in order to show the order of the layers, but within various quantum dot devices 100, 200, and 300 each of such quantum well stacks would be rotated by 90 degrees to be in a vertical position (i.e. perpendicular to the substrate) as described herein.

[0053] In some embodiments, the layers of the quantum well stacks 104 may be grown by epitaxy. Although the quantum well stacks 104 illustrated in FIG. 4 each include two quantum well layers 152 (e.g., as appropriate for a double-sided device, as discussed above with reference to FIG. 3), in some embodiments, the quantum well stack 104 included in any of the quantum dot devices 100, 200, and 300 may include one quantum well layer 152 or more than two quantum well layers 152; elements may be omitted from the quantum well stacks 104, or added to the quantum well stacks 104, to achieve various embodiments, as appropriate. Layers other than the quantum well layer(s) 152 in a quantum well stack 104 may have higher threshold voltages for conduction than the quantum well layer(s) 152 so that when the quantum well layer(s) 152 are biased at their threshold voltages, the quantum well layer(s) 152 conduct and the other layers of the quantum well stack 104 do not. This may avoid parallel conduction in both the quantum well layer(s) 152 and the other layers, and thus avoid compromising the strong mobility of the quantum well layer(s) 152 with conduction in layers having inferior mobility.

[0054] FIG. 4A is a cross-sectional view of a quantum well stack 104 including only a quantum well layer 152-1, a barrier layer 154, and a quantum well layer 152-2. In some embodiments, the quantum well layers 152 of FIG. 4A may be formed of intrinsic silicon, and the gate dielectrics 112 may be formed of silicon oxide; in such an arrangement, during use of the quantum dot device 100, a 2DEG may form in the intrinsic silicon at the interface between the intrinsic silicon and the proximate silicon oxide. Embodiments in which the quantum well layers 152 of FIG. 4A are formed of intrinsic silicon may be particularly advantageous for electron-type quantum dot devices 100, 200, and 300. In some embodiments, the quantum well layers 152 of FIG. 4A may be formed of intrinsic germanium, and the gate dielectrics 112 may be formed of germanium oxide; in such an arrangement, during use of the quantum dot devices 100, 200, or/and 300, a 2DEG may form in the intrinsic germanium at the interface between the intrinsic germanium and the proximate germanium oxide. Such embodiments may be particularly advantageous for hole-type quantum dot

devices 100, 200, and 300. In some embodiments, the quantum well layers 152 may be strained, while in other embodiments, the quantum well layers 152 may not be strained.

[0055] The barrier layer 154 of FIG. 4A may provide a potential barrier between the quantum well layer 152-1 and the quantum well layer 152-2. In some embodiments in which the quantum well layers 152 of FIG. 4A are formed of silicon, the barrier layer 154 may be formed of silicon germanium. The germanium content of this silicon germanium may be about 20-80% (e.g., about 30%). In some embodiments in which the quantum well layers 152 are formed of germanium, the barrier layer 154 may be formed of silicon germanium (with a germanium content of about 20-80% (e.g., about 70%)).

[0056] The thicknesses (i.e., dimensions measure along the y-axis of the coordinate systems shown in FIGS. 1-3) of the layers in the quantum well stack 104 of FIG. 4A may take any suitable values. For example, in some embodiments, the thickness of the barrier layer 154 (e.g., silicon germanium) may be between about 0 and 400 nm, including all values and ranges therein, e.g. below about 100 nm. In some embodiments, the thickness of the quantum well layers 152 (e.g., silicon or germanium) may be between about 5 and 30 nm, including all values and ranges therein.

[0057] FIG. 4B is a cross-sectional view of a quantum well stack 104 including quantum well layers 152-1 and 152-2, a barrier layer 154-2 disposed between the quantum well layers 152-1 and 152-2, and additional barrier layers 154-1 and 154-3. In the double-sided quantum dot device 300, the barrier layer 154-1 may be disposed between the quantum well layer 152-1 and the first gate dielectric 112-1, while the barrier layer 154-3 may be disposed between the quantum well layer 152-2 and the second gate dielectric 112-2. In some embodiments, the barrier layer 154-3 may be formed of a material (e.g., silicon germanium), and when the quantum well stack 104 is being grown, the barrier layer 154-3 may include a buffer region of that material. This buffer region may trap defects that form in this material as it is grown, and in some embodiments, the buffer region may be grown under different conditions (e.g., deposition temperature or growth rate) from the rest of the barrier layer 154-3. In particular, the rest of the barrier layer 154-3 may be grown under conditions that achieve fewer defects than the buffer region. In some embodiments, the buffer region may be lattice mismatched with the quantum well layer(s) 152 in a quantum well stack 104, imparting biaxial strain to the quantum well layer(s) 152.

[0058] The barrier layers 154-1 and 154-3 may provide potential energy barriers around the quantum well layers 152-1 and 152-2, respectively, and the barrier layer 154-1 may take the form of any of the embodiments of the barrier layer 154-3 discussed herein. In some embodiments, the barrier layer 154-1 may have a similar form as the barrier layer 154-3, but may not include a "buffer region" as discussed above; in the quantum dot device 100, the barrier layer 154-3 and the barrier

layer 154-1 may have substantially the same structure. The barrier layer 154-2 may take the form of any of the embodiments of the barrier layer 154 discussed above with reference to FIG. 4A. The thicknesses (i.e., y-heights) of the layers in the quantum well stack 104 of FIG. 4B may take any suitable values. For example, in some embodiments, the thickness of the barrier layers 154-1 and 154-3 (e.g., silicon germanium) in the quantum dot device 100 may be between about 0 and 400 nm. In some embodiments, the thickness of the quantum well layers 152 (e.g., silicon or germanium) may be between about 5 and 30 nm (e.g., about 10 nm). In some embodiments, the thickness of the barrier layer 154-2 (e.g., silicon germanium) may be between about 25 and 75 nm (e.g., about 32 nm).

[0059] FIGS. 4C-4D illustrate examples of quantum well stacks 104 including doped layer(s) 137. As noted above, doped layer(s) 137 may be included in a quantum well stack 104 instead of or in addition to an accumulation region 162.

[0060] FIG. 4C is a cross-sectional view of a quantum well stack 104 including a buffer layer 176, a barrier layer 155-2, a quantum well layer 152-2, a barrier layer 154-2, a doped layer 137, a barrier layer 154-1, a quantum well layer 152-1, and a barrier layer 155-1.

[0061] The buffer layer 176 may be formed of the same material as the barrier layer 155-2, and may be present to trap defects that form in this material as it is grown. In some embodiments, the buffer layer 176 may be grown under different conditions (e.g., deposition temperature or growth rate) from the barrier layer 155-2. In particular, the barrier layer 155-2 may be grown under conditions that achieve fewer defects than the buffer layer 176. In some embodiments in which the buffer layer 176 includes silicon germanium, the silicon germanium of the buffer layer 176 may have a germanium content that varies to the barrier layer 155-2; for example, the silicon germanium of the buffer layer 176 may have a germanium content that varies from zero percent to a non-zero percent (e.g., about 30%) at the barrier layer 155-2. The buffer layer 176 may be grown beyond its critical layer thickness such that it is substantially free of stress from the underlying base (and thus may be referred to as "relaxed"). In some embodiments, the thickness of the buffer layer 176 (e.g., silicon germanium) may be between about 0.3 and 4 microns (e.g., about 0.3-2 microns, or 0.5 microns). In some embodiments, the buffer layer 176 may be lattice mismatched with the quantum well layer(s) 152 in a quantum well stack 104, imparting biaxial strain to the quantum well layer(s) 152.

[0062] The barrier layer 155-2 may provide a potential energy barrier proximate to the quantum well layer 152-2. The barrier layer 155-2 may be formed of any suitable materials. For example, in some embodiments in which the quantum well layer 152 is formed of silicon or germanium, the barrier layer 155-2 may be formed of silicon germanium. In some embodiments, the thickness of the barrier layer 155-2 may be between about 0 and 400 nm (e.g., between about 25 and 75 nm).

[0063] The quantum well layer 152-2 may be formed of a different material than the barrier layer 155-2. Generally, a quantum well layer 152 may be formed of a material such that, during operation of the quantum dot devices 100, 200, and 300, a 2DEG may form in the quantum well layer 152. Embodiments in which the quantum well layer 152 is formed of intrinsic silicon may be particularly advantageous for electron-type quantum dot devices 100, 200, and 300. Embodiments in which a quantum well layer 152 is formed of intrinsic germanium may be particularly advantageous for hole-type quantum dot devices 100, 200, and 300. In some embodiments, a quantum well layer 152 may be strained, while in other embodiments, a quantum well layer 152 may not be strained. The thickness of a quantum well layer 152 may take any suitable values; in some embodiments, a quantum well layer 152 may have a thickness between about 5 and 30 nm.

[0064] In the quantum well stack 104 of FIG. 4C, the doped layer 137 may be "shared" by the two quantum well layers 152 in the quantum well stack 104, in that the doped layer 137 provides carriers to the quantum well layer 152-1 and the quantum well layer 152-2 during use. In the double-sided quantum dot device 300, the quantum well layer 152-1 may be disposed between the doped layer 137 and the first gate dielectric 112-1, while the quantum well layer 152-2 may be disposed between the doped layer 137 and the second gate dielectric 112-2. The doped layer 137 of FIG. 4C may be doped with an n-type material (e.g., for an electron-type quantum dot devices 100, 200, and 300) or a p-type material (e.g., for a hole-type quantum dot devices 100, 200, and 300). In some embodiments, the doping concentration of the doped layer 137 may be between about $10^{17}/cm^3$ and $10^{20}/cm^3$ (e.g., between about $10^{17}/cm^3$ and $10^{18}/cm^3$). The thickness (i.e., z-height) of the doped layer 137 may depend on the doping concentration, among other factors, and in some embodiments, may be between about 5 and 50 nm (e.g., between about 20 and 30 nm).

[0065] A doped layer 137 may be formed using any of a number of techniques. In some embodiments, a doped layer 137 may be formed of an undoped base material (e.g., silicon germanium) that is doped in situ during growth of the base material by epitaxy. In some embodiments, a doped layer 137 may initially be fully formed of an undoped base material (e.g., silicon germanium), then a layer of dopant may be deposited on this base material (e.g., a monolayer of the desired dopant), and an annealing process may be performed to drive the dopant into the base material. In some embodiments, a doped layer 137 may initially be fully formed of an undoped base material (e.g., silicon germanium), and the dopant may be implanted into the lattice (and, in some embodiments, may be subsequently annealed). In some embodiments, a doped layer 137 may be provided by a silicon germanium layer (e.g., with about 90% germanium content) doped with an n-type dopant. In general, any suitable technique may be used to form a doped layer 137.

[0066] The barrier layer 154-2 may not be doped, and thus may provide a barrier to prevent impurities in the doped layer 137 from diffusing into the quantum well layer 152-2 and forming recombination sites or other defects that may reduce channel conduction and thereby impede performance of the quantum dot devices 100, 200, and 300. In some embodiments of the quantum well stack 104 of FIG. 4C, the doped layer 137 may include a same material as the barrier layer 154-2, but the barrier layer 154-2 may not be doped. For example, in some embodiments, the doped layer 137 and the barrier layer 154-2 may both be silicon germanium. In some embodiments in which the quantum well layer 152-2 is formed of silicon, the barrier layer 154-2 may be formed of silicon germanium. The germanium content of this silicon germanium may be about 20-80% (e.g., about 30%). In some embodiments in which the quantum well layer 152-2 is formed of germanium, the barrier layer 154-2 may be formed of silicon germanium (with a germanium content of about 20-80% (e.g., about 70%)). The thickness of the barrier layer 154-2 may depend on the doping concentration of the doped layer 137, among other factors discussed below, and in some embodiments, may be between about 5 and 50 nm (e.g., between about 20 and 30 nm).

[0067] The barrier layer 154-1 may provide a barrier to prevent impurities in the doped layer 137 from diffusing into the quantum well layer 152-1, and may take any of the forms described herein for the barrier layer 154-2. Similarly, the quantum well layer 152-1 may take any of the forms described herein for the quantum well layer 152-2. The barrier layer 155-1 may provide a potential energy barrier proximate to the quantum well layer 152-1 (as discussed above with reference to the barrier layer 155-2 and the quantum well layer 152-2), and may take any of the forms described herein for the barrier layer 155-2.

[0068] The thickness of a barrier layer 154 may impact the ease with which carriers in the doped layer 137 can move into a quantum well layer 152 disposed on the other side of the barrier layer 154. The thicker the barrier layer 154, the more difficult it may be for carriers to move into the quantum well layer 152; at the same time, the thicker the barrier layer 154, the more effective it may be at preventing impurities from the doped layer 137 from moving into the quantum well layer 152. Additionally, the diffusion of impurities may depend on the temperature at which the quantum dot devices 100, 200, and 300 operate. Thus, the thickness of the barrier layer 154 may be adjusted to achieve a desired energy barrier and impurity screening effect between the doped layer 137 and the quantum well layer 152 during expected operating conditions.

[0069] In some embodiments of the quantum well stack 104 of FIG. 4C (e.g., those included in "single-sided" quantum dot devices described herein, e.g. quantum dot device 100), only a single quantum well layer 152 may be included. For example, the layers 154-1 and 152-1 may be omitted, and gates may be formed proximate to the barrier layer 155-1 such that the quantum well layer 152-

1 is disposed between the gates and the doped layer 137. In other embodiments, the layers 154-1, 152-1, and 155-2 may be omitted, and gates may be formed proximate to the doped layer 137. In some embodiments, the buffer layer 176 and/or the barrier layer 155-2 may be omitted from the quantum well stack 104 of FIG. 4C.

[0070] FIG. 4D is a cross-sectional view of a quantum well stack 104 that is similar to the quantum well stack 104 of FIG. 4C, except that in the place of the single doped layer 137 shared by two quantum well layers 152, the quantum well stack 104 of FIG. 4D includes two different doped layers 137-2 and 137-1 (spaced apart by a barrier layer 155-3). In such an embodiment, the doped layer 137-2 may provide a source of carriers for the quantum well layer 152-2, and the doped layer 137-1 may provide a source of carriers for the quantum well layer 152-1. The barrier layer 155-3 may provide a potential barrier between the two doped layers 137, and may take any suitable form. Generally, the elements of the quantum well stack 104 of FIG. 4D may take the form of any of the corresponding elements of the quantum well stack 104 of FIG. 4C. The doped layers 137-1 and 137-2 may have the same geometry and material composition, or may have different geometries and/or material compositions.

[0071] FIG. 4E is a cross-sectional view of a quantum well stack 104 in which two doped layers 137-1 and 137-2 are disposed toward the "outside" of the quantum well stack 104, rather than the "inside" of the quantum well stack 104, as illustrated in FIGS. 4C and 4D. In particular, the quantum well layer 152-2 is disposed between the doped layer 137-2 and the quantum well layer 152-1, and the quantum well layer 152-1 is disposed between the doped layer 137-1 and the quantum well layer 152-2. In the double-sided quantum dot device 300, the doped layer 137-1 may be disposed between the quantum well layer 152-1 and the first gate dielectric 112-1, while the doped layer 137-2 may be disposed between the quantum well layer 152-2 and the second gate dielectric 112-2. In the quantum well stack 104 of FIG. 4E, a barrier layer 155-3 provides a potential barrier between the quantum well layers 152-1 and 152-2 (rather than between the doped layers 137-1 and 137-2, as illustrated in the quantum well stack 104 of FIG. 4D). Generally, the elements of the quantum well stack 104 of FIG. 4E may take the form of any of the corresponding elements of the quantum well stack 104 of FIGS. 4A-D.

[0072] In some particular embodiments in which the quantum dot device 100 is a "single-sided" device with only one set of gates, the quantum well stack 104 may include a silicon base, a buffer layer 176 of silicon germanium (e.g., with 30% germanium content), then a doped layer 137 formed of silicon germanium doped with an n-type dopant, a thin barrier layer 154 formed of silicon germanium (e.g., silicon germanium with 70% germanium content), a silicon quantum well layer 152, and a barrier layer 155 formed of silicon germanium (e.g., with 30% germanium content); in such an

embodiment, the gates may be disposed on the barrier layer 155. In some other particular embodiments in which the quantum dot device 100 is a "single-sided" device with only one set of gates, the quantum well stack 104 may include a silicon base, a doped layer 137 formed of silicon doped with an n-type dopant, a thin barrier layer 154 formed of silicon germanium, and a silicon quantum well layer 152; in such an embodiment, the gates may be disposed on the silicon quantum well layer 152.

Fabrication of quantum dot devices with vertical quantum well layers

[0073] In general, quantum dot devices with quantum well layers perpendicular to the substrate, as described herein, may be fabricated any suitable techniques. FIGS. 5A-5B provide a flow chart of one exemplary method 500 for fabricating quantum dot devices with vertical quantum well layers as described herein, according to some embodiments of the present disclosure. While the method 500 is particularly adapted for fabricating a double-sided quantum dot device, e.g. as the one shown in FIG. 3, this method is also applicable for fabricating single-sided quantum dot devices, possibly with minor modifications.

[0074] Although the operations of the method 500 are illustrated in FIGS. 5A-5B once each and in a particular order, the operations may be performed in any suitable order and repeated as desired. For example, one or more operations may be performed in parallel to manufacture multiple quantum circuit assemblies as described herein substantially simultaneously. In another example, the operations may be performed in a different order to reflect the architecture of a particular quantum circuit component in which one or more quantum circuit assemblies with vertical quantum well layers fabricated according to the method 500 are to be included.

[0075] In addition, the exemplary manufacturing method 500 may include other operations not specifically shown in FIGS. 5A-5B, such as e.g. various cleaning or planarization operations as known in the art. For example, in some embodiments, the substrate may be cleaned prior to or/and after any of the processes of the method 500 described herein, e.g. to remove oxides, surface-bound organic and metallic contaminants, as well as subsurface contamination. In some embodiments, cleaning may be carried out using e.g. a chemical solutions (such as peroxide), and/or with ultraviolet (UV) radiation combined with ozone, and/or oxidizing the surface (e.g., using thermal oxidation) then removing the oxide (e.g. using hydrofluoric acid (HF)). In another examples, the structures/assemblies described herein may be planarized prior to or/and after any of the processes of the method 500 described herein, e.g. to remove overburden or excess materials. In some embodiments, planarization may be carried out using either wet or dry planarization processes, e.g. planarization be a chemical mechanical planarization (CMP), which may be understood as a process

that utilizes a polishing surface, an abrasive and a slurry to remove the overburden and planarize the surface.

[0076] Various operations of the method 500 may be illustrated with reference to exemplary embodiments shown in FIGS. 6A-6K, but the method 500 may be used to manufacture any suitable quantum circuit assemblies with vertical quantum well layers according to any embodiments of the present disclosure. FIGS. 6A-6K are cross-sections illustrating various example stages in the manufacture of a quantum circuit assembly using the method of FIGS. 5A-5B in accordance with some embodiments of the present disclosure. Each one of FIGS. 6A-6K illustrates a top down view and two cross-sectional views similar to FIGS. 1 and 3.

[0077] The method 500 may begin with providing, over a substrate, a stack of gate metal layers separated by spacer dielectric layers (process 502 shown in FIG. 5A, a result of which is illustrated with an assembly 602 shown in FIG. 6A). The assembly 602 illustrates the substrate 102, with pairs of a spacer dielectric, e.g. the spacer 114, and gate metal, e.g. the gate metal 110, layers stacked over one another, forming a stack 630. In some embodiments, the first gate metal layer may be provided over the substrate 102 without the spacer 114 in between. The number of gate metal layers provided in the process 502 will define the number of staircase “steps” (i.e. the number of rows 122) of the future gate stack array.

[0078] In various embodiments, any suitable deposition techniques, possibly in combination with patterning, may be used for providing the stack of gate metal layers separated by spacer dielectric layers in the process 502. Examples of deposition techniques for depositing layers of electrically conductive gate metal layers include atomic layer deposition (ALD), physical vapor deposition (PVD) (e.g. evaporative deposition, magnetron sputtering, or e-beam deposition), chemical vapor deposition (CVD), or electroplating. Examples of deposition techniques for depositing layers of dielectric spacer layers include ALD, PVD, CVD, spin-coating, or dip-coating. The layers may include materials and have thicknesses as described above with reference to the gate metals 110 and the spacer 114.

[0079] The method 500 may then proceed with patterning the stack of gate metal layers separated by spacer dielectric layers to form strips of gate metals (process 504 shown in FIG. 5A, a result of which is illustrated with an assembly 604 shown in FIG. 6B). The assembly 604 illustrates the stack 630 patterned to create openings 632 extending through the stack to the substrate 102, thus defining gate metal strips and forming the columns 120 of the future gate stack array as described above.

[0080] In various embodiments, any suitable patterning techniques may be used for forming openings 632 in the stack 630 in the process 504. Examples of such techniques include

photolithographic or electron-beam (e-beam) patterning, possibly in conjunction with a dry etch, such as e.g. RF reactive ion etch (RIE) or inductively coupled plasma (ICP) RIE, to pattern the stack 630 of continuous layers into columns of specified geometries for a given implementation. The distances by which neighboring columns 120 may be separated from one another are described above.

[0081] The method 500 may then proceed with filling the openings between the gate metal columns with a dielectric material (process 506 shown in FIG. 5A, a result of which is illustrated with an assembly 606 shown in FIG. 6C). The assembly 606 illustrates that the spacer 114 may be deposited in between and above the columns 120. In other embodiments, a dielectric material different from the spacer 114 may be provided in the process 506, e.g. the ILD 116 as described above, or any other dielectric material that is able to be deposited into the openings 632 and which can serve to provide electrical isolation between the different columns 120.

[0082] In various embodiments, any suitable deposition techniques for filling in dielectric materials may be used for filling the openings 632 with the dielectric material in the process 506. Examples of such techniques include ALD, PVD, CVD, spin-coating, or dip-coating.

[0083] Next, an opening for the future quantum well stack and gate dielectric of a quantum dot device may be created within the stack 630 patterned into columns 120 (process 508 shown in FIG. 5A, a result of which is illustrated with an assembly 608 shown in FIG. 6D). The assembly 608 illustrates that an opening 634 extending through the stack 630 to the substrate 102 may be created, e.g. in the center of the stack 630 (center along the y-axis). In other embodiments, the opening 634 does not have to be in the center. The assembly 608 further illustrates sidewalls 636 and a bottom 638 of the opening 634.

[0084] In various embodiments, any suitable patterning techniques may be used for forming the openings 634 in the process 508, such as e.g. those described above with reference to the process 504. Dimensions of the opening 634 may be such as to allow providing the gate dielectric 112 and the quantum well stack 104, both as described above, within the opening 634.

[0085] Next, at least the sidewalls of the opening for the future quantum well stack and gate dielectric of a quantum dot device may then be lined with a gate dielectric material (process 510 shown in FIG. 5A, a result of which is illustrated with an assembly 610 shown in FIG. 6E). The assembly 610 illustrates that the sidewalls 636 and the bottom 638 of the opening 634 may be lined with the gate dielectric 112. As a result of depositing the gate dielectric 112 as a liner within the opening 634, the volume of the opening 634 is reduced but there still remains a smaller opening, as indicated in FIG. 6E with a smaller opening 640. Although not specifically illustrated in FIG. 6E, in some implementations, as a result of performing the process 510, the gate dielectric 112 may be

deposited not only within the opening 634, but also over upper surfaces 642 of the stack 630. Such a layer over the upper surfaces 642 may subsequently be removed, e.g. using a suitable planarization technique.

[0086] In various embodiments, any suitable deposition techniques for conformally depositing materials onto selected surfaces may be used to line the opening 634 with the dielectric material in the process 510. Examples of such techniques include ALD, CVD, plasma enhanced CVD (PECVD), or/and PVD processes. Thickness of the gate dielectric liner deposited in the process 510 is described above with reference to the gate dielectric 112.

[0087] The method 500 may then proceed with removing the gate dielectric material from the bottom of the opening, thereby exposing the underlying substrate (process 512 shown in FIG. 5A, a result of which is illustrated with an assembly 612 shown in FIG. 6F). The assembly 612 illustrates that the gate dielectric 112 is removed to expose the substrate 102 at the bottom 638 of the opening 640. As a result, the gate dielectric 112 is separated into the first gate dielectric 112-1 on one of the sidewalls 636 of the opening 634 and the second gate dielectric 112-2 on the other sidewall, and the opening 640 is transformed into an opening 644, as also shown in the assembly 612.

[0088] In various embodiments, any suitable techniques for recessing dielectric materials may be used to remove the gate dielectric 112 from the bottom 638 of the opening 640 in the process 512. Examples of such techniques include various RIE processes.

[0089] Next, the method 500 may proceed with filling at least a portion of the opening resulting from performing the process 512 with a quantum well stack (process 514 shown in FIG. 5B, a result of which is illustrated with an assembly 614 shown in FIG. 6G). The assembly 614 illustrates the quantum well stack 104 provided within the opening 644. The quantum well stack 104 may include any suitable stack of materials as described above, and may be provided using various deposition techniques, such as e.g. epitaxial growth.

[0090] Next, the columns 120 of the stack 630 may be patterned to create the staircase profile where the gate metal elements at different distances from the substrate have different lengths (process 516 shown in FIG. 5B, a result of which is illustrated with an assembly 616 shown in FIG. 6H).

[0091] In various embodiments, any suitable patterning techniques may be used for forming the steps of the gate metals 110 in the process 516, such as e.g. those described above with reference to the process 504. Lengths of the gate metals 110 in different rows 122 may be as described above.

[0092] The method 500 may then proceed with filling the openings which may be created as a result of forming the staircase profile with a dielectric material (process 518 shown in FIG. 5B, a

result of which is illustrated with an assembly 618 shown in FIG. 6I). The assembly 618 illustrates that the ILD 116 may be deposited in the process 518. In other embodiments, a dielectric material different from the ILD 116 may be provided in the process 518, e.g. the spacer 114 as described above, or any other suitable dielectric material.

[0093] In various embodiments, any suitable deposition techniques for filling in dielectric materials may be used for filling the dielectric material in the process 518. Examples of such techniques include ALD, PVD, CVD, spin-coating, or dip-coating.

[0094] Next, opening for the future gate contacts to the gate metals of a quantum dot device may be created (process 520 shown in FIG. 5B, a result of which is illustrated with an assembly 620 shown in FIG. 6J). The assembly 620 illustrates that openings 646, e.g. via openings, extending through the stack 630 to respective steps of the gate metals 110 may be created in the process 520.

[0095] In various embodiments, any suitable patterning techniques may be used for forming the via openings 646 in the process 520, such as e.g. those described above with reference to the process 504. Dimensions of the openings 646 may be such as to allow providing suitable electrical conductive materials within the openings 646 in order to create gate contacts 118 as described above.

[0096] The method 500 may finish with providing electrically conductive gate contact materials within the via openings formed in the process 520 (process 522 shown in FIG. 5B, a result of which is illustrated with an assembly 622 shown in FIG. 6K). The assembly 622 illustrates that the openings 646 are filled with the gate contact material 118, however, in other embodiments, the gate contact material 118 may be provided only on the sidewalls of the openings 646 and the center of the openings 646 may be either left void or filled with a different material, which material could then be either conductive (e.g. a conductive but not superconductive material) or a dielectric material (e.g. a ceramic).

[0097] In various embodiments, any suitable deposition techniques for providing electrically conductive materials within via openings may be used to fill the opening 646 with the gate contact material 118 in the process 522. Examples of such techniques include ALD, CVD, plasma enhanced CVD (PECVD), or/and PVD processes.

[0098] In various embodiments of the method 500 described above, processes may be performed in a different order. For example, the staircase profile may be created right after the continuous layers of the stack 630 are patterned into columns 120, or right after any other one of the processes shown in FIG. 5A.

[0099] Furthermore, as mentioned above, the method 500 may also be applicable for fabricating single-sided quantum dot devices, with suitable differences to produce gates on only one side.

Exemplary quantum dot devices

[0100] Quantum dot devices with vertical quantum well layers as described above may be included in any kind of qubit device assemblies or quantum processing devices/structures. Some examples of such devices/structures are illustrated in FIGS. 7A-7B, 8, and 9.

[0101] FIGS. 7A-7B are top views of a wafer 1100 and dies 1102 that may be formed from the wafer 1100, according to some embodiments of the present disclosure. The die 1102 may include any of the quantum dot devices 100, 200, or/and 300 disclosed herein. The wafer 1100 may include semiconductor material and may include one or more dies 1102 having conventional and quantum circuit device elements formed on a surface of the wafer 1100. Each of the dies 1102 may be a repeating unit of a semiconductor product that includes any suitable conventional and/or quantum circuit qubit device. After the fabrication of the semiconductor product is complete, the wafer 1100 may undergo a singulation process in which each of the dies 1102 is separated from one another to provide discrete "chips" of the semiconductor product. A die 1102 may include one or more quantum circuit assemblies with vertical quantum well layers in accordance with any of the designs described herein, as well as other IC components. In some embodiments, the wafer 1100 or the die 1102 may include a memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 1102. For example, a memory array formed by multiple memory devices may be formed on a same die 1102 as a processing device (e.g., the processing device 2002 of FIG. 9) or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array.

[0102] FIG. 8 is a cross-sectional side view of a device assembly 1200 that may include any of the quantum dot devices 100, 200, or/and 300 described herein. The device assembly 1200 includes a number of components disposed on a circuit board 1202. The device assembly 1200 may include components disposed on a first face 1240 of the circuit board 1202 and an opposing second face 1242 of the circuit board 1202; generally, components may be disposed on one or both faces 1240 and 1242.

[0103] In some embodiments, the circuit board 1202 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 1202. Signal transfer between components or layer may happen with both low resistance DC connections or by either in-plane or out-of-plane capacitive

connections. In other embodiments, the circuit board 1202 may be a package substrate or flexible board.

[0104] The IC device assembly 1200 illustrated in FIG. 8 may include a package-on-interposer structure 1236 coupled to the first face 1240 of the circuit board 1202 by coupling components 1216. The coupling components 1216 may electrically and mechanically couple the package-on-interposer structure 1236 to the circuit board 1202, and may include solder balls (as shown in FIG. 8), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure. The coupling components 1216 may include other forms of electrical connections that may have no mechanical contact, such as parallel-plate capacitors or inductors, which can allow high-frequency connection between components without mechanical or DC connection.

[0105] The package-on-interposer structure 1236 may include a package 1220 coupled to an interposer 1204 by coupling components 1218. The coupling components 1218 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 1216. Although a single package 1220 is shown in FIG. 8, multiple packages may be coupled to the interposer 1204; indeed, additional interposers may be coupled to the interposer 1204. The interposer 1204 may provide an intervening substrate used to bridge the circuit board 1202 and the package 1220. In some implementations, the package 1220 may be a quantum circuit device package as described herein, e.g. a package including one or more dies with any of the quantum dot devices 100, 200, or/and 300 described herein. In other implementations, the package 1220 may be a conventional IC package with non-quantum circuit assemblies. Generally, the interposer 1204 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 1204 may couple the package 1220 (e.g., a die) to a ball grid array (BGA) of the coupling components 1216 for coupling to the circuit board 1202. In the embodiment illustrated in FIG. 8, the package 1220 and the circuit board 1202 are attached to opposing sides of the interposer 1204; in other embodiments, the package 1220 and the circuit board 1202 may be attached to a same side of the interposer 1204. In some embodiments, three or more components may be interconnected by way of the interposer 1204.

[0106] The interposer 1204 may be formed of a crystalline material, such as silicon, germanium, or other semiconductors, an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some embodiments, the interposer 1204 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 1204 may include metal interconnects 1210 and vias 1208, including but not limited

to through-silicon vias (TSVs) 1206. The interposer 1204 may further include embedded devices 1214, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as RF devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 1204. The package-on-interposer structure 1236 may take the form of any of the package-on-interposer structures known in the art.

[0107] The device assembly 1200 may include a package 1224 coupled to the first face 1240 of the circuit board 1202 by coupling components 1222. The coupling components 1222 may take the form of any of the embodiments discussed above with reference to the coupling components 1216, and the package 1224 may take the form of any of the embodiments discussed above with reference to the package 1220. Thus, the package 1224 may be a package including any of the quantum dot devices 100, 200, or/and 300 described herein or may be a conventional IC package, for example.

[0108] The device assembly 1200 illustrated in FIG. 8 includes a package-on-package structure 1234 coupled to the second face 1242 of the circuit board 1202 by coupling components 1228. The package-on-package structure 1234 may include a package 1226 and a package 1232 coupled together by coupling components 1230 such that the package 1226 is disposed between the circuit board 1202 and the package 1232. The coupling components 1228 and 1230 may take the form of any of the embodiments of the coupling components 1216 discussed above, and the packages 1226 and 1232 may take the form of any of the embodiments of the package 1220 discussed above. Each of the packages 1226 and 1232 may be a qubit device package with any of the quantum dot devices 100, 200, or/and 300 as described herein or may be a conventional IC package, for example.

[0109] FIG. 9 is a block diagram of an exemplary quantum computing device 2000 that may include one or more of quantum circuit assemblies with any of the quantum dot devices 100, 200, or/and 300 in accordance with any of the configurations described herein, according to some embodiments of the present disclosure. A number of components are illustrated in FIG. 9 as included in the quantum computing device 2000, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the quantum computing device 2000 may be attached to one or more PCBs (e.g., a motherboard), and may be included in, or include, any of the quantum circuits with any of the quantum circuit assemblies described herein. In some embodiments, various ones of these components may be fabricated onto a single system-on-a-chip (SoC) die. Additionally, in various embodiments, the quantum computing device 2000 may not include one or more of the

components illustrated in FIG. 9, but the quantum computing device 2000 may include interface circuitry for coupling to the one or more components. For example, the quantum computing device 2000 may not include a display device 2006, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 2006 may be coupled. In another set of examples, the quantum computing device 2000 may not include an audio input device 2018 or an audio output device 2008, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 2018 or audio output device 2008 may be coupled. In further examples, the quantum computing device 2000 may include a microwave input device or a microwave output device (not specifically shown in FIG. 9), or may include microwave input or output device interface circuitry (e.g., connectors and supporting circuitry) to which a microwave input device or microwave output device may be coupled.

[0110] The quantum computing device 2000 may include a processing device 2002 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 2002 may include a quantum processing device 2026 (e.g., one or more quantum processing devices), and a non-quantum processing device 2028 (e.g., one or more non-quantum processing devices). The quantum processing device 2026 may include one or more of any of the quantum dot devices 100, 200, or/and 300 arranged in accordance with various embodiments described herein, and may perform data processing by performing operations on the quantum dots that may be generated in these quantum circuit assemblies, and monitoring the result of those operations. For example, different quantum dots may be allowed to interact, the quantum states of different quantum dots may be set or transformed, and the quantum states of different quantum dots may be read. The quantum processing device 2026 may be a universal quantum processor, or specialized quantum processor configured to run one or more particular quantum algorithms. In some embodiments, the quantum processing device 2026 may execute algorithms that are particularly suitable for quantum computers, such as cryptographic algorithms that utilize prime factorization, encryption/decryption, algorithms to optimize chemical reactions, algorithms to model protein folding, etc. The quantum processing device 2026 may also include support circuitry to support the processing capability of the quantum processing device 2026, such as input/output channels, multiplexers, signal mixers, quantum amplifiers, and analog-to-digital converters.

[0111] As noted above, the processing device 2002 may include a non-quantum processing device 2028. In some embodiments, the non-quantum processing device 2028 may provide peripheral logic to support the operation of the quantum processing device 2026. For example, the non-quantum

processing device 2028 may control the performance of a read operation, control the performance of a write operation, control the clearing of quantum bits, etc. The non-quantum processing device 2028 may also perform conventional computing functions to supplement the computing functions provided by the quantum processing device 2026. For example, the non-quantum processing device 2028 may interface with one or more of the other components of the quantum computing device 2000 (e.g., the communication chip 2012 discussed below, the display device 2006 discussed below, etc.) in a conventional manner, and may serve as an interface between the quantum processing device 2026 and conventional components. The non-quantum processing device 2028 may include one or more digital signal processors (DSPs), application-specific ICs (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices.

[0112] The quantum computing device 2000 may include a memory 2004, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid-state memory, and/or a hard drive. In some embodiments, the states of quantum dots in the quantum processing device 2026 may be read and stored in the memory 2004. In some embodiments, the memory 2004 may include memory that shares a die with the non-quantum processing device 2028. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random access memory (STT-MRAM).

[0113] The quantum computing device 2000 may include a cooling apparatus 2024. The cooling apparatus 2024 may maintain the quantum processing device 2026, in particular the quantum dot devices 100, 200, or/and 300 as described herein, at a predetermined low temperature during operation to avoid qubit decoherence and to reduce the effects of scattering in the quantum processing device 2026. This predetermined low temperature may vary depending on the setting; in some embodiments, the temperature may be 5 degrees Kelvin or less. In some embodiments, the non-quantum processing device 2028 (and various other components of the quantum computing device 2000) may not be cooled by the cooling apparatus 2030, and may instead operate at room temperature. The cooling apparatus 2024 may be, for example, a dilution refrigerator, a helium-3 refrigerator, or a liquid helium refrigerator.

[0114] In some embodiments, the quantum computing device 2000 may include a communication chip 2012 (e.g., one or more communication chips). For example, the communication chip 2012 may be configured for managing wireless communications for the transfer of data to and from the quantum computing device 2000. The term "wireless" and its derivatives may be used to describe

circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0115] The communication chip 2012 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip 2012 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 2012 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 2012 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 2012 may operate in accordance with other wireless protocols in other embodiments. The quantum computing device 2000 may include an antenna 2022 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0116] In some embodiments, the communication chip 2012 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 2012 may include multiple communication chips. For instance, a first communication chip 2012 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 2012 may be dedicated to longer-range wireless communications such as global positioning system (GPS), EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 2012 may be dedicated to wireless communications, and a second communication chip 2012 may be dedicated to wired communications.

[0117] The quantum computing device 2000 may include battery/power circuitry 2014. The battery/power circuitry 2014 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the quantum computing device 2000 to an energy source separate from the quantum computing device 2000 (e.g., AC line power).

[0118] The quantum computing device 2000 may include a display device 2006 (or corresponding interface circuitry, as discussed above). The display device 2006 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0119] The quantum computing device 2000 may include an audio output device 2008 (or corresponding interface circuitry, as discussed above). The audio output device 2008 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0120] The quantum computing device 2000 may include an audio input device 2018 (or corresponding interface circuitry, as discussed above). The audio input device 2018 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0121] The quantum computing device 2000 may include a GPS device 2016 (or corresponding interface circuitry, as discussed above). The GPS device 2016 may be in communication with a satellite-based system and may receive a location of the quantum computing device 2000, as known in the art.

[0122] The quantum computing device 2000 may include an other output device 2010 (or corresponding interface circuitry, as discussed above). Examples of the other output device 2010 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0123] The quantum computing device 2000 may include an other input device 2020 (or corresponding interface circuitry, as discussed above). Examples of the other input device 2020 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0124] The quantum computing device 2000, or a subset of its components, may have any appropriate form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a

printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device.

Select Examples

[0125] The following paragraphs provide examples of various ones of the embodiments disclosed herein.

[0126] Example 1 provides a quantum dot device that includes a substrate, a quantum well stack provided over the substrate, and at least one gate stack, preferably a plurality of gate stacks. The quantum well stack includes a plurality of planar layers, where planes of the plurality of layers are substantially perpendicular to the substrate (in other words, the layers of the quantum well stack are stacked in a direction substantially parallel to the substrate, or, phrased differently, a normal to the planes of the layers of the quantum well stack is substantially parallel to the substrate). The at least one gate stack is adjacent to a portion of a first layer of the plurality of layers of the quantum well stack (such a "first layer" is the layer closest to the gate dielectric as described herein). In case a plurality of gate stacks are used, the gate stacks are adjacent to different portions of the first layer of the plurality of layers of the quantum well stack, where some of the different portions could be at different distances from the substrate.

[0127] Example 2 provides the quantum dot device according to Example 1, where the at least one gate stack includes a gate dielectric adjacent to the portion of the first layer and a gate metal, and where the gate dielectric is between the portion of the first layer and the gate metal.

[0128] Example 3 provides the quantum dot device according to Examples 1 or 2, where at least one gate stack is at least one first gate stack, and the quantum dot device further includes at least one second gate stack adjacent to the quantum well stack opposite the at least one first gate stack. Thus, the quantum dot device could be a double-sided device having gate stacks on both sides of the quantum well stack.

[0129] Example 4 provides the quantum dot device according to any one Examples 1-3, where at least one gate stack includes a plurality of gate stacks adjacent to different portions of the first layer, where individual gate stacks of the plurality of gate stacks are provided at different distances from the substrate. Thus, the plurality of gate stacks may be seen as arranged in a vertical array along a plane that is substantially perpendicular to the plane of the substrate and is substantially parallel to the planes of the plurality of layers of the quantum well stack.

[0130] Example 5 provides the quantum dot device according to Example 1, where at least one gate stack includes a plurality of gate stacks adjacent to different portions of the first layer, with individual gate stacks of the plurality of gate stacks being aligned along a line substantially perpendicular to the substrate. In other words, the individual gate stacks may be stacked above one

another, so that, in operation, quantum dots formed in portions of the quantum well stacks adjacent to at least some of such gate stacks are arranged substantially vertically with respect to the substrate (i.e. quantum dots are arranged along a line perpendicular to the substrate, at a distance from one another).

[0131] Vertical quantum dot arrays may allow for easier control of individual gates/quantum dots, especially when an arrangement described herein as a "step-like" arrangement is used.

[0132] Example 6 provides the quantum dot device according to Example 5, where each gate stack of the plurality of gate stacks includes a gate dielectric and a gate metal, and where the gate metals of different gate stacks of the plurality of gate stacks extend away from the first layer by different lengths.

[0133] Example 7 provides the quantum dot device according to Example 5, where each gate stack of the plurality of gate stacks includes a gate dielectric and a gate metal, and where the gate metals of different gate stacks are arranged over the substrate above one another as steps (i.e. in a step-like arrangement).

[0134] Example 8 provides the quantum dot device according to Example 5, where each gate stack of the plurality of gate stacks includes a gate dielectric and a gate metal, and where contacts to individual gate metals of the plurality of gate stacks include electrically conductive vias arranged along a single plane substantially perpendicular to the substrate.

[0135] Example 9 provides the quantum dot device according to any one of Examples 6-8, where the gate metals of different gate stacks are electrically isolated from one another, e.g. using a spacer material, which could be any suitable dielectric material.

[0136] Example 10 provides the quantum dot device according to any one of Examples 6-9, where the gate dielectric is adjacent to the first layer, and is between the first layer and the gate metal. In other words, the materials of the gate stacks (namely, the gate dielectric and the gate metal) are stacked over the quantum well stack in a direction substantially parallel to the substrate. Thus, starting with the quantum well stack which includes a stack of layers provided substantially perpendicular to the substrate, gate dielectrics are provided adjacent to different portions of the first layer of the stack of layers, and gate metals are provided so that, for each of the gate stacks, at least a portion of the gate dielectric is between the first layer of the quantum well stack and the corresponding gate metal. The gate metals of different gate stacks are electrically isolated from one another.

[0137] Example 11 provides the quantum dot device according to any one of Examples 6-10, where the gate dielectrics of different gate stacks are parts of a substantially continuous layer of a dielectric

material adjacent the first layer of the quantum well stack. In other words, the gate dielectric may continuously extend between the gate metal of different gate stacks and the quantum well stack.

[0138] Example 12 provides the quantum dot device according to Example 1, where at least one gate stack includes a plurality of gate stacks aligned with (or, phrased differently, arranged as) points of an NxM array (i.e. aligned with points where different lines of an NxM grid of lines intersect one another), where each of N and M is an integer, and at least one of them is greater than 1, and where a plane of the NxM array is substantially parallel to the planes of the plurality of layers of the quantum well stack and is substantially perpendicular to the substrate. As a result, during operation of the quantum dot device, quantum dots will be formed within the quantum well layer in an array that is substantially perpendicular to the substrate, thus forming a vertical quantum dot array.

[0139] Example 13 provides the quantum dot device according to Example 12, where an individual gate stack of the plurality of gate stacks includes a gate dielectric and a gate metal.

[0140] Example 14 provides the quantum dot device according to Example 13, where the gate metals of different individual gate stacks are electrically isolated from one another, e.g. using a spacer material.

[0141] Example 15 provides the quantum dot device according to Examples 13 or 14, where the gate dielectric of the individual gate stack is adjacent to the first layer, and is between the first layer and the corresponding gate metal. In some embodiments, the gate dielectric may continuously extend between the gate metal of different gate stacks and the quantum well stack.

[0142] Example 16 provides the quantum dot device according to any one of Examples 4-15, where the plurality of gate stacks includes a plurality of quantum dot gates and a plurality of barrier gates.

[0143] Example 17 provides the quantum dot device according to Example 16, where a quantum dot gate is between each nearest neighbor pair of barrier gates.

[0144] Example 18 provides the quantum dot device according to any one of Examples 4-17, where the plurality of gate stacks have a pitch between about 10 and 500 nm, including all values and ranges therein, e.g. between about 20 and 200 nm, or between about 35 and 50 nm.

[0145] Example 19 provides a method for forming a quantum dot device. The method includes providing a stack of alternating layers of electrically conductive and dielectric materials over a substrate; patterning the stack to form two or more columns of the alternating layers of electrically conductive and dielectric materials, where each two nearest columns are separated by a respective opening; patterning the stack to create a staircase profile where alternating layers further away from the substrate are shorter than alternating layers closer to the substrate; providing electrical connections to at least some of the layers of the electrically conductive material; providing an opening within the stack; providing a gate dielectric on sidewalls of the opening; providing a

quantum well stack within the opening with the gate dielectric so that layers of the quantum well stack are substantially perpendicular to the substrate.

[0146] Example 20 provides the method according to Example 19, where providing the gate dielectric on the sidewalls of the opening includes conformally depositing the gate dielectric on the sidewalls and bottom of the opening, followed by removal of the gate dielectric deposited on the bottom of the opening.

[0147] Example 21 provides the method according to Examples 19 or 20, further including depositing a dielectric material into the respective openings between each two nearest columns.

[0148] Example 22 provides a quantum computing device that includes a quantum processing device that includes a quantum dot device and a memory device to store data generated during operation of the quantum processing device. The quantum dot device includes a quantum well stack provided over a substrate and including a plurality of layers, where planes of the plurality of layers are substantially perpendicular to the substrate, and a plurality of gate stacks adjacent to different portions of a first layer of the plurality of layers of the quantum well stack.

[0149] Example 23 provides the quantum computing device according to Example 22, further including a cooling apparatus configured to maintain the temperature of the quantum processing device below 5 degrees Kelvin. Example 24 provides the quantum computing device according to any of Examples 22-23, where the memory device is configured to store instructions for a quantum computing algorithm to be executed by the quantum processing device. Example 25 provides the quantum computing device according to any of Examples 22-24, further including a non-quantum processing device coupled to the quantum processing device. In various further Examples, the quantum dot device of the quantum processing device according to any one of Examples 22-25 may be Example provides the quantum dot device according to any one of the preceding Examples (e.g. Example provides the quantum dot device according to any one of Examples 1-18).

[0150] The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize. These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Claims:

1. A quantum dot device, comprising:

a substrate;

a quantum well stack comprising a plurality of layers, where planes of one or more of the plurality of layers are perpendicular to the substrate; and

at least one gate stack adjacent to a portion of a first layer of the plurality of layers of the quantum well stack.

2. The quantum dot device according to claim 1, wherein the at least one gate stack includes a gate dielectric adjacent to the portion of the first layer and a gate metal, and wherein the gate dielectric is between the portion of the first layer and the gate metal.

3. The quantum dot device according to claim 1, wherein at least one gate stack is at least one first gate stack, and the quantum dot device further comprises at least one second gate stack adjacent to the quantum well stack opposite the at least one first gate stack.

4. The quantum dot device according to claim 1, wherein at least one gate stack comprises a plurality of gate stacks adjacent to different portions of the first layer, where individual gate stacks are at different distances from the substrate.

5. The quantum dot device according to claim 1, wherein at least one gate stack comprises a plurality of gate stacks adjacent to different portions of the first layer, with individual gate stacks aligned along a line perpendicular to the substrate.

6. The quantum dot device according to claim 5, wherein each gate stack of the plurality of gate stacks comprises a gate dielectric and a gate metal, and wherein the gate metals of different gate stacks of the plurality of gate stacks extend away from the first layer by different lengths.

7. The quantum dot device according to claim 5, wherein each gate stack of the plurality of gate stacks comprises a gate dielectric and a gate metal, and wherein the gate metals of different gate stacks are arranged over the substrate above one another as steps.

8. The quantum dot device according to claim 5, wherein each gate stack of the plurality of gate stacks comprises a gate dielectric and a gate metal, and wherein contacts to individual gate metals of the plurality of gate stacks include electrically conductive vias arranged along a single plane perpendicular to the substrate.

9. The quantum dot device according to any one of claims 6-8, wherein the gate metals of different gate stacks are electrically isolated from one another.

10. The quantum dot device according to any one of claims 6-8, wherein the gate dielectric is adjacent to the first layer, and is between the first layer and the gate metal.

11. The quantum dot device according to any one of claims 6-8, wherein the gate dielectrics of different gate stacks are parts of a continuous layer of a dielectric material adjacent the first layer of the quantum well stack.

12. The quantum dot device according to claim 1, wherein at least one gate stack comprises a plurality of gate stacks aligned with points of an NxM array, where each of N and M is an integer and where a plane of the NxM array is substantially parallel to the planes of the plurality of layers.

13. The quantum dot device according to claim 12, wherein an individual gate stack of the plurality of gate stacks comprises a gate dielectric and a gate metal.

14. The quantum dot device according to claim 13, wherein the gate metals of different individual gate stacks are electrically isolated from one another.

15. The quantum dot device according to claim 13, wherein the gate dielectric of the individual gate stack is adjacent to the first layer, and is between the first layer and the gate metal.

16. The quantum dot device according to any one of claims 12-15, wherein the plurality of gate stacks comprises a plurality of quantum dot gates and a plurality of barrier gates.

17. The quantum dot device according to claim 16, wherein a quantum dot gate is between each nearest neighbor pair of barrier gates.

18. The quantum dot device according to any one of claims 4-8 or 12-15, wherein the plurality of gate stacks have a pitch between 10 and 500 nanometers.

19. A method for forming a quantum dot device, the method comprising:

providing a stack of alternating layers of electrically conductive and dielectric materials over a substrate;

providing electrical connections to at least some of the layers of the electrically conductive material;

providing an opening within the stack;

providing a gate dielectric on sidewalls of the opening;

providing a quantum well stack within the opening with the gate dielectric so that one or more layers of the quantum well stack are perpendicular to the substrate.

20. The method according to claim 19, wherein providing the gate dielectric on the sidewalls of the opening comprises conformally depositing the gate dielectric on the sidewalls and bottom of the opening.

21. The method according to claims 19 or 20, further comprising:

patterning the stack to form two or more columns of the alternating layers of electrically conductive and dielectric materials, where each two nearest columns are separated by a respective opening; and

patterning the stack to create a staircase profile where alternating layers further away from the substrate are shorter than alternating layers closer to the substrate.

22. A quantum computing device, comprising:

a quantum processing device that includes a quantum dot device; and

a memory device to store data generated during operation of the quantum processing device,

wherein the quantum dot device includes:

a quantum well stack over a substrate and comprising a plurality of layers, wherein planes of at least one or more of the plurality of layers are perpendicular to the substrate, and

a plurality of gate stacks adjacent to different portions of a first layer of the plurality of layers of the quantum well stack.

23. The quantum computing device according to claim 22, further comprising a cooling apparatus to maintain the temperature of the quantum processing device below 5 degrees Kelvin.

24. The quantum computing device according to any of claims 22-23, wherein the memory device is to store instructions for a quantum computing algorithm to be executed by the quantum processing device.

25. The quantum computing device according to any of claims 22-23, further comprising a non-quantum processing device coupled to the quantum processing device.

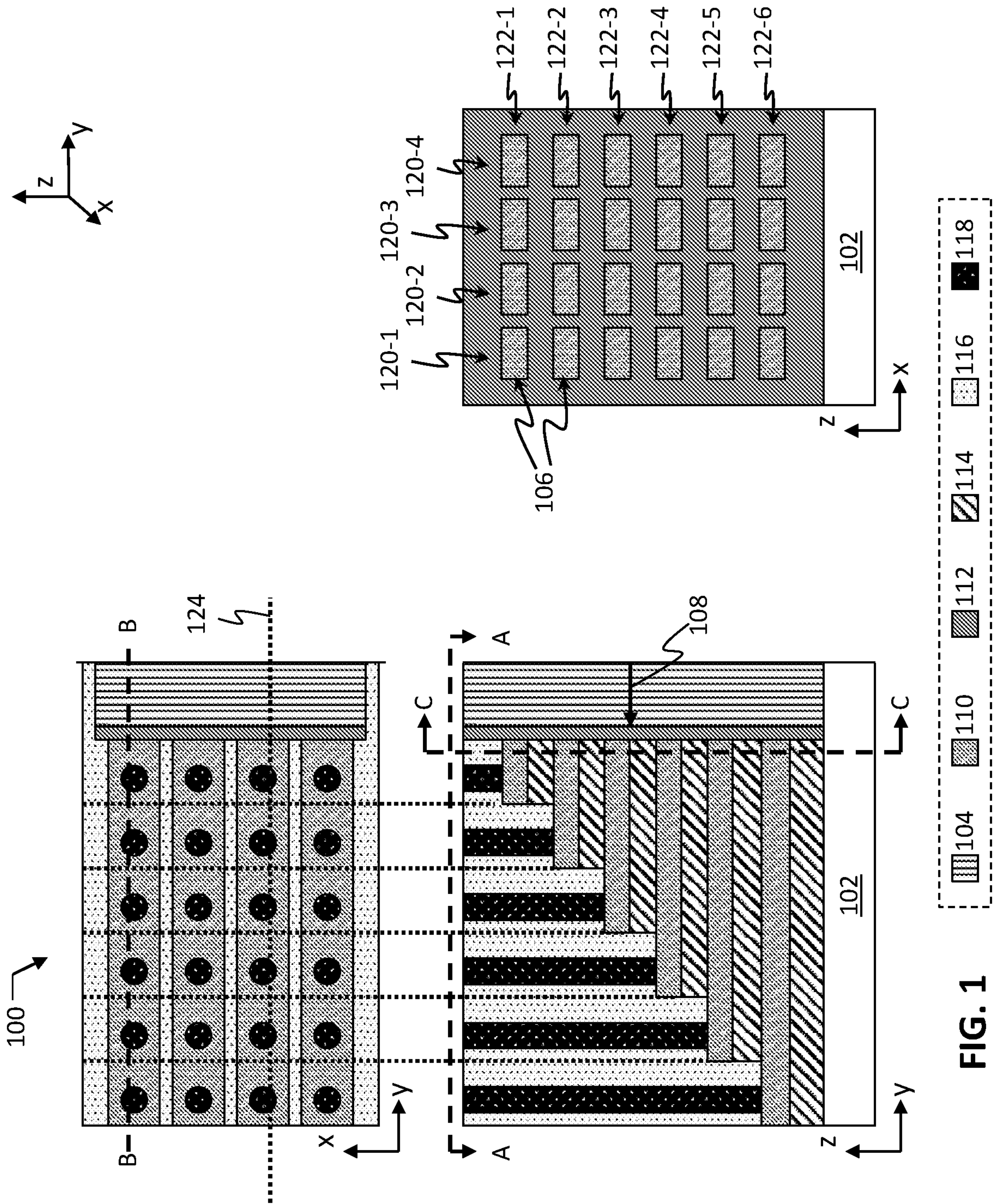

FIG. 1

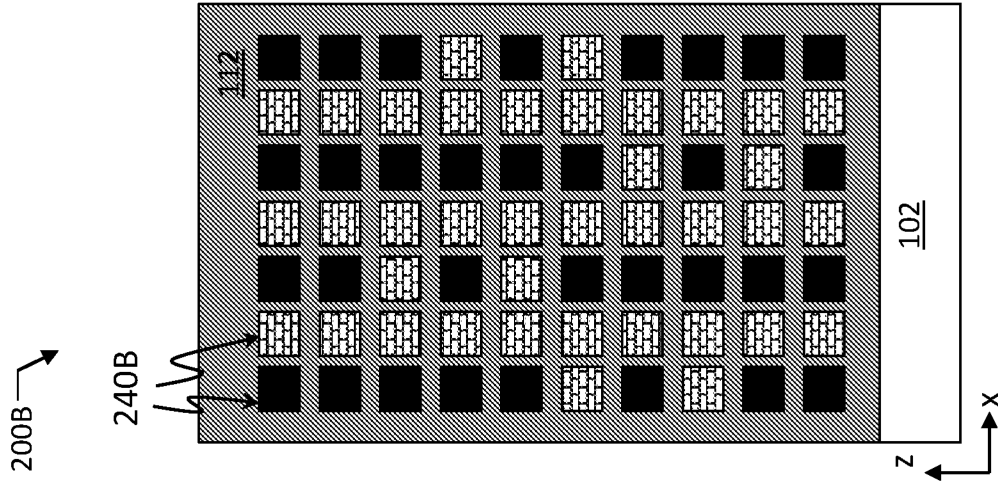

FIG. 2B

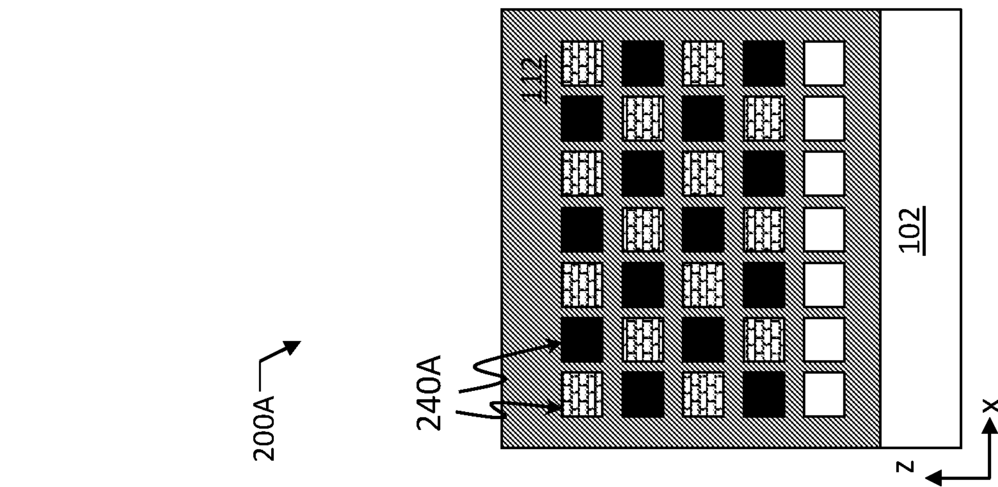

FIG. 2A

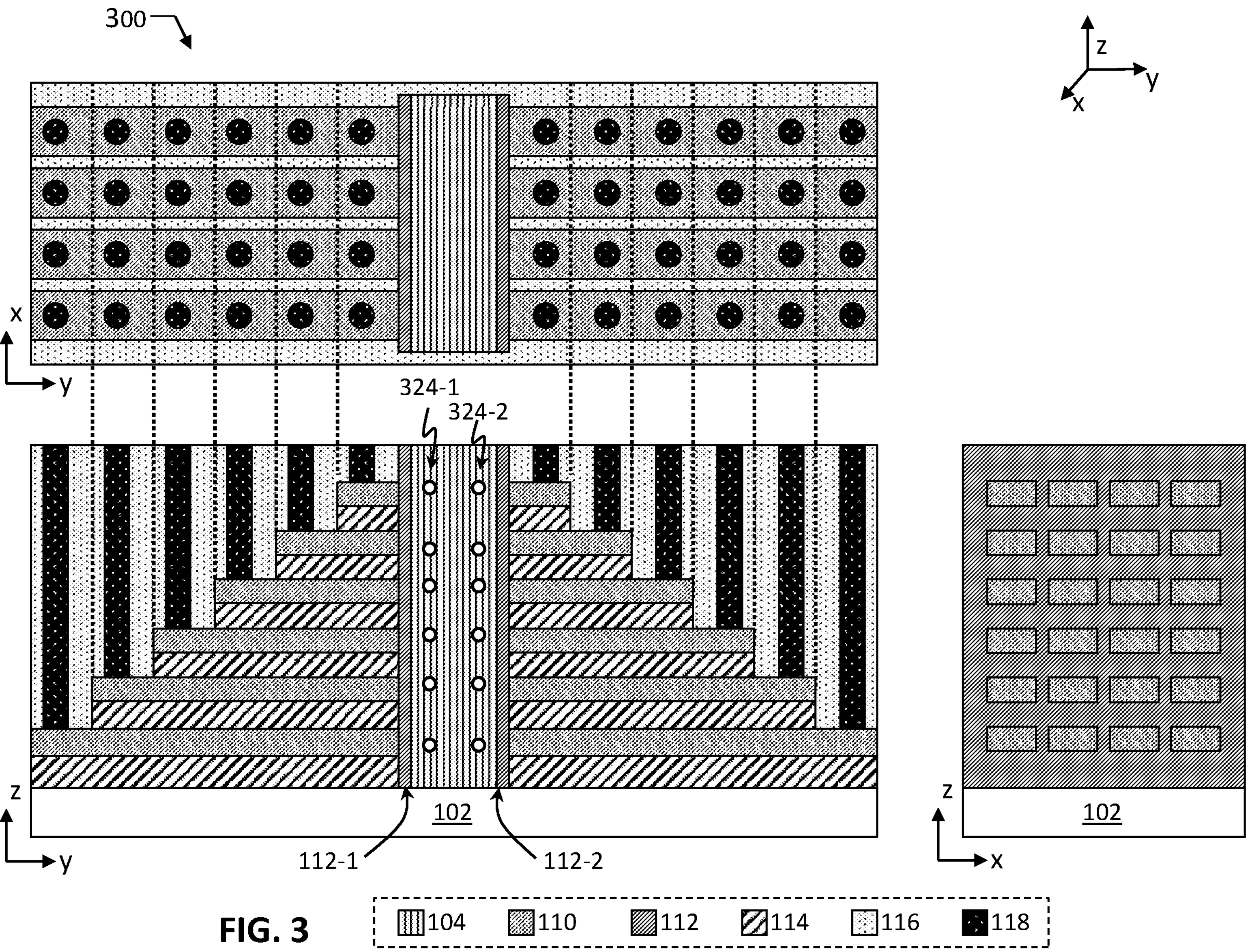

FIG. 3

104

152-1
154
152-2

FIG. 4A

104

154-1
152-1
154-2
152-2
154-3

FIG. 4B

104

155-1
152-1
154-1
137
154-2
152-2
155-2
176

FIG. 4C

104

155-1
152-1
154-1
137-1
155-3
137-2
154-2
152-2
155-2
176

FIG. 4D

104

155-1
137-1
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FIG. 4E

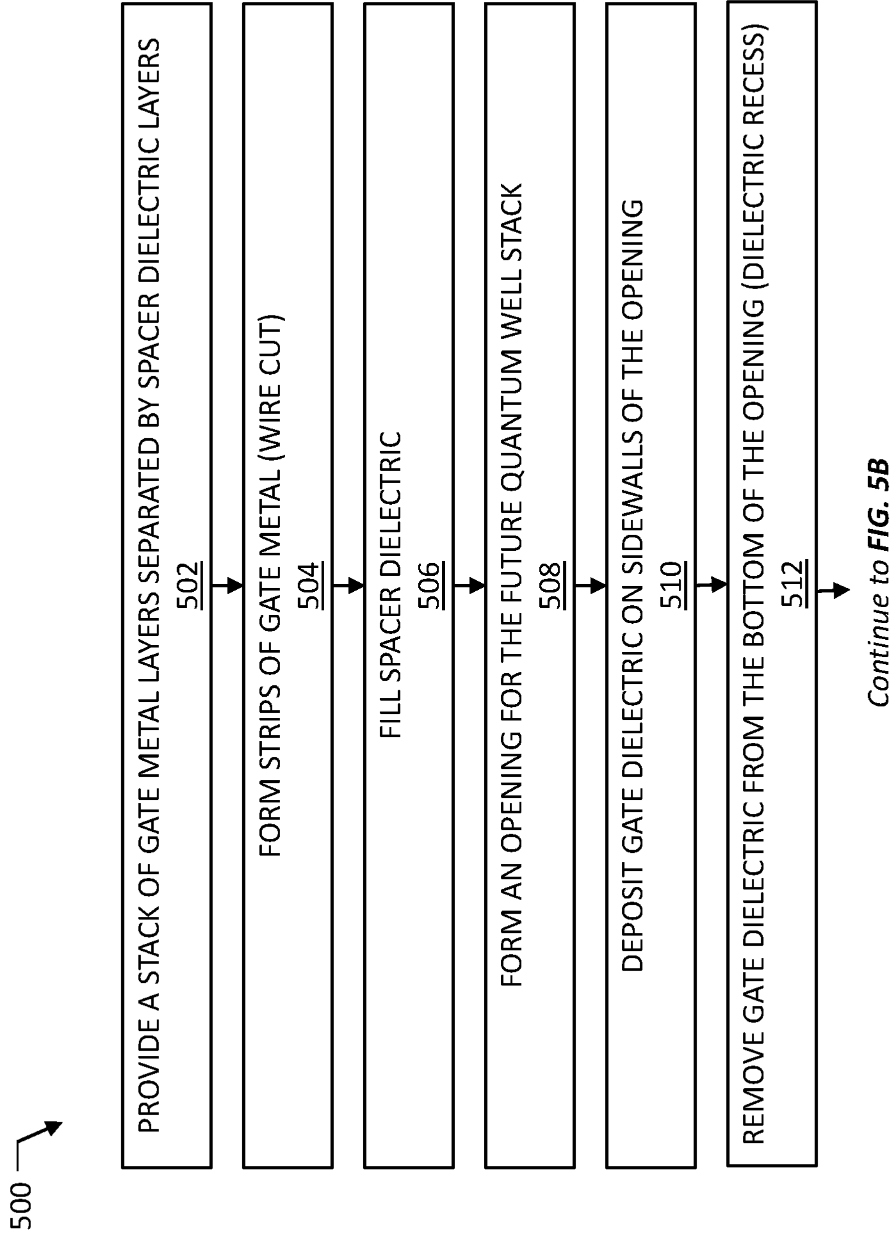

FIG. 5A

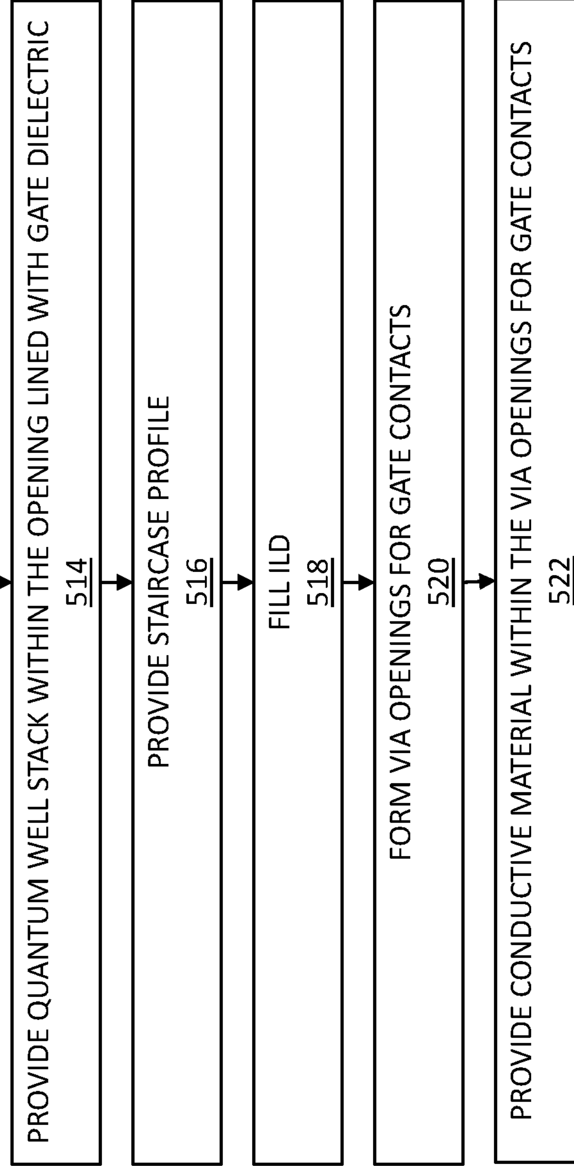

FIG. 5B

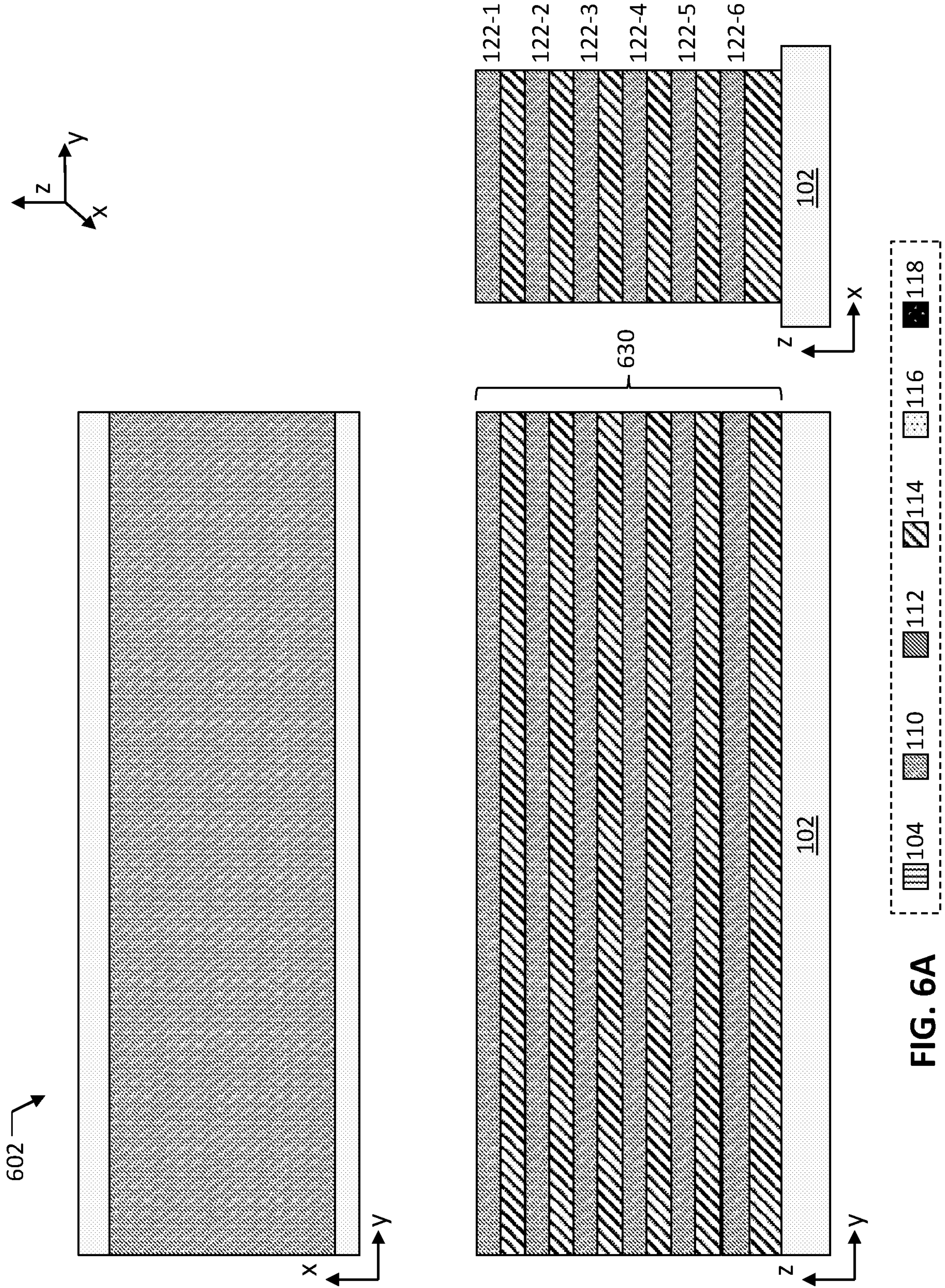

FIG. 6A

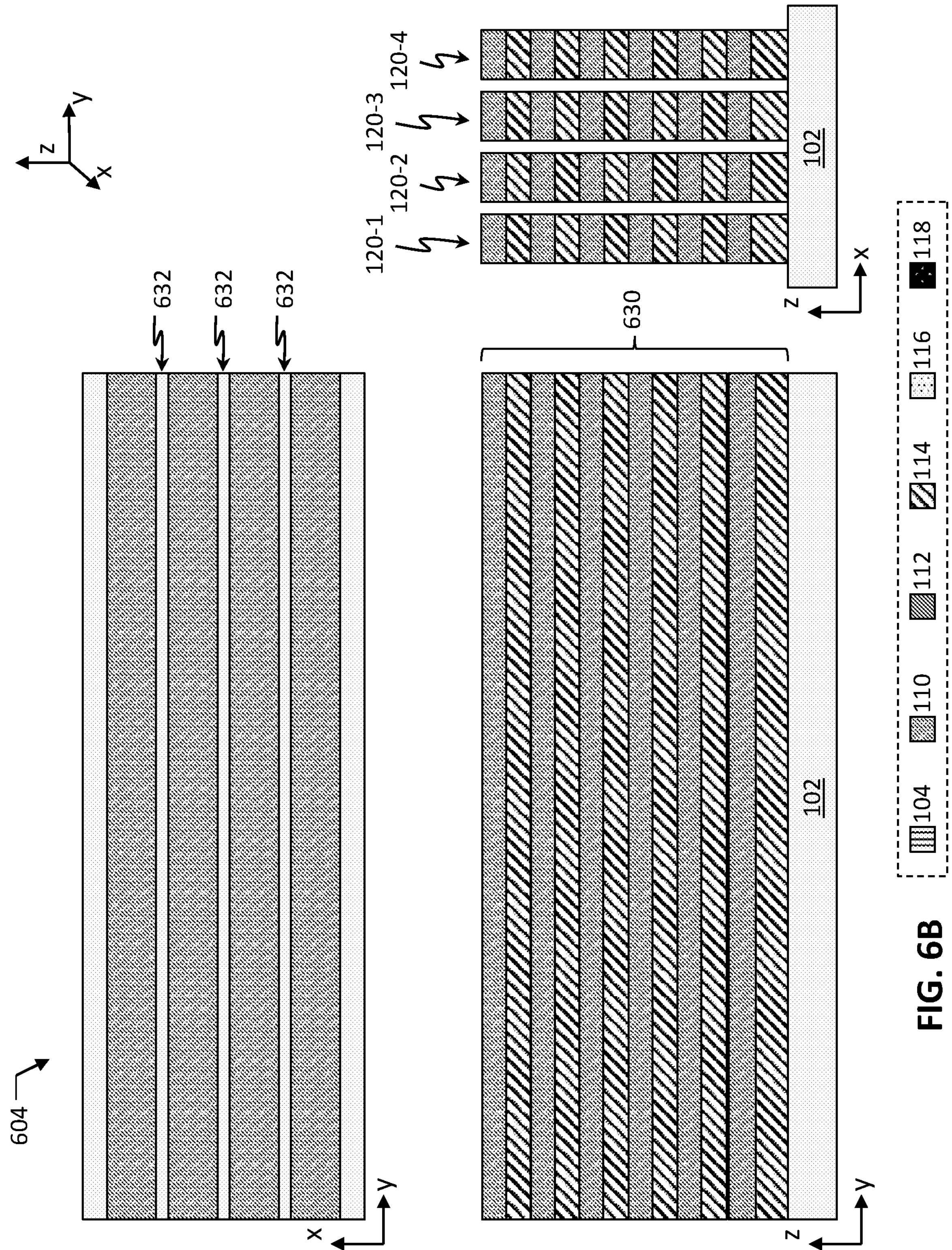

FIG. 6B

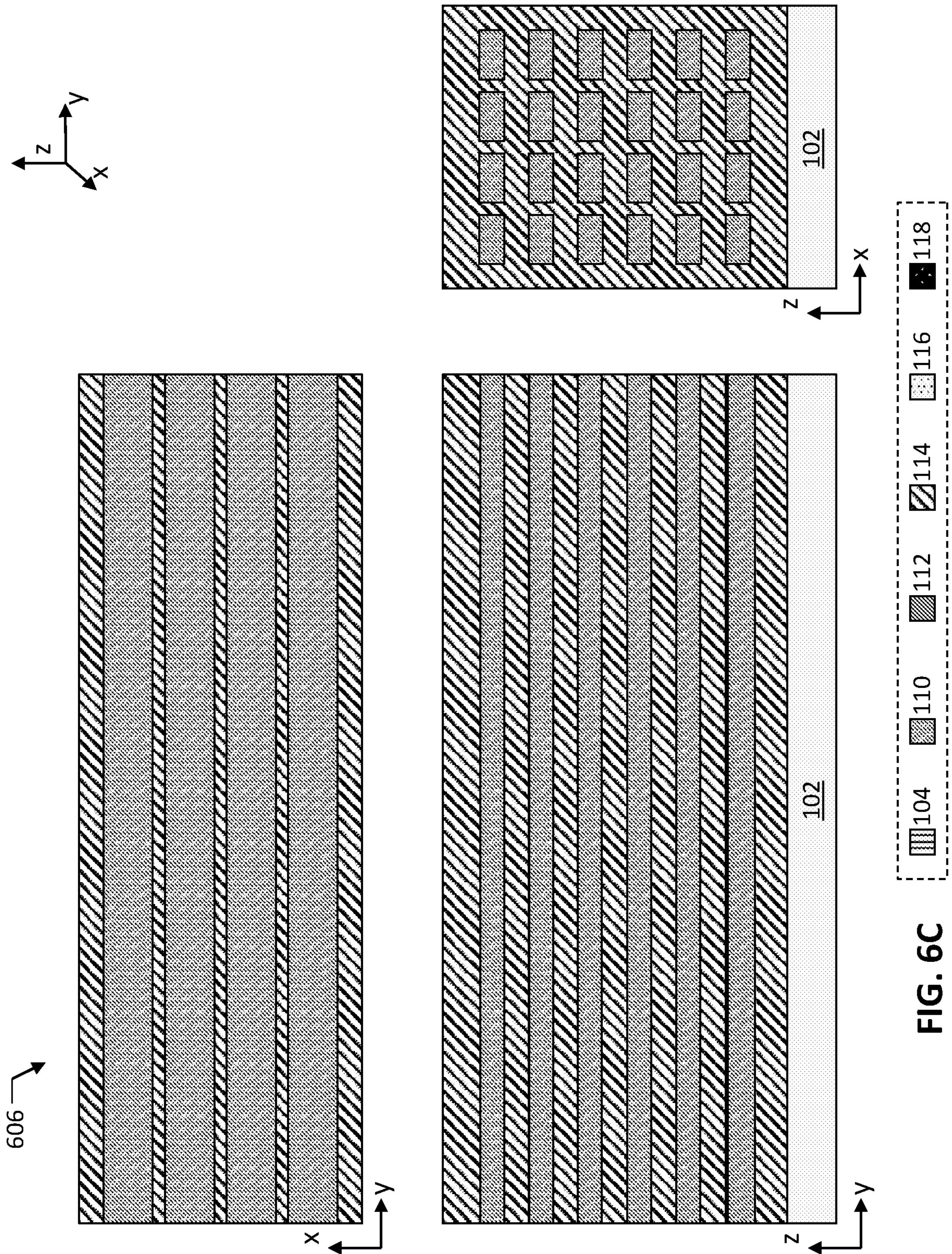

FIG. 6C

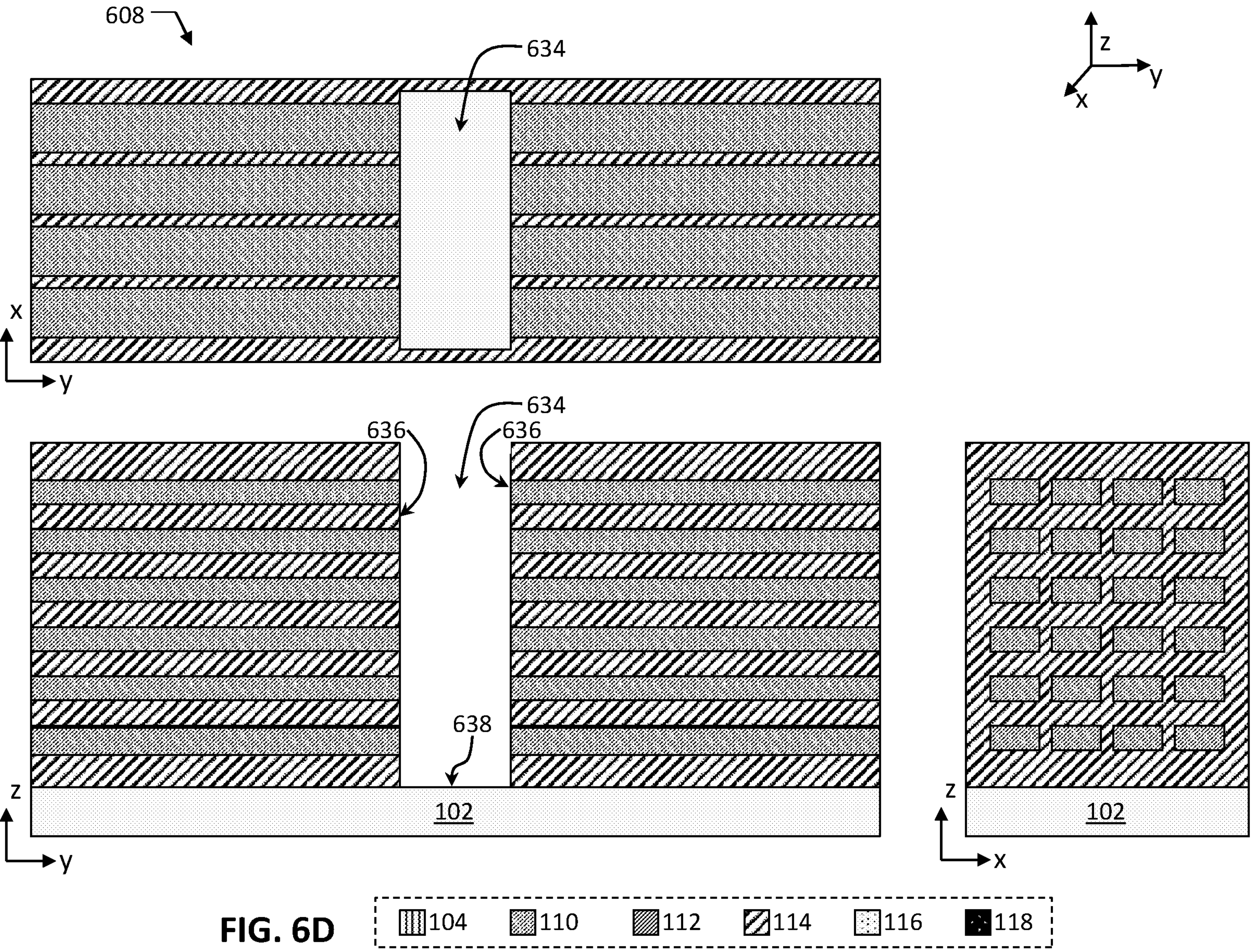

FIG. 6D

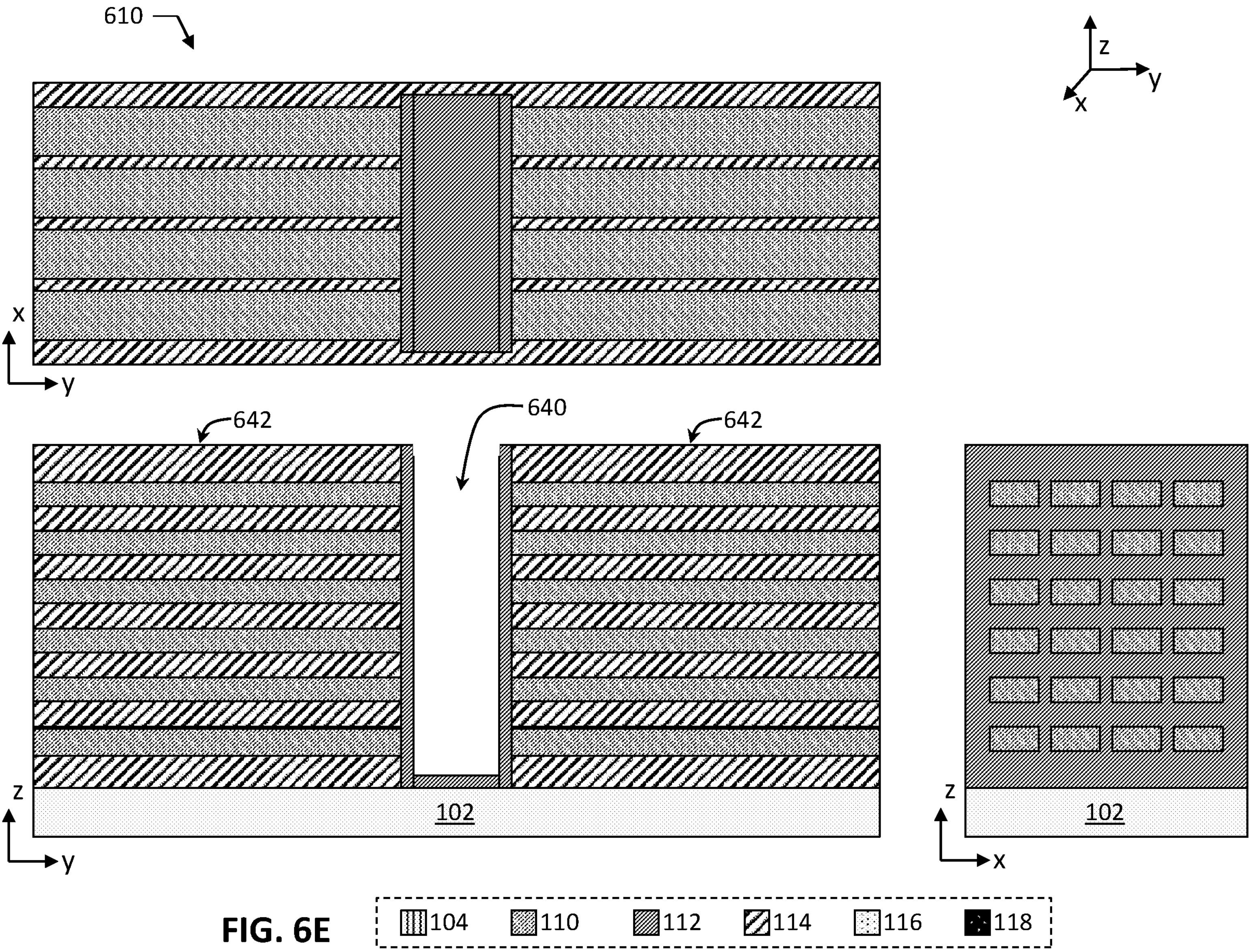

FIG. 6E

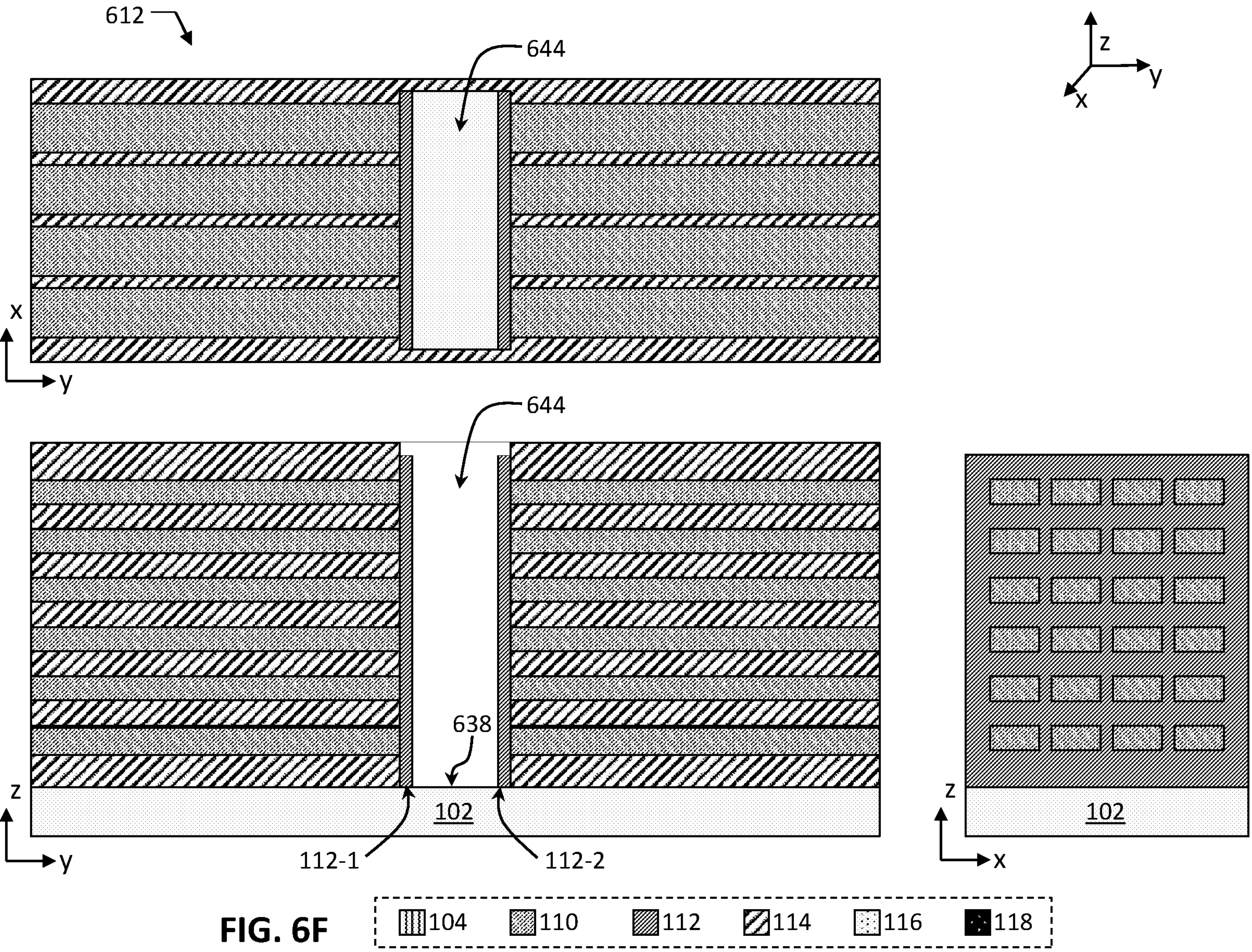

FIG. 6F

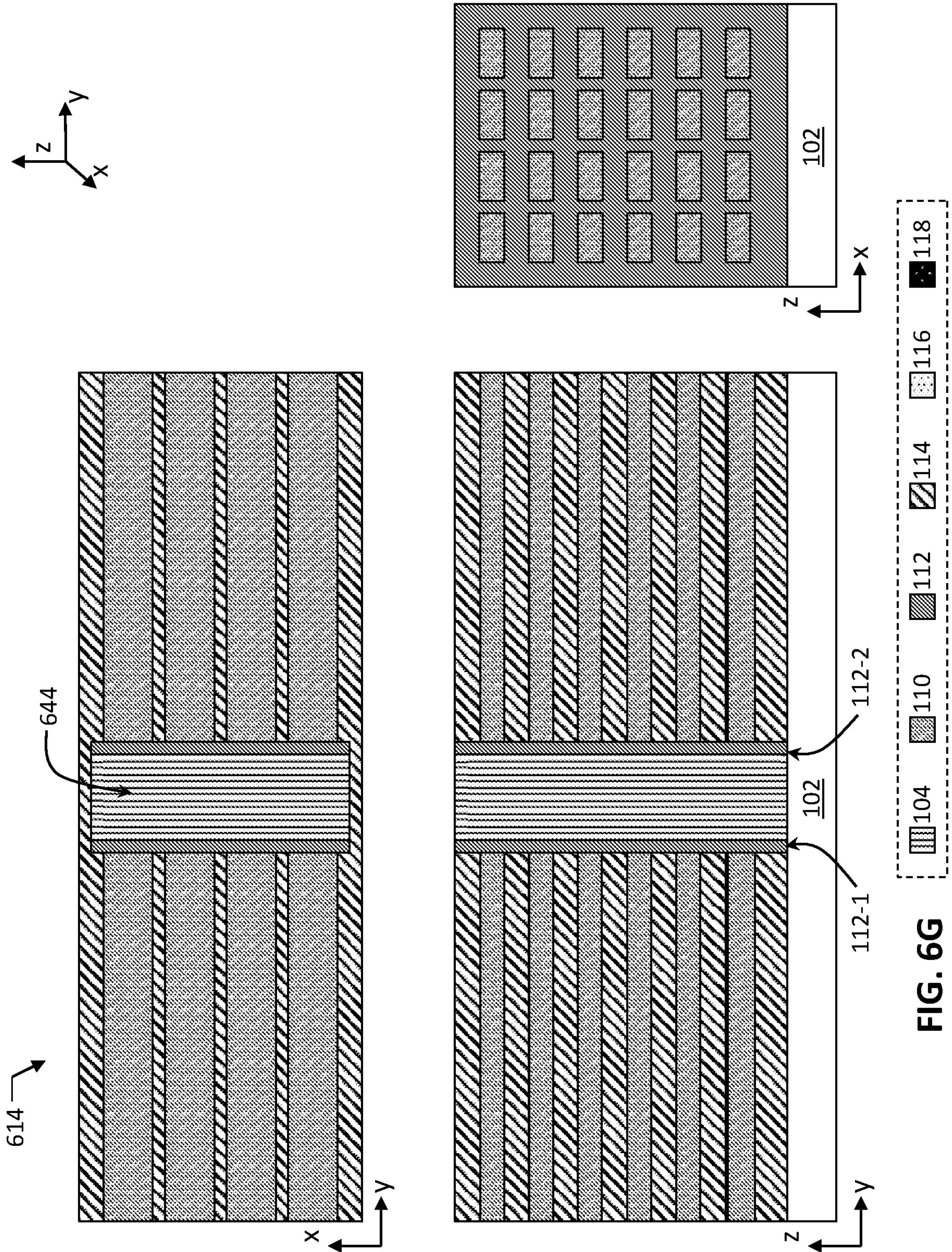

FIG. 6G

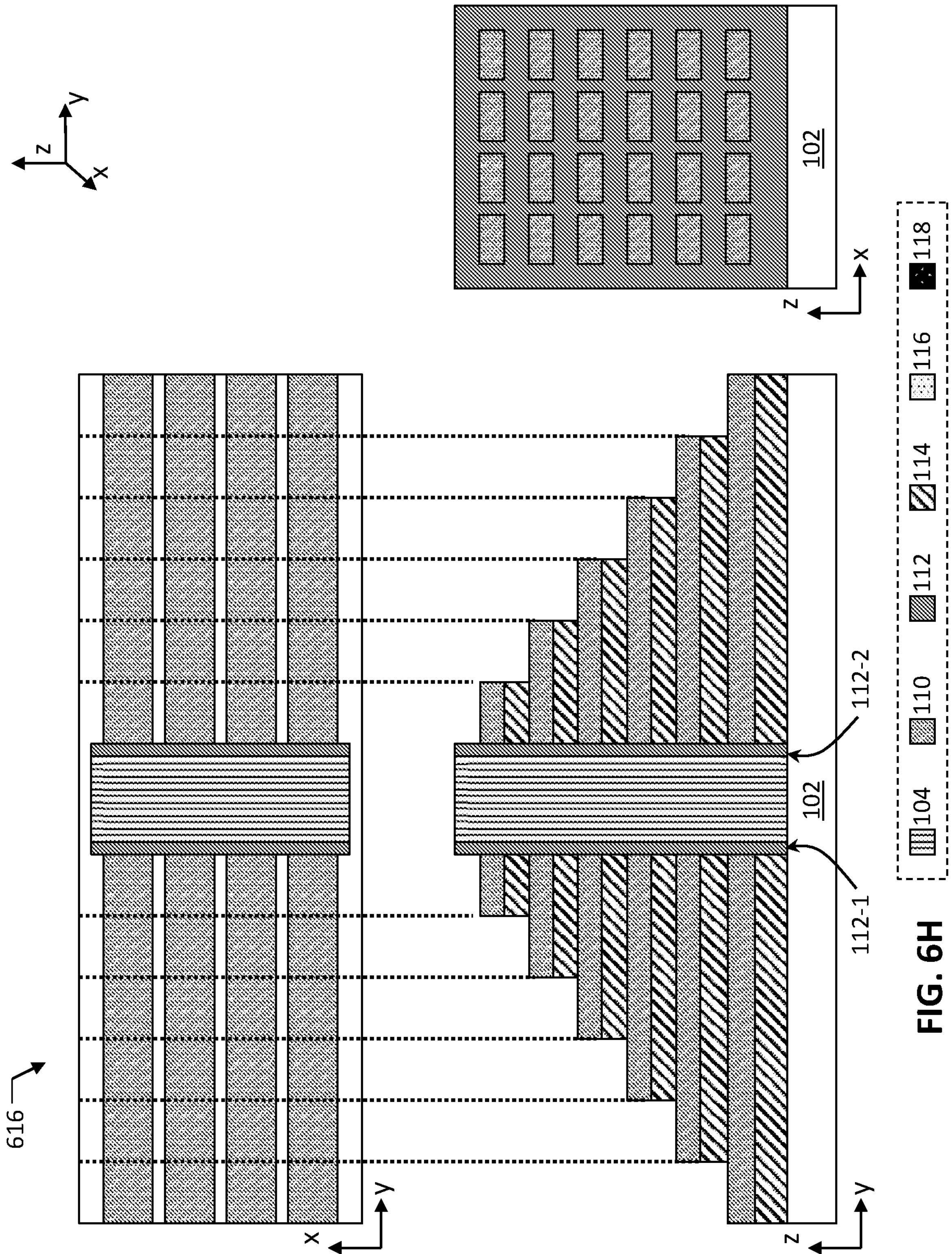

FIG. 6H

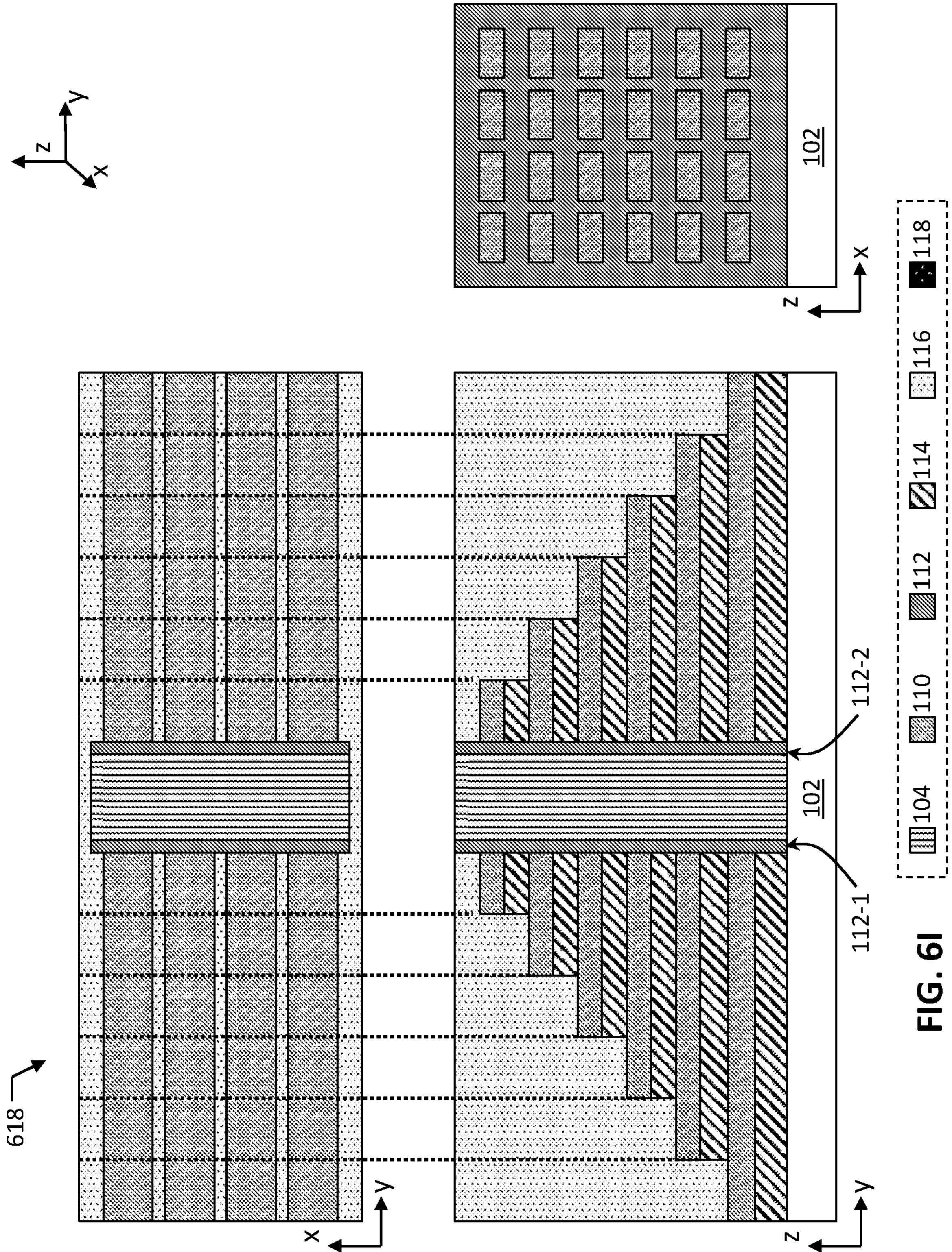

FIG. 6I

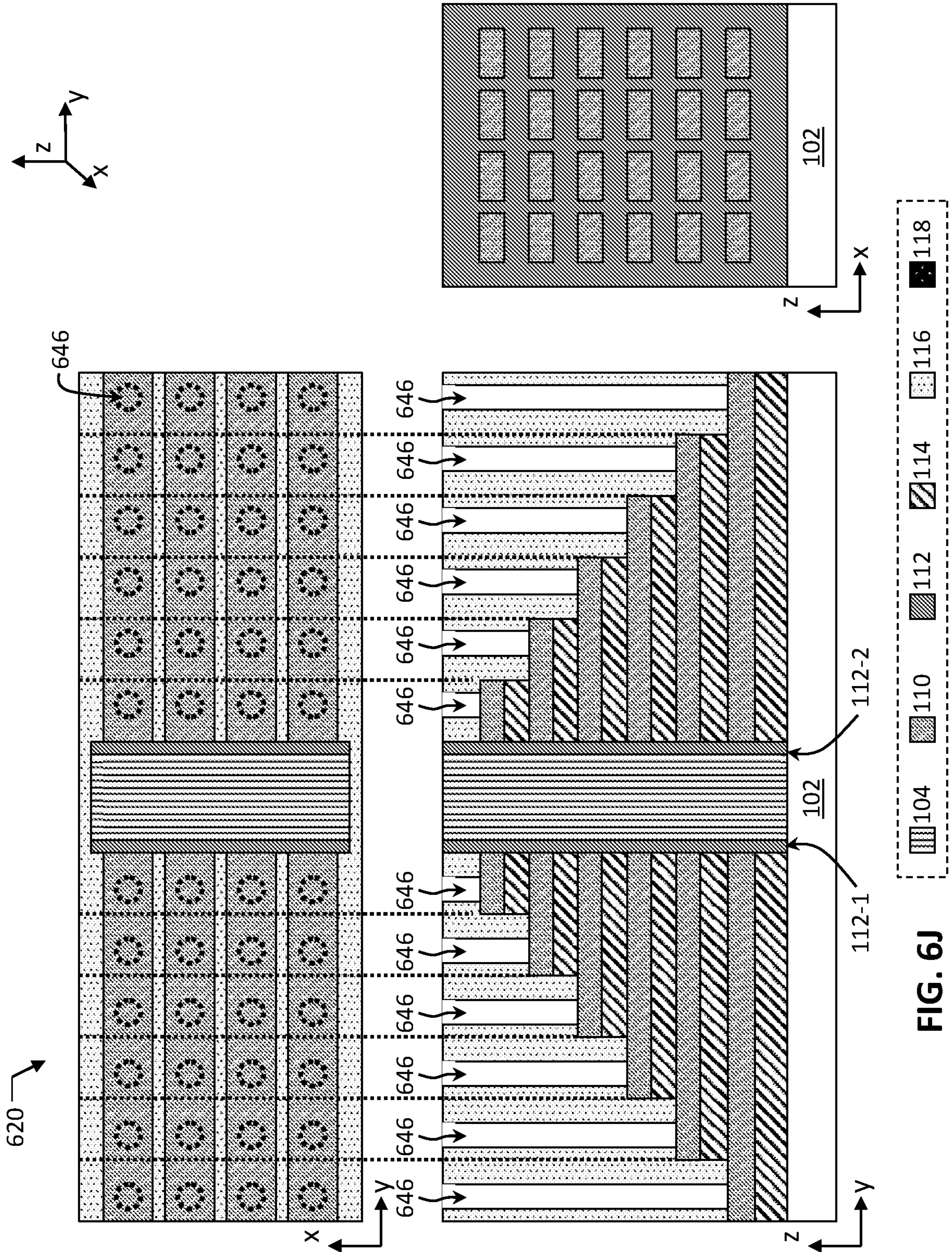

FIG. 6J

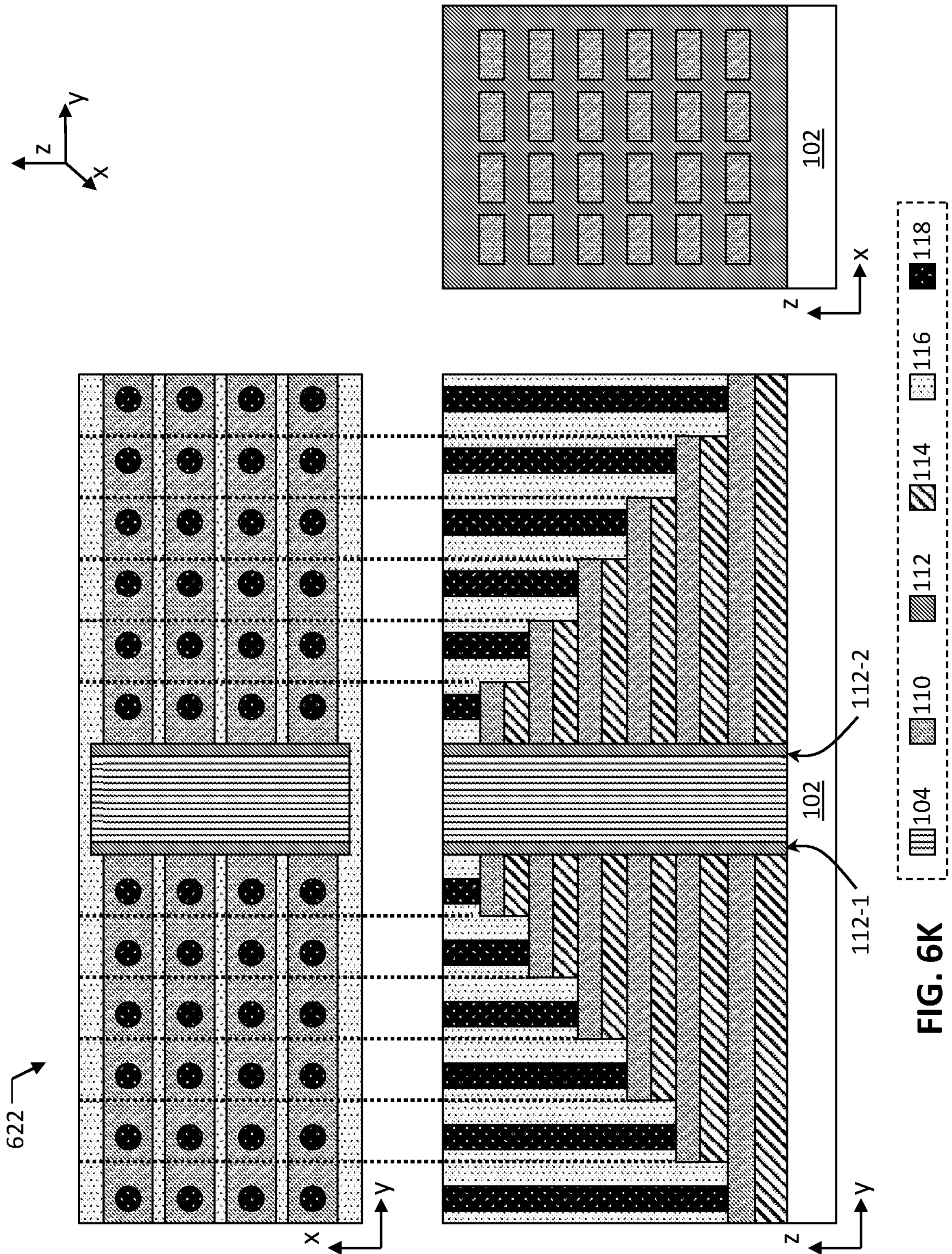

FIG. 6K

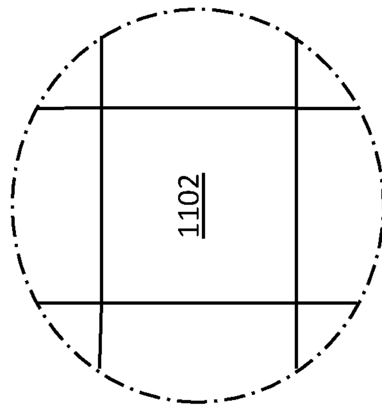

FIG. 7B

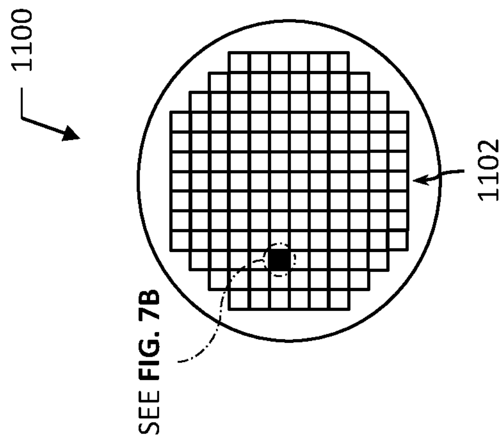

FIG. 7A

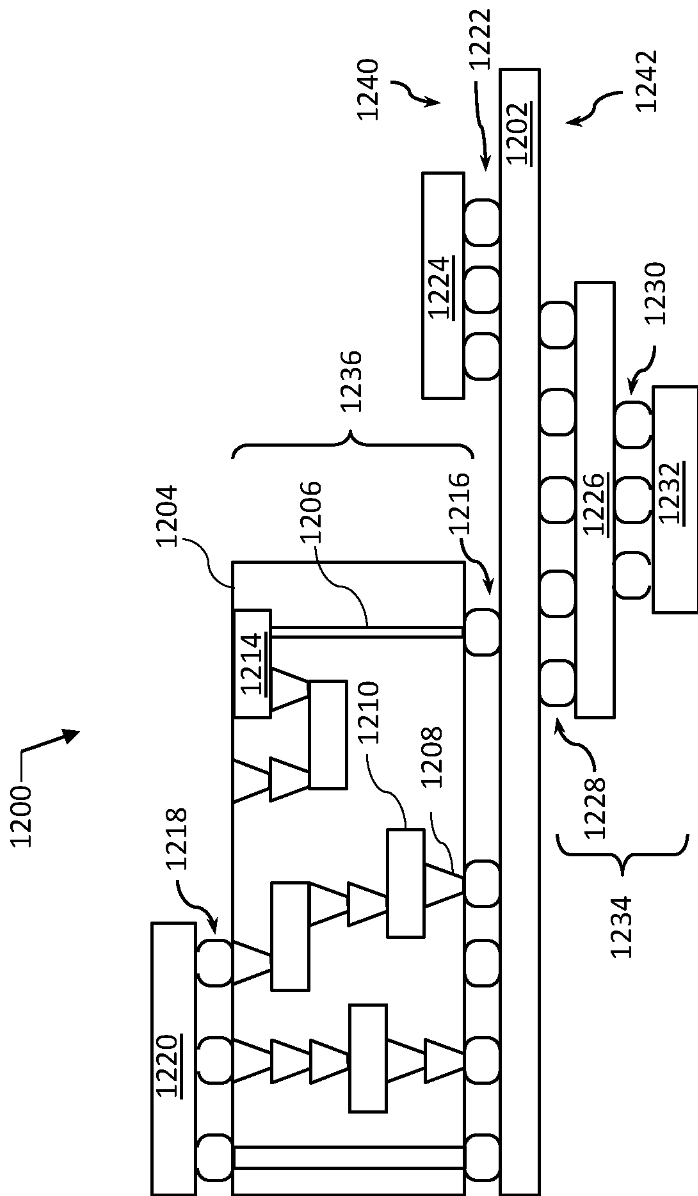

FIG. 8

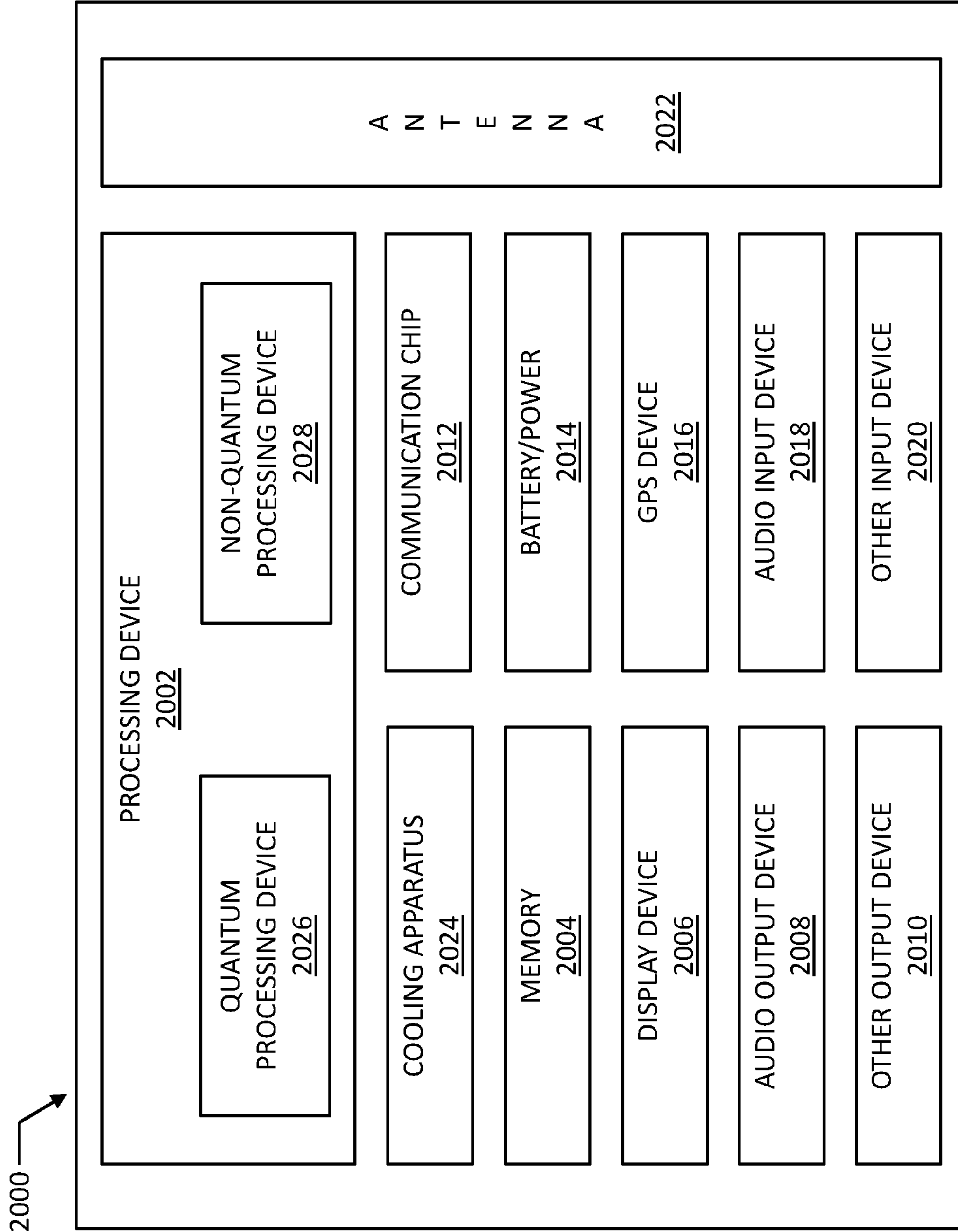

FIG. 9

INTERNATIONAL SEARCH REPORT	International application No. **PCT/US2017/066916**

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/15(2006.01)i, H01L 29/12(2006.01)i, H01L 29/66(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/15; H01L 21/20; G11C 16/02; H01L 29/06; G11C 16/34; H01L 33/12; H01L 29/775; H01L 29/66; H01L 33/04; H01L 27/10; H01L 29/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: quantum dot device, quantum well, gate, qubits, memory

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	WO 2017-020095 A1 (NEWSOUTH INNOVATIONS PTY LIMITED) 09 February 2017 See pages 11-15 and figures 1(a), 1(b).	1-25
A	US 2013-0221330 A1 (JUNG BUM CHOI et al.) 29 August 2013 See paragraphs [0099], [0100] and figure 13.	1-25
A	KR 10-2015-0134494 A (SAMSUNG ELECTRONICS CO., LTD.) 02 December 2015 See paragraphs [0031]-[0047] and figures 2-5.	1-25
A	KR 10-2016-0019037 A (CHANG YU CHEN) 18 February 2016 See paragraphs [0022]-[0025] and figure 1.	1-25

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 August 2018 (27.08.2018)	**27 August 2018 (27.08.2018)**

Name and mailing address of the ISA/KR

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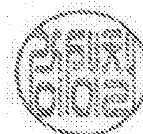
Authorized officer

KANG, Sung Chul



Telephone No. +82-42-481-8405

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
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