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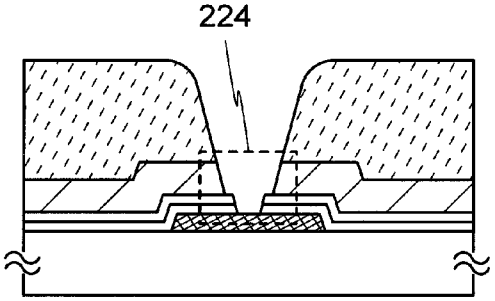
(54) **Title**: METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

FIG. 2B



(57) **Abstract**: An object is to provide a method for manufacturing a semiconductor device including an oxide semiconductor and having improved electric characteristics. The semiconductor device includes an oxide semiconductor film, a gate electrode overlapping the oxide semiconductor film, and a source electrode and a drain electrode electrically connected to the oxide semiconductor film. The method includes the steps of forming a first insulating film including gallium oxide over and in contact with the oxide semiconductor film; forming a second insulating film over and in contact with the first insulating film; forming a resist mask over the second insulating film; forming a contact hole by performing dry etching on the first insulating film and the second insulating film; removing the resist mask by ashing using oxygen plasma; and forming a wiring electrically connected to at least one of the gate electrode, the source electrode, and the drain electrode through the contact hole.

DESCRIPTION

METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device and a method for manufacturing the semiconductor device.

[0002]

In this specification, a semiconductor device generally means a device which can function by utilizing semiconductor characteristics, and electrooptic devices, semiconductor circuits, and electronic devices are all semiconductor devices.

BACKGROUND ART

[0003]

A technique by which a transistor is manufactured using a semiconductor thin film formed over a substrate having an insulating surface has been attracting attention. The transistor is applied to a wide range of electronic devices such as an integrated circuit (IC) or an image display device (a display device). A silicon-based semiconductor material is widely known as a material for a semiconductor thin film applicable to a transistor. As another material, an oxide semiconductor has been attracting attention.

[0004]

For example, a transistor whose semiconductor layer used for a channel formation region is formed using an amorphous oxide including indium (In), gallium (Ga), and zinc (Zn) and having an electron carrier concentration lower than 10^{18} /cm^3 is disclosed (see Patent Document 1).

[Reference]

[Patent Document]

[0005]

[Patent Document 1] Japanese Published Patent Application No. 2006-165528

DISCLOSURE OF INVENTION

[0006]

However, the electric conductivity of an oxide semiconductor might change when deviation from the stoichiometric composition ratio due to deficiency of oxygen or the like occurs, or when hydrogen or water behaving as electron donor enters the oxide semiconductor during a manufacturing process of a device. Such phenomena are factors of variation in electric characteristics of a semiconductor device such as a transistor including an oxide semiconductor.

[0007]

In view of the above problem, an object is to provide a method for manufacturing a semiconductor device including an oxide semiconductor and having improved electric characteristics.

[0008]

Another object is to solve a problem which may arise in the manufacture of the semiconductor device including an oxide semiconductor and having improved electric characteristics.

[0009]

In one embodiment of the present invention, an insulating film including a constituent element of an oxide semiconductor film (e.g., an insulating film including gallium oxide) is provided so as to be in contact with the oxide semiconductor film, and direct wet treatment is not used in an etching step of the insulating film, whereby a favorable condition is maintained at an interface between the oxide semiconductor film and the insulating film. More concretely, the following structure can be given as example.

[0010]

One embodiment of the disclosed invention is a method for manufacturing a semiconductor device including an oxide semiconductor film, a gate electrode, and a source electrode and a drain electrode that are electrically connected to the oxide semiconductor film. The method includes the steps of forming the oxide semiconductor film over the gate electrode; forming a first insulating film including gallium oxide over and in contact with the oxide semiconductor film, the source electrode, and the drain electrode; forming a second insulating film over and in contact

with the first insulating film; forming a resist mask over the second insulating film; forming a contact hole by performing dry etching on the first insulating film and the second insulating film; removing the resist mask by ashing using oxygen plasma; and forming a wiring electrically connected to at least one of the gate electrode, the source electrode, and the drain electrode through the contact hole.

[0011]

Another embodiment of the disclosed invention is a method for manufacturing a semiconductor device including an oxide semiconductor film, a gate electrode, and a source electrode and a drain electrode that are electrically connected to the oxide semiconductor film. The method includes the steps of forming a first insulating film including gallium oxide over and in contact with the oxide semiconductor film, the source electrode, and the drain electrode; forming the gate electrode over and in contact with the first insulating film to overlap with the oxide semiconductor film; forming a second insulating film over and in contact with the first insulating film; forming a resist mask over the second insulating film; forming a contact hole by performing dry etching on the first insulating film and the second insulating film; removing the resist mask by ashing using oxygen plasma; and forming a wiring electrically connected to at least one of the source electrode and the drain electrode through the contact hole.

[0012]

In the above structure, the diameter of the contact hole in the first insulating film is preferably smaller than the diameter of the contact hole in the second insulating film. The thickness of the second insulating film is preferably larger than the thickness of the first insulating film.

[0013]

Further, a gas including fluorine is preferably used in the dry etching.

[0014]

In the case where the first insulating film further includes aluminum oxide, a gas including chlorine is preferably used in the dry etching.

[0015]

In addition, it is preferable that the first insulating film be formed while applying heat.

[0016]

Further, the oxide semiconductor film is preferably an i-type oxide semiconductor film. Here, an i-type (intrinsic) oxide semiconductor refers to an oxide semiconductor which is highly purified by removing hydrogen, which is an n-type impurity for an oxide semiconductor, from the oxide semiconductor so that impurities that are not main components of the oxide semiconductor are included as few as possible, and in which oxygen deficiency defects are reduced by supplying oxygen. In an i-type oxide semiconductor film, hydrogen atoms serving as electron donors and defects due to oxygen deficiency are sufficiently reduced; therefore, degradation of the interface characteristics due to impurities and defects can be suppressed.

[0017]

Note that purification of an oxide semiconductor also has an effect of preventing variation in electric characteristics of a transistor. Therefore, purification of an oxide semiconductor is extremely effective for improvement in transistor characteristics.

[0018]

According to one embodiment of the present invention, a method for manufacturing a semiconductor device in which a favorable condition is maintained at an interface between an oxide semiconductor film and an insulating film can be provided. Thus, a method for manufacturing a semiconductor device having improved electric characteristics can be provided.

BRIEF DESCRIPTION OF DRAWINGS

[0019]

In the accompanying drawings:

FIGS. 1A to 1E illustrate an example of a manufacturing process of a semiconductor device;

FIGS. 2A to 2C illustrate an example of a manufacturing process of a semiconductor device;

FIGS. 3A to 3E illustrate an example of a manufacturing process of a semiconductor device;

FIGS. 4A, 4B1, and 4B2 illustrate discharge states in an AC sputtering method;

FIGS. 5A to 5C illustrate embodiments of a semiconductor device;

FIG. 6 illustrates one embodiment of a semiconductor device;

FIG. 7 illustrates one embodiment of a semiconductor device;

FIG. 8 illustrates one embodiment of a semiconductor device;

FIGS. 9A to 9F illustrate electronic devices;

FIGS. 10A and 10B are SEM images of samples according to Example 1; and

FIGS. 11A and 11B are SEM images of samples according to Example 1.

BEST MODE FOR CARRYING OUT THE INVENTION

[0020]

Hereinafter, embodiments and an example of the present invention will be described in detail with reference to the accompanying drawings. However, the present invention is not limited to the description below, and it is easily understood by those skilled in the art that modes and details disclosed herein can be modified in various ways. Therefore, the present invention is not construed as being limited to description of the embodiments. Note that in the following description, portions that are common between drawings are denoted by the same reference numerals, and repeated description is omitted.

[0021]

Note that in this specification the ordinal numbers such as "first" and "second" are used for convenience and do not denote the order of steps or the stacking order of layers. In addition, the ordinal numbers in this specification do not denote particular names which specify the invention.

[0022]

(Embodiment 1)

In this embodiment, one embodiment of a semiconductor device and one embodiment of a method for manufacturing the semiconductor device will be described with reference to FIGS. 1A to 1E, FIGS. 2A to 2C, FIGS. 3A to 3E, and FIGS. 4A, 4B1, and 4B2.

[0023]

<Manufacturing Process of Transistor 110>

FIGS. 1A to 1E are cross-sectional views illustrating a manufacturing process of a transistor 110 as an example of a method for manufacturing a semiconductor device

according to one embodiment of the disclosed invention. Here, the transistor 110 includes, over a substrate 200, a gate electrode 202, an insulating film 204, an oxide semiconductor film 206, a source electrode 208a, a drain electrode 208b, an insulating film 210, an insulating film 212, and a wiring 216. In the transistor illustrated in FIG. 1E, the insulating film 210, including gallium oxide, is provided in contact with the oxide semiconductor film 206, and the insulating film 212 is provided over and in contact with the insulating film 210 including gallium oxide. In addition, the wiring 216 is electrically connected to the source electrode 208a through a contact hole 218 formed in the insulating film 212 and the insulating film 210.

[0024]

Here, the oxide semiconductor film 206 is preferably an oxide semiconductor film which is highly purified by sufficiently removing impurities such as hydrogen or water, or by sufficiently supplying oxygen. Specifically, the hydrogen concentration of the oxide semiconductor film 206 is 5×10^{19} atoms/cm^3 or lower, preferably 5×10^{18} atoms/cm^3 or lower, further preferably 5×10^{17} atoms/cm^3 or lower, for example. Note that the hydrogen concentration of the oxide semiconductor film 206 is measured by secondary ion mass spectrometry (SIMS). In the oxide semiconductor film 206 which is highly purified by sufficiently reducing the hydrogen concentration and in which defect levels in the energy gap due to oxygen deficiency are reduced by sufficiently supplying oxygen, the carrier concentration is lower than 1×10^{12} /cm^3, preferably lower than 1×10^{11} /cm^3, further preferably lower than 1.45×10^{10} /cm^3. For example, the off-state current (here, current per micrometer (μm) of channel width) at room temperature (25 °C) is lower than or equal to 100 zA (1 zA (zeptoampere) is 1×10^{-21} A), preferably lower than or equal to 10 zA. In this manner, by using an i-type oxide semiconductor, a transistor having favorable electric characteristics can be obtained.

[0025]

In many cases, an oxide semiconductor material used for the oxide semiconductor film 206 includes gallium. Therefore, when the insulating film 204 or the insulating film 210, which is in contact with the oxide semiconductor film, is formed using a material including gallium oxide, a favorable condition can be maintained at an interface between the oxide semiconductor film and the insulating film.

For example, by providing the oxide semiconductor film in contact with the insulating film including gallium oxide, an accumulation of hydrogen at an interface between the oxide semiconductor film and the insulating film can be reduced. This is because a material including gallium oxide is compatible with an oxide semiconductor material.

[0026]

Note that, in the case where an element belonging to the same group as a constituent element of the oxide semiconductor is used for the insulating film 204 or the insulating film 210, a similar effect can be obtained. That is, it is also effective to additionally use a material including aluminum oxide or the like for the insulating film 204 or the insulating film 210. Aluminum oxide tends to resist to water penetration; therefore, it is preferable to use a material including aluminum oxide in the optic of preventing water from entering the oxide semiconductor film. For example, a material including gallium and aluminum, such as aluminum gallium oxide (or gallium aluminum oxide) may be used for the insulating film 204 or the insulating film 210. In this case, both the effect resulting from inclusion of gallium and the effect resulting from inclusion of aluminum can be obtained, which is preferable. By providing the oxide semiconductor film in contact with an insulating film including aluminum gallium oxide, for example, water can be prevented from entering the oxide semiconductor film and an accumulation of hydrogen at an interface between the oxide semiconductor film and the insulating film can be sufficiently reduced.

[0027]

An example of the manufacturing process of the transistor 110 illustrated in FIG. 1E will be described below with reference to FIGS. 1A to 1E.

[0028]

First, a conductive film for forming the gate electrode (including a wiring formed in the same layer as the gate electrode) is formed over the substrate 200 and then processed, so that the gate electrode 202 is formed. After that, the insulating film 204 is formed so as to cover the gate electrode 202 (see FIG. 1A).

[0029]

There is no particular limitation on the material or the like of the substrate 200 as long as the material has heat resistance enough to withstand at least heat treatment performed later. For example, a glass substrate, a ceramic substrate, a quartz substrate,

a sapphire substrate, or the like can be used as the substrate 200. Alternatively, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon, silicon carbide, or the like, a compound semiconductor substrate made of silicon germanium or the like, an SOI substrate, or the like can be used. Further alternatively, any of these substrates provided with a semiconductor element may be used as the substrate 200.

[0030]

A flexible substrate may be used as the substrate 200. In the case where a transistor is provided over a flexible substrate, for example, the transistor can be directly formed over the flexible substrate.

[0031]

As the conductive film used for the gate electrode 202, for example, a metal film including an element selected from molybdenum, titanium, tantalum, tungsten, aluminum, copper, neodymium, and scandium; an alloy material including any of these elements as a main component; or the like can be used. The gate electrode 202 may have a single-layer structure or a stacked-layer structure.

[0032]

The conductive film can be processed by being etched after a mask having a desired shape is formed over the conductive film. As the above mask, a resist mask or the like can be used.

[0033]

The insulating film 204 functions as a gate insulating film of the transistor 110. The insulating film 204 is formed using, for example, a material such as silicon oxide, silicon nitride, silicon oxynitride, or silicon nitride oxide. Further, the insulating film 204 can be formed using a material including gallium oxide. The material including gallium oxide may further include aluminum oxide; that is, a material including aluminum gallium oxide or gallium aluminum oxide, or the like may be used. Here, aluminum gallium oxide refers to a substance that includes aluminum at a content (atomic%) higher than that of gallium, and gallium aluminum oxide refers to a substance that includes gallium at a content (atomic%) higher than or equal to that of aluminum. A material having a high dielectric constant, such as hafnium oxide,

tantalum oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)) to which nitrogen is added, or hafnium aluminate ($HfAl_xO_y$ ($x > 0$, $y > 0$)) to which nitrogen is added may be used. The insulating film 204 can be formed to have a single-layer structure or a stacked-layer structure using any of the above materials.

[0034]

A gallium oxide film used as the insulating film 204 preferably has a composition of $Ga_2O_{3+\alpha}$ ($\alpha > 0$). It is preferable that α be greater than or equal to 3.04 and less than or equal to 3.09. Alternatively, an aluminum gallium oxide film used as the insulating film 204 preferably has a composition of $Al_xGa_{2-x}O_{3+\alpha}$ ($1 < x < 2$, $\alpha > 0$). Further alternatively, a gallium aluminum oxide film used as the insulating film 204 preferably has a composition of $Al_xGa_{2-x}O_{3+\alpha}$ ($0 < x \leq 1$, $\alpha > 0$) by being doped with oxygen.

[0035]

In many cases, an oxide semiconductor material used for the oxide semiconductor film includes gallium. Therefore, in the case where the insulating film 204 which is in contact with the oxide semiconductor film is formed using a material including gallium oxide, a favorable condition can be maintained at an interface between the oxide semiconductor film and the insulating film 204. For example, by providing the oxide semiconductor film in contact with an insulating film including gallium oxide, an accumulation of hydrogen at an interface between the oxide semiconductor film and the insulating film can be reduced. This is because a material including gallium oxide is compatible with an oxide semiconductor material.

[0036]

Note that, in the case where an element belonging to the same group as a constituent element of the oxide semiconductor is used for the insulating film 204, a similar effect can be obtained. That is, it is also effective to additionally use a material including aluminum oxide or the like for the insulating film 204. Aluminum oxide tends to resist to water penetration; therefore, it is preferable to use the material including aluminum oxide in the optic of preventing water from entering the oxide semiconductor film. For example, a material including gallium and aluminum, such as

aluminum gallium oxide (or gallium aluminum oxide) described above may be used for the insulating film 204. In this case, both the effect resulting from inclusion of gallium and the effect resulting from inclusion of aluminum can be obtained, which is preferable. By providing the oxide semiconductor film in contact with an insulating film including aluminum gallium oxide, for example, water can be prevented from entering the oxide semiconductor film and an accumulation of hydrogen at an interface between the oxide semiconductor film and the insulating film can be sufficiently reduced.

[0037]

The insulating film 204 is preferably formed by a method with which impurities such as hydrogen or water do not enter the insulating film 204. This is because, when impurities such as hydrogen or water are included in the insulating film 204, the impurities such as hydrogen or water enter the oxide semiconductor film formed later or oxygen in the oxide semiconductor film is extracted by the impurities such as hydrogen or water, so that a back channel of the oxide semiconductor film might have lower resistance (have n-type conductivity) and a parasitic channel might be formed. Therefore, the insulating film 204 is preferably formed so as to include impurities such as hydrogen or water as few as possible. For example, the insulating film 204 is preferably formed by a sputtering method, and a high-purity gas from which impurities such as hydrogen or water are removed is preferably used as a sputtering gas used for film formation.

[0038]

Examples of the sputtering method include a DC sputtering method in which a direct current power source is used, a pulsed DC sputtering method in which a direct bias is applied in a pulsed manner, an AC sputtering method, and the like.

[0039]

Here, a sputtering method using AC discharge will be described with reference to FIGS. 4A, 4B1, and 4B2. In AC discharge, adjacent targets alternately have a cathode potential and an anode potential. In a period A shown in FIG. 4A, a target 301 functions as a cathode and a target 302 functions as an anode as illustrated in FIG. 4B1. In a period B shown in FIG. 4A, the target 301 functions as an anode and the target 302 functions as a cathode as illustrated in FIG. 4B2. The total time of the period A and the period B is 20 μsec to 50 μsec, and the period A and the period B are repeated at a

constant frequency. In this manner, by making the two adjacent targets function as a cathode and as an anode alternately, stable discharge can be realized. As a result, even when a large-sized substrate is used, uniform discharge is possible; accordingly, uniform film characteristics can be obtained also in the case of using the large-sized substrate. Moreover, since the large-sized substrate can be used, productivity can be increased.

[0040]

For example, in the AC sputtering method, aluminum oxide is used as the target 301 and gallium oxide is used as the target 302, whereby a gallium aluminum oxide film or an aluminum gallium oxide film can be formed. As the target 301 and the target 302, a gallium oxide target to which aluminum particles are added may be used. By using a gallium oxide target to which an aluminum element is added, conductivity of the target can be increased and discharge can be easily performed during the AC sputtering.

[0041]

Next, oxygen doping treatment is preferably performed on the insulating film 204. Oxygen doping refers to addition of oxygen (which includes at least one of an oxygen radical, an oxygen atom, and an oxygen ion) to a bulk. Note that the term "bulk" is used in order to clarify that oxygen is added not only to a surface of a thin film but also to the inside of the thin film. In addition, the oxygen doping includes oxygen plasma doping in which oxygen that is made to be plasma is added to a bulk.

[0042]

When the oxygen doping treatment is performed on the insulating film 204, a region where the amount of oxygen is larger than that in the stoichiometric composition ratio is formed in the insulating film 204. By providing such a region, oxygen can be supplied to the oxide semiconductor film and oxygen deficiency defects in the oxide semiconductor film can be reduced.

[0043]

Note that in the case where an oxide semiconductor without defects (oxygen deficiency) is used, the amount of oxygen included in the insulating film 204 may be equal to that in the stoichiometric composition. However, in order to ensure reliability, for example, to suppress variation in the threshold voltage of the transistor, the insulating film 204 preferably includes oxygen at an amount which is larger than that in

the stoichiometric composition, in consideration of oxygen deficiency that may occur in the oxide semiconductor film.

[0044]

In this manner, the oxygen doping treatment makes it easy to obtain a gallium oxide film having a composition of $Ga_2O_{3+\alpha}$ ($\alpha > 0$), which can be used as the insulating film 204, and to set α to be greater than or equal to 3.04 and less than or equal to 3.09. Alternatively, the oxygen doping treatment makes it easy to obtain an aluminum gallium oxide film having a composition of $Al_xGa_{2-x}O_{3+\alpha}$ ($1 < x < 2$, $\alpha > 0$), which can be used as the insulating film 204. Further alternatively, the oxygen doping treatment makes it easy to obtain a gallium aluminum oxide film having a composition of $Al_xGa_{2-x}O_{3+\alpha}$ ($0 < x \leq 1$, $\alpha > 0$), which can be used as the insulating film 204.

[0045]

Next, an oxide semiconductor film is formed over the insulating film 204 and then processed, so that the oxide semiconductor film 206 having an island shape is formed (see FIG. 1B).

[0046]

As a material used for the oxide semiconductor film 206, a four-component metal oxide such as an In-Sn-Ga-Zn-O-based material; a three-component metal oxide such as an In-Ga-Zn-O-based material, an In-Sn-Zn-O-based material, an In-Al-Zn-O-based material, a Sn-Ga-Zn-O-based material, an Al-Ga-Zn-O-based material, or a Sn-Al-Zn-O-based material; a two-component metal oxide such as an In-Zn-O-based material, a Sn-Zn-O-based material, an Al-Zn-O-based material, a Zn-Mg-O-based material, a Sn-Mg-O-based material, an In-Mg-O-based material, or an In-Ga-O-based material; a single-component metal oxide such as an In-O-based material, a Sn-O-based material, or a Zn-O-based material, or the like can be used. In addition, the above materials may include SiO_2. Here, for example, an In-Ga-Zn-O-based material means an oxide film including indium (In), gallium (Ga), and zinc (Zn), and there is no particular limitation on the composition ratio thereof. Further, the In-Ga-Zn-O-based material may include an element other than In, Ga, and Zn.

[0047]

The oxide semiconductor film 206 can be a thin film formed using a material expressed by the chemical formula, $InMO_3(ZnO)_m$ ($m > 0$). Here, M represents one or more metal elements selected from Ga, Al, Mn, and Co. For example, M can be Ga, Ga and Al, Ga and Mn, Ga and Co, or the like.

[0048]

The thickness of the oxide semiconductor film 206 is preferably greater than or equal to 3 nm and less than or equal to 30 nm. This is because the transistor might be normally on when the oxide semiconductor film 206 is too thick (e.g., the thickness is 50 nm or more).

[0049]

It is preferable to form the oxide semiconductor film by a method with which impurities such as hydrogen, water, hydroxyl group, or hydride do not easily enter the oxide semiconductor film. For example, a sputtering method or the like can be used.

[0050]

In this embodiment, the oxide semiconductor film is formed by a sputtering method using an In-Ga-Zn-O-based oxide target.

[0051]

As the In-Ga-Zn-O-based oxide target, for example, an oxide target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:1 [molar ratio] can be used. Note that it is not necessary to limit the material and the composition ratio of the target to the above. For example, an oxide target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:2 [molar ratio] can be used.

[0052]

In the case where an In-Zn-O-based material is used as the oxide semiconductor, a target to be used has a composition ratio of In:Zn = 50:1 to 1:2 in atomic ratio (In_2O_3:ZnO = 25:1 to 1:4 in a molar ratio), preferably In:Zn = 20:1 to 1:1 in atomic ratio (In_2O_3:ZnO = 10:1 to 1:2 in molar ratio), further preferably In:Zn = 15:1 to 1.5:1 in atomic ratio (In_2O_3:ZnO = 15:2 to 3:4 in molar ratio). For example, in a target used for formation of an In-Zn-O-based oxide semiconductor which has an atomic ratio of In:Zn:O = X:Y:Z, the relation of $Z > 1.5X+Y$ is satisfied.

[0053]

The filling rate of the oxide target is higher than or equal to 90 % and lower than or equal to 100 %, preferably higher than or equal to 95 % and lower than or equal to 99.9 %. With the use of the metal oxide target with a high filling rate, a dense oxide semiconductor film can be formed.

[0054]

The atmosphere for film formation may be a rare gas (typically argon) atmosphere, an oxygen atmosphere, a mixed atmosphere of a rare gas and oxygen, or the like. Further, in order to prevent impurities such as hydrogen or water from entering the oxide semiconductor film, it is preferable to use an atmosphere of a high-purity gas from which impurities such as hydrogen or water are sufficiently removed.

[0055]

For example, the oxide semiconductor film can be formed as follows.

[0056]

First, the substrate 200 is held in a deposition chamber kept under reduced pressure, and heating is performed so that the substrate temperature becomes higher than 200 °C and lower than or equal to 500 °C, preferably higher than 300 °C and lower than or equal to 500 °C, further preferably higher than or equal to 350 °C and lower than or equal to 450 °C.

[0057]

Next, a high-purity gas from which impurities such as hydrogen or water are sufficiently removed is introduced into the deposition chamber while moisture remaining therein is being removed, and the oxide semiconductor film is formed over the insulating film 204 with the use of the target. In order to remove moisture remaining in the deposition chamber, an entrapment vacuum pump such as a cryopump, an ion pump, or a titanium sublimation pump is preferably used as an evacuation unit. The evacuation unit may be a turbo pump provided with a cold trap. In the deposition chamber which is evacuated with the cryopump, for example, impurities such as hydrogen or water (preferably, also a compound including a carbon atom), and the like are removed, so that the concentration of an impurity such as hydrogen or water included in the oxide semiconductor film formed in the deposition chamber can be

reduced.

[0058]

When the substrate temperature during film formation is low (e.g., lower than or equal to 100 °C), impurities such as hydrogen or water might enter the oxide semiconductor film; therefore, the substrate 200 is preferably heated as specified above. The substrate 200 is heated as specified above and the oxide semiconductor film is formed. When the oxide semiconductor film is formed with the substrate 200 heated as specified above, the substrate temperature is high, so that hydrogen bonds are cut by heat and hydrogen is less likely to be introduced into the oxide semiconductor film. Therefore, by forming the oxide semiconductor film with the substrate 200 heated as specified above, the concentration of impurities such as hydrogen or water in the oxide semiconductor film can be sufficiently reduced. Moreover, damage due to sputtering can be reduced.

[0059]

Note that, as a method for measuring the amount of water in the oxide semiconductor film, thermal desorption spectroscopy (TDS) is given. For example, when the temperature is increased from room temperature to approximately 400 °C, elimination of water, hydrogen, hydroxyl group, and the like in the oxide semiconductor film can be observed in the range of 200 °C to 300 °C approximately.

[0060]

As an example of film formation conditions, the following conditions are employed: the distance between the substrate and the target is 60 mm; the pressure is 0.4 Pa; the direct-current (DC) power is 0.5 kW; the substrate temperature is 400 °C; and the deposition atmosphere is an oxygen atmosphere (the proportion of the oxygen flow rate is 100 %). Note that a pulsed direct-current power source is preferably used because powder substances (also referred to as particles or dust) generated in the film formation can be reduced and the film thickness can be uniform.

[0061]

Note that before the oxide semiconductor film is formed by a sputtering method, powder substances (also referred to as particles or dust) which are attached to a surface of the insulating film 204 are preferably removed by reverse sputtering in which

an argon gas is introduced and plasma is generated. The reverse sputtering refers to a method in which voltage is applied to a substrate to generate plasma in the vicinity of the substrate so that a surface on the substrate side is modified. Note that instead of argon, a gas of nitrogen, helium, oxygen, or the like may be used.

[0062]

The oxide semiconductor film can be processed by being etched after a mask having a desired shape is formed over the oxide semiconductor film. The above mask can be formed by a method such as photolithography. Alternatively, a method such as an inkjet method may be used to form the mask. For the etching of the oxide semiconductor film, either dry etching or wet etching may be employed. Needless to say, both of them may be employed in combination.

[0063]

The oxide semiconductor film 206 formed in such a manner may be subjected to heat treatment (first heat treatment). The heat treatment further removes impurities such as hydrogen or water included in the oxide semiconductor film 206; thus, the structure of the oxide semiconductor film 206 can be improved and defect levels in the energy gap can be reduced.

[0064]

The heat treatment is performed in an inert gas atmosphere at higher than or equal to 250 °C and lower than or equal to 700 °C, preferably higher than or equal to 450 °C and lower than or equal to 600 °C or lower than a strain point of the substrate. The inert gas atmosphere is preferably an atmosphere which includes nitrogen or a rare gas (such as helium, neon, or argon) as a main component and does not include impurities such as hydrogen or water. For example, the purity of nitrogen or a rare gas such as helium, neon, or argon introduced into a heat treatment apparatus can be higher than or equal to 6N (99.9999 %), preferably higher than or equal to 7N (99.99999 %) (i.e., the impurity concentration is lower than or equal to 1 ppm, preferably lower than or equal to 0.1 ppm).

[0065]

The heat treatment can be performed in such a manner that, for example, an object to be heated is introduced into an electric furnace in which a resistance heating

element or the like is used and heated at 450 °C for one hour in a nitrogen atmosphere. The oxide semiconductor film 206 is not exposed to the air during the heat treatment so that entry of impurities such as hydrogen or water can be prevented.

[0066]

The above heat treatment can also be referred to as dehydration treatment, dehydrogenation treatment, or the like because of its effect of removing impurities such as hydrogen or water. The heat treatment can be performed at the timing, for example, after the oxide semiconductor film is formed. Such dehydration treatment or dehydrogenation treatment may be conducted once or plural times.

[0067]

Next, treatment for supplying oxygen (also referred to as oxygen doping treatment, or the like) is preferably performed on the oxide semiconductor film 206. As the treatment for supplying oxygen, heat treatment in an oxygen atmosphere (second heat treatment), treatment using oxygen plasma, and the like are given. Alternatively, oxygen may be added by performing irradiation with an oxygen ion accelerated by an electric field.

[0068]

Note that an electric bias may be applied to the substrate in order to add oxygen more favorably.

[0069]

By performing the oxygen doping treatment on the oxide semiconductor film 206, oxygen can be included in the oxide semiconductor film 206 or/and in the vicinity of the interface of the oxide semiconductor film 206. In that case, the amount of oxygen is preferably larger than that in the stoichiometric composition ratio of the oxide semiconductor film.

[0070]

Note that, heat treatment may be performed on the oxide semiconductor film 206 which has been subjected to the oxygen doping treatment. The heat treatment is performed at higher than or equal to 250 °C and lower than or equal to 700 °C, preferably higher than or equal to 400 °C and lower than or equal to 600 °C or lower than the strain point of the substrate.

[0071]

Through the heat treatment, water, hydroxide (OH), and the like generated by reaction between oxygen and an oxide semiconductor material can be removed from the oxide semiconductor film. By this heat treatment, hydrogen or the like that has entered the oxide semiconductor film 206 or the like during the above oxygen doping treatment can also be removed. The heat treatment may be performed in an atmosphere of nitrogen, oxygen, ultra-dry air (air where the moisture content is 20 ppm (−55 °C by conversion into a dew point) or less, preferably 1 ppm or less, further preferably 10 ppb or less when measurement is performed using a dew-point meter of a cavity ring down laser spectroscopy (CRDS) system), a rare gas (such as argon or helium), or the like in which water, hydrogen, and the like are sufficiently reduced. In particular, the heat treatment is preferably performed in an atmosphere including oxygen. Further, the purity of nitrogen, oxygen, or a rare gas introduced into a heat treatment apparatus is preferably higher than or equal to 6N (99.9999 %) (i.e., the impurity concentration is lower than or equal to 1 ppm), further preferably higher than or equal to 7N (99.99999 %) (i.e., the impurity concentration is lower than or equal to 0.1 ppm).

[0072]

Note that the timing of the oxygen doping treatment is not limited to the timing described above. However, the oxygen doping treatment is preferably performed after the heat treatment for dehydration or the like.

[0073]

As described above, the heat treatment for dehydration or the like, and the oxygen doping treatment or the heat treatment for supply of oxygen are performed, whereby the oxide semiconductor film 206 can be highly purified so as to include elements (impurity elements) that are not main components of the oxide semiconductor film 206 as few as possible. The highly purified oxide semiconductor film 206 includes extremely few carriers derived from a donor.

[0074]

Next, a conductive film for forming the source electrode and the drain electrode (including a wiring formed in the same layer as the source electrode and the

drain electrode) is formed over the insulating film 204 and the oxide semiconductor film 206 and then processed, so that the source electrode 208a and the drain electrode 208b are formed (see FIG. 1B). Note that a channel length *L* of the transistor is determined by the distance between the edges of the source electrode 208a and the drain electrode 208b which are formed here.

[0075]

As the conductive film used for the source electrode 208a and the drain electrode 208b, for example, a metal film including an element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, and tungsten; a metal nitride film including any of the above elements as a component (a titanium nitride film, a molybdenum nitride film, or a tungsten nitride film); or the like can be used. The source electrode 208a and the drain electrode 208b may have a single-layer structure or a stacked-layer structure. A high-melting-point metal film of titanium, molybdenum, tungsten, or the like or a metal nitride film thereof (a titanium nitride film, a molybdenum nitride film, or a tungsten nitride film) may be stacked on one or both of top and bottom sides of a metal film of aluminum, copper, or the like.

[0076]

Alternatively, the conductive film used for the source electrode 208a and the drain electrode 208b may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), indium oxide-tin oxide alloy (In_2O_3-SnO_2; abbreviated to ITO), indium oxide-zinc oxide alloy (In_2O_3-ZnO), or any of these metal oxide materials including silicon oxide can be used.

[0077]

The conductive film can be processed by being etched after a mask having a desired shape is formed over the conductive film. As the above mask, a resist mask or the like can be used. Ultraviolet light, KrF laser light, ArF laser light, or the like is preferably used for light exposure at the time of forming the resist mask.

[0078]

In the case where the channel length *L* is less than 25 nm, the light exposure at the time of forming the resist mask is preferably performed using, for example, extreme ultraviolet light having an extremely short wavelength of several nanometers to several

tens of nanometers. In the light exposure by extreme ultraviolet light, the resolution is high and the focus depth is large. Thus, the channel length L of the transistor formed later can be reduced, whereby the operation speed of a circuit can be increased.

[0079]

An etching step may be performed using a resist mask formed using a so-called multi-tone mask. A resist mask formed using a multi-tone mask has a plurality of thicknesses and can be further changed in shape by ashing; thus, such a resist mask can be used in a plurality of etching steps for different patterns. Therefore, a resist mask corresponding to at least two kinds of different patterns can be formed by using one multi-tone mask. In other words, the manufacturing process can be simplified.

[0080]

Note that in the etching of the conductive film, part of the oxide semiconductor film 206 is etched, so that the oxide semiconductor film 206 has a groove (a recessed portion) in some cases.

[0081]

After that, by plasma treatment using a gas such as N_2O, N_2, or Ar, impurities such as hydrogen or water attached to a surface of an exposed portion of the oxide semiconductor film 206 may be removed.

[0082]

Next, the insulating film 210 is formed so as to cover the source electrode 208a and the drain electrode 208b and be partly in contact with the oxide semiconductor film 206, and the insulating film 212 is formed over and in contact with the insulating film 210. Then, a resist mask 214 is formed over the insulating film 212 (see FIG. 1C).

[0083]

The insulating film 210 functions as a protective film of the transistor 110. The insulating film 210 can be formed using a material including gallium oxide. The material including gallium oxide may further include aluminum oxide; that is, a material including aluminum gallium oxide or gallium aluminum oxide, or the like may be used. In addition, the thickness of the insulating film 210 is preferably greater than or equal to 10 nm and less than 100 nm.

[0084]

Here, a gallium oxide film used as the insulating film 210 can have a

composition of $Ga_2O_{3+\alpha}$ ($\alpha > 0$). It is preferable that α be greater than or equal to 3.04 and less than or equal to 3.09. Alternatively, an aluminum gallium oxide film used as the insulating film 210 preferably has a composition of $Al_xGa_{2-x}O_{3+\alpha}$ ($1 < x < 2$, $\alpha > 0$). Further alternatively, a gallium aluminum oxide film used as the insulating film 210 preferably has a composition of $Al_xGa_{2-x}O_{3+\alpha}$ ($0 < x \leq 1$, $\alpha > 0$) by being doped with oxygen.

[0085]

The insulating film 210 is preferably formed by a method with which impurities such as hydrogen or water do not enter the insulating film 210. This is because, when impurities such as hydrogen or water are included in the insulating film 210, the impurities such as hydrogen or water enter the oxide semiconductor film formed later or oxygen in the oxide semiconductor film is extracted by the impurities such as hydrogen or water, so that a back channel of the oxide semiconductor film might have lower resistance (have n-type conductivity) and a parasitic channel might be formed. Therefore, the insulating film 210 is preferably formed so as to include impurities such as hydrogen or water as few as possible. For example, the insulating film 210 is preferably formed by a sputtering method. A high-purity gas from which impurities such as hydrogen or water are removed is preferably used as a sputtering gas used for film formation.

[0086]

Examples of the sputtering method include a DC sputtering method in which a direct current power source is used, a pulsed DC sputtering method in which a direct bias is applied in a pulsed manner, an AC sputtering method, and the like.

[0087]

Note that the insulating film 210 is preferably formed while the substrate 200 is being heated..

[0088]

In many cases, an oxide semiconductor material used for the oxide semiconductor film includes gallium. Therefore, the insulating film 210 which is in contact with the oxide semiconductor film is formed using a material including gallium oxide, whereby a favorable condition can be maintained at an interface between the

oxide semiconductor film and the insulating film 210. For example, by providing the oxide semiconductor film in contact with the insulating film 210 including gallium oxide, an accumulation of hydrogen at an interface between the oxide semiconductor film and the insulating film can be reduced. This is because a material including gallium oxide is compatible with an oxide semiconductor material.

[0089]

Note that, in the case where an element belonging to the same group as a constituent element of the oxide semiconductor is used for the insulating film 210, a similar effect can be obtained. That is, it is also effective to additionally use a material including aluminum oxide or the like for the insulating film 210. Aluminum oxide tends to prevent water penetration; therefore, it is preferable to use the material including aluminum oxide in the optic of preventing water from entering the oxide semiconductor film. For example, a material including gallium and aluminum, such as aluminum gallium oxide (or gallium aluminum oxide) may be used for the insulating film 210. In this case, both the effect resulting from inclusion of gallium and the effect resulting from inclusion of aluminum can be obtained, which is preferable. By providing the oxide semiconductor film in contact with an insulating film including aluminum gallium oxide, for example, water can be prevented from entering the oxide semiconductor film and an accumulation of hydrogen at an interface between the oxide semiconductor film and the insulating film can be sufficiently reduced.

[0090]

Note that oxygen doping treatment may be performed on the insulating film 210 here. Oxygen doping refers to addition of oxygen (which includes at least one of an oxygen radical, an oxygen atom, and an oxygen ion) to a bulk. Note that the term "bulk" is used in order to clarify that oxygen is added not only to a surface of a thin film but also to the inside of the thin film. In addition, the oxygen doping includes oxygen plasma doping in which oxygen that is made to be plasma is added to a bulk.

[0091]

When the oxygen doping treatment is performed on the insulating film 210, a region where the amount of oxygen is larger than that in the stoichiometric composition ratio is formed in the insulating film 210. By providing such a region, oxygen can be supplied to the oxide semiconductor film and oxygen deficiency defects in the oxide

semiconductor film can be reduced.

[0092]

Note that in the case where an oxide semiconductor without defects (oxygen deficiency) is used, the amount of oxygen included in the insulating film 210 may be equal to that in the stoichiometric composition. However, in order to ensure reliability, for example, to suppress variation in the threshold voltage of the transistor, the insulating film 210 preferably includes oxygen at an amount which is larger than that in the stoichiometric composition, in consideration of oxygen deficiency that may occur in the oxide semiconductor film.

[0093]

In this manner, the oxygen doping treatment makes it easy to obtain a gallium oxide film having a composition of $Ga_2O_{3+\alpha}$ ($\alpha > 0$), which can be used as the insulating film 210, and to set α to be greater than or equal to 3.04 and less than or equal to 3.09. Alternatively, the oxygen doping treatment makes it easy to obtain an aluminum gallium oxide film having a composition of $Al_xGa_{2-x}O_{3+\alpha}$ ($1 < x < 2$, $\alpha > 0$), which can be used as the insulating film 210. Further alternatively, the oxygen doping treatment makes it easy to obtain a gallium aluminum oxide film having a composition of $Al_xGa_{2-x}O_{3+\alpha}$ ($0 < x \leq 1$, $\alpha > 0$), which can be used as the insulating film 210.

[0094]

The insulating film 212 also functions as a protective film of the transistor 110. The insulating film 212 can be formed by a plasma CVD method using a material such as silicon oxide, silicon nitride, silicon oxynitride, or silicon nitride oxide or a sputtering method, for example. In addition, the thickness of the insulating film 212 is larger than the thickness of the insulating film 210 and is preferably greater than or equal to 100 nm and less than or equal to 300 nm.

[0095]

The insulating film 210 and the insulating film 212 having a larger thickness than the insulating film 210 are stacked in this manner, so that a favorable condition can be maintained at the interface between the oxide semiconductor film and the protective film by the insulating film 210 including gallium oxide and an adequate thickness for the protective film of the transistor 110 can be secured by the insulating film 212.

Further, by thus increasing the thickness of the stack of the insulating film 210 and the insulating film 212, which functions as the protective film of the transistor 110, parasitic capacitance between the transistor and a wiring formed in a subsequent step can be reduced.

[0096]

The resist mask 214 can be formed using a material such as a photosensitive resin by a photolithography method. Here, if the insulating film 210 including gallium oxide is subjected to wet treatment using a developer or the like, the region which is in the insulating film 210 and is needed in design might be dissolved. However, by stacking the insulating film 210 and the insulating film 212 as described in this embodiment and providing the resist mask 214 over the insulating film 212, the resist mask 214 can be formed without the insulating film 210 including gallium oxide being in contact with the developer. Thus, the resist mask 214 can be formed without a possibility that the region which is in the insulating film 210 including gallium oxide and is needed in design is dissolved.

[0097]

Next, dry etching is performed on the insulating film 210 and the insulating film 212 with the use of the resist mask 214, so that the contact hole 218 is formed (see FIG. 1D).

[0098]

If wet treatment such as wet etching is performed here, the region which is in the insulating film 210 including gallium oxide and is needed in design might be dissolved. Therefore, particularly in the case of miniaturizing the semiconductor device, it is extremely difficult to process the insulating film 210 including gallium oxide by wet etching to have a designed size.

[0099]

Thus, the insulating film 210 and the insulating film 212 are processed by dry etching in this embodiment. For the dry etching, a parallel plate reactive ion etching (RIE) method, an inductively coupled plasma (ICP) etching method, or the like can be used. Etching conditions (such as the amount of power applied to a coil-shaped electrode, the amount of power applied to an electrode on a substrate side, and the temperature of the electrode on the substrate side) may be set as appropriate in

accordance with the material so that the films can be etched into desired shapes.

[0100]

As an etching gas that can be used for the dry etching, a gas including fluorine (a fluorine-based gas such as carbon tetrafluoride (CF_4), sulfur hexafluoride (SF_6), nitrogen trifluoride (NF_3), or trifluoromethane (CHF_3)); octafluorocyclobutane (C_4F_8); any of these gases to which a rare gas such as helium (He) or argon (Ar) is added; and the like can be given. By etching the insulating film 210 and the insulating film 212 with the use of such a gas including fluorine, etching can be performed such that etching selectivity of the insulating films with respect to the source electrode 208a is high. For example, conditions of etching using an ICP etching method are set as follows: 7.5 sccm of trifluoromethane and 142.5 sccm of helium are used as an etching gas; the power applied to the coil-shaped electrode is 475 W; the power applied to the electrode on the substrate side is 300 W; the pressure is 5.5 Pa; and the temperature of a lower electrode is 70 °C.

[0101]

Further, a gas including chlorine (a chlorine-based gas such as chlorine (Cl_2), boron trichloride (BCl_3), silicon tetrachloride ($SiCl_4$), or carbon tetrachloride (CCl_4)) or the like may be used. In the case where an insulating film including gallium oxide and aluminum oxide is used as the insulating film 210, the insulating film 210 can be easily etched using such a gas including chlorine.

[0102]

In the dry etching, the etching rate of the insulating film 210 including gallium oxide tends to be lower than the etching rate of the insulating film 212. Accordingly, the diameter of the contact hole 218 in the insulating film 210 can be easily made smaller than the diameter of the contact hole 218 in the insulating film 212 as illustrated in FIG. 1D. That is, the contact hole 218 can have a stepped shape. By forming the contact hole 218 having such a stepped shape, coverage with the wiring 216 formed later can be improved. Alternatively, the contact hole 218 may be formed to have a shape where the diameter of the contact hole 218 in the insulating film 210 is substantially equal to the diameter of the contact hole 218 in the insulating film 212 by setting etching conditions (such as an etching gas, the etching time, and the temperature) as appropriate so that the insulating film 210 and the insulating film 212

have the same or substantially the same etching rate.

[0103]

By performing dry etching on the insulating film 210 and the insulating film 212 in this manner, the contact hole 218 can be formed in the insulating film 210 and the insulating film 212 without a possibility that the region which is in the insulating film 210 including gallium oxide and is needed in design is dissolved.

[0104]

Next, the resist mask 214 is removed by ashing using oxygen plasma, and the wiring 216 is formed so as to be electrically connected to the source electrode 208a through the contact hole 218 (see FIG. 1E).

[0105]

Here, if an alkali stripper solution is used for the removal of the resist mask 214, the region which is in the insulating film 210 including gallium oxide and is needed in design might be dissolved. Therefore, in this embodiment, the resist mask 214 is removed by ashing using oxygen plasma.

[0106]

The ashing treatment using oxygen plasma is performed in an oxygen atmosphere in such a manner that oxygen is made to be plasma by high frequency power or the like and the resist mask 214 is decomposed and removed by the oxygen that is made to be plasma. By removing the resist mask 214 in this manner, the resist mask 214 can be removed without a possibility that the region which is in the insulating film 210 including gallium oxide and is needed in design is dissolved. For example, conditions of the ashing treatment using oxygen plasma, in which an ICP apparatus is used, are set as follows: 300 sccm of an oxygen gas is used; the power of an RF power source is 1800 W; the pressure is 66.5 Pa; and the treatment duration is 180 seconds.

[0107]

By the ashing treatment using oxygen plasma, the resist mask 214 can be removed without generation of a residue of the resist mask 214 or a reaction product of the residue. Accordingly, a surface of the insulating film 212 can be kept clean after the resist mask 214 is removed.

[0108]

The wiring 216 is electrically connected to the source electrode 208a of the

transistor 110 and functions as a so-called source wiring. The wiring 216 can be formed using a material and a method similar to those of the source electrode 208a and the drain electrode 208b.

[0109]

As described above, even when an insulating film formed using a material including gallium oxide is used, the insulating film is not directly subjected to wet treatment; thus, the transistor 110 can be formed without a possibility that a region which is in the insulating film including gallium oxide and is needed in design is dissolved (see FIG. 1E).

[0110]

Note that in the manufacturing process of the transistor 110 in FIGS. 1A to 1E, the step of electrically connecting the wiring 216 to the source electrode 208a is described; however, the disclosed invention is not limited to this. For example, a wiring formed over the insulating film 212 may be electrically connected to the drain electrode 208b by a similar method. In the case where the transistor is used for a pixel portion, a pixel electrode may be electrically connected to the source electrode 208a or the drain electrode 208b by a similar method. In addition, a wiring formed over the insulating film 212 may be electrically connected to the gate electrode (or a wiring formed in the same layer as the gate electrode) by a similar method.

[0111]

Here, a step in which a wiring 222 that is electrically connected to the gate electrode 202 (or a wiring formed in the same layer as the gate electrode 202) illustrated in FIGS. 1A to 1E through a contact hole 224 is formed over the insulating film 212 will be described with reference to FIGS. 2A to 2C. Here, the gate electrode 202 and the wiring 222 are electrically connected to each other in a region where the gate electrode 202 does not overlap with the oxide semiconductor film 206, the source electrode 208a, or the drain electrode 208b.

[0112]

First, steps similar to those comprised in the manufacturing process of the transistor 110 are performed up to and including the step illustrated in FIG. 1C; thus, the resist mask 214 is formed so that the contact hole 224 can be formed in a region where the gate electrode 202 does not overlap with the oxide semiconductor film 206, the

source electrode 208a, and the drain electrode 208b (see FIG. 2A).

[0113]

Next, dry etching is performed on the insulating film 204, the insulating film 210, and the insulating film 212 by a method similar to that used in the step illustrated in FIG. 1D, so that the contact hole 224 is formed (see FIG. 2B). Here, the insulating film 204 is also etched in the same step, which is different from the step illustrated in FIG. 1D; when the insulating film 204 is formed using a material similar to that of the insulating film 210 or the insulating film 212, the insulating film 204 can be etched in a manner similar to that of the insulating film 210 or the insulating film 212.

[0114]

Then, the resist mask 214 is removed by ashing using oxygen plasma by a method similar to that used in the step illustrated in FIG. 1E, and the wiring 222 is formed so as to be electrically connected to the gate electrode 202 through the contact hole 224 (see FIG. 2C). Here, the wiring 222 functions as a so-called gate wiring and can be formed using a method and a material similar to those of the wiring 216 illustrated in FIG. 1E.

[0115]

As described above, even when an insulating film formed using a material including gallium oxide is used, the insulating film is not directly subjected to wet treatment; thus, the wiring 222 which is electrically connected to the gate electrode 202 (including the wiring formed in the same layer as the gate electrode 202) through the contact hole 224 can be formed over the insulating film 212 without a possibility that a region which is in the insulating film including gallium oxide and is needed in design is dissolved.

[0116]

In addition, as the manufacturing process of the transistor 110 in FIGS. 1A to 1E, a process for manufacturing the bottom-gate transistor 110 in which the gate electrode 202 is provided below the oxide semiconductor film 206 to overlap therewith is described; however, the disclosed invention is not limited to this. For example, a top-gate transistor in which a gate electrode is provided over an oxide semiconductor film to overlap therewith may be manufactured by a similar method.

[0117]

Here, an example of a manufacturing process of a top-gate transistor 310 illustrated in FIG. 3E will be described with reference to FIGS. 3A to 3E. Here, the transistor 310 includes, over a substrate 400, an oxide semiconductor film 406, a source electrode 408a, a drain electrode 408b, an insulating film 410, a gate electrode 402, an insulating film 412, and a wiring 416. In the transistor illustrated in FIG. 3E, the insulating film 410 including gallium oxide is provided in contact with the oxide semiconductor film 406, and the insulating film 412 is provided over and in contact with the insulating film 410 including gallium oxide. In addition, the wiring 416 is electrically connected to the source electrode 408a through a contact hole 418 formed in the insulating film 412 and the insulating film 410.

[0118]

First, an oxide semiconductor film for forming the oxide semiconductor film 406 is formed over the substrate 400 and then processed into an island shape, so that the oxide semiconductor film 406 is formed. After that, a conductive film for forming the source electrode and the drain electrode (including a wiring formed in the same layer as the source electrode and the drain electrode) is formed over and in contact with the oxide semiconductor film 406. The conductive film is processed, so that the source electrode 408a and the drain electrode 408b are formed (see FIG. 3A). The substrate 400, the oxide semiconductor film 406, the source electrode 408a, and the drain electrode 408b can be formed using materials and methods similar to those of the substrate 200, the oxide semiconductor film 206, the source electrode 208a, and the drain electrode 208b illustrated in FIGS. 1A to 1E.

[0119]

Note that a base insulating film is preferably formed over the substrate 400 before the oxide semiconductor film 406 is formed. The base insulating film can be formed using a material and a method similar to those of the insulating film 204 illustrated in FIGS. 1A to 1E, and is preferably formed using a material including gallium oxide or a material including gallium oxide and aluminum oxide. Thus, a favorable condition can be maintained at an interface where the base insulating film is in contact with the oxide semiconductor film.

[0120]

Next, the insulating film 410 is formed so as to cover the oxide semiconductor

film 406, the source electrode 408a, and the drain electrode 408b. Then, a conductive film for forming the gate electrode (including a wiring formed in the same layer as the gate electrode) is formed and then processed, so that the gate electrode 402 is formed to overlap with the oxide semiconductor film 406 (see FIG. 3B). The gate electrode 402 can be formed using a material and a method similar to those of the gate electrode 202 illustrated in FIGS. 1A to 1E. The insulating film 410 can be formed using a material and a method similar to those of the insulating film 210 illustrated in FIGS. 1C to 1E. Further, the insulating film 410 may have a stacked-layer structure including an insulating film formed using a material similar to that of the insulating film 204 illustrated in FIGS. 1A to 1E. In this manner, by using a material including gallium oxide for the insulating film 410, a favorable condition can be maintained at an interface where the insulating film 410 is in contact with the oxide semiconductor film.

[0121]

Next, the insulating film 412 is formed so as to cover the gate electrode 402 and insulating film 410, and then a resist mask 414 is formed over the insulating film 412 (see FIG. 3C). The insulating film 412 and the resist mask 414 can be formed using materials and methods similar to those of the insulating film 212 and the resist mask 214 illustrated in FIGS. 1C to 1E.

[0122]

Next, dry etching is performed on the insulating film 410 and the insulating film 412 with the use of the resist mask 414, so that the contact hole 418 is formed (see FIG. 3D). The contact hole 418 can be formed by a method similar to that of the contact hole 218 illustrated in FIGS. 1D and 1E.

[0123]

Then, the resist mask 414 is removed by ashing using oxygen plasma, and the wiring 416 is formed so as to be electrically connected to the source electrode 408a through the contact hole 418 (see FIG. 3E). The resist mask 414 can be removed by a method similar to that used in the removal of the resist mask 214 illustrated in the FIGS. 1C and 1D. The wiring 416 can be formed using a material and a method similar to those of the wiring 216 illustrated in FIG. 1E.

[0124]

As described above, even when an insulating film formed using a material

including gallium oxide is used, the insulating film is not directly subjected to wet treatment; thus, the transistor 310 can be formed without possibility that a region in the insulating film including gallium oxide and needed in design is dissolved (see FIG. 3E).

[0125]

As the manufacturing process of the transistor illustrated in FIGS. 1A to 1E or FIGS. 3A to 3E, a process for manufacturing the transistor in which at least a top surface of the oxide semiconductor film is electrically connected to the source electrode or the drain electrode is described; however, the disclosed invention is not limited to this. For example, a transistor in which at least a bottom surface of an oxide semiconductor film is electrically connected to a source electrode or a drain electrode may be manufactured by a similar method.

[0126]

In this embodiment, etching treatment is performed on the insulating films obtained by providing, over and in contact with the insulating film including gallium oxide, another insulating film; however, the disclosed invention is not limited to this.

[0127]

As described in this embodiment, an insulating film which is in contact with an oxide semiconductor film is formed using a material including gallium oxide, whereby a favorable condition can be maintained at an interface between the oxide semiconductor film and the insulating film.

[0128]

In an etching step of the insulating film formed using a material including gallium oxide, the insulating film is not directly subjected to wet treatment; thus, the insulating film including gallium oxide can be etched without possibility that a region in the insulating film including gallium oxide and needed in design is dissolved.

[0129]

Accordingly, a semiconductor device including an oxide semiconductor and having stable electric characteristics can be provided. Therefore, a semiconductor device having high reliability can be provided.

[0130]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in

the other embodiments.

[0131]

(Embodiment 2)

A semiconductor device having a display function (also referred to as a display device) can be manufactured using the transistor described in Embodiment 1. Moreover, part or all of a driver circuit which includes the transistor can be formed over a substrate where a pixel portion is formed, whereby a system-on-panel can be obtained.

[0132]

In FIG. 5A, a sealant 4005 is provided so as to surround a pixel portion 4002 provided over a first substrate 4001, and the pixel portion 4002 is sealed by using a second substrate 4006. In FIG. 5A, a signal line driver circuit 4003 and a scan line driver circuit 4004 which are formed using a single crystal semiconductor film or a polycrystalline semiconductor film over a substrate separately prepared are mounted in a region that is different from the region surrounded by the sealant 4005 over the first substrate 4001. Various signals and potentials are supplied from flexible printed circuits (FPCs) 4018a and 4018b to the signal line driver circuit 4003 and the scan line driver circuit 4004, which are separately formed, and the pixel portion 4002.

[0133]

In FIGS. 5B and 5C, the sealant 4005 is provided so as to surround the pixel portion 4002 and the scan line driver circuit 4004 which are provided over the first substrate 4001. The second substrate 4006 is provided over the pixel portion 4002 and the scan line driver circuit 4004. Consequently, the pixel portion 4002 and the scan line driver circuit 4004 are sealed together with a display element, by the first substrate 4001, the sealant 4005, and the second substrate 4006. In FIGS. 5B and 5C, the signal line driver circuit 4003 which is formed using a single crystal semiconductor film or a polycrystalline semiconductor film over a substrate separately prepared is mounted in a region that is different from the region surrounded by the sealant 4005 over the first substrate 4001. In FIGS. 5B and 5C, various signals and potentials are supplied from an FPC 4018 to the separately formed signal line driver circuit 4003, the scan line driver circuit 4004, and the pixel portion 4002.

[0134]

Although FIGS. 5B and 5C each illustrate an example in which the signal line

driver circuit 4003 is formed separately and mounted on the first substrate 4001, the disclosed invention is not limited to this structure. The scan line driver circuit may be separately formed and then mounted, or only part of the signal line driver circuit or part of the scan line driver circuit may be separately formed and then mounted.

[0135]

Note that there is no particular limitation on the connection method of a separately formed driver circuit, and a chip on glass (COG) method, a wire bonding method, a tape automated bonding (TAB) method, or the like can be used. FIG. 5A illustrates an example in which the signal line driver circuit 4003 and the scan line driver circuit 4004 are mounted by a COG method. FIG. 5B illustrates an example in which the signal line driver circuit 4003 is mounted by a COG method. FIG. 5C illustrates an example in which the signal line driver circuit 4003 is mounted by a TAB method.

[0136]

In addition, the display device includes a panel in which the display element is sealed, and a module in which an IC including a controller or the like is mounted on the panel.

[0137]

Note that a display device in this specification means an image display device, a display device, or a light source (including a lighting device). Further, the display device includes the following modules in its category: a module to which a connector such as an FPC, a TAB tape, or a TCP is attached; a module having a TAB tape or a TCP at the tip of which a printed wiring board is provided; and a module in which an integrated circuit (IC) is directly mounted on a display element by a COG method.

[0138]

Further, the pixel portion and the scan line driver circuit which are provided over the first substrate include a plurality of transistors, to which the transistor described in Embodiment 1 can be applied.

[0139]

As the display element provided in the display device, a liquid crystal element (also referred to as a liquid crystal display element) or a light-emitting element (also referred to as a light-emitting display element) can be used. The light-emitting

element includes, in its category, an element whose luminance is controlled by current or voltage, and specifically includes an inorganic electroluminescent (EL) element, an organic EL element, and the like. Furthermore, a display medium whose contrast is changed by an electric effect, such as electronic ink, can be used.

[0140]

One embodiment of a semiconductor device will be described with reference to FIG. 6, FIG. 7, and FIG. 8. FIG. 6, FIG. 7, and FIG. 8 correspond to cross-sectional views along line M-N in FIG. 5B.

[0141]

As illustrated in FIG. 6, FIG. 7, and FIG. 8, the semiconductor device includes a connection terminal electrode 4015 and a terminal electrode 4016. The connection terminal electrode 4015 and the terminal electrode 4016 are electrically connected to a terminal included in the FPC 4018 through an anisotropic conductive film 4019.

[0142]

The connection terminal electrode 4015 is formed using the same conductive film as a first electrode layer 4030. The terminal electrode 4016 is formed using the same conductive film as source electrodes and drain electrodes of a transistor 4010 and a transistor 4011.

[0143]

The pixel portion 4002 and the scan line driver circuit 4004 which are provided over the first substrate 4001 include a plurality of transistors. In FIG. 6, FIG. 7, and FIG. 8, the transistor 4010 included in the pixel portion 4002 and the transistor 4011 included in the scan line driver circuit 4004 are illustrated as an example.

[0144]

In this embodiment, the transistor described in Embodiment 1 can be applied to the transistor 4010 and the transistor 4011. Variation in electric characteristics of the transistor 4010 and the transistor 4011 is suppressed and the transistor 4010 and the transistor 4011 are electrically stable. Accordingly, semiconductor devices having high reliability can be provided as the semiconductor devices of this embodiment illustrated in FIG. 6, FIG. 7, and FIG. 8.

[0145]

The transistor 4010 provided in the pixel portion 4002 is electrically connected

to a display element to form a display panel. A variety of display elements can be used as the display element without particular limitation as long as display can be performed.

[0146]

An example of a liquid crystal display device using a liquid crystal element as the display element is illustrated in FIG. 6. In FIG. 6, a liquid crystal element 4013 which is a display element includes the first electrode layer 4030, a second electrode layer 4031, and a liquid crystal layer 4008. An insulating film 4032 and an insulating film 4033 which function as alignment films are provided so that the liquid crystal layer 4008 is sandwiched therebetween. The second electrode layer 4031 is provided on the second substrate 4006 side, and the first electrode layer 4030 and the second electrode layer 4031 are stacked with the liquid crystal layer 4008 positioned therebetween.

[0147]

A columnar spacer denoted by reference numeral 4035 is obtained by selective etching of an insulating film and is provided in order to control the thickness (a cell gap) of the liquid crystal layer 4008. Alternatively, a spherical spacer may be used.

[0148]

In the case where a liquid crystal element is used as the display element, thermotropic liquid crystal, low-molecular liquid crystal, high-molecular liquid crystal, polymer dispersed liquid crystal, ferroelectric liquid crystal, anti-ferroelectric liquid crystal, or the like can be used. Such a liquid crystal material exhibits a cholesteric phase, a smectic phase, a cubic phase, a chiral nematic phase, an isotropic phase, or the like depending on requirements.

[0149]

Alternatively, liquid crystal exhibiting a blue phase for which an alignment film is unnecessary may be used. A blue phase is one of liquid crystal phases, which is generated just before a cholesteric phase changes into an isotropic phase while temperature of cholesteric liquid crystal is increased. Since the blue phase is generated only in a narrow temperature range, a liquid crystal composition in which 5 wt.% or more of a chiral agent is mixed is used for the liquid crystal layer in order to improve the temperature range. The liquid crystal composition which includes liquid crystal exhibiting a blue phase and a chiral agent has a short response time of 1 millisecond or less, has optical isotropy, which makes an alignment process unneeded, and has a small

viewing angle dependence. In addition, since an alignment film does not need to be provided and rubbing treatment is unnecessary, electrostatic discharge damage caused by the rubbing treatment can be prevented and defects and damage of the liquid crystal display device can be reduced in the manufacturing process. Thus, productivity of the liquid crystal display device can be improved.

[0150]

The specific resistivity of the liquid crystal material is 1×10^9 Ω·cm or higher, preferably 1×10^{11} Ω·cm or higher, further preferably 1×10^{12} Ω·cm or higher. The value of the specific resistivity in this specification is measured at 20 °C.

[0151]

The size of a storage capacitor formed in the liquid crystal display device is set considering the leakage current or the like of the transistor provided in the pixel portion so that electric charge can be held for a predetermined period. By using the transistor including the high-purity oxide semiconductor film, it is satisfactory to provide a storage capacitor having a capacitance that is 1/3 or less, preferably 1/5 or less with respect to liquid crystal capacitance of each pixel.

[0152]

In the transistor including the highly purified oxide semiconductor film used in this embodiment, the current in an off state (the off-state current) can be reduced. Therefore, an electrical signal such as an image signal can be held for a longer period, and a writing interval can be set longer when the power is on. Accordingly, frequency of refresh operation can be reduced, which leads to an effect of suppressing power consumption.

[0153]

In addition, the transistor including the highly purified oxide semiconductor film used in this embodiment can have relatively high field-effect mobility and thus is capable of high speed operation. Therefore, by using the transistor in the pixel portion of the liquid crystal display device, a high-quality image can be provided. Further, since the transistor can be separately provided in a driver circuit portion and a pixel portion over one substrate, the number of components of the liquid crystal display device can be reduced.

[0154]

For the liquid crystal display device, a twisted nematic (TN) mode, an in-plane-switching (IPS) mode, a fringe field switching (FFS) mode, an axially symmetric aligned micro-cell (ASM) mode, an optical compensated birefringence (OCB) mode, a ferroelectric liquid crystal (FLC) mode, an antiferroelectric liquid crystal (AFLC) mode, or the like can be used.

[0155]

A normally black liquid crystal display device such as a transmissive liquid crystal display device utilizing a vertical alignment (VA) mode may be used. The vertical alignment mode is a method of controlling the alignment of liquid crystal molecules of a liquid crystal display panel, in which liquid crystal molecules are aligned vertically to a panel surface when no voltage is applied. Some examples are given as the vertical alignment mode. For example, a multi-domain vertical alignment (MVA) mode, a patterned vertical alignment (PVA) mode, an ASV mode, or the like can be used. Moreover, it is possible to use a method called domain multiplication or multi-domain design, in which a pixel is divided into some regions (subpixels) and molecules are aligned in different directions in their respective regions.

[0156]

In the display device, a black matrix (a light-blocking layer), an optical member (an optical substrate) such as a polarizing member, a retardation member, or an anti-reflection member, and the like are provided as appropriate. For example, circular polarization may be employed by using a polarizing substrate and a retardation substrate. In addition, a backlight, a side light, or the like may be used as a light source.

[0157]

In addition, it is possible to employ a time-division display method (a field-sequential driving method) with the use of a plurality of light-emitting diodes (LEDs) as a backlight. By employing a field-sequential driving method, color display can be performed without using a color filter.

[0158]

As a display method in the pixel portion, a progressive method, an interlace method, or the like can be employed. Further, color elements controlled in a pixel at the time of color display are not limited to three colors: R, G, and B (R, G, and B

correspond to red, green, and blue, respectively). For example, R, G, B, and W (W corresponds to white); or R, G, B, and one or more of yellow, cyan, magenta, and the like can be used. Further, the sizes of display regions may be different between respective dots of color elements. The present invention is not limited to the application to a display device for color display but can also be applied to a display device for monochrome display.

[0159]

Alternatively, as the display element included in the display device, a light-emitting element utilizing electroluminescence can be used. Light-emitting elements utilizing electroluminescence are classified according to whether a light-emitting material is an organic compound or an inorganic compound. In general, the former is referred to as an organic EL element, and the latter is referred to as an inorganic EL element.

[0160]

In an organic EL element, by application of voltage to a light-emitting element, electrons and holes are separately injected from a pair of electrodes into a layer including a light-emitting organic compound, and current flows. The carriers (electrons and holes) are recombined, and thus the light-emitting organic compound is excited. The light-emitting organic compound returns to a ground state from the excited state, thereby emitting light. Owing to such a mechanism, this light-emitting element is referred to as a current-excitation light-emitting element.

[0161]

Inorganic EL elements are classified according to their element structures into a dispersion-type inorganic EL element and a thin-film inorganic EL element. A dispersion-type inorganic EL element has a light-emitting layer where particles of a light-emitting material are dispersed in a binder, and its light emission mechanism is donor-acceptor recombination type light emission that utilizes a donor level and an acceptor level. A thin-film inorganic EL element has a structure where a light-emitting layer is sandwiched between dielectric layers, which are further sandwiched between electrodes, and its light emission mechanism is localized type light emission that utilizes inner-shell electron transition of metal ions. Note that an example of an organic EL element is described here as a light-emitting element.

[0162]

In order to extract light emitted from the light-emitting element, at least one of a pair of electrodes is transparent. Then, a transistor and a light-emitting element are formed over a substrate. The light-emitting element can have any of the following structures: a top emission structure in which light is extracted through a surface opposite to the substrate; a bottom emission structure in which light is extracted through a surface on the substrate side; or a dual emission structure in which light is extracted through the surface opposite to the substrate and the surface on the substrate side.

[0163]

An example of a light-emitting device in which a light-emitting element is used as the display element is illustrated in FIG. 7. A light-emitting element 4513 which is a display element is electrically connected to the transistor 4010 provided in the pixel portion 4002. A structure of the light-emitting element 4513 is not limited to the stacked-layer structure including the first electrode layer 4030, an electroluminescent layer 4511, and the second electrode layer 4031. The structure of the light-emitting element 4513 can be changed as appropriate depending on the direction in which light is extracted from the light-emitting element 4513, or the like.

[0164]

A partition wall 4510 is formed using an organic insulating material or an inorganic insulating material. It is particularly preferable that the partition wall 4510 be formed using a photosensitive resin material to have an opening over the first electrode layer 4030 so that a sidewall of the opening is formed as a tilted surface with continuous curvature.

[0165]

The electroluminescent layer 4511 may be formed using a single layer or a plurality of layers stacked.

[0166]

A protective film may be formed over the second electrode layer 4031 and the partition wall 4510 in order to prevent entry of oxygen, hydrogen, moisture, carbon dioxide, or the like into the light-emitting element 4513. As the protective film, a silicon nitride film, a silicon nitride oxide film, a DLC film, or the like can be formed. In a space which is formed with the first substrate 4001, the second substrate 4006, and

the sealant 4005, a filler 4514 is provided for sealing. It is preferable that a panel be packaged (sealed) with a protective film (such as a laminate film or an ultraviolet curable resin film) or a cover material with high air-tightness and little degasification so that the panel is not exposed to the outside air, in this manner.

[0167]

As the filler 4514, an ultraviolet curable resin or a thermosetting resin as well as an inert gas such as nitrogen or argon can be used. For example, polyvinyl chloride (PVC), acrylic, polyimide, an epoxy resin, a silicone resin, polyvinyl butyral (PVB), or ethylene vinyl acetate (EVA) can be used. For example, nitrogen may be used for the filler.

[0168]

In addition, as needed, an optical film such as a polarizing plate, a circularly polarizing plate (including an elliptically polarizing plate), a retardation plate (a quarter-wave plate or a half-wave plate), or a color filter may be provided as appropriate on a light-emitting surface of the light-emitting element. Further, the polarizing plate or the circularly polarizing plate may be provided with an anti-reflection film. For example, anti-glare treatment by which reflected light is diffused by projections and depressions on the surface so that the glare can be reduced can be performed.

[0169]

Further, electronic paper in which electronic ink is driven can be provided as the display device. The electronic paper is also referred to as an electrophoretic display device (an electrophoretic display) and is advantageous in that it has the same level of readability as plain paper, it has lower power consumption than other display devices, and it can be made thin and lightweight.

[0170]

An electrophoretic display device can have various modes. An electrophoretic display device includes a plurality of microcapsules dispersed in a solvent or a solute; each microcapsule includes first particles which are positively charged and second particles which are negatively charged. By applying an electric field to the microcapsules, the particles in the microcapsules move in opposite directions to each other and only the color of the particles gathering on one side is displayed. Note that the first particles and the second particles each include pigment

and do not move without an electric field. Further, the first particles and the second particles have different colors (which may be colorless).

[0171]

Thus, an electrophoretic display device is a display that utilizes a so-called dielectrophoretic effect by which a substance having a high dielectric constant moves to a high-electric field region.

[0172]

A solution in which the above microcapsules are dispersed in a solvent is referred to as electronic ink. This electronic ink can be printed on a surface of glass, plastic, cloth, paper, or the like. Furthermore, by using a color filter or particles that have pigment, color display can be achieved.

[0173]

Note that the first particles and the second particles in the microcapsules may each be formed using a single material selected from a conductive material, an insulating material, a semiconductor material, a magnetic material, a liquid crystal material, a ferroelectric material, an electroluminescent material, an electrochromic material, and a magnetophoretic material, or formed using a composite material of any of these.

[0174]

As the electronic paper, a display device using a twisting ball display system can be used. The twisting ball display system refers to a method in which spherical particles each colored in black and white are arranged between a first electrode layer and a second electrode layer which are electrode layers used for a display element, and a potential difference is generated between the first electrode layer and the second electrode layer to control the orientation of the spherical particles, so that display is performed.

[0175]

FIG. 8 illustrates active matrix electronic paper as one embodiment of a semiconductor device. The electronic paper in FIG. 8 is an example of a display device using a twisting ball display system.

[0176]

Between the first electrode layer 4030 connected to the transistor 4010 and the

second electrode layer 4031 provided on the second substrate 4006, spherical particles 4613 each of which includes a black region 4615a, a white region 4615b, and a cavity 4612 around the regions which is filled with liquid are provided. A space around the spherical particles 4613 is filled with a filler 4614 such as a resin. The second electrode layer 4031 corresponds to a common electrode (a counter electrode). The second electrode layer 4031 is electrically connected to a common potential line.

[0177]

In FIG. 6, FIG. 7, and FIG. 8, a flexible substrate as well as a glass substrate can be used as the first substrate 4001 and the second substrate 4006. For example, a plastic substrate having a light-transmitting property or the like can be used. As plastic, a fiberglass-reinforced plastics (FRP) plate, a polyvinyl fluoride (PVF) film, a polyester film, or an acrylic resin film can be used. In addition, a sheet with a structure in which an aluminum foil is sandwiched between PVF films or polyester films can be used.

[0178]

An insulating layer 4021 can be formed using an inorganic insulating material or an organic insulating material. Note that the insulating layer 4021 formed using a heat-resistant organic insulating material such as an acrylic resin, polyimide, a benzocyclobutene resin, polyamide, or an epoxy resin is preferably used as a planarization insulating film. Other than such organic insulating materials, it is possible to use a low-dielectric constant material (a low-k material), a siloxane-based resin, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), or the like. The insulating layer may be formed by stacking a plurality of insulating films formed using any of these materials.

[0179]

There is no particular limitation on the method for forming the insulating layer 4021, and the following method can be used depending on the material: a sputtering method, a spin coating method, a dipping method, spray coating, a droplet discharge method (such as an inkjet method, screen printing, or offset printing), roll coating, curtain coating, knife coating, or the like.

[0180]

The display device displays an image by transmitting light from a light source or a display element. Therefore, the substrate and the thin films such as the insulating

film and the conductive film provided for the pixel portion where light is transmitted have light-transmitting properties with respect to light in the visible-light wavelength range.

[0181]

The first electrode layer and the second electrode layer (each of which is also referred to as a pixel electrode layer, a common electrode layer, a counter electrode layer, or the like) for applying voltage to the display element may have light-transmitting properties or light-reflecting properties, which depends on the direction in which light is extracted, the position where the electrode layer is provided, and the pattern structure of the electrode layer.

[0182]

The first electrode layer 4030 and the second electrode layer 4031 can be formed using a light-transmitting conductive material such as indium oxide including tungsten oxide, indium zinc oxide including tungsten oxide, indium oxide including titanium oxide, indium tin oxide including titanium oxide, indium tin oxide (hereinafter referred to as ITO), indium zinc oxide, or indium tin oxide to which silicon oxide is added.

[0183]

Alternatively, the first electrode layer 4030 and the second electrode layer 4031 can be formed using one or more kinds of materials selected from metals such as tungsten (W), molybdenum (Mo), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), cobalt (Co), nickel (Ni), titanium (Ti), platinum (Pt), aluminum (Al), copper (Cu), and silver (Ag); alloys of these metals; and nitrides of these metals.

[0184]

A conductive composition including a conductive high molecular weight molecule (also referred to as a conductive polymer) can be used for the first electrode layer 4030 and the second electrode layer 4031. As the conductive high molecular weight molecule, a so-called π-electron conjugated conductive polymer can be used. For example, polyaniline or a derivative thereof, polypyrrole or a derivative thereof, polythiophene or a derivative thereof, and a copolymer of two or more of aniline, pyrrole, and thiophene or a derivative thereof can be given.

[0185]

Since the transistor is easily broken owing to static electricity or the like, a protection circuit for protecting the driver circuit is preferably provided. The protection circuit is preferably formed using a nonlinear element.

[0186]

As described above, by using the transistor described in Embodiment 1, a semiconductor device having high reliability can be provided. Note that the transistor described in Embodiment 1 can be applied to not only semiconductor devices having the display functions described above but also semiconductor devices having a variety of functions, such as a power device which is mounted on a power supply circuit, a semiconductor integrated circuit such as an LSI, and a semiconductor device having an image sensor function of reading information of an object.

[0187]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0188]

(Embodiment 3)

A semiconductor device disclosed in this specification can be applied to a variety of electronic devices (including game machines). Examples of electronic devices are a television set (also referred to as a television or a television receiver), a monitor of a computer or the like, a camera such as a digital camera or a digital video camera, a digital photo frame, a mobile phone (also referred to as a cellular phone or a mobile phone device), a portable game machine, a portable information terminal, an audio reproducing device, a large-sized game machine such as a pachinko machine, and the like. Examples of an electronic device including the liquid crystal display device described in the above embodiment will be described.

[0189]

FIG. 9A illustrates a laptop personal computer which includes a main body 3001, a housing 3002, a display portion 3003, a keyboard 3004, and the like. By applying the semiconductor device described in Embodiment 1 or 2, the laptop personal computer can have high reliability.

[0190]

FIG. 9B illustrates a portable information terminal (PDA) which includes a display portion 3023, an external interface 3025, operation buttons 3024, and the like in a main body 3021. A stylus 3022 is provided as an accessory for operation. By applying the semiconductor device described in Embodiment 1 or 2, the portable information terminal (PDA) can have higher reliability.

[0191]

FIG. 9C illustrates an example of an electronic book reader. For example, an electronic book reader 2700 includes two housings, a housing 2701 and a housing 2703. The housing 2701 and the housing 2703 are combined with a hinge 2711 so that the electronic book reader 2700 can be opened and closed with the hinge 2711 as an axis. With such a structure, the electronic book reader 2700 can be used like a paper book.

[0192]

A display portion 2705 and a display portion 2707 are incorporated in the housing 2701 and the housing 2703, respectively. The display portion 2705 and the display portion 2707 may display one image or different images. In the case where the display portion 2705 and the display portion 2707 display different images, for example, a display portion on the right side (the display portion 2705 in FIG. 9C) can display text and a display portion on the left side (the display portion 2707 in FIG. 9C) can display graphics. By applying the semiconductor device described in Embodiment 1 or 2, the electronic book reader 2700 can have high reliability.

[0193]

Further, FIG. 9C illustrates an example in which the housing 2701 is provided with an operation portion and the like. For example, the housing 2701 is provided with a power switch 2721, operation keys 2723, a speaker 2725, and the like. With the operation keys 2723, pages can be turned. Note that a keyboard, a pointing device, or the like may also be provided on the surface of the housing, on which the display portion is provided. Furthermore, an external connection terminal (such as an earphone terminal or a USB terminal), a recording medium insertion portion, and the like may be provided on the back surface or the side surface of the housing. Moreover, the electronic book reader 2700 may have a function of an electronic dictionary.

[0194]

The electronic book reader 2700 may have a configuration capable of wirelessly transmitting and receiving data. Through wireless communication, desired book data or the like can be purchased and downloaded from an electronic book server.

[0195]

FIG. 9D illustrates a mobile phone which includes two housings, a housing 2800 and a housing 2801. The housing 2801 includes a display panel 2802, a speaker 2803, a microphone 2804, a pointing device 2806, a camera lens 2807, an external connection terminal 2808, and the like. In addition, the housing 2800 includes a solar cell 2810 having a function of charging the portable information terminal, an external memory slot 2811, and the like. Further, an antenna is incorporated in the housing 2801. By applying the semiconductor device described in Embodiment 1 or 2, the mobile phone can have high reliability.

[0196]

Further, the display panel 2802 is provided with a touch panel. A plurality of operation keys 2805 that is displayed as images is illustrated by dashed lines in FIG. 9D. Note that a boosting circuit by which voltage output from the solar cell 2810 is raised to be sufficiently high for each circuit is also provided.

[0197]

In the display panel 2802, the display direction can be appropriately changed depending on a usage pattern. Further, the mobile phone is provided with the camera lens 2807 on the same surface as the display panel 2802, and thus it can be used as a video phone. The speaker 2803 and the microphone 2804 can be used for videophone calls, recording and playing sound, and the like as well as voice calls. Further, the housings 2800 and 2801 in a state where they are developed as illustrated in FIG. 9D can shift by sliding so that one is lapped over the other; therefore, the size of the mobile phone can be reduced, which makes the mobile phone suitable for being carried.

[0198]

The external connection terminal 2808 can be connected to an AC adapter and various types of cables such as a USB cable, and charging and data communication with a personal computer or the like are possible. Moreover, a larger amount of data can be saved and moved by inserting a recording medium to the external memory slot 2811.

[0199]

Further, in addition to the above functions, an infrared communication function, a television reception function, or the like may be provided.

[0200]

FIG. 9E illustrates a digital video camera which includes a main body 3051, a display portion A 3057, an eyepiece 3053, an operation switch 3054, a display portion B 3055, a battery 3056, and the like. By applying the semiconductor device described in Embodiment 1 or 2, the digital video camera can have high reliability.

[0201]

FIG. 9F illustrates an example of a television set. In a television set 9600, a display portion 9603 is incorporated in a housing 9601. The display portion 9603 can display images. Here, the housing 9601 is supported by a stand 9605. By applying the semiconductor device described in Embodiment 1 or 2, the television set 9600 can have high reliability.

[0202]

The television set 9600 can be operated by an operation switch of the housing 9601 or a separate remote controller. Further, the remote controller may be provided with a display portion for displaying data output from the remote controller.

[0203]

Note that the television set 9600 is provided with a receiver, a modem, and the like. With the use of the receiver, a general television broadcast can be received. Moreover, when the television set is connected to a communication network with or without wires via the modem, one-way (from a sender to a receiver) or two-way (between a sender and a receiver or between receivers) data communication can be performed.

[0204]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[Example 1]

[0205]

In this example, a contact hole formed in the following manner was evaluated: insulating films were formed so that a first silicon oxide (SiO_x) film, a gallium oxide

(GaO_x) film, and a second silicon oxide (SiO_x) film were sequentially stacked in a manner similar to that of Embodiment 1, and dry etching was performed on the insulating films with the use of a photolithography step.

[0206]

Firstly, a manufacturing process of the insulating films used in this example, in which the first silicon oxide film, the gallium oxide film, and the second silicon oxide film were sequentially stacked, is described.

[0207]

First, the first silicon oxide film was formed over a tungsten substrate so as to have a thickness of 100 nm. Here, the first silicon oxide film was formed by a sputtering method under conditions where the flow rate of an argon gas was 25 sccm, the flow rate of an oxygen gas was 25 sccm, the power of an RF power source was 2 kW, the pressure was 0.4 Pa, and the temperature was 100 °C.

[0208]

Next, the gallium oxide film was formed over and in contact with the first silicon oxide film so as to have a thickness of 100 nm. Here, gallium oxide was deposited by a sputtering method under conditions where the flow rate of an argon gas was 10.5 sccm, the flow rate of an oxygen gas was 4.5 sccm, the power of the RF power source was 200 W, the pressure was 0.4 Pa, and the temperature was room temperature.

[0209]

Next, the second silicon oxide film was formed over the gallium oxide film so as to have a thickness of 300 nm. Here, the second silicon oxide film was formed by a sputtering method under conditions where the flow rate of an argon gas was 40 sccm, the flow rate of an oxygen gas was 10 sccm, the power of the RF power source was 1.5 kW, the pressure was 0.4 Pa, and the temperature was 100 °C. Through the above steps, the insulating films in which the first silicon oxide film, the gallium oxide film, and the second silicon oxide film were sequentially stacked were formed.

[0210]

Then, dry etching was performed on the insulating films, so that a contact hole was formed. Here, a contact hole was formed by forming a resist mask over the second silicon oxide film, performing dry etching on the insulating films, and removing

the resist mask by only ashing using oxygen plasma, so that Sample A was formed. A contact hole was formed by forming a resist mask over the second silicon oxide film, performing rinse treatment, performing dry etching on the insulating films, and removing the resist mask by ashing using oxygen plasma and treatment using a resist stripper solution, so that Sample B was formed.

[0211]

A manufacturing process of Sample A is described in detail. First, the resist mask was formed over the second silicon oxide film by a photolithography method. Here, in the manufacture of Sample A, rinse treatment was not performed when a resist pattern was formed.

[0212]

Next, with the use of the resist mask, dry etching was performed on the insulating films having the structure in which the first silicon oxide film, the gallium oxide film, and the second silicon oxide film were sequentially stacked, so that the contact hole was formed. Here, the dry etching was performed by an ICP etching method. Etching conditions were set as follows: the flow rate of a trifluoromethan gas was 7.5 sccm; the flow rate of a helium gas was 142.5 sccm; the power applied to a coil-shaped electrode was 475 W; the power applied to an electrode on the substrate side was 300 W; the pressure was 5.5 Pa, and the temperature of a lower electrode was 70 °C.

[0213]

Then, the resist mask formed over the second silicon oxide film was removed by only ashing using oxygen plasma. Here, conditions of the ashing treatment using oxygen plasma were set as follows: the flow rate of an oxygen gas was 300 sccm; the power of the RF power source was 1800 W; the pressure was 66.5 Pa; and the treatment time was 180 seconds. Through the above steps, Sample A was manufactured where the contact hole was formed in the insulating films in which the first silicon oxide film, the gallium oxide film, and the second silicon oxide film were sequentially stacked.

[0214]

Next, a manufacturing process of Sample B is described in detail. A difference between the manufacturing processes of Sample A and Sample B is in that rinse treatment was performed in the manufacturing process of Sample B when a resist

pattern was formed. In addition, in the manufacturing process of Sample B, the resist mask was removed by ashing using oxygen plasma and treatment using a resist stripper solution. Conditions of the ashing treatment were set as follows: the flow rate of an oxygen gas was 100 sccm; the power of the RF power source was 200 W; the pressure was 66.5 Pa; and the treatment time was 300 seconds. As the resist stripper solution, a stripping agent N-300 (produced by Nagase & Co., Ltd.) was used. The other steps of manufacturing Sample B were performed by a method similar to that of the manufacturing process of Sample A.

[0215]

FIGS. 10A and 10B are SEM images of Sample A and Sample B, respectively. When FIGS. 10A and 10B are compared with each other, a surface of the second silicon oxide film is kept clean in Sample A, whereas a residue of the resist mask, a reaction product of the residue, and the like remain on a surface of the second silicon oxide film in Sample B.

[0216]

FIGS. 11A and 11B are respective enlarged SEM images of cross-sectional portions of the insulating films in the SEM images of FIGS. 10A and 10B. From comparison between FIGS. 11A and 11B, it is found that a sidewall of the contact hole projects in the gallium oxide film portion to form a stepped shape in Sample A, whereas a sidewall of the contact hole is deeply dissolved in the gallium oxide film portion to form a depression in Sample B. Thus, the gallium oxide film in the sidewall portion, which is needed for the contact hole, is also removed in Sample B.

[0217]

As described above, a region which is in a gallium oxide film and is needed in design might be dissolved by wet treatment such as rinse treatment or treatment using a resist stripper solution as in Sample B. Therefore, by employing a manufacturing process in which a gallium oxide film is not directly subjected to wet treatment in a step of forming a contact hole in an insulating film including gallium oxide as in Sample A, a possibility that a region which is in the gallium oxide film and is needed in design is dissolved can be reduced.

EXPLANATION OF REFERENCES

[0218]

110: transistor, 200: substrate, 202: gate electrode, 204: insulating film, 206: oxide semiconductor film, 208a: source electrode, 208b: drain electrode, 210: insulating film, 212: insulating film, 214: resist mask, 216: wiring, 218: contact hole, 222: wiring, 224: contact hole, 301: target, 302: target, 310: transistor, 400: substrate, 402: gate electrode, 406: oxide semiconductor film, 408a: source electrode, 408b: drain electrode, 410: insulating film, 412: insulating film, 414: resist mask, 416: wiring, 418: contact hole, 2700: electronic book reader, 2701: housing, 2703: housing, 2705: display portion, 2707: display portion, 2711: hinge, 2721: power switch, 2723: operation key, 2725: speaker, 2800: housing, 2801: housing, 2802: display panel, 2803: speaker, 2804: microphone, 2805: operation key, 2806: pointing device, 2807: camera lens, 2808: external connection terminal, 2810: solar cell, 2811: external memory slot, 3001: main body, 3002: housing, 3003: display portion, 3004: keyboard, 3021: main body, 3022: stylus, 3023: display portion, 3024: operation button, 3025: external interface, 3051: main body, 3053: eyepiece, 3054: operation switch, 3055: display portion B, 3056: battery, 3057: display portion A, 4001: substrate, 4002: pixel portion, 4003: signal line driver circuit, 4004: scan line driver circuit, 4005: sealant, 4006: substrate, 4008: liquid crystal layer, 4010: transistor, 4011: transistor, 4013: liquid crystal element, 4015: connection terminal electrode, 4016: terminal electrode, 4018: FPC, 4018a: FPC, 4018b: FPC, 4019: anisotropic conductive film, 4021: insulating layer, 4030: electrode layer, 4031: electrode layer, 4032: insulating film, 4033: insulating film, 4510: partition wall, 4511: electroluminescent layer, 4513: light-emitting element, 4514: filler, 4612: cavity, 4613: spherical particle, 4614: filler, 4615a: black region, 4615b: white region, 9600: television set, 9601: housing, 9603: display portion, and 9605: stand. This application is based on Japanese Patent Application serial no. 2010-139715 filed with Japan Patent Office on June 18, 2010, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A method for manufacturing an electronic device comprising a conductive layer, a first insulating layer, and a protective insulating film, the method comprising the steps of:

forming the first insulating layer over the conductive layer;

forming the protective insulating film over the first insulating layer;

forming a resist mask over the protective insulating film;

forming a hole by dry etching the protective insulating film and the first insulating layer according to the resist mask; and

removing the resist mask by ashing using oxygen plasma,

wherein a width of the hole in the first insulating layer is smaller than or equal to a width of the hole in the protective insulating film.

2. A method for manufacturing a transistor comprising an oxide semiconductor layer, a gate electrode, one of a source electrode and a drain electrode electrically connected to the oxide semiconductor layer, a first insulating layer, a protective insulating film, and a wiring, the method comprising the steps of:

forming the oxide semiconductor layer over the gate electrode;

forming the one of the source electrode and the drain electrode in electrical contact with the oxide semiconductor layer;

forming the first insulating layer over the one of the source electrode and the drain electrode, and on and in contact with the oxide semiconductor layer;

forming the protective insulating film over the first insulating layer;

forming a resist mask over the protective insulating film;

forming a contact hole by dry etching the protective insulating film and the first insulating layer according to the resist mask;

removing the resist mask by ashing using oxygen plasma; and

forming the wiring over the protective insulating film and in electrical contact with at least one of the gate electrode and the one of the source electrode and the drain electrode, through the contact hole,

wherein a width of the contact hole in the first insulating layer is smaller than or equal to a width of the contact hole in the protective insulating film.

3. A method for manufacturing a transistor comprising an oxide semiconductor layer, a gate electrode, one of a source electrode and a drain electrode electrically connected to the oxide semiconductor layer, a first insulating layer, a protective insulating film, and a wiring, the method comprising the steps of:

forming the one of the source electrode and the drain electrode in electrical contact with the oxide semiconductor layer;

forming the first insulating layer over the one of the source electrode and the drain electrode, and on and in contact with the oxide semiconductor layer;

forming the gate electrode over the first insulating layer;

forming the protective insulating film over the first insulating layer and the gate electrode;

forming a resist mask over the protective insulating film;

forming a contact hole by dry etching the protective insulating film and the first insulating layer according to the resist mask;

removing the resist mask by ashing using oxygen plasma; and

forming the wiring over the protective insulating film and in electrical contact with at least one of the gate electrode and the one of the source electrode and the drain electrode, through the contact hole,

wherein a width of the contact hole in the first insulating layer is smaller than or equal to a width of the contact hole in the protective insulating film.

4. The method for manufacturing an electronic device according to claim 1, wherein the first insulating layer comprises gallium oxide.

5. The method for manufacturing a transistor according to claim 2, wherein the first insulating layer comprises gallium oxide.

6. The method for manufacturing a transistor according to claim 3, wherein the first insulating layer comprises gallium oxide.

7. The method for manufacturing a transistor according to claim 2, wherein the oxide semiconductor layer comprises gallium.

8. The method for manufacturing a transistor according to claim 3, wherein the oxide semiconductor layer comprises gallium.

9. The method for manufacturing an electronic device according to claim 1, wherein the first insulating layer comprises aluminum oxide, and wherein a gas comprising chlorine is used in the dry etching.

10. The method for manufacturing a transistor according to claim 2, wherein the first insulating layer comprises aluminum oxide, and wherein a gas comprising chlorine is used in the dry etching.

11. The method for manufacturing a transistor according to claim 3, wherein the first insulating layer comprises aluminum oxide, and wherein a gas comprising chlorine is used in the dry etching.

12. The method for manufacturing an electronic device according to claim 1, wherein the first insulating layer is formed while being heated.

13. The method for manufacturing a transistor according to claim 2, wherein the first insulating layer is formed while being heated.

14. The method for manufacturing a transistor according to claim 3, wherein the first insulating layer is formed while being heated.

15. The method for manufacturing an electronic device according to claim 1, further comprising a step of oxygen doping of the first insulating layer.

16. The method for manufacturing a transistor according to claim 2,

further comprising a step of oxygen doping of the first insulating layer.

17. The method for manufacturing a transistor according to claim 3,
further comprising a step of oxygen doping of the first insulating layer.

18. The method for manufacturing an electronic device according to claim 1,
wherein the protective insulating film comprises silicon and at least one of oxygen and nitrogen.

19. The method for manufacturing a transistor according to claim 2,
wherein the protective insulating film comprises silicon and at least one of oxygen and nitrogen.

20. The method for manufacturing a transistor according to claim 3,
wherein the protective insulating film comprises silicon and at least one of oxygen and nitrogen.

FIG. 1A

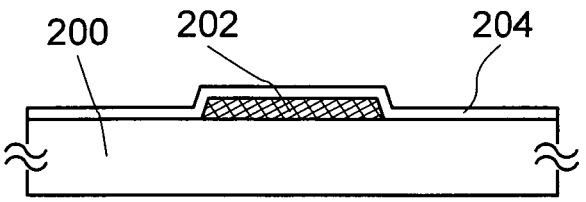


FIG. 1B

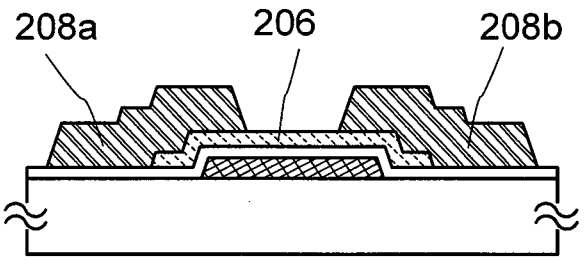


FIG. 1C

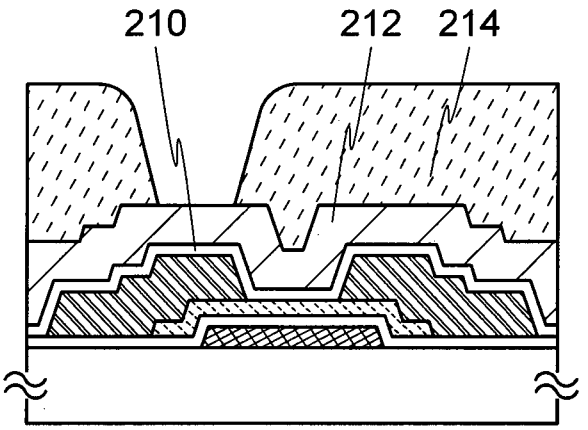


FIG. 1D

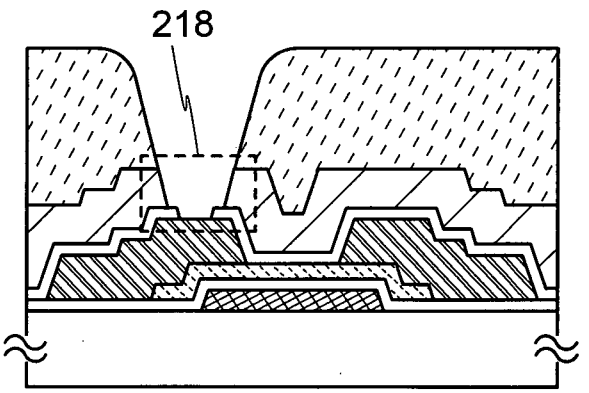


FIG. 1E

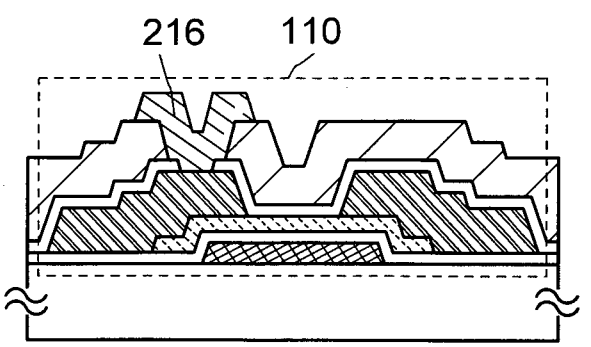


FIG. 2A

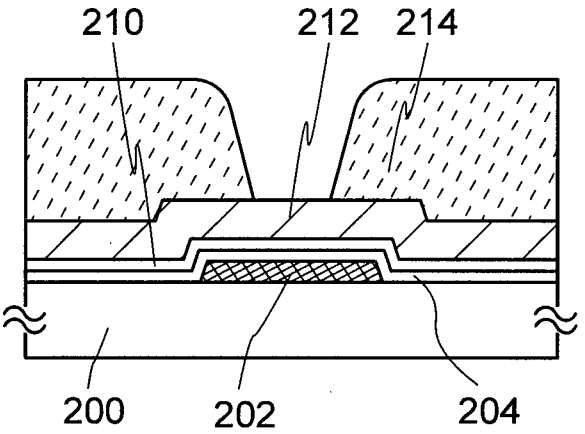


FIG. 2B

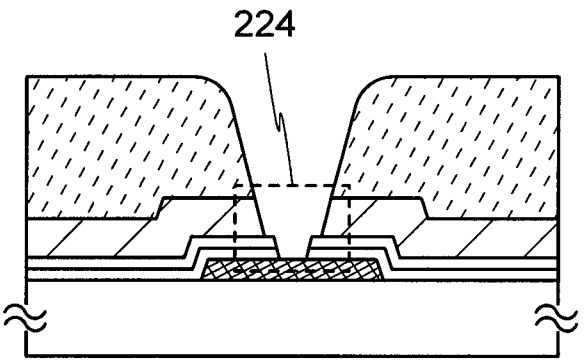


FIG. 2C

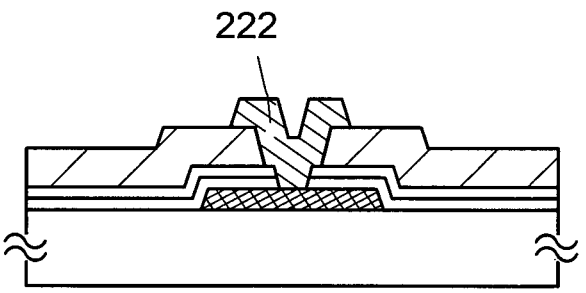


FIG. 3A

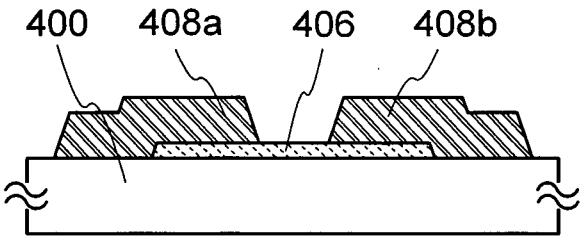


FIG. 3B

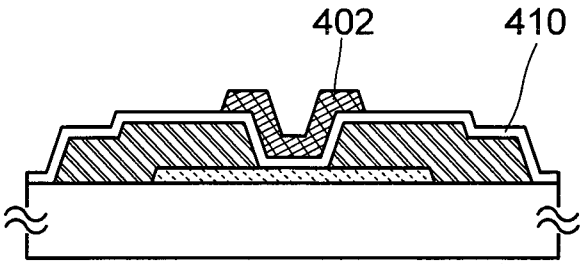


FIG. 3C

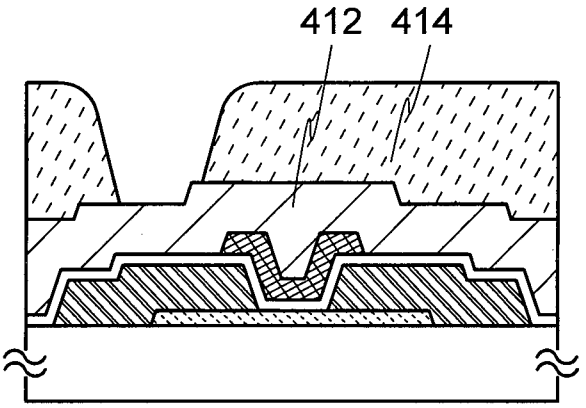


FIG. 3D

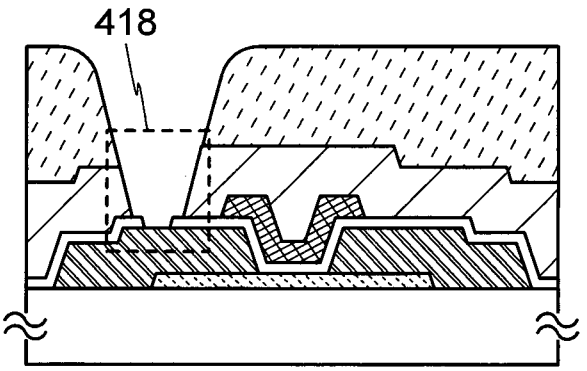


FIG. 3E

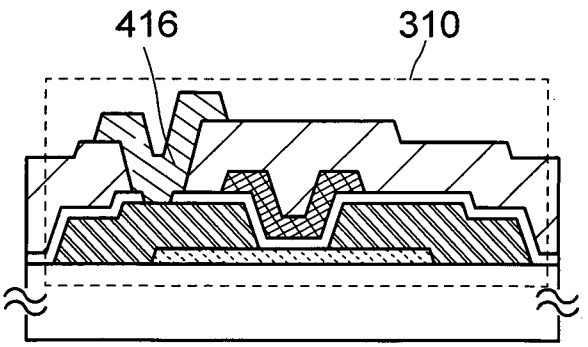


FIG. 4A

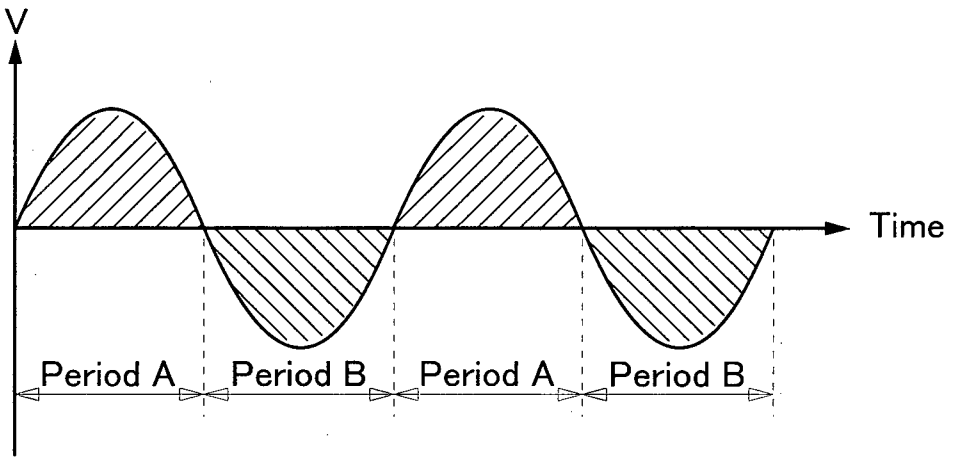


FIG. 4B1

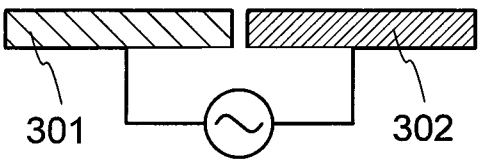


FIG. 4B2

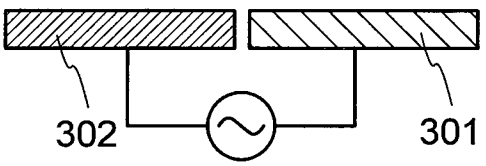


FIG. 5A

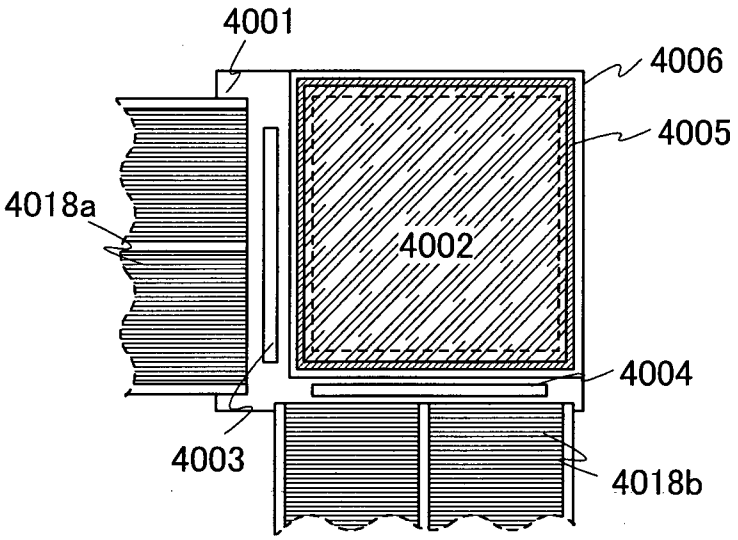


FIG. 5B

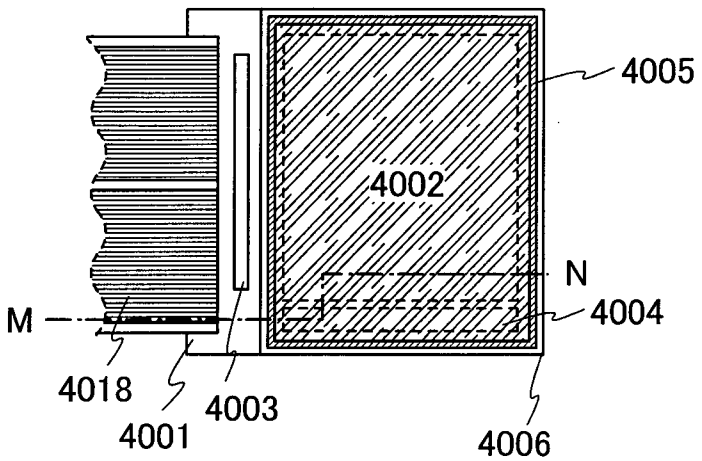


FIG. 5C

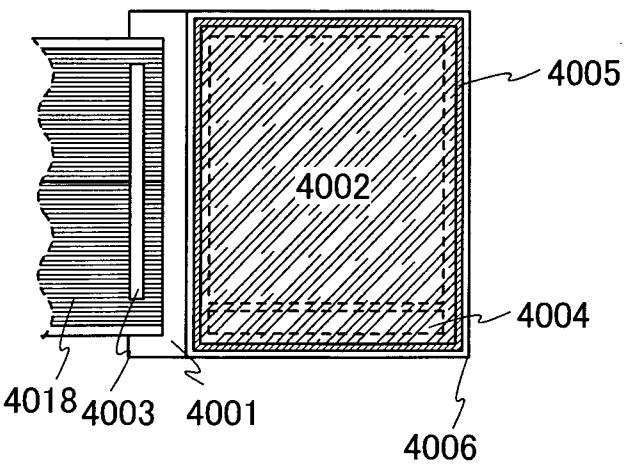


FIG. 6

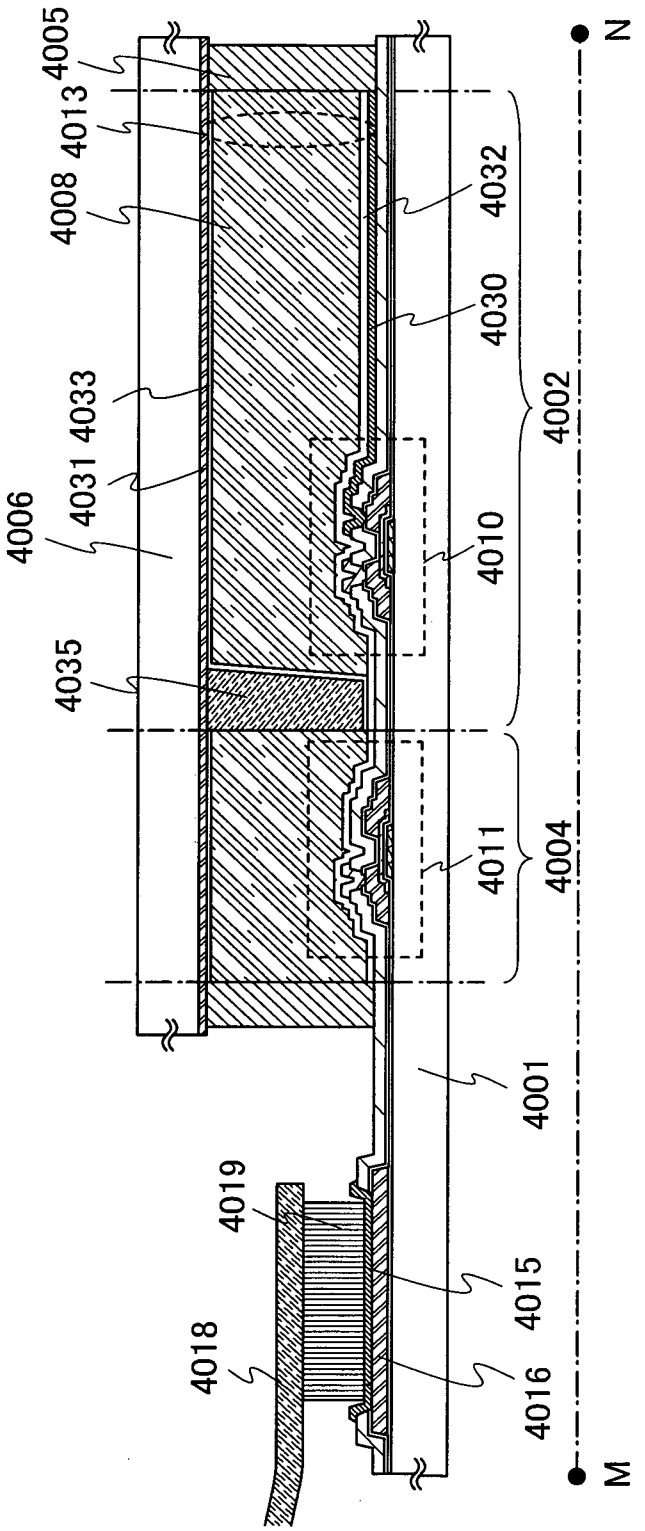

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FIG. 7

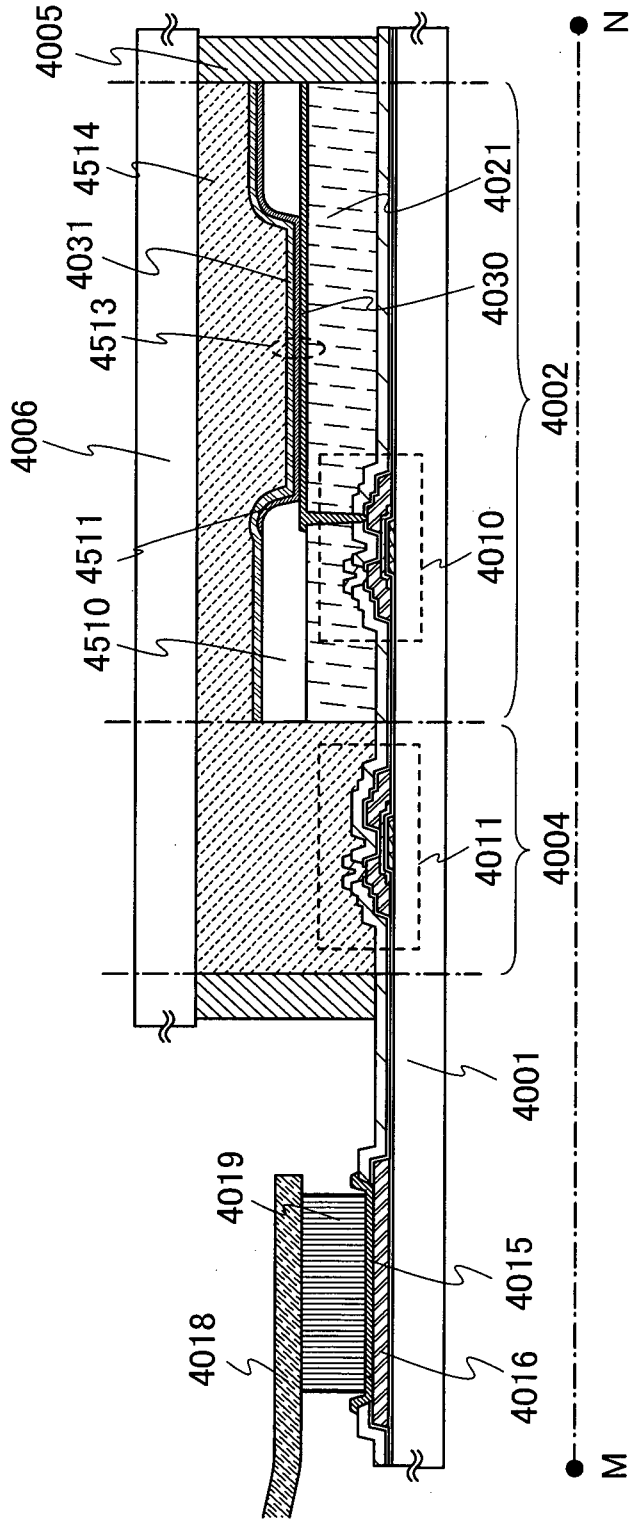
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FIG. 8

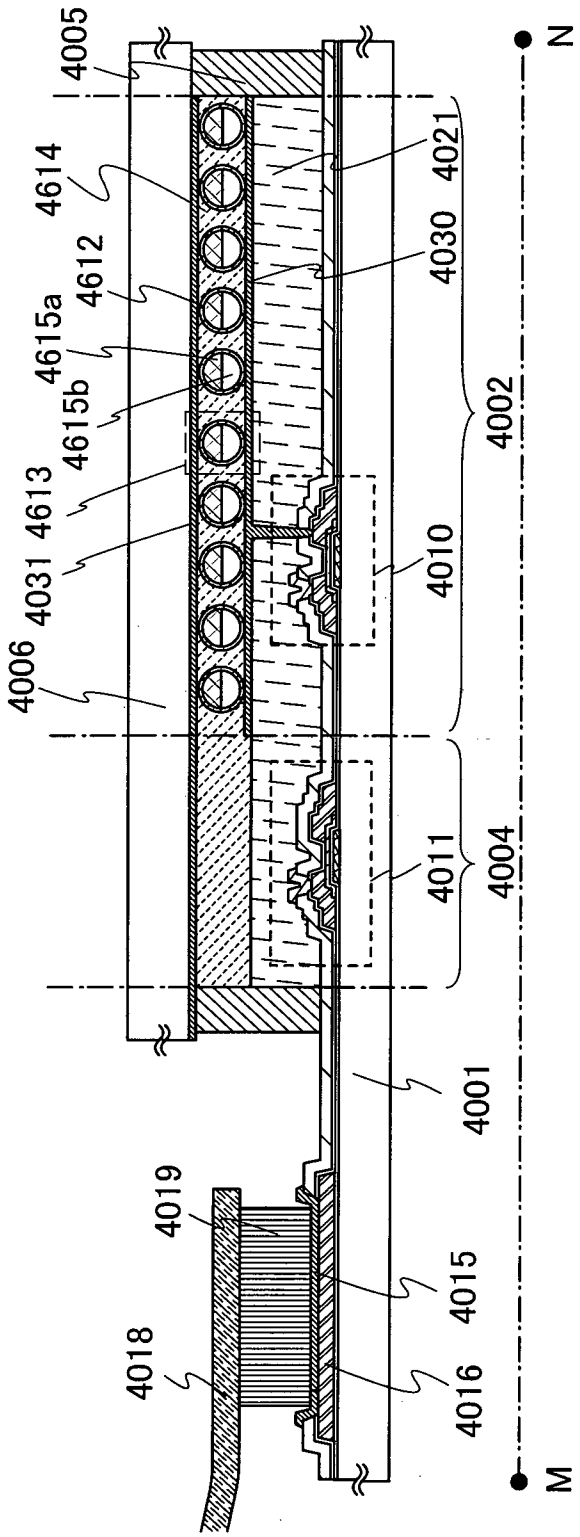
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FIG. 9A

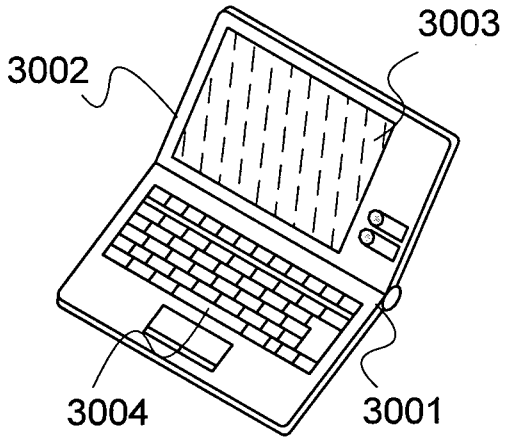


FIG. 9B

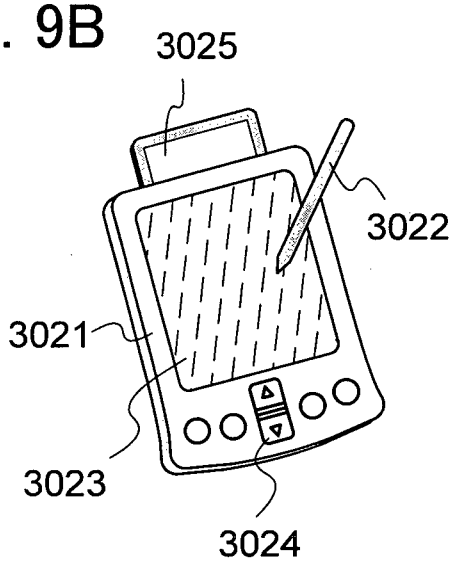


FIG. 9C

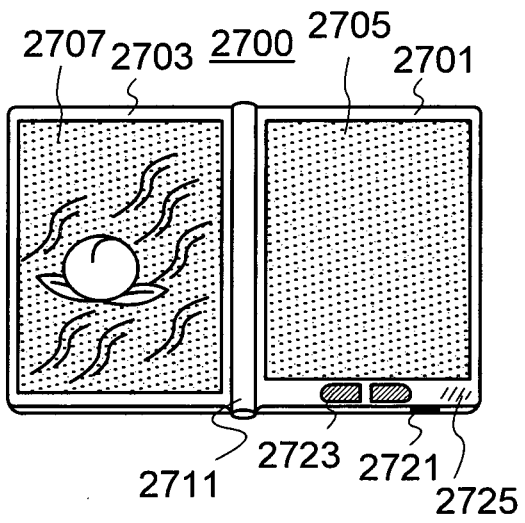


FIG. 9D

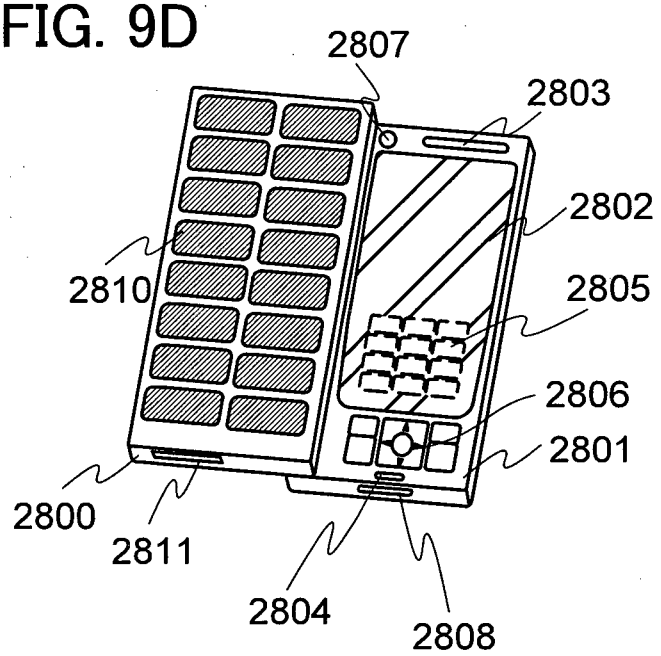


FIG. 9E

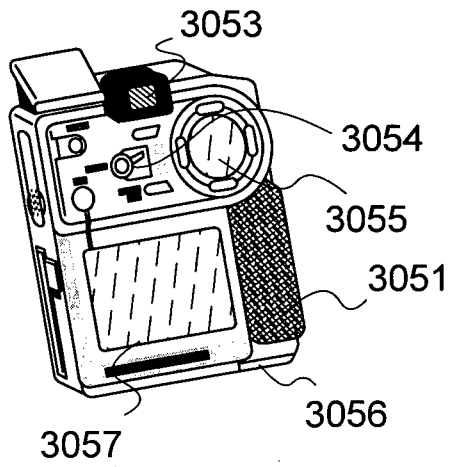


FIG. 9F

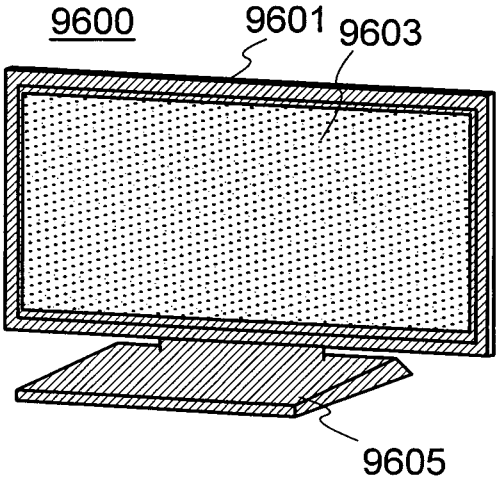


FIG. 10A

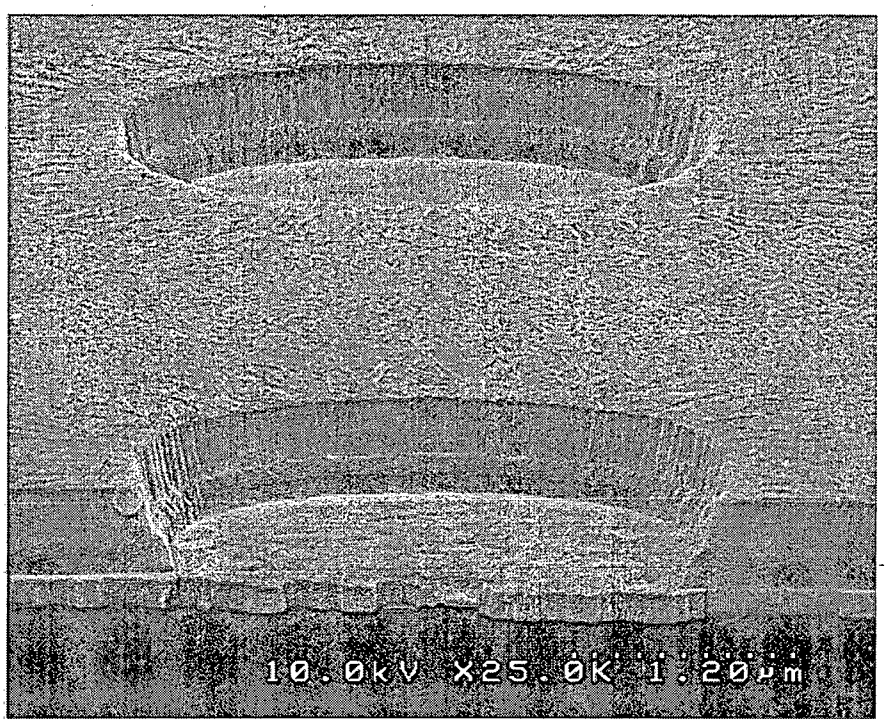


FIG. 10B

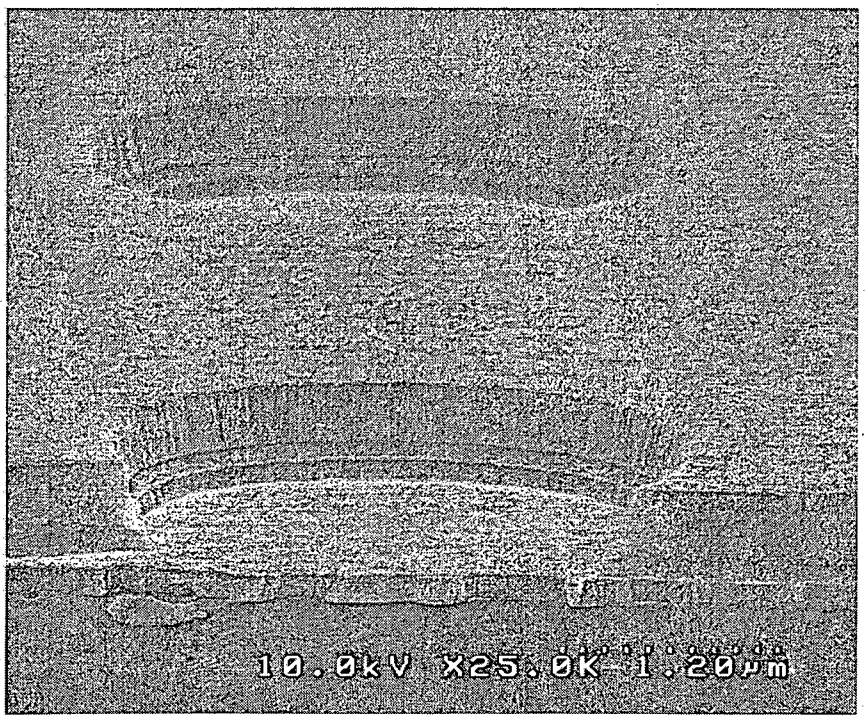


FIG. 11A

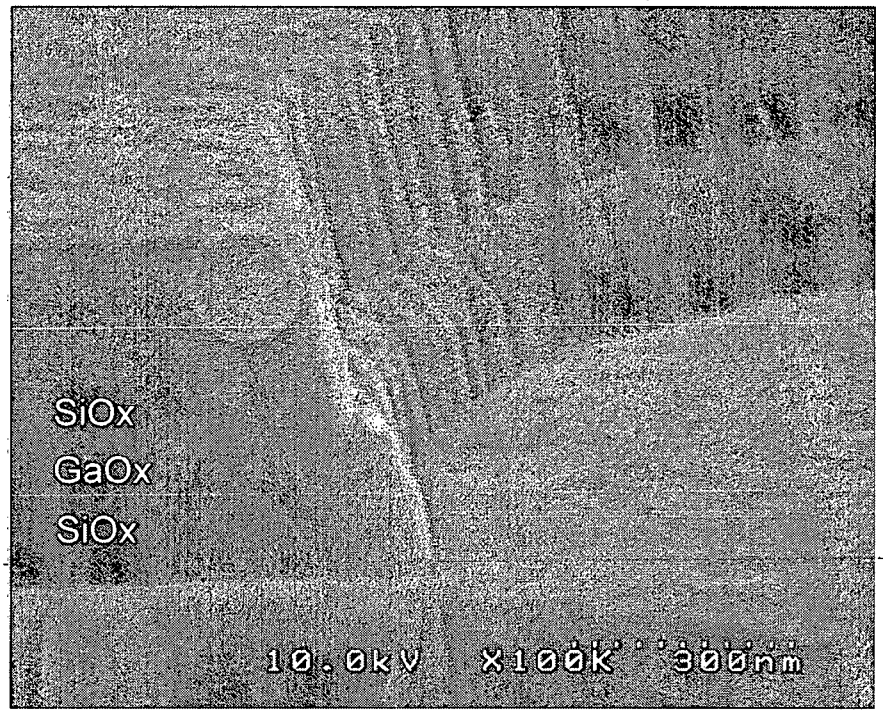
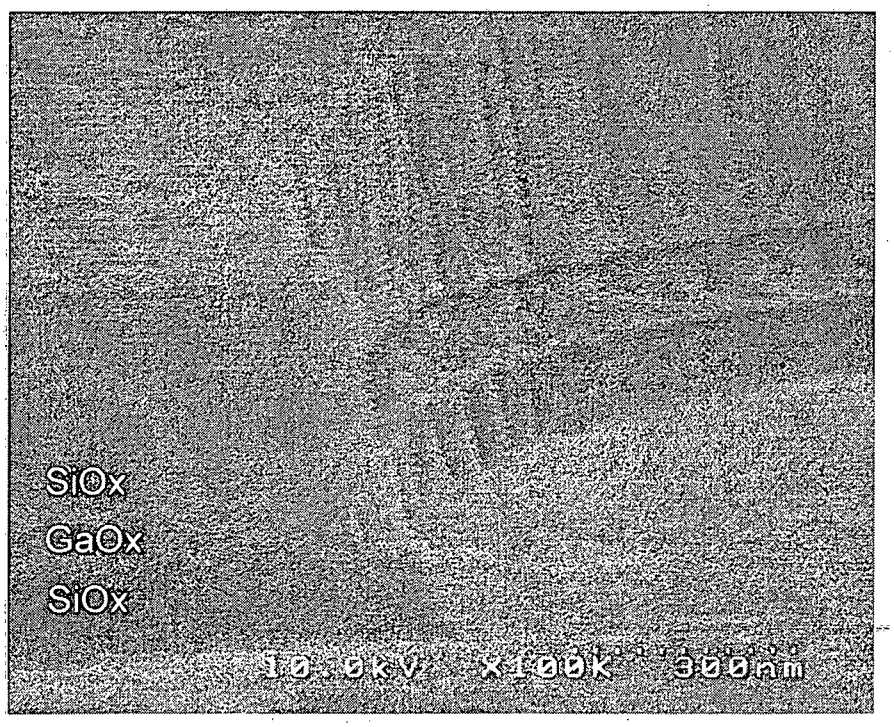


FIG. 11B



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/063092

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H01L29/786(2006.01)i, H01L21/28(2006.01)i, H01L21/336(2006.01)i, H01L21/768(2006.01)i, H01L23/522(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, H01L21/28, H01L21/336, H01L21/768, H01L23/522

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2004-335848 A (SEIKO EPSON CORPORATION) 2004.11.25, Par. Nos. [0026], [0036] to [0044], [0052], [0061], Figs 1 to 3 (Family: none)	1-20
Y	JP 2009-260329 A (ADVANCED LCD TECHNOLOGIES DEVELOPMENT CENTER CO., LTD.) 2009.11.05, Par. No. [0067] (Family: none)	1-20
Y	JP 2010-80952 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2010.04.08, Par. No. [0060], [0071] to [0078], Figs 26 to 30 & US 2010/0051949 A & EP 2159845 A1 & KR 10-2010-0027067 A & CN 101882630 A	2, 5, 7, 10, 13, 15-17, 19

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
01.07.2011	12.07.2011

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Japan Patent Office
3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan

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Soichiro Suzuki
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Telephone No. +81-3-3581-1101 Ext. 3498

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/063092

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2008-135520 A (CASIO COMPUTER CO., LTD.) 2008.06.12, Par. Nos. [0015] to [0022] (Family: none)	3, 6, 8, 11, 14, 17, 20
Y	JP 2008-270723 A (TOPPAN PRINTING CO., LTD.) 2008.11.06, Par. Nos. [0034], [0043] & US 2008/0237600 A1	4-8
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