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(54) **METHOD FOR ELECTROCHEMICAL PLATING ON SEMICONDUCTOR WAFERS**

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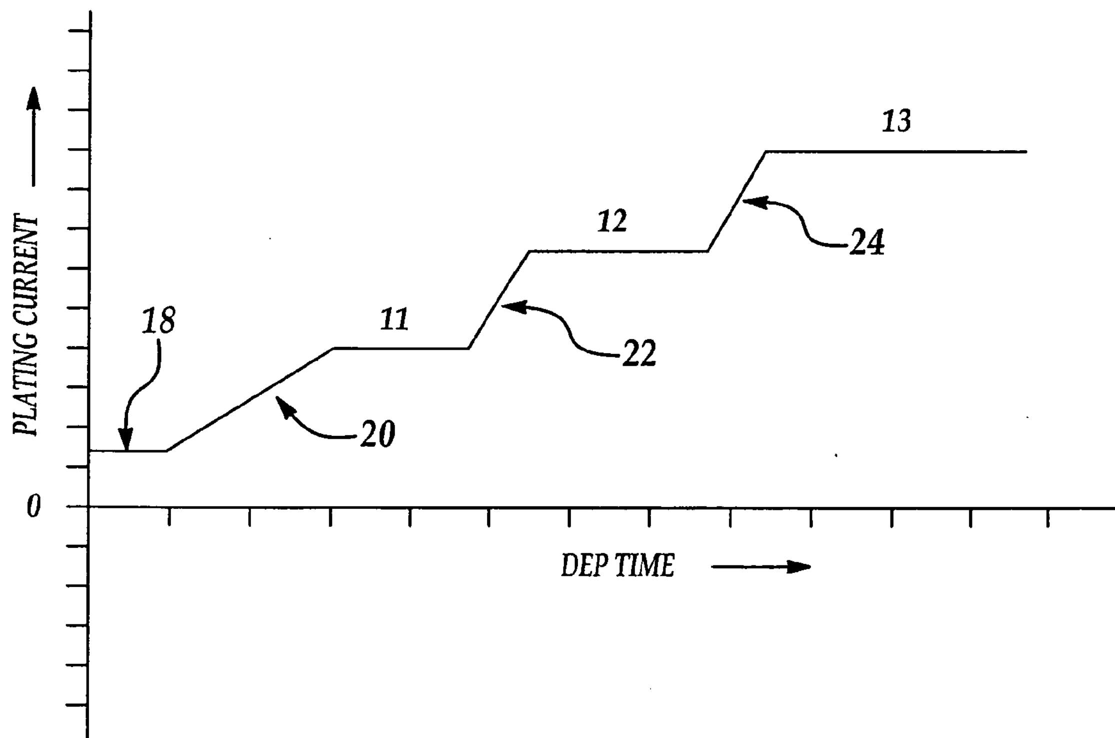
(57) **ABSTRACT**

A method of electroplating conductive material on semiconductor wafers improves deposited film quality by providing greater control over the formation of the film grain structure. Better grain size control is achieved by applying a continuous DC plating current to the wafer which avoids sharp discontinuities in the current as the applied current is increased in successive stages during a plating cycle. Current discontinuities are avoided by gradually increasing the current in a ramp-like fashion between the successive plating stages.



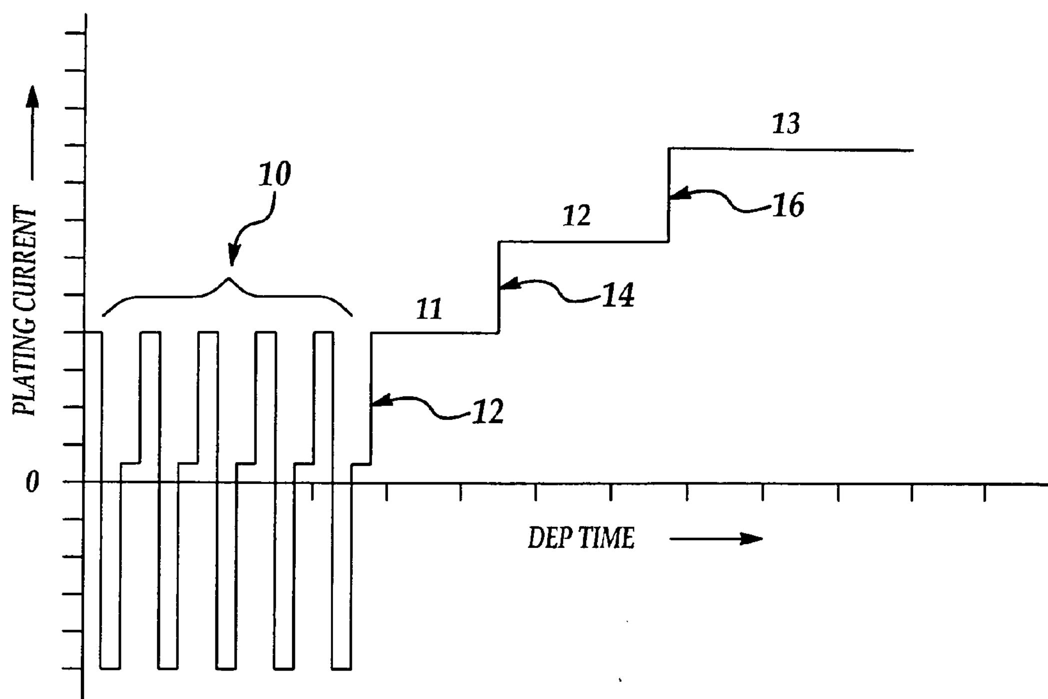


Figure 1
Prior Art

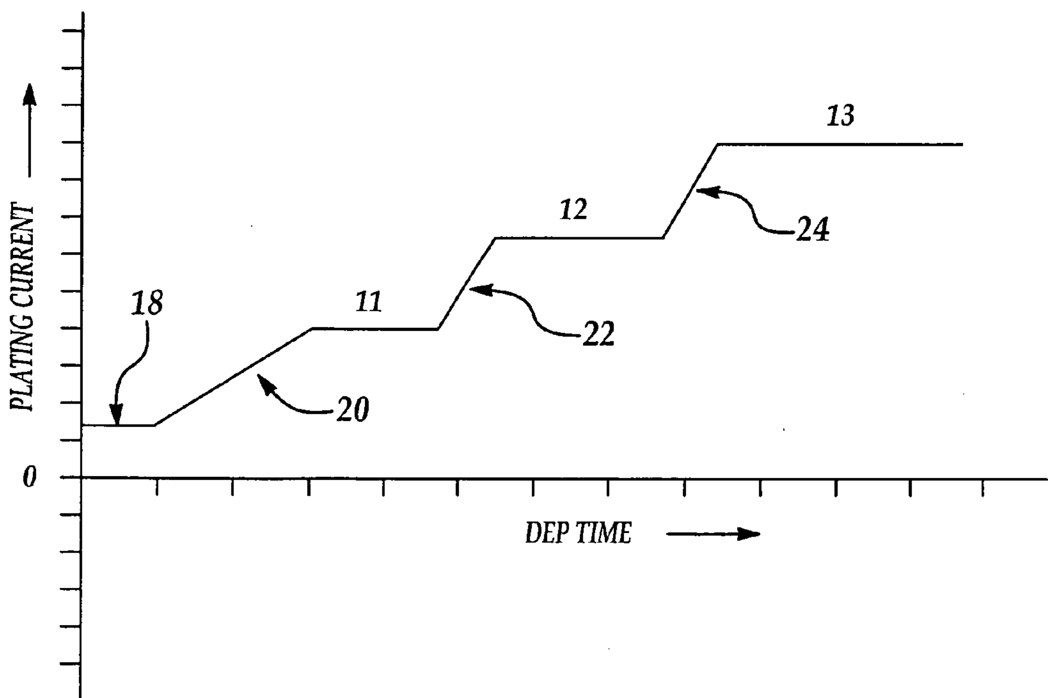


Figure 2

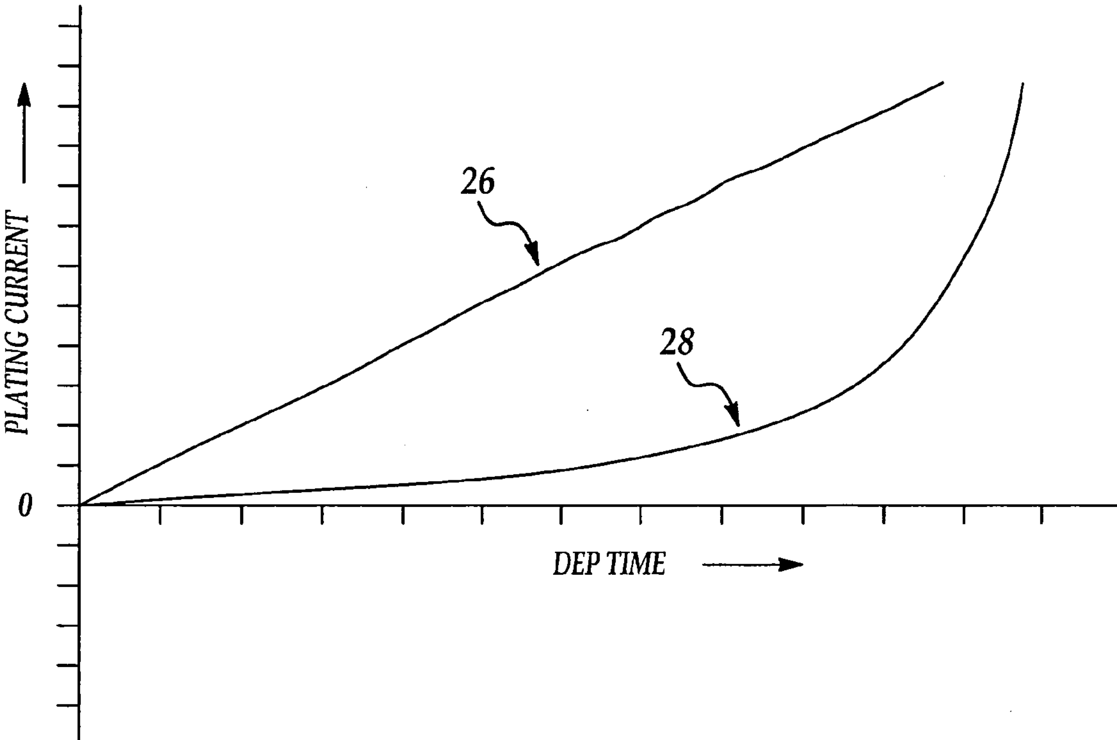


Figure 3

METHOD FOR ELECTROCHEMICAL PLATING ON SEMICONDUCTOR WAFERS

FIELD OF THE INVENTION

[0001] This invention generally relates to electrodeposition of conductive films on semiconductor wafers, and deals more particularly with an improved method of controlling the electroplating current in order to better control grain size and improve film quality.

BACKGROUND OF THE INVENTION

[0002] Many typical phototolithographic integrated circuit chip fabrication processes include a deposition phase in which material of different electrical characteristics is deposited in a space created in a diffusion material. Deposition phases of lithographic processes are often utilized to create components such as resistors, diodes and transistors, and electrical interconnections between components. Current technology electrical connections often include lines and plugs that are deposited in dielectric layers of the wafer. In the past, lines typically comprised aluminum, or an aluminum alloy, and plugs included tungsten. However, as component sizes become smaller and more layers of metallization are fabricated, interconnections comprising copper are becoming more prevelant. Copper interconnections typically provide several advantages over other materials, including lower electrical resistivity and better electromigration resistance. The techniques used to achieve copper metallization include CVD, selective electroless deposition, sputtering (PVD) and electroplating. Electrochemical deposition of copper is a leading technology because of its low cost, fast deposition rate, and superior copper properties. Copper interconnect electrodeposition faces a number of challenges in the form of non-uniformity of the copper layer over the wafer and filling small, high aspect ratio contactless without void formation.

[0003] Electrochemical plating techniques and apparatus are well developed in the art. The electrochemical deposition of copper is caused by the passage of the electrical current between two electrodes through a copper sulfate solution or other copper containing electrolytes. The electrical current to the electrode is electronic, while the current in the electrolyte is ionic. At the cathode, electrochemical reduction occurs, while electrochemical oxidation occurs at the anode which is normally formed of copper. In this arrangement, copper ions removed at the cathode are replaced by copper ions produced at the anode. Copper ions are transported to the cathode by electrical drift, diffusion and convection. Electroplating can be carried out at constant current, constant voltage or variable forms of current or voltage. The distribution of current, and hence the distribution of the thickness of the copper layer across the cathode depends on its geometry, the kinetics of the electrochemical reaction and concentration variations, as determined by the hydrodynamics and the convection mass transport in the electrolyte. In the case of copper electroplating on a silicon wafer, the SiO_2-covered wafer is coated with a thin conductive layer of copper, normally referred to as the seed layer, in order to assure electronic conductivity. The wafer is exposed to an electrolyte containing copper ions and the electrical contact is established between the seed layer and the power supply by several contact points along the periphery of the wafer. Constant current is passed for a certain length of time, resulting in a corresponding thickness of the copper layer.

[0004] Because copper reacts with SiO_2, it is necessary to confine it using a barrier layer material, such as tantalum nitride which is pre-deposited on the SiO_2 by sputtering. The copper seed layer is then deposited in order to assure good electrical contact and adhesion. Copper electroplating is usually obtained from an aqueous solution of $CUSO_4$ and H_2SO**4**, in the presence of several additives and leveling agents. Additives such as accelerators and suppressors are used to control the deposition rate and assure void-free filling of the sub-.25 micron high aspect ratio structures.

[0005] Rather than supply a single level of current throughout the plating process in order to achieve a desired thickness of the copper film, the electroplated copper film is formed in several distinct stages in which differing amounts of current, and sometimes voltages, are applied to achieve different deposition rates and microstructure formation. The electrical current is switched almost instantly from one level to another as one stage is finished and the next stage is commenced, resulting in a step-like discontinuity in the applied current waveform. It is known that the grain size formation of the copper film is directly related to current density, consequently a sharp change in grain structure occurs when the current is switched from one level to another. It is also known that there is a relationship between the grain size and resistivity; the larger the grain size, the lower the resistivity.

[0006] Sharp changes in grain size, and thus of resistivity, is undesirable for a number of reasons, including the creation of unbalanced thermal stresses, for example that can result in defects such as so called "edge pullback." Edge pullback is a phenomenon where low or sometimes no copper plating occurs on the edges of adjacent surface features. Accordingly, it would be desirable to provide an improved process for electroplating conductive metal such as copper which yields a more uniform grain size, avoids local stresses in the plated film, and increases the window for the thermal budget in post processing of the plated wafer. The present invention is directed toward satisfying this need.

SUMMARY OF THE INVENTION

[0007] According to one aspect of the invention, a method is provided for a electroplating conductive materials such as copper on a semiconductor wafer, comprising the steps of immersing the wafer in a plating bath; applying a continuous DC current to the wafer in order to effect electroplating of the material onto the wafer; increasing the magnitude of the DC current over time as the DC current is being continuously applied to the wafer. The DC current is increased gradually between successive stages of the plating process. These gradual increases in the applied electrical current are preferably linear.

[0008] According to another aspect of the invention, a method of electroplating and conductive material on a semiconductor wafer comprises the steps of immersing the wafer in a plating bath; applying a continuously positive DC current to the wafer in each of a plurality of separate stages in order to achieve differing plated material structures on the wafer; and, gradually increasing the applied current between the stages to avoid discontinuities in the current flow to the wafer.

[0009] As a result of the gradual increase of the current between successive stages, a more uniform and continuous grain structure is achieved throughout the plated film. As a result of the more uniform grain structure, thermal stresses within the film are reduced, and overall film quality is improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] In the drawings, which form an integral part of the specification and are to be read to the conjunction therewith, and in which like reference numerals are employed to designate identical components in the various views:

[0011] **FIG. 1** is a graph showing the current applied in a prior art, multistage electroplating process;

[0012] **FIG. 2** is a view similar to **FIG. 1**, but showing the applied current when using the method forming a preferred embodiment of the present invention; and,

[0013] **FIG. 3** is a graph showing the applied plating current. As a result of the smooth, continuous current between successive stages, a more uniform and continuous grain structure is achieved throughout the plated film. As a result of the more uniform grain structure, thermal stresses within the film are reduced, and overall film quality is improved. The more robust Cu film will not shrink or expand even by the high thermal budget of post process.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0014] Referring first to **FIG. 1**, a typical process for electroplating copper on a semiconductor wafer began with depositing a barrier layer of a material such as tantalum nitride by means of sputtering. Next, a seed layer of copper is applied over the barrier layer using, for example, atomic layer deposition techniques. The seed layer of copper is applied to assure good electrical contact and adhesion of subsequent layers of copper. The seed layer of copper may be between 100 and 1000 angstroms, for example. Copper electroplating is then performed using a conventional electroplating apparatus which includes a vessel (not shown) containing an aqueous solution of $CuSO_4$ and H_2SO_4, in the presence of various additives and leveling agents. The wafer is held by flexibly mounted gripping fingers (not shown) on the bottom of a spinning clam shell support which rotates the wafer while submerged within the plating bath. The wafer is electrically connected to a power source and acts as a cathode. A copper anode disposed within the bath is also connected to the electrical power source. Suitable pumps are used to create a flow of the plating bath over the face of the wafer as the latter is rotated up to speeds of 2000 rpms.

[0015] Typically, the "recipe" used to form the copper film calls for multiple steps or stages in which differing levels of electrical current are applied to the wafer for differing amounts of time. For example, one level of continuous or pulse current signals are delivered to the plating circuit as the wafer is initially being immersed, following which the current is increased to an intermediate but lower level but while the initial level of the film is being formed. Subsequently, the current is increased in order to accelerate the deposition process. These multiple stages are followed in order to obtain a desired grain structure and assure plating of specific wafer features, including filling gaps and trenches.

[0016] One typical recipe used in the prior art is shown in **FIG. 1** in which a series of alternating positive and negative current pulses **10** are initially applied, following which current is instantaneously increased at **12** to an initial, continuous level I**1**. After a desired period of time, the current is again instantaneously increased at **14** to a higher current level I**2**, and after another interval, time the current is finally increased in an instantaneous, step like fashion at **16** to highest level of current I**3**. From **FIG. 1** it can be seen that a series of "discontinuities" occur in the applied current, respectively at **12**, **14** and **16**. These discontinuities and the rapid changes in current flow result in relatively sharp boundaries between grain structures of differing sizes. These relatively sharp boundaries and differing grain structures produce stresses in the microstructure of the film which can impair film quality and even result in film defects.

[0017] In accordance with the present invention a novel method of electroplating conductive material on a semiconductor wafer controls transition in the applied current during successive stages of the electroplating process which substantially reduces or eliminates sharp changes in the grain structure of the plated film. Referring to **FIG. 2**, in accordance to the present invention, an initial, positive, continuous level of current is applied to the plating circuit at **18** for an initial period of time which could be considered the first step or stage in the plating recipe cycle. The current is then gradually increased at **20**, in a straight line or linear fashion over a period of time until the current increases to a second, higher level I**1** representing the second stage in the plating cycle. Similarly, the current is increased from I**1** to a higher level I**2** in a gradual, linear manner indicated at **22**. Finally, the current is increased from I**2** in a linear, gradual manner designated at **24** until current level I**3** is achieved representing the fourth and final stage of the plating process. Generally, during the first stage indicated at **18** an initial, thin film layer is formed. In the second stage the thickness of the film is increased at a more rapid deposition rate. During the third stage the time-current recipe is selected primarily to fill gaps following which the thickness of the film is increased until the last stage is reached which is particularly directed at filling trenches.

[0018] Applying a continuous, positive current to the wafer and gradually increasing the current from each level to a higher level has been found to provide a more continuous grain structure, free of sharp boundaries that can later result in thermal stresses causing defects or inadequate plating coverage. In contrast to the prior art method in which discontinuities are present in the current waveform, the current is applied in a continuous, smooth manner, free of sharp discontinuities.

[0019] As a result of the smooth, continuous current between successive stages, a more uniform and continuous grain structure is achieved throughout the plated film. As a result of the more uniform grain structure, thermal stresses within the film are reduced, and overall film quality is improved. The more robust Cu film will not shrink or expand even by the high thermal budget of post process.

[0020] From the forgoing, it is apparent that the novel method of electroplating conductive material on a semiconductor wafer not only provides for the reliable accomplishment of the objects of the invention but does so in a particularly simple and economical manner. Those skilled in

the art will recognize that various modifications may be made to the embodiment chosen to illustrate the invention without departing from the spirit and scope of the present contribution of the art. Accordingly, it is to be understood that the protection sought and to be afforded hereby should be deemed to extend to the subject matter claimed in all equivalents thereof fairly within the scope of the invention.

What is claimed is:

1. A method of electroplating conductive material on a semiconductor wafer, comprising the steps of:

(A) immersing the wafer in a plating bath;

(B) applying a continuous DC current to the wafer in order to effect electroplating of the material onto the wafer; and,

(C) increasing the magnitude of DC current over time as the DC current is being continuously applied to the wafer.

2. The method of claim 1, wherein:

step (C) includes increasing the applied DC current to each of a plurality of discrete current levels, and

step (B) includes gradually increasing the applied DC current between the discrete current levels.

3. The method of claim 1, wherein:

step (C) includes increasing the applied DC current from at least a first current level to a second current level, and

step (B) includes gradually ramping up the current from the first level to the second level.

4. The method of claim 2, wherein step (C) includes successively increasing the current in 3 stages to respectively deposit an initial film of the material on the wafer, fill gaps in the wafer and fill trenches in the wafer.

5. The method of claim 4, wherein step (B) includes gradually increasing the current between each of the stages.

6. The method of claim 1, wherein step (B) includes gradually ramping up the current between the successive stages.

7. The method of claim 5, wherein the gradual increase in current is essentially linear.

8. The method of claim 6, wherein each of the upward current ramps is linear.

9. The method of claim 1, wherein the continuously applied current in step (B) is a positive current.

10. The method of claim 1, wherein the material is copper.

11. A method of electroplating a conductive material on a semiconductor wafer, comprising the steps of:

(A) immersing the wafer in a plating bath;

(B) applying a continuously positive DC current to the wafer in each of a plurality of separate stages in order to achieve differing plated material structures on the wafer; and,

(C) gradually increasing the applied current between the stages to avoid discontinuities in the current flow to the wafer.

12. The method of claim 11, wherein:

step (B) includes increasing the applied DC current to each of a plurality of discrete current levels, and

step (C) includes gradually increasing the applied DC current between the discrete current levels.

13. The method of claim 11, wherein:

step (B) includes increasing the applied DC current from at least a first current level to a second current level, and

step (C) includes gradually ramping up the current from the first level to the second level.

14. The method of claim 12, wherein step (B) includes successively increasing the current in 3 stages to respectively deposit an initial film of the material on the wafer, fill gaps in the wafer and fill trenches in the wafer.

15. The method of claim 14, wherein the gradual increase of current in step (C) is linear.

16. The method of claim 11, wherein the gradual increase of current in step (C) is linear.

17. The method of claim 13, wherein the current is ramped linearly.

18. The method of claim 11, wherein the material is copper.

19. The method of claim 11, wherein step (B) the current is applied in 3 stages.

20. The method of claim 13, wherein the material is copper.

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