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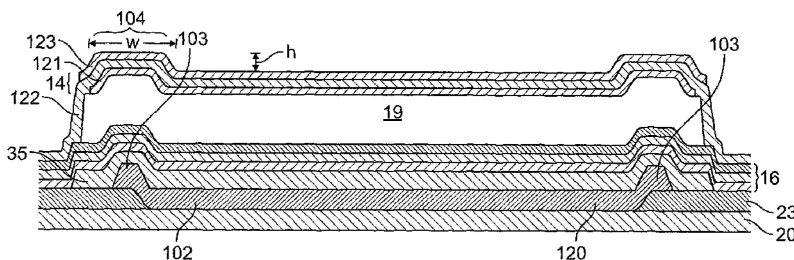

Figure 9M

(57) Abstract: This disclosure provides mechanical layers (14) and methods of forming the same. In one aspect, an electromechanical systems device includes a substrate (20) and a mechanical layer (14) having an actuated position and a relaxed position. The mechanical layer is spaced from the substrate to define a collapsible gap (19). The gap is in a collapsed condition when the mechanical layer is in the actuated position and in a non - collapsed condition when the mechanical layer is in the relaxed position. The mechanical layer includes a reflective layer(121), a conductive layer (123), and a supporting layer (122). The supporting layer is positioned between the reflective layer and the conductive layer and is configured to support the mechanical layer.

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MECHANICAL LAYER OF AN ELECTROMECHANICAL DEVICE AND METHODS OF FORMING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The disclosure claims priority to U.S. Provisional Patent Application No. 61/322,776 filed April 9, 2010 entitled “MECHANICAL LAYER AND METHODS OF FORMING THE SAME,” and assigned to the assignee hereof. The disclosure of the prior application is considered part of, and is incorporated by reference in, this disclosure.

TECHNICAL FIELD

[0002] The disclosure relates to electromechanical systems.

DESCRIPTION OF THE RELATED TECHNOLOGY

[0003] Electromechanical systems include devices having electrical and mechanical elements, actuators, transducers, sensors, optical components (e.g., mirrors) and electronics. Electromechanical systems can be manufactured at a variety of scales including, but not limited to, microscales and nanoscales. For example, microelectromechanical systems (MEMS) devices can include structures having sizes ranging from about a micron to hundreds of microns or more. Nanoelectromechanical systems (NEMS) devices can include structures having sizes smaller than a micron including, for example, sizes smaller than several hundred nanometers. Electromechanical elements may be created using deposition, etching, lithography, and/or other micromachining processes that etch away parts of substrates and/or deposited material layers, or that add layers to form electrical and electromechanical devices.

[0004] One type of electromechanical systems device is called an interferometric modulator (IMOD). As used herein, the term interferometric modulator or interferometric light modulator refers to a device that selectively absorbs and/or reflects light using the principles of optical interference. In some implementations, an interferometric modulator may include a pair of conductive plates, one or both of which may be transparent and/or reflective,

wholly or in part, and capable of relative motion upon application of an appropriate electrical signal. In an implementation, one plate may include a stationary layer deposited on a substrate and the other plate may include a reflective membrane separated from the stationary layer by an air gap. The position of one plate in relation to another can change the optical interference of light incident on the interferometric modulator. Interferometric modulator devices have a wide range of applications, and are anticipated to be used in improving existing products and creating new products, especially those with display capabilities.

[0005] An interferometric device array can include a mechanical layer that is anchored at corners of each pixel. There is a need for interferometric devices having smaller anchoring areas for the mechanical layer and improved fill factor.

SUMMARY

[0006] The systems, methods and devices of the disclosure each have several innovative aspects, no single one of which is solely responsible for the desirable attributes disclosed herein.

[0007] One innovative aspect of the subject matter described in this disclosure can be implemented in an electromechanical device including a substrate, a partially reflective optical stack disposed on the substrate, and a movable mechanical layer positioned so that the partially reflective optical stack is between the mechanical layer and the substrate, the mechanical layer including a reflective layer, a conductive layer, and a supporting layer that is disposed between the reflective layer and the conductive layer. The supporting layer is anchored on the optical stack in an optically non-active anchor region and extends from the anchor region away from the optical stack spacing the mechanical layer from the optical stack to define a collapsible gap between the mechanical layer and the optical stack. The mechanical layer is movable to an actuated position and a relaxed position by applying a voltage across the mechanical layer and a stationary electrode disposed between the substrate and the collapsible gap. The collapsible gap is in a collapsed state when the mechanical layer is in the actuated position and the gap is in a non-collapsed state when the mechanical layer is in the relaxed position.

[0008] In some implementations, the mechanical layer further includes a kink disposed adjacent to the anchor region and in at least a portion of an optically non-active region. In some implementations, the kink in the mechanical layer includes a rising portion extending away from the gap and a falling portion extending towards the gap.

[0009] In some implementations, the reflective layer and the conductive layer include aluminum alloys. In some implementations, the supporting layer includes silicon oxynitride (SiON).

[0010] Another innovative aspect of the subject matter described in this disclosure can be implemented in a device including a substrate, means for partially reflecting light disposed on the substrate, and movable means for interferometrically reflecting light. The movable reflecting light means includes a means for supporting the movable reflecting means, the supporting means anchored on the partially reflecting means in an optically non-active anchor region. The supporting means extends from the anchor region away from the partially reflecting means spacing the movable reflecting means from the partially reflecting means to define a collapsible gap between the movable reflecting light means and the partially reflecting light means. The movable reflecting light means is movable to an actuated position and a relaxed position by applying a voltage across the movable reflecting light means and a stationary electrode disposed between the substrate and the collapsible gap. The collapsible gap is in a collapsed state when the movable reflecting light means is in the actuated position and the gap is in a non-collapsed state when the movable reflecting light means is in the relaxed position.

[0011] In some implementations, the movable reflecting light means includes a reflective layer and a conductive layer, and the support layer is disposed between the reflective layer and the conductive layer.

[0012] Another innovative aspect of the subject matter described in this disclosure can be implemented in a method of forming a mechanical layer in an electromechanical device. The method includes providing a substrate, forming an optical stack over the substrate, providing a sacrificial layer over the optical stack, removing a portion of the sacrificial layer that is disposed over an anchoring region, forming a mechanical layer over the sacrificial layer and the anchoring region, and removing the sacrificial layer to form a collapsible gap between

the mechanical layer and the substrate. Forming the mechanical layer includes providing a reflective layer over the sacrificial layer, removing a portion of the reflective layer that is disposed over the anchoring region, providing a supporting layer over the reflective layer such that a portion of the supporting layer contacts the anchoring region, and providing a conductive layer over the supporting layer.

[0013] In some implementations, the method further includes depositing a shaping layer over at least a portion of the substrate, the shaping layer including at least one protrusion adjacent to the anchoring region. In some implementations, the method further includes forming the sacrificial layer as a conformal layer over the shaping layer including over the at least one protrusion, and forming the mechanical layer further includes forming the mechanical layer over the sacrificial layer and the shaping layer including the at least one protrusion as a conformal layer such that a kink is formed in a portion of the mechanical layer over each at least one protrusion.

[0014] Details of one or more implementations of the subject matter described in this specification are set forth in the accompanying drawings and the description below. Other features, aspects, and advantages will become apparent from the description, the drawings, and the claims. Note that the relative dimensions of the following figures may not be drawn to scale.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Figure 1 shows an example of an isometric view depicting two adjacent pixels in a series of pixels of an interferometric modulator (IMOD) display device.

[0016] Figure 2 shows an example of a system block diagram illustrating an electronic device incorporating a 3x3 interferometric modulator display.

[0017] Figure 3 shows an example of a diagram illustrating movable reflective layer position versus applied voltage for the interferometric modulator of Figure 1.

[0018] Figure 4 shows an example of a table illustrating various states of an interferometric modulator when various common and segment voltages are applied.

[0019] Figure 5A shows an example of a diagram illustrating a frame of display data in the 3x3 interferometric modulator display of Figure 2.

[0020] Figure 5B shows an example of a timing diagram for common and segment signals that may be used to write the frame of display data illustrated in Figure 5A.

[0021] Figure 6A shows an example of a partial cross-section of the interferometric modulator display of Figure 1.

[0022] Figures 6B–6E show examples of cross-sections of varying implementations of interferometric modulators.

[0023] Figure 7 shows an example of a flow diagram illustrating a manufacturing process for an interferometric modulator.

[0024] Figures 8A–8E show examples of cross-sectional schematic illustrations of various stages in a method of making an interferometric modulator.

[0025] Figures 9A–9P show examples of cross-sectional schematic illustrations of various stages in methods of making interferometric modulators according to various implementations.

[0026] Figures 10A–10C show examples of cross-sectional schematic illustrations of various interferometric modulator devices.

[0027] Figure 11 is a graph of simulated mechanical layer position in the actuated and relaxed states for three examples of interferometric modulator devices.

[0028] Figures 12A–12F show examples of cross-sectional schematic illustrations of various stages in a method of making an interferometric modulator.

[0029] Figure 13 shows an example of a flow diagram illustrating a manufacturing process for an interferometric modulator.

[0030] Figures 14A and 14B show examples of system block diagrams illustrating a display device that includes a plurality of interferometric modulators.

[0031] Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0032] The following detailed description is directed to some implementations for the purposes of describing the innovative aspects. However, the teachings herein can be applied in a multitude of different ways. The described implementations may be implemented

in any device that is configured to display an image, whether in motion (e.g., video) or stationary (e.g., still image), and whether textual, graphical or pictorial. More particularly, it is contemplated that the implementations may be implemented in or associated with a variety of electronic devices such as, but not limited to, mobile telephones, multimedia Internet enabled cellular telephones, mobile television receivers, wireless devices, smartphones, Bluetooth devices, personal data assistants (PDAs), wireless electronic mail receivers, hand-held or portable computers, netbooks, notebooks, smartbooks, printers, copiers, scanners, facsimile devices, GPS receivers/navigators, cameras, MP3 players, camcorders, game consoles, wrist watches, clocks, calculators, television monitors, flat panel displays, electronic reading devices (e.g., e-readers), computer monitors, auto displays (e.g., odometer display, etc.), cockpit controls and/or displays, camera view displays (e.g., display of a rear view camera in a vehicle), electronic photographs, electronic billboards or signs, projectors, architectural structures, microwaves, refrigerators, stereo systems, cassette recorders or players, DVD players, CD players, VCRs, radios, portable memory chips, washers, dryers, washer/dryers, parking meters, packaging (e.g., MEMS and non-MEMS), aesthetic structures (e.g., display of images on a piece of jewelry) and a variety of electromechanical systems devices. The teachings herein also can be used in non-display applications such as, but not limited to, electronic switching devices, radio frequency filters, sensors, accelerometers, gyroscopes, motion-sensing devices, magnetometers, inertial components for consumer electronics, parts of consumer electronics products, varactors, liquid crystal devices, electrophoretic devices, drive schemes, manufacturing processes, electronic test equipment. Thus, the teachings are not intended to be limited to the implementations depicted solely in the Figures, but instead have wide applicability as will be readily apparent to one having ordinary skill in the art.

[0033] An electromechanical device is disclosed having a self-supporting mechanical layer. In some implementations described herein, electromechanical devices are provided that can be formed without a post or rivet structure, thereby reducing the area of the anchoring region and permitting a pixel array with improved fill factor. Additionally, the mechanical layer can be flexible so as to reduce the bending height of the mechanical layer when in the actuated position. Reducing the mechanical layer bending height can decrease the

brightness of the portion of the mechanical layer that does not contact with the optical stack when the device is actuated, thereby improving the black state and increasing contrast ratio, gamut, and color saturation of a display that includes such devices.

[0034] Particular implementations of the subject matter described in this disclosure can be implemented to realize one or more of the following potential advantages. In some implementations, the subject matter described in this disclosure can be implemented to improve fill factor of a pixel array. Additionally, some implementations can reduce bending height of a mechanical layer. Furthermore, some implementations can increase contrast ratio, gamut, and/or color saturation of a display including such devices.

[0035] An example of a suitable electromechanical device, to which the described implementations may apply, is a reflective display device. Reflective display devices can incorporate interferometric modulators (IMODs) to selectively absorb and/or reflect light incident thereon using principles of optical interference. IMODs can include an absorber, a reflector that is movable with respect to the absorber, and an optical resonant cavity defined between the absorber and the reflector. The reflector can be moved to two or more different positions, which can change the size of the optical resonant cavity and thereby affect the reflectance of the interferometric modulator. The reflectance spectrums of IMODs can create fairly broad spectral bands which can be shifted across the visible wavelengths to generate different colors. The position of the spectral band can be adjusted by changing the thickness of the optical resonant cavity, i.e., by changing the position of the reflector.

[0036] Figure 1 shows an example of an isometric view depicting two adjacent pixels in a series of pixels of an interferometric modulator (IMOD) display device. The IMOD display device includes one or more interferometric MEMS display elements. In these devices, the pixels of the MEMS display elements can be in either a bright or dark state. In the bright ("relaxed," "open" or "on") state, the display element reflects a large portion of incident visible light, e.g., to a user. Conversely, in the dark ("actuated," "closed" or "off") state, the display element reflects little incident visible light. In some implementations, the light reflectance properties of the on and off states may be reversed. MEMS pixels can be configured to reflect predominantly at particular wavelengths allowing for a color display in addition to black and white.

[0037] The IMOD display device can include a row/column array of IMODs. Each IMOD can include a pair of reflective layers, i.e., a movable reflective layer and a fixed partially reflective layer, positioned at a variable and controllable distance from each other to form an air gap (also referred to as an optical gap or cavity). The movable reflective layer may be moved between at least two positions. In a first position, i.e., a relaxed position, the movable reflective layer can be positioned at a relatively large distance from the fixed partially reflective layer. In a second position, i.e., an actuated position, the movable reflective layer can be positioned more closely to the partially reflective layer. Incident light that reflects from the two layers can interfere constructively or destructively depending on the position of the movable reflective layer, producing either an overall reflective or non-reflective state for each pixel. In some implementations, the IMOD may be in a reflective state when unactuated, reflecting light within the visible spectrum, and may be in a dark state when unactuated, reflecting light outside of the visible range (e.g., infrared light). In some other implementations, however, an IMOD may be in a dark state when unactuated, and in a reflective state when actuated. In some implementations, the introduction of an applied voltage can drive the pixels to change states. In some other implementations, an applied charge can drive the pixels to change states.

[0038] The depicted portion of the pixel array in Figure 1 includes two adjacent interferometric modulators **12**. In the IMOD **12** on the left (as illustrated), a mechanical layer or movable reflective layer **14** is illustrated in a relaxed position at a predetermined distance from an optical stack **16**, which includes a partially reflective layer. The voltage V_0 applied across the IMOD **12** on the left is insufficient to cause actuation of the movable reflective layer **14**. In the IMOD **12** on the right, the movable reflective layer **14** is illustrated in an actuated position near or adjacent the optical stack **16**. The voltage V_{bias} applied across the IMOD **12** on the right is sufficient to maintain the movable reflective layer **14** in the actuated position.

[0039] In Figure 1, the reflective properties of pixels **12** are generally illustrated with arrows **13** indicating light incident upon the pixels **12**, and light **15** reflecting from the pixel **12** on the left. Although not illustrated in detail, most of the light **13** incident upon the pixels **12** will be transmitted through the transparent substrate **20**, toward the optical stack **16**.

A portion of the light incident upon the optical stack **16** will be transmitted through the partially reflective layer of the optical stack **16**, and a portion will be reflected back through the transparent substrate **20**. The portion of light **13** that is transmitted through the optical stack **16** will be reflected at the movable reflective layer **14**, back toward (and through) the transparent substrate **20**. Interference (constructive or destructive) between the light reflected from the partially reflective layer of the optical stack **16** and the light reflected from the movable reflective layer **14** will determine the wavelength(s) of light **15** reflected from the pixel **12**.

[0040] The optical stack **16** can include a single layer or several layers. The layer(s) can include one or more of an electrode layer, a partially reflective and partially transmissive layer and a transparent dielectric layer. In some implementations, the optical stack **16** is electrically conductive, partially transparent and partially reflective, and may be fabricated, for example, by depositing one or more of the above layers onto a transparent substrate **20**. The electrode layer can be formed from a variety of materials, such as various metals, for example indium tin oxide (ITO). The partially reflective layer can be formed from a variety of materials that are partially reflective, such as various metals, e.g., chromium (Cr), semiconductors, and dielectrics. The partially reflective layer can be formed of one or more layers of materials, and each of the layers can be formed of a single material or a combination of materials. In some implementations, the optical stack **16** can include a single semi-transparent thickness of metal or semiconductor which serves as both an optical absorber and conductor, while different, more conductive layers or portions (e.g., of the optical stack **16** or of other structures of the IMOD) can serve to bus signals between IMOD pixels. The optical stack **16** also can include one or more insulating or dielectric layers covering one or more conductive layers or a conductive/absorptive layer.

[0041] In some implementations, the layer(s) of the optical stack **16** can be patterned into parallel strips, and may form row electrodes in a display device as described further below. As will be understood by one having skill in the art, the term "patterned" is used herein to refer to masking as well as etching processes. In some implementations, a highly conductive and reflective material, such as aluminum (Al), may be used for the movable reflective layer **14**, and these strips may form column electrodes in a display device. The

movable reflective layer **14** may be formed as a series of parallel strips of a deposited metal layer or layers (orthogonal to the row electrodes of the optical stack **16**) to form columns deposited on top of posts **18** and an intervening sacrificial material deposited between the posts **18**. When the sacrificial material is etched away, a defined gap **19**, or optical cavity, can be formed between the movable reflective layer **14** and the optical stack **16**. In some implementations, the spacing between posts **18** may be approximately 1–1000 um, while the gap **19** may be on the order of less than 10,000 Angstroms (Å).

[0042] In some implementations, each pixel of the IMOD, whether in the actuated or relaxed state, is essentially a capacitor formed by the fixed and moving reflective layers. When no voltage is applied, the movable reflective layer **14** remains in a mechanically relaxed state, as illustrated by the pixel **12** on the left in Figure 1, with the gap **19** between the movable reflective layer **14** and optical stack **16**. However, when a potential difference, e.g., voltage, is applied to at least one of a selected row and column, the capacitor formed at the intersection of the row and column electrodes at the corresponding pixel becomes charged, and electrostatic forces pull the electrodes together. If the applied voltage exceeds a threshold, the movable reflective layer **14** can deform and move near or against the optical stack **16**. A dielectric layer (not shown) within the optical stack **16** may prevent shorting and control the separation distance between the layers **14** and **16**, as illustrated by the actuated pixel **12** on the right in Figure 1. The behavior is the same regardless of the polarity of the applied potential difference. Though a series of pixels in an array may be referred to in some instances as “rows” or “columns,” a person having ordinary skill in the art will readily understand that referring to one direction as a “row” and another as a “column” is arbitrary. Restated, in some orientations, the rows can be considered columns, and the columns considered to be rows. Furthermore, the display elements may be evenly arranged in orthogonal rows and columns (an “array”), or arranged in non-linear configurations, for example, having certain positional offsets with respect to one another (a “mosaic”). The terms “array” and “mosaic” may refer to either configuration. Thus, although the display is referred to as including an “array” or “mosaic,” the elements themselves need not be arranged orthogonally to one another, or disposed in an even distribution, in any instance, but may include arrangements having asymmetric shapes and unevenly distributed elements.

[0043] Figure 2 shows an example of a system block diagram illustrating an electronic device incorporating a 3x3 interferometric modulator display. The electronic device includes a processor **21** that may be configured to execute one or more software modules. In addition to executing an operating system, the processor **21** may be configured to execute one or more software applications, including a web browser, a telephone application, an email program, or any other software application.

[0044] The processor **21** can be configured to communicate with an array driver **22**. The array driver **22** can include a row driver circuit **24** and a column driver circuit **26** that provide signals to, e.g., a display array or panel **30**. The cross section of the IMOD display device illustrated in Figure 1 is shown by the lines 1–1 in Figure 2. Although Figure 2 illustrates a 3x3 array of IMODs for the sake of clarity, the display array **30** may contain a very large number of IMODs, and may have a different number of IMODs in rows than in columns, and vice versa.

[0045] Figure 3 shows an example of a diagram illustrating movable reflective layer position versus applied voltage for the interferometric modulator of Figure 1. For MEMS interferometric modulators, the row/column (i.e., common/segment) write procedure may take advantage of a hysteresis property of these devices as illustrated in Figure 3. An interferometric modulator may use, for example, about a 10-volt potential difference to cause the movable reflective layer, or mirror, to change from the relaxed state to the actuated state. When the voltage is reduced from that value, the movable reflective layer maintains its state as the voltage drops back below, e.g., 10-volts, however, the movable reflective layer does not relax completely until the voltage drops below 2-volts. Thus, a range of voltage, approximately 3 to 7-volts, as shown in Figure 3, exists where there is a window of applied voltage within which the device is stable in either the relaxed or actuated state. This is referred to herein as the “hysteresis window” or “stability window.” For a display array **30** having the hysteresis characteristics of Figure 3, the row/column write procedure can be designed to address one or more rows at a time, such that during the addressing of a given row, pixels in the addressed row that are to be actuated are exposed to a voltage difference of about 10-volts, and pixels that are to be relaxed are exposed to a voltage difference of near zero volts. After addressing, the pixels are exposed to a steady state or bias voltage difference

of approximately 5-volts such that they remain in the previous strobing state. In this example, after being addressed, each pixel sees a potential difference within the "stability window" of about 3–7-volts. This hysteresis property feature enables the pixel design, e.g., illustrated in Figure 1, to remain stable in either an actuated or relaxed pre-existing state under the same applied voltage conditions. Since each IMOD pixel, whether in the actuated or relaxed state, is essentially a capacitor formed by the fixed and moving reflective layers, this stable state can be held at a steady voltage within the hysteresis window without substantially consuming or losing power. Moreover, essentially little or no current flows into the IMOD pixel if the applied voltage potential remains substantially fixed.

[0046] In some implementations, a frame of an image may be created by applying data signals in the form of "segment" voltages along the set of column electrodes, in accordance with the desired change (if any) to the state of the pixels in a given row. Each row of the array can be addressed in turn, such that the frame is written one row at a time. To write the desired data to the pixels in a first row, segment voltages corresponding to the desired state of the pixels in the first row can be applied on the column electrodes, and a first row pulse in the form of a specific "common" voltage or signal can be applied to the first row electrode. The set of segment voltages can then be changed to correspond to the desired change (if any) to the state of the pixels in the second row, and a second common voltage can be applied to the second row electrode. In some implementations, the pixels in the first row are unaffected by the change in the segment voltages applied along the column electrodes, and remain in the state they were set to during the first common voltage row pulse. This process may be repeated for the entire series of rows, or alternatively, columns, in a sequential fashion to produce the image frame. The frames can be refreshed and/or updated with new image data by continually repeating this process at some desired number of frames per second.

[0047] The combination of segment and common signals applied across each pixel (that is, the potential difference across each pixel) determines the resulting state of each pixel. Figure 4 shows an example of a table illustrating various states of an interferometric modulator when various common and segment voltages are applied. As will be readily understood by one having ordinary skill in the art, the "segment" voltages can be applied to

either the column electrodes or the row electrodes, and the "common" voltages can be applied to the other of the column electrodes or the row electrodes.

[0048] As illustrated in Figure 4 (as well as in the timing diagram shown in Figure 5B), when a release voltage VC_{REL} is applied along a common line, all interferometric modulator elements along the common line will be placed in a relaxed state, alternatively referred to as a released or unactuated state, regardless of the voltage applied along the segment lines, i.e., high segment voltage VS_H and low segment voltage VS_L. In particular, when the release voltage VC_{REL} is applied along a common line, the potential voltage across the modulator (alternatively referred to as a pixel voltage) is within the relaxation window (see Figure 3, also referred to as a release window) both when the high segment voltage VS_H and the low segment voltage VS_L are applied along the corresponding segment line for that pixel.

[0049] When a hold voltage is applied on a common line, such as a high hold voltage VC_{HOLD_H} or a low hold voltage VC_{HOLD_L}, the state of the interferometric modulator will remain constant. For example, a relaxed IMOD will remain in a relaxed position, and an actuated IMOD will remain in an actuated position. The hold voltages can be selected such that the pixel voltage will remain within a stability window both when the high segment voltage VS_H and the low segment voltage VS_L are applied along the corresponding segment line. Thus, the segment voltage swing, i.e., the difference between the high VS_H and low segment voltage VS_L, is less than the width of either the positive or the negative stability window.

[0050] When an addressing, or actuation, voltage is applied on a common line, such as a high addressing voltage VC_{ADD_H} or a low addressing voltage VC_{ADD_L}, data can be selectively written to the modulators along that line by application of segment voltages along the respective segment lines. The segment voltages may be selected such that actuation is dependent upon the segment voltage applied. When an addressing voltage is applied along a common line, application of one segment voltage will result in a pixel voltage within a stability window, causing the pixel to remain unactuated. In contrast, application of the other segment voltage will result in a pixel voltage beyond the stability window, resulting in actuation of the pixel. The particular segment voltage which causes actuation can vary depending upon which

addressing voltage is used. In some implementations, when the high addressing voltage VC_{ADD_H} is applied along the common line, application of the high segment voltage VS_H can cause a modulator to remain in its current position, while application of the low segment voltage VS_L can cause actuation of the modulator. As a corollary, the effect of the segment voltages can be the opposite when a low addressing voltage VC_{ADD_L} is applied, with high segment voltage VS_H causing actuation of the modulator, and low segment voltage VS_L having no effect (i.e., remaining stable) on the state of the modulator.

[0051] In some implementations, hold voltages, address voltages, and segment voltages may be used which produce the same polarity potential difference across the modulators. In some other implementations, signals can be used which alternate the polarity of the potential difference of the modulators. Alternation of the polarity across the modulators (that is, alternation of the polarity of write procedures) may reduce or inhibit charge accumulation which could occur after repeated write operations of a single polarity.

[0052] Figure 5A shows an example of a diagram illustrating a frame of display data in the 3x3 interferometric modulator display of Figure 2. Figure 5B shows an example of a timing diagram for common and segment signals that may be used to write the frame of display data illustrated in Figure 5A. The signals can be applied to the, e.g., 3x3 array of Figure 2, which will ultimately result in the line time **60e** display arrangement illustrated in Figure 5A. The actuated modulators in Figure 5A are in a dark-state, i.e., where a substantial portion of the reflected light is outside of the visible spectrum so as to result in a dark appearance to, e.g., a viewer. Prior to writing the frame illustrated in Figure 5A, the pixels can be in any state, but the write procedure illustrated in the timing diagram of Figure 5B presumes that each modulator has been released and resides in an unactuated state before the first line time **60a**.

[0053] During the first line time **60a**, a release voltage **70** is applied on common line 1; the voltage applied on common line 2 begins at a high hold voltage **72** and moves to a release voltage **70**; and a low hold voltage **76** is applied along common line 3. Thus, the modulators (common 1, segment 1), (1,2) and (1,3) along common line 1 remain in a relaxed, or unactuated, state for the duration of the first line time **60a**, the modulators (2,1), (2,2) and (2,3) along common line 2 will move to a relaxed state, and the modulators (3,1), (3,2) and

(3,3) along common line 3 will remain in their previous state. With reference to Figure 4, the segment voltages applied along segment lines 1, 2 and 3 will have no effect on the state of the interferometric modulators, as none of common lines 1, 2 or 3 are being exposed to voltage levels causing actuation during line time **60a** (i.e., VC_{REL} – relax and VC_{HOLD_L} – stable).

[0054] During the second line time **60b**, the voltage on common line 1 moves to a high hold voltage **72**, and all modulators along common line 1 remain in a relaxed state regardless of the segment voltage applied because no addressing, or actuation, voltage was applied on the common line 1. The modulators along common line 2 remain in a relaxed state due to the application of the release voltage **70**, and the modulators (3,1), (3,2) and (3,3) along common line 3 will relax when the voltage along common line 3 moves to a release voltage **70**.

[0055] During the third line time **60c**, common line 1 is addressed by applying a high address voltage **74** on common line 1. Because a low segment voltage **64** is applied along segment lines 1 and 2 during the application of this address voltage, the pixel voltage across modulators (1,1) and (1,2) is greater than the high end of the positive stability window (i.e., the voltage differential exceeded a predefined threshold) of the modulators, and the modulators (1,1) and (1,2) are actuated. Conversely, because a high segment voltage **62** is applied along segment line 3, the pixel voltage across modulator (1,3) is less than that of modulators (1,1) and (1,2), and remains within the positive stability window of the modulator; modulator (1,3) thus remains relaxed. Also during line time **60c**, the voltage along common line 2 decreases to a low hold voltage **76**, and the voltage along common line 3 remains at a release voltage **70**, leaving the modulators along common lines 2 and 3 in a relaxed position.

[0056] During the fourth line time **60d**, the voltage on common line 1 returns to a high hold voltage **72**, leaving the modulators along common line 1 in their respective addressed states. The voltage on common line 2 is decreased to a low address voltage **78**. Because a high segment voltage **62** is applied along segment line 2, the pixel voltage across modulator (2,2) is below the lower end of the negative stability window of the modulator, causing the modulator (2,2) to actuate. Conversely, because a low segment voltage **64** is applied along segment lines 1 and 3, the modulators (2,1) and (2,3) remain in a relaxed

position. The voltage on common line 3 increases to a high hold voltage **72**, leaving the modulators along common line 3 in a relaxed state.

[0057] Finally, during the fifth line time **60e**, the voltage on common line 1 remains at high hold voltage **72**, and the voltage on common line 2 remains at a low hold voltage **76**, leaving the modulators along common lines 1 and 2 in their respective addressed states. The voltage on common line 3 increases to a high address voltage **74** to address the modulators along common line 3. As a low segment voltage **64** is applied on segment lines 2 and 3, the modulators (3,2) and (3,3) actuate, while the high segment voltage **62** applied along segment line 1 causes modulator (3,1) to remain in a relaxed position. Thus, at the end of the fifth line time **60e**, the 3x3 pixel array is in the state shown in Figure 5A, and will remain in that state as long as the hold voltages are applied along the common lines, regardless of variations in the segment voltage which may occur when modulators along other common lines (not shown) are being addressed.

[0058] In the timing diagram of Figure 5B, a given write procedure (i.e., line times **60a**–**60e**) can include the use of either high hold and address voltages, or low hold and address voltages. Once the write procedure has been completed for a given common line (and the common voltage is set to the hold voltage having the same polarity as the actuation voltage), the pixel voltage remains within a given stability window, and does not pass through the relaxation window until a release voltage is applied on that common line. Furthermore, as each modulator is released as part of the write procedure prior to addressing the modulator, the actuation time of a modulator, rather than the release time, may determine the line time. Specifically, in implementations in which the release time of a modulator is greater than the actuation time, the release voltage may be applied for longer than a single line time, as depicted in Figure 5B. In some other implementations, voltages applied along common lines or segment lines may vary to account for variations in the actuation and release voltages of different modulators, such as modulators of different colors.

[0059] The details of the structure of interferometric modulators that operate in accordance with the principles set forth above may vary widely. For example, Figures 6A–6E show examples of cross-sections of varying implementations of interferometric modulators, including the movable reflective layer 14 and its supporting structures. Figure 6A shows an

example of a partial cross-section of the interferometric modulator display of Figure 1, where a strip of metal material, i.e., the movable reflective layer **14** is deposited on supports **18** extending orthogonally from the substrate **20**. In Figure 6B, the movable reflective layer **14** of each IMOD is generally square or rectangular in shape and attached to supports at or near the corners, on tethers **32**. In Figure 6C, the movable reflective layer **14** is generally square or rectangular in shape and suspended from a deformable layer **34**, which may include a flexible metal. The deformable layer **34** can connect, directly or indirectly, to the substrate **20** around the perimeter of the movable reflective layer **14**. These connections are herein referred to as support posts. The implementation shown in Figure 6C has additional benefits deriving from the decoupling of the optical functions of the movable reflective layer **14** from its mechanical functions, which are carried out by the deformable layer **34**. This decoupling allows the structural design and materials used for the movable reflective layer **14** and those used for the deformable layer **34** to be optimized independently of one another.

[0060] Figure 6D shows another example of an IMOD, where the movable reflective layer **14** includes a reflective sub-layer **14a**. The movable reflective layer **14** rests on a support structure, such as support posts **18**. The support posts **18** provide separation of the movable reflective layer **14** from the lower stationary electrode (i.e., a portion of the optical stack **16** in the illustrated IMOD) so that a gap **19** is formed between the movable reflective layer **14** and the optical stack **16**, for example when the movable reflective layer **14** is in a relaxed position. The movable reflective layer **14** also can include a conductive layer **14c**, which may be configured to serve as an electrode, and a support layer **14b**. In this example, the conductive layer **14c** is disposed on one side of the support layer **14b**, distal from the substrate **20**, and the reflective sub-layer **14a** is disposed on the other side of the support layer **14b**, proximal to the substrate **20**. In some implementations, the reflective sub-layer **14a** can be conductive and can be disposed between the support layer **14b** and the optical stack **16**. The support layer **14b** can include one or more layers of a dielectric material, for example, silicon oxynitride (SiON) or silicon dioxide (SiO_2). In some implementations, the support layer **14b** can be a stack of layers, such as, for example, a SiO_2/SiON/SiO_2 tri-layer stack. Either or both of the reflective sub-layer **14a** and the conductive layer **14c** can include, e.g., an aluminum (Al) alloy with about 0.5% copper (Cu), or another reflective material. Employing

conductive layers **14a**, **14c** above and below the dielectric support layer **14b** can balance stresses and provide enhanced conduction. In some implementations, the reflective sub-layer 14a and the conductive layer **14c** can be formed of different materials for a variety of design purposes, such as achieving specific stress profiles within the movable reflective layer **14**.

[0061] As illustrated in Figure 6D, some implementations also can include a black mask structure **23**. The black mask structure **23** can be formed in optically inactive regions (e.g., between pixels or under posts **18**) to absorb ambient or stray light. The black mask structure **23** also can improve the optical properties of a display device by inhibiting light from being reflected from or transmitted through inactive portions of the display, thereby increasing the contrast ratio. Additionally, the black mask structure **23** can be conductive and be configured to function as an electrical bussing layer. In some implementations, the row electrodes can be connected to the black mask structure **23** to reduce the resistance of the connected row electrode. The black mask structure **23** can be formed using a variety of methods, including deposition and patterning techniques. The black mask structure **23** can include one or more layers. For example, in some implementations, the black mask structure **23** includes a molybdenum-chromium (MoCr) layer that serves as an optical absorber, a silicon dioxide (SiO_2) layer, and an aluminum alloy that serves as a reflector and a bussing layer, with a thickness in the range of about 30–80 Å, 500–1000 Å, and 500–6000 Å, respectively. The one or more layers can be patterned using a variety of techniques, including photolithography and dry etching, including, for example, carbon tetrafluoromethane (CF_4) and/or oxygen (O_2) for the MoCr and SiO_2 layers and chlorine (Cl_2) and/or boron trichloride (BCl_3) for the aluminum alloy layer. In some implementations, the black mask **23** can be an etalon or interferometric stack structure. In such interferometric stack black mask structures **23**, the conductive reflectors can be used to transmit or bus signals between lower, stationary electrodes in the optical stack **16** of each row or column. In some implementations, a spacer layer **35** can serve to generally electrically isolate the absorber layer **16a** from the conductive layers in the black mask **23**.

[0062] Figure 6E shows another example of an IMOD, where the movable reflective layer **14** is self supporting. In contrast with Figure 6D, the implementation of Figure 6E does not include support posts **18**. Instead, the movable reflective layer **14** contacts the

underlying optical stack **16** at multiple locations, and the curvature of the movable reflective layer **14** provides sufficient support that the movable reflective layer **14** returns to the unactuated position of Figure 6E when the voltage across the interferometric modulator is insufficient to cause actuation. The optical stack **16**, which may contain a plurality of several different layers, is shown here for clarity including an optical absorber **16a**, and a dielectric **16b**. In some implementations, the optical absorber **16a** may serve both as a fixed electrode and as a partially reflective layer.

[0063] In implementations such as those shown in Figures 6A–6E, the IMODs function as direct-view devices, in which images are viewed from the front side of the transparent substrate **20**, i.e., the side opposite to that upon which the modulator is arranged. In these implementations, the back portions of the device (that is, any portion of the display device behind the movable reflective layer **14**, including, for example, the deformable layer **34** illustrated in Figure 6C) can be configured and operated upon without impacting or negatively affecting the image quality of the display device, because the reflective layer **14** optically shields those portions of the device. For example, in some implementations a bus structure (not illustrated) can be included behind the movable reflective layer **14** which provides the ability to separate the optical properties of the modulator from the electromechanical properties of the modulator, such as voltage addressing and the movements that result from such addressing. Additionally, the implementations of Figures 6A–6E can simplify processing, such as, e.g., patterning.

[0064] Figure 7 shows an example of a flow diagram illustrating a manufacturing process **80** for an interferometric modulator, and Figures 8A–8E show examples of cross-sectional schematic illustrations of corresponding stages of such a manufacturing process **80**. In some implementations, the manufacturing process **80** can be implemented to manufacture, e.g., interferometric modulators of the general type illustrated in Figures 1 and 6, in addition to other blocks not shown in Figure 7. With reference to Figures 1, 6 and 7, the process **80** begins at block **82** with the formation of the optical stack **16** over the substrate **20**. Figure 8A illustrates such an optical stack **16** formed over the substrate **20**. The substrate **20** may be a transparent substrate such as glass or plastic, it may be flexible or relatively stiff and unbending, and may have been subjected to prior preparation processes, e.g., cleaning, to

facilitate efficient formation of the optical stack **16**. As discussed above, the optical stack 16 can be electrically conductive, partially transparent and partially reflective and may be fabricated, for example, by depositing one or more layers having the desired properties onto the transparent substrate **20**. In Figure 8A, the optical stack **16** includes a multilayer structure having sub-layers **16a** and **16b**, although more or fewer sub-layers may be included in some other implementations. In some implementations, one of the sub-layers **16a**, **16b** can be configured with both optically absorptive and conductive properties, such as the combined conductor/absorber sub-layer **16a**. Additionally, one or more of the sub-layers **16a**, **16b** can be patterned into parallel strips, and may form row electrodes in a display device. Such patterning can be performed by a masking and etching process or another suitable process known in the art. In some implementations, one of the sub-layers **16a**, **16b** can be an insulating or dielectric layer, such as sub-layer **16b** that is deposited over one or more metal layers (e.g., one or more reflective and/or conductive layers). In addition, the optical stack **16** can be patterned into individual and parallel strips that form the rows of the display.

[0065] The process **80** continues at block **84** with the formation of a sacrificial layer **25** over the optical stack **16**. The sacrificial layer **25** is later removed (e.g., at block **90**) to form the cavity **19** and thus the sacrificial layer **25** is not shown in the resulting interferometric modulators **12** illustrated in Figure 1. Figure 8B illustrates a partially fabricated device including a sacrificial layer **25** formed over the optical stack **16**. The formation of the sacrificial layer **25** over the optical stack **16** may include deposition of a xenon difluoride (XeF_2)-etchable material such as molybdenum (Mo) or amorphous silicon (a-Si), in a thickness selected to provide, after subsequent removal, a gap or cavity **19** (see also Figures 1 and 8E) having a desired design size. Deposition of the sacrificial material may be carried out using deposition techniques such as physical vapor deposition (PVD, e.g., sputtering), plasma-enhanced chemical vapor deposition (PECVD), thermal chemical vapor deposition (thermal CVD), or spin-coating.

[0066] The process **80** continues at block **86** with the formation of a support structure e.g., a post **18** as illustrated in Figures 1, 6 and 8C. The formation of the post **18** may include patterning the sacrificial layer **25** to form a support structure aperture, then depositing a material (e.g., a polymer or an inorganic material, e.g., silicon oxide) into the

aperture to form the post **18**, using a deposition method such as PVD, PECVD, thermal CVD, or spin-coating. In some implementations, the support structure aperture formed in the sacrificial layer can extend through both the sacrificial layer **25** and the optical stack **16** to the underlying substrate **20**, so that the lower end of the post **18** contacts the substrate **20** as illustrated in Figure 6A. Alternatively, as depicted in Figure 8C, the aperture formed in the sacrificial layer **25** can extend through the sacrificial layer **25**, but not through the optical stack **16**. For example, Figure 8E illustrates the lower ends of the support posts **18** in contact with an upper surface of the optical stack **16**. The post **18**, or other support structures, may be formed by depositing a layer of support structure material over the sacrificial layer **25** and patterning to remove portions of the support structure material located away from apertures in the sacrificial layer **25**. The support structures may be located within the apertures, as illustrated in Figure 8C, but also can, at least partially, extend over a portion of the sacrificial layer **25**. As noted above, the patterning of the sacrificial layer **25** and/or the support posts **18** can be performed by a patterning and etching process, but also may be performed by alternative etching methods.

[0067] The process **80** continues at block **88** with the formation of a movable reflective layer or membrane such as the movable reflective layer **14** illustrated in Figures 1, 6 and 8D. The movable reflective layer **14** may be formed by employing one or more deposition steps, e.g., reflective layer (e.g., aluminum, aluminum alloy) deposition, along with one or more patterning, masking, and/or etching steps. The movable reflective layer **14** can be electrically conductive, and referred to as an electrically conductive layer. In some implementations, the movable reflective layer **14** may include a plurality of sub-layers **14a**, **14b**, **14c** as shown in Figure 8D. In some implementations, one or more of the sub-layers, such as sub-layers **14a**, **14c**, may include highly reflective sub-layers selected for their optical properties, and another sub-layer **14b** may include a mechanical sub-layer selected for its mechanical properties. Since the sacrificial layer **25** is still present in the partially fabricated interferometric modulator formed at block **88**, the movable reflective layer **14** is typically not movable at this stage. A partially fabricated IMOD that contains a sacrificial layer **25** may also be referred to herein as an "unreleased" IMOD. As described above in connection with

Figure 1, the movable reflective layer **14** can be patterned into individual and parallel strips that form the columns of the display.

[0068] The process **80** continues at block **90** with the formation of a cavity, e.g., cavity **19** as illustrated in Figures 1, 6 and 8E. The cavity **19** may be formed by exposing the sacrificial material **25** (deposited at block **84**) to an etchant. For example, an etchable sacrificial material such as molybdenum (Mo) or amorphous silicon (a-Si) may be removed by dry chemical etching, e.g., by exposing the sacrificial layer **25** to a gaseous or vaporous etchant, such as vapors derived from solid xenon difluoride (XeF_2) for a period of time that is effective to remove the desired amount of material, typically selectively removed relative to the structures surrounding the cavity **19**. Other etching methods, e.g. wet etching and/or plasma etching, also may be used. Since the sacrificial layer **25** is removed during block **90**, the movable reflective layer **14** is typically movable after this stage. After removal of the sacrificial material **25**, the resulting fully or partially fabricated IMOD may be referred to herein as a "released" IMOD.

[0069] In some implementations, self-supporting electromechanical devices can be formed that do not use a post or rivet structure, but instead use a portion of the mechanical layer to support the rest of the mechanical layer to be positioned above the optical stack. Some examples of implementations of self-supported mechanical layers are illustrated in Figures 6C, 6E, 9O, and 10C. Such devices can have a reduced bending height when in the actuated position, which can reduce the portion of the mechanical layer that is not in contact with the optical stack during actuation. In other words, reducing the bending height can increase the overall or side-to-side flatness of the portion of the mechanical layer that is in an optically active area of a pixel, in particular at the edges of the active area pixel. Having a more uniformly flat contact area in the active area of a pixel improves the uniformity of a reflection characteristic of the device when in the actuated state (for example, the "black" state) and can increase contrast ratio, gamut, and/or color saturation of a display using such devices. Additionally, mechanical layers that are configured to be self-supporting also can use a reduced area to anchor the mechanical layer over the substrate (e.g., on the substrate, the optical stack, or another intervening layer between the substrate and the particular regions that

the mechanical layer contacts when anchored) at corners of pixels, thereby improving fill factor when the device is disposed in a pixel array.

[0070] Figures 9A–9P show examples of cross-sectional schematic illustrations of various stages in methods of making interferometric modulators according to various implementations. While particular parts and steps are described as suitable for interferometric modulator implementations, in other electromechanical device implementations different materials can be used or parts can be modified, omitted, or added.

[0071] In Figure 9A, a black mask structure **23** has been provided and patterned on a substrate **20**. The substrate **20** can be formed from a variety of materials, including glass or a transparent polymeric material which permits images to be viewed through the substrate **20**. The substrate **20** can be subjected to one or more prior preparation steps such as, for example, a cleaning step to facilitate efficient formation of black mask structure **23**. Additionally, one or more layers can be provided on the substrate before providing the black mask structure **23**. For example, in one embodiment, an aluminum oxide layer having a thickness in the range of about 50–250 Å is provided on the substrate before formation of the black mask structure **23**, and the aluminum oxide layer can serve as an etch-stop when patterning the black mask structure.

[0072] The black mask structure **23** can be configured to absorb ambient or stray light in optically inactive regions (e.g., between pixels) to improve the optical properties of a display device by increasing the contrast ratio. Additionally, the black mask structure **23** can include a plurality of layers, including a conductive layer configured to function as an electrical bussing layer. In one embodiment, the row electrodes are connected to the black mask structure **23** to reduce the resistance of the connected row electrode. The black mask structure **23** can be formed using a variety of methods, including deposition and patterning techniques. As used herein, and as will be understood by one having skill in the art, the term "patterned" is used herein to refer to masking as well as etching processes. Although Figure 9A is shown as including the black mask structure **23**, methods of forming a mechanical layer as described herein also can be applicable to processes lacking the black mask structure **23**.

[0073] Figure 9B illustrates providing a shaping structure **102** over the substrate **20** and the black mask structure **23**. The shaping structure **102** can include a buffer oxide,

such as silicon dioxide (SiO_2) and/or silicon oxynitride (SiON), and can aid in maintaining a relatively planar profile across the substrate by filling in gaps between bussing or black mask structures **23**. In one embodiment, the shaping structure **102** has a thickness in the range of about 500–6000 Å. However, the shaping structure **102** can have a variety of thicknesses depending on the desired optical properties of the interferometric modulator.

[0074] The shaping structure **102** can be used to form a kink in the mechanical layer, as will be described in detail below (for example, in reference to Figure 9M). In particular, one or more layers, including the mechanical layer, can be deposited over the shaping structure **102**, thereby substantially replicating one or more geometric features of the shaping structure **102**. For example, as illustrated in Figure 9B, the shaping structure **102** can overlap the black mask structure **23**, thereby forming a protrusion **103**. The protrusion **103** can produce an upwardly extending portion wave (or kink) in a subsequently deposited conformal layer, such as a subsequently deposited mechanical layer.

[0075] A thickness dimension of the shaping structure **102**, including the protrusion **103**, can be used to adjust the relative heights of the "rising" and "falling" structural portions of the kink **104**. This can affect (or control) stress characteristics in a subsequently deposited mechanical layer to achieve a desired mirror curvature and/or a launch height, as will be described below. In the illustrated example, the thickness and shape of the shaping structure **102** and the thickness of the black mask **23**, can affect characteristics or dimensions of the kink **104**, for example, its height, symmetry, width and/or the angle of its non-flat portions.

[0076] Although various electromechanical systems devices illustrated herein are shown and described as including the shaping structure **102**, the methods of forming a mechanical layer as described herein can be applicable to processes lacking the shaping structure **102**. For example, the embodiment shown in Figure 9P is one example of an electromechanical systems device produced as described herein without the shaping structure **102**.

[0077] Figures 9C illustrates an example of providing a dielectric structure **35,** which is formed over the shaping structure **102** and the black mask **23**. Figure 9D illustrates an example of patterning the dielectric structure **35**. Materials used for the dielectric structure

35 can include, for example, silicon dioxide (SiO_2), silicon oxynitride (SiON), and/or tetraethyl orthosilicate (TEOS). In one embodiment, the thickness of the dielectric structure **35** is in the range of about 3000–5000 Å. However, the dielectric structure **35** can be configured to have a variety of thicknesses depending on desired optical properties of the modulator. In some implementations, a portion of the dielectric structure **35** can be removed above the black mask structure **23** ("above" here refers to the side of the black mask structure **23** opposite the substrate **20**), to permit routing of electrodes (e.g., row electrodes) to the black mask structure **23** in implementations in which the black mask structure **23** serves to bus signals. As illustrated in Figure 9D, the dielectric structure **35** can be deposited conformally such that the protrusion **103** produces a kink in the dielectric structure **35**, and this shape can be propagated up to subsequently deposited conformal layers, as illustrated in Figures 9E–9O.

[0078] Figure 9E illustrates an example of providing an optical stack **16** formed over the dielectric structure **35** and the black mask structure **23**. The optical stack **16** can include a plurality of layers, including, for example, a transparent conductor, such as indium tin oxide (ITO), a partially reflective optical absorber layer, such as chromium, and a transparent dielectric. The optical stack **16** can thus be electrically conductive, partially transparent and partially reflective. As illustrated in Figure 9E, one or more layers of the optical stack **16** may physically and electrically contact the black mask structure **23**.

[0079] Figures 9F and 9G illustrate examples of providing a sacrificial layer **25** over the optical stack **16** and patterning the sacrificial layer **25**. The sacrificial layer **25** is later removed to form a gap (or cavity). In some implementations, the sacrificial layer **25** can include more than one layer, or include a layer of varying thickness, to aid in the formation of a display device having a multitude of display elements that include different size gaps between the mechanical layer and the optical layer **16**. For an interferometric modulator array, each different gap size may produce different reflected color. As shown in Figure 9G, the sacrificial layer **25** can be removed in the region between pixels to form anchoring holes or regions **132**. The anchoring regions **132** is an area formed to permit a subsequently deposited layer, such as a dielectric or supporting layer of a mechanical layer to contact one or more layers underlying the sacrificial layer **25**, thereby aiding in forming a self-supporting mechanical layer, as will be described below.

[0080] Figures 9H illustrates implementations having a reflective layer **121** over the sacrificial layer **25** and optical stack **16.** Figure 9I illustrates an example of an implementation after patterning the reflective layer **121** to remove the portion of the reflective layer that is disposed over the anchor regions **132**. As illustrated in Figure 9H, the reflective layer **121** can be provided conformally over the sacrificial layer **25** and the optical stack **16**. Thereafter, as shown in Figure 9I, a portion of the reflective layer **121** over the anchor regions **132** can be removed to permit a subsequently deposited layer to contact the optical stack **16**, thereby aiding in the formation of a self-supporting mechanical layer, as will be described in further detail below. The reflective layer **121** can be formed from any suitable reflective material, including, for example, a metal, such as an aluminum alloy. In one implementation, the reflective layer **121** includes aluminum-copper (AlCu) having copper by weight in the range of about 0.3 % to 1.0%, for example, about 0.5%. The thickness of the reflective layer **121** can be any suitable thickness, such as a thickness in the range of about 200–500 Å, for example, about 300 Å.

[0081] Figure 9J illustrates a supporting layer **122** formed over the reflective layer **121**, the sacrificial layer **25**, and the optical stack **16**. The supporting layer **122** can be a dielectric layer of, for example, silicon oxynitride (SiON). As will be described in further detail below, characteristics (e.g., thickness) of the supporting layer **122** can be selected to provide at least partial support for the mechanical layer in the actuated and relaxed positions without the need for a post or rivet structure. Configuring the supporting layer **122** to provide at least partial support for the mechanical layer can increase the density of pixels as compared to a design in which the mechanical layer is supported by posts or rivets. In one implementation, the thickness of the supporting layer **122** can be in the range of about 500–8000 Å. The thickness of the supporting layer **122** can be determined based on a variety of factors, including, for example, the desired stiffness of the supporting layer **122**, which can aid in achieving the same pixel actuation voltage for pixels having different sized air-gaps in color display applications.

[0082] Figures 9K illustrates an implementation having a conductive or cap layer **123** formed (or provided) over the supporting layer **122.** Figure 9L illustrates an example of a patterned conductive layer **123** and patterning the conductive layer **123** to form a portion of a

mechanical layer **14**. The sacrificial layer **25** is still present so the mechanical layer **14** is typically not moveable at this stage. The conductive layer **123** can be provided conformally over the supporting layer **122** and patterned so as to substantially replicate the pattern of the reflective layer **121**, thereby aiding in balancing stresses in the mechanical layer **14**. The conductive layer **123** can include a metallic material, for example, the same aluminum alloy as the reflective layer **121**. In one implementation, the conductive layer **123** includes aluminum-copper (AlCu) having copper by weight in the range of about 0.3 % to 1.0%, for example, about 0.5%, and the thickness of the conductive layer **123** is selected to be in the range of about 200–500 Å, for example, about 300 Å.

[0083] The reflective layer **121** and the conductive layer **123** can be formed to have similar thickness and composition, thereby aiding in balancing stresses in the mechanical layer. Having balanced stresses in the mechanical layer can reduce the sensitivity of deformation of the mechanical layer, and correspondingly changes in the gap height due to temperature variation. Additionally, forming the reflective layer **121** and the conductive layer **123** from similar materials that have similar thermal coefficients of expansion can further reduce deformation of the mechanical layer, and variations in the gap height, caused by changes in temperature.

[0084] Figure 9M illustrates the removal of the sacrificial layer **25** and the formation of a gap **19**. The sacrificial layer **25** can be removed at this point to form the gap **19** using a variety of methods, as was described above. Before it is removed, the sacrificial layer **25** can provide a counterforce that can prevent the mechanical layer **14** from deflecting under the influence of residual stresses, such as residual stresses in one or more sub-layers of the mechanical layer **14**. However, upon removal of the sacrificial layer **25**, the stress-induced forces of the mechanical layer **14** can cause the mechanical layer **14** to change shape and/or curvature and to become displaced away from the pre-released position by a distance of a "launch height".

[0085] Having a particular distance or "launch height" of the mechanical layer **14** away from the pre-released position can be desirable to mitigate stiction. For example, forming a pixel in an interferometric modulator to have a selected pixel launch height to be in the range of about 500 Å to about 1000 Å away from the pre-released position can reduce

pixel stiction between the mechanical layer **14** and the optical stack **16**. However, a relatively large pixel launch height can decrease the sacrificial layer thickness needed for a particular gap size to a level which is not desirable from a fabrication standpoint.

[0086] Still referring to Figure 9M, the mechanical layer **14** includes a bend, or a kink **104**, that is formed by providing the mechanical layer **14** over the shaping structure **102**, and particularly over the protrusion **103**, with the intervening layers formed conformally. The kink **104** is aligned with the shaping structure, for example, the kink **104** is vertically aligned relative to the shaping structure **102** when the substrate **20** is oriented horizontally. In implementations having one or more layers that are formed over the shaping structure **102** and there are multiple layers formed over the protrusion **103** before the mechanical layer **14** is formed, the kink **104** in the mechanical layer is wider than the protrusion **103**. The kink **104** can have certain geometric features. The geometric features can be controlled by varying the geometry of the shaping structure **102** and the protrusion **103** to form a mechanical layer having a desired shape that affects (or controls) the mechanical stresses in the mechanical layer **14**. For example, the kink **104** can be shaped to control the launch height of the mechanical layer upon release. Control of the launch height can allow the selection of a sacrificial layer thickness needed for a particular gap size which is desirable from a fabrication and optical performance standpoint. Additionally, the kink **104** can be employed to control the curvature of the mechanical layer after release, and so that the mechanical layer is substantially flat when under bias. In some implementations, the height **h** of the kink **104** is selected to be about 100–6000 Å, or more particularly 400–5000 Å. The width **w** of the kink can be selected to be, for example, a width in the range of about 0.2 µm–5µm, or more particularly, about 0.5 µm–2µm. In some implementations, the kink **104** can be spaced from the anchoring region by, for example, a distance of less than about 5 µm.

[0087] Figure 9M illustrates an example of an implementation having a supporting layer **122** configured to support the mechanical layer **14** without the need for a post or rivet structure. Such implementations can allow for arrangements of increased pixel density. This also can increases the fill factor of pixels for a certain area, as compared to implementations where the mechanical layer is supported by posts or rivets that use a larger anchor footprint.

[0088] Figures 9N–9O illustrates an example of another implementation of an interferometric device. Specifically, Figure 9N illustrates a dielectric layer **124** that was provided (or formed) over the conductive layer **123** and the supporting layer **122,** (shown in Figure 9L) to form a mechanical layer **14**. The dielectric layer **124** includes a dielectric material for example, silicon oxynitride (SiON). In implementation, The dielectric layer **124** can be configured to have a thickness in the range of about 500–4000 Å. Figure 9O illustrates the device illustrated in Figure 9N after forming a gap **19** (or cavity) between the optical stack **16** and the mechanical layer **14**. The sacrificial layer can be removed in a manner similar to that described above with reference to Figure 9M.

[0089] The dielectric layer **124** can aid in controlling the stresses in the mechanical layer **14**. For example, the dielectric layer **124** can be formed to have a stress greater than or less than the stress of the supporting layer **122,** which affects the launch height of the mechanical layer **14** when the sacrificial layer **25** is removed. Control of the launch height can determine the selection of a sacrificial layer thickness needed for a particular gap size which is desirable from a fabrication and optical performance standpoint. Additionally, the dielectric layer **124** can be configured (e.g., to have a certain thickness or stress) to control the curvature of the mechanical layer **14** after release, and so that the mechanical layer **14** is substantially flat when under bias. The dielectric layer **124** and the kink **104** each can be configured (e.g., with a certain height, width, and/or thickness dimension) to control the shaping and curvature of the mechanical layer **14** which can aid increasing design flexibility of the interferometric modulator.

[0090] In some implementations, one or more additional layers can be formed over the dielectric layer **124** of the electromechanical systems device shown in Figure 9N before the mechanical layer is released. For example, an additional conductive layer can be provided over the dielectric layer **124** before release. The additional conductive layer can include a metallic material (for example an aluminum alloy), and can be patterned to have a similar shape as the reflective and cap layers **121**, **123**. In one implementation, the additional conductive layer includes aluminum-copper (AlCu) having copper by weight in the range of about 0.3 % and 1.0%, for example, about 0.5%. The additional conductive layer can be configured to have a thickness of between about 200 and about 500 Å. In some particular

implementations the additional conductive layer has a thickness of about 300Å. The additional conductive layer can cause the mechanical layer to be substantially symmetric (e.g., the stress of the material forming the conductive layer, disposed on one side of the supporting layer, is the same or similar to the stress of the material forming the reflective layer) which aids in balancing stresses in the mechanical layer. Mechanical layers formed to have balanced stresses can reduce the amount of change in the gap height due to variations in temperature.

[0091] Figures 9P illustrates an interferometric device according to another implementation. In contrast to the electromechanical systems device illustrated in Figure 9M, the electromechanical systems device example illustrated in Figure 9P does not include the shaping structure **102** and the kink **104**. The supporting layer **122** can include a dielectric material, for example, silicon oxynitride (SiON). The thickness of the supporting layer **122** can be formed to have a thickness that is sufficient to provide support for the mechanical layer **14** in the actuated and relaxed positions, without the need for a post or rivet supporting structure. Configuring the supporting layer **122** to provide support for the mechanical layer **14** can increase the density of pixels as compared to a design in which support is provided by posts or rivets. In one implementation, supporting layer **122** has a thickness of about 500–8000 Å.

[0092] Although not illustrated in the implementation shown in Figure 9P, a dielectric layer can be included over the conductive layer **123** of the electromechanical systems device of Figure 9P. The dielectric layer can be similar to the dielectric layer **124** of Figure 9O, and can be configured to control the launch height and curvature of the mechanical layer **14** upon release. One or more additional layers, such as an additional conductive layer, can be provided over the dielectric layer to allow the mechanical layer to be substantially symmetric, thereby aiding in balancing stresses in the mechanical layer.

[0093] For clarity of illustration, the sequence and drawings have been simplified to omit some details. For example, as will be described with reference to Figures 12A–12F below, in a color interferometric display system, multiple different devices may have different gap sizes to interferometrically enhance, for example, red, green, and blue. Similarly, three different mechanical layer materials or thicknesses can be employed to allow use of the same actuation voltage for collapsing the mechanical layer in three different gap sizes.

[0094] Figures 10A–10C show examples of cross-sectional schematic illustrations of various interferometric modulator devices.

[0095] Figure 10A is a schematic cross-section illustration of one example of an interferometric modulator. As illustrated in Figure 10, the interferometric modulator includes a substrate **20**, a black mask structure **23**, a shaping structure **102**, a dielectric structure **35**, an optical stack **16**, a gap **19**, a post structure **18**, and a mechanical layer **14** that includes a reflective layer **121**, a supporting layer **122**, and a conductive layer **123**. The post structure **18** can be positioned at each pixel corner to support the mechanical layer **14** over the substrate **20**. The fill factor of the illustrated interferometric modulator can be constrained by the minimum size of the post structure **18**, which can be determined by lithography resolution, layer to layer alignment accuracy and/or critical dimension bias. The post **18** can be formed by forming an anchor region or hole in a sacrificial layer, and includes wings **131** for supporting the mechanical layer **14**. The minimum width d_1 of the anchor hole can be partially determined by the minimum resolvable lithography feature size of the fabrication tools, and the total width d_2 of the post **18** to the edges of the wings **131** can be partially determined by critical dimension bias of sacrificial and post etching, as well as the misalignment between the sacrificial layer **35** and the layer used to form the post **18**. With reference to Figure 10A, the total post width d_2 can be the critical dimension, since total post width d_2 should be larger than the anchor hole width d_1.

[0096] Figure 10B is a schematic cross-section of another example of an interferometric modulator. The illustrated interferometric modulator includes a substrate **20**, a black mask structure **23**, a shaping structure **102**, a dielectric structure **35**, an optical stack **16**, a gap **19**, a rivet structure **129**, and a mechanical layer **14** that includes a reflective layer **121**, a supporting layer **122**, and a conductive layer **123**. In contrast to the interferometric modulator of Figure 10A, the illustrated interferometric modulator includes the rivet structure **129** and does not include the post **18**. The width d_1 of the anchor hole can be the critical dimension of the device, and thus, the illustrated interferometric modulator can have an improved fill factor relative to the interferometric modulator shown in Figure 10A.

[0097] Figure 10C is a schematic cross-section of yet another example of an interferometric modulator. The illustrated interferometric modulator includes a substrate **20**, a

black mask structure **23**, a shaping structure **102**, a dielectric structure **35**, an optical stack **16**, a gap **19**, and a mechanical layer **14** that includes a reflective layer **121**, a supporting layer **122**, a conductive layer **123**, and a dielectric layer **124**. In contrast to the interferometric modulator devices of Figures 10A–10B, the interferometric modulator device of Figure 10C does not include the post **18** or the rivet structure **129**. Since the interferometric modulator device of Figure 10C does not include the post structure **18**, the interferometric modulator shown in Figure 10C is not constrained by the total post width d_2 of Figure 10A. Thus, a pixel array using the interferometric modulator of Figure 10C can have a greater fill factor relative to a pixel array employing the device shown in Figure 10A.

[0098] Additionally, the interferometric modulator in Figure 10C can have a flexible anchoring structure, which can result in an improved dark state relative to the interferometric modulators of Figures 10A–10B. In particular, the dark state can be influenced by the bending height of the mechanical layer **14** between the relaxed and actuated positions near the anchoring hole. The flexible anchoring structure can reduce the bending height of the mechanical layer **14**, thereby decreasing the brightness of the portion of the mechanical layer **14** out of contact with the optical stack during actuation and improving the color gamut and/or dark state of a display using the device. Brightness, color gamut, and dark state can be the three most critical performance parameters of a display, and in some implementations can only be improved by increasing fill factor, flattening mirror curvature, and/or decreasing the mechanical layer bending height. The lack of the rivet structure **129** in the interferometric modulator of Figure 10C can reduce the bending height of the device relative to the interferometric modulator shown in Figure 10B.

[0099] Furthermore, the interferometric modulator of Figure 10C can have a continuous supporting layer **122** relative to the supporting posts **18** of the interferometric modulator of Figure 10A. A continuous supporting layer **122** can reduce manufacturing defects, thereby increasing yield and reducing manufacturing cost.

[0100] Moreover, the interferometric modulator of Figure 10C can, but need not, include both the supporting layer **122** and the dielectric layer **124**. The supporting layer **122** and the dielectric layer **124** can be tuned to control the mechanical stresses of the interferometric modulator. Residual stresses among different layers in an unreleased

interferometric modulator can affect mirror curvature, and can reduce display color gamut if not controlled. The dielectric layer **124** can have a stress selected to be greater than or less than the stress of the supporting layer **122**, thereby permitting control of the curvature and launch height of the mechanical layer upon release. Control of the curvature of the interferometric modulator permits selection of a sacrificial layer thickness which can easily be deposited and which does not produce a large bending height of the mechanical layer **14**. Reducing bending height of the mechanical layer **14** can decrease the brightness of the portion of the mechanical layer **14** out of contact with the optical stack **16** during actuation, thereby improving the device's black state and the display's contrast ratio, gamut, and color saturation.

[0101] Figure 11 is a graph **150** of simulated mechanical layer position in the actuated and relaxed states for three examples of interferometric modulator devices. The three examples of interferometric modulator devices represent a device having a post structure (for example, Figure 10A), a rivet structure (for example, Figure 10B), and no post or rivet structure (for example, Figure 10C). The graph **150** shows simulated mirror shape along a cross-section of the mechanical layer taken along a diagonal of a pixel, for both actuated and relaxed conditions when biased at the center of the stability window. The vertical line at a distance of about 18 μm represents the edge of the black mask **23**. Thus, the region of the graph **150** to the left of the black mask edge can be the optically active area of the pixel, and the region to the right of the black mask edge can be the mechanical layer anchoring region. The upper three lines of the graph **150** are mechanical layer shapes of the interferometric modulator devices in the relaxed position, while the bottom three lines of the graph **150** are mechanical layer shapes of the devices in the actuated position. As shown in Figure 11, an interferometric modulator device having no post or rivet structure can have a smaller bending height when in the actuated position relative to devices having post or rivet structures. The reduced bending height of the mechanical layer can decrease the brightness of the portion of the mechanical layer out of contact with the optical stack during actuation, thereby improving the black state of the device.

[0102] Figures 12A–12F show examples of cross-sectional schematic illustrations of various stages in a method of making an interferometric modulator. Not all of the

illustrated steps are required, and this process can be modified without departing from the spirit and scope of the invention. Certain details of the process can be similar to those described earlier with reference to Figures 9A–9P.

[0103] With reference to Figure 12A, the cross-section illustrates the processing of sacrificial structure with deposition, lithography and etch to form a first sacrificial structure **25a**, a second sacrificial structure **25b**, and a third sacrificial structure **25c**, each of which have a different thickness. The formation of the first, second and third sacrificial structures **25a–25c** over the optical stack **16** can include deposition of molybdenum (Mo) or amorphous silicon (a-Si), and a plurality of layers can be used to form each structure.

[0104] In a color interferometric display system, the thickness of the sacrificial structures **25a–25c** can correspond to a gap size configured to interferometrically enhance different colors. For example, the first sacrificial structure **25a** can define the height a high gap sub-pixel **125a**, the second sacrificial structure **25b** can define the height of a mid gap sub-pixel **125b**, and the third sacrificial structure **25c** can define the height of a low gap sub-pixel **125c**, and the first, second and third sacrificial structures **25a–25c** can have heights selected to interferometrically enhance, for instance, blue, red, and green, respectively. In one implementation, the first sacrificial structure **25a** includes Molybdenum (Mo) and has a thickness ranging between about 1000 Å to about 4,000 Å, for example, about 2,400 Å, the second sacrificial structure **25b** includes Mo and has a thickness ranging between about 800 Å to about 3,000 Å, for example, about 2000 Å, and the third sacrificial structure **25c** includes Mo and has a thickness ranging between about 600 Å to about 2,000 Å, for example, about 1,600 Å.

[0105] As illustrated in Figure 12A, the sacrificial structures **25a–25c** can be removed in regions between pixels to define anchor holes **132**. The anchor holes **132** permit a subsequently deposited layer, such as a supporting layer of a mechanical layer, to reach the optical stack **16** and/or any other layer disposed beneath the sacrificial structures **25a–25c**. Forming the anchor holes **132** in this manner can aid in forming a mechanical layer that can be supported without the use of post or rivet structures.

[0106] Figure 12B illustrates providing and patterning a reflective layer **121** over the sacrificial structures **25a–25c**. The reflective layer **121** can be, for example, an aluminum

alloy (AlCu) mirror layer. Additional details of the reflective layer **121** can be as described above with reference to Figures 9H–9I.

[0107] Figure 12C illustrates depositing a supporting layer **122** over the reflective layer **121** and the first, second and third sacrificial structures **25a**–**25c**. Additional details of the supporting layer **122** can be as described above with reference to Figure 9J.

[0108] With reference to Figure 12D, the cross-section illustrates depositing and etching a conductive or cap layer **123** over the supporting layer **122**. The conductive layer **123** can be, for example, an aluminum alloy layer, and can be as described above with reference to Figures 9K-9L.

[0109] Figure 12E illustrates providing and patterning a dielectric layer **124** over the conductive layer **123**. The dielectric layer **124** can have a stress different than that of the supporting layer **122**, and, thus, can be employed to tune the launch height and curvature of the mechanical layer **14** upon release, as described above. The stress of the dielectric layer **124** can be controlled relative to the stress of the supporting layer **122** by selecting a different material and/or thickness for the dielectric layer **124** and the supporting layer **122**. Additionally, by controlling certain processing parameters, including, for example, plasma power, pressure, process gas composition, plasma gas ratio, and/or temperature, the stress of the dielectric layer **124** and/or the supporting layer **122** can be controlled.

[0110] As shown in Figure 12E, the dielectric layer **124** can selectively etched to form different patterns across the high gap, mid gap and low gap sub-pixels **125a**–**125c**. In one implementation, the dielectric layer **124** over the high gap sub-pixel **125a** is substantially etched away, while the dielectric layer **124** over the low gap sub-pixel **125c** is kept substantially intact. Additionally, for the mid gap sub-pixel **125b**, the dielectric layer **124** can be patterned with patterns **39** to meet a desired stiffness requirement, such as a stiffness that permits the same actuation voltage to collapse the mechanical layer **14** for high-gap and/or low-gap sub-pixels. When viewed from above the sub-pixel, the patterns **39** can include a variety of shapes, such as, for example, holes or slots.

[0111] Figure 12F illustrates the release of the high gap, mid gap, and low gap sub-pixels **125a**–**125c** to form gaps **19a**–**19c**, respectively. The release of the sub-pixel devices can be similar to that described earlier with reference to Figure 9M, and can include

removal of the sacrificial structures **25a**–**25c**. As shown in Figure 12F, the sub-pixels **125a**–**125c** have no post or rivet structures.

[0112] Although Figures 12A–12F is illustrated for the case of a supporting layer **122** and a dielectric layer **124**, more or fewer dielectric layers can be employed. In one implementation, a supporting layer and first and second dielectric layers are used for high gap, mid gap, and low gap sub-pixels. For example, low gap sub-pixels can have the supporting layer and the first and second dielectric layers, mid gap sub-pixels can have the supporting layer and the first dielectric layer, and high gap sub-pixels can have the supporting layer. The supporting layer can be separated from the first dielectric layer by a conductive layer, such as a metallic layer including aluminum. Likewise, the first and second dielectric layers can be separated by another conductive layer. The tuning of each sub-pixel gap size for stiffness and mirror curvature can be facilitated by the use of first and second dielectric layers, rather than the use of a dielectric layer which is selectively patterned. However, in some implementations, use of a supporting layer and a patterned dielectric layer can be desired to reduce the number of photomasks.

[0113] Figure 13 shows an example of a flow diagram illustrating a manufacturing process **160** for an interferometric modulator. The process **160** starts at block **164**.

[0114] The process **160** continues at a block **166**, in which a sacrificial layer is deposited over a substrate. The sacrificial layer can include, for example, molybdenum (Mo) and/or amorphous silicon (a-Si), and can be used to define a height of an interferometric cavity.

[0115] In some implementations, a shaping layer is deposited over the substrate to form a protrusion. The shaping layer or structure can include, for example, an oxide, and can be used to maintain a relatively planar profile across the substrate, such as in implementations in which the substrate includes a black mask structure. The protrusion can be formed by an overlap of the shaping layer with another layer, such as a black mask layer, and can be used to produce an upwardly extending wave or kink in a subsequently deposited conformal layer, such as a subsequently deposited mechanical layer.

[0116] In block **168**, a portion of the sacrificial layer is removed to form one or more anchoring regions. For example, the sacrificial layer can be etched at pixel corners to define an anchoring hole at each pixel corner.

[0117] In block **170**, a multi-layer mechanical layer is formed over the sacrificial layer and the anchoring region. The mechanical layer includes a reflective layer, a dielectric layer, and a cap layer, and the dielectric layer can be disposed between the reflective layer and the cap layer. The reflective layer can be selectively etched over the anchor regions, thereby permitting the dielectric layer to contact one or more layers underlying the sacrificial layer, which can aid in forming a self-supporting mechanical layer.

[0118] The dielectric layer of the mechanical layer can be configured to support the mechanical layer. For example, the dielectric layer can be used to anchor the mechanical layer at the anchoring region of the pixel formed in block **168**, and can have a thickness and composition selected to be sufficient to provide support for the mechanical layer after the sacrificial layer is removed. Thus, the dielectric layer can support the mechanical layer in the actuated and relaxed positions without the need for a post or rivet structure. Configuring the dielectric layer to provide support for the mechanical layer can increase the density of pixels as compared to a design in which support is provided by posts or rivets.

[0119] In implementations including a shaping layer deposited to form a protrusion, the mechanical layer can be conformally deposited over the shaping layer and can include a kink over the protrusion. The kink can be adjacent the anchoring region formed in block **168**..

[0120] In a block **172**, the sacrificial layer is removed to form a gap. Upon release of the mechanical layer, the mechanical layer can launch away from the pre-released location due to residual mechanical stresses, as was described above. The stresses in one or more sub-layers of the mechanical layer, such as the stress of the dielectric layer, can be used to tune the launch of the dielectric layer. Additionally, in implementations including a kink in the mechanical layer, the geometry of the kink can be used to fine-tune launch of the mechanical layer, as was described above. The process **160** ends at **176**.

[0121] Figures 14A and 14B show examples of system block diagrams illustrating a display device **40** that includes a plurality of interferometric modulators. The display device

40 can be, for example, a cellular or mobile telephone. However, the same components of the display device **40** or slight variations thereof are also illustrative of various types of display devices such as televisions, e-readers and portable media players.

[0122] The display device **40** includes a housing **41**, a display **30**, an antenna **43**, a speaker **45**, an input device **48**, and a microphone **46**. The housing **41** can be formed from any of a variety of manufacturing processes, including injection molding, and vacuum forming. In addition, the housing **41** may be made from any of a variety of materials, including, but not limited to: plastic, metal, glass, rubber, and ceramic, or a combination thereof. The housing **41** can include removable portions (not shown) that may be interchanged with other removable portions of different color, or containing different logos, pictures, or symbols.

[0123] The display **30** may be any of a variety of displays, including a bi-stable or analog display, as described herein. The display **30** also can be configured to include a flat-panel display, such as plasma, EL, OLED, STN LCD, or TFT LCD, or a non-flat-panel display, such as a CRT or other tube device. In addition, the display **30** can include an interferometric modulator display, as described herein.

[0124] The components of the display device **40** are schematically illustrated in Figure 14B. The display device **40** includes a housing **41** and can include additional components at least partially enclosed therein. For example, the display device **40** includes a network interface **27** that includes an antenna **43** which is coupled to a transceiver **47**. The transceiver **47** is connected to a processor **21**, which is connected to conditioning hardware **52**. The conditioning hardware **52** may be configured to condition a signal (e.g., filter a signal). The conditioning hardware **52** is connected to a speaker **45** and a microphone **46**. The processor **21** is also connected to an input device **48** and a driver controller **29**. The driver controller **29** is coupled to a frame buffer **28**, and to an array driver **22**, which in turn is coupled to a display array **30**. A power supply **50** can provide power to all components based on the particular display device **40** design.

[0125] The network interface **27** includes the antenna **43** and the transceiver **47** so that the display device **40** can communicate with one or more devices over a network. The network interface **27** also may have some processing capabilities to relieve, e.g., data processing requirements of the processor **21**. The antenna **43** can transmit and receive signals.

In some implementations, the antenna **43** transmits and receives RF signals according to the IEEE 16.11 standard, including IEEE 16.11(a), (b), or (g), or the IEEE 802.11 standard, including IEEE 802.11a, b, g or n. In some other implementations, the antenna **43** transmits and receives RF signals according to the BLUETOOTH standard. In the case of a cellular telephone, the antenna **43** is designed to receive code division multiple access (CDMA), frequency division multiple access (FDMA), time division multiple access (TDMA), Global System for Mobile communications (GSM), GSM/General Packet Radio Service (GPRS), Enhanced Data GSM Environment (EDGE), Terrestrial Trunked Radio (TETRA), Wideband-CDMA (W-CDMA), Evolution Data Optimized (EV-DO), 1xEV-DO, EV-DO Rev A, EV-DO Rev B, High Speed Packet Access (HSPA), High Speed Downlink Packet Access (HSDPA), High Speed Uplink Packet Access (HSUPA), Evolved High Speed Packet Access (HSPA+), Long Term Evolution (LTE), AMPS, or other known signals that are used to communicate within a wireless network, such as a system utilizing 3G or 4G technology. The transceiver **47** can pre-process the signals received from the antenna **43** so that they may be received by and further manipulated by the processor **21**. The transceiver **47** also can process signals received from the processor **21** so that they may be transmitted from the display device **40** via the antenna **43**.

[0126] In some implementations, the transceiver **47** can be replaced by a receiver. In addition, the network interface **27** can be replaced by an image source, which can store or generate image data to be sent to the processor **21**. The processor **21** can control the overall operation of the display device **40**. The processor **21** receives data, such as compressed image data from the network interface **27** or an image source, and processes the data into raw image data or into a format that is readily processed into raw image data. The processor **21** can send the processed data to the driver controller **29** or to the frame buffer **28** for storage. Raw data typically refers to the information that identifies the image characteristics at each location within an image. For example, such image characteristics can include color, saturation, and gray-scale level.

[0127] The processor **21** can include a microcontroller, CPU, or logic unit to control operation of the display device **40**. The conditioning hardware **52** may include amplifiers and filters for transmitting signals to the speaker **45**, and for receiving signals from

the microphone **46**. The conditioning hardware **52** may be discrete components within the display device **40**, or may be incorporated within the processor **21** or other components.

[0128] The driver controller **29** can take the raw image data generated by the processor **21** either directly from the processor **21** or from the frame buffer **28** and can re-format the raw image data appropriately for high speed transmission to the array driver **22**. In some implementations, the driver controller **29** can re-format the raw image data into a data flow having a raster-like format, such that it has a time order suitable for scanning across the display array **30**. Then the driver controller **29** sends the formatted information to the array driver **22**. Although a driver controller **29**, such as an LCD controller, is often associated with the system processor **21** as a stand-alone Integrated Circuit (IC), such controllers may be implemented in many ways. For example, controllers may be embedded in the processor **21** as hardware, embedded in the processor **21** as software, or fully integrated in hardware with the array driver **22**.

[0129] The array driver **22** can receive the formatted information from the driver controller **29** and can re-format the video data into a parallel set of waveforms that are applied many times per second to the hundreds, and sometimes thousands (or more), of leads coming from the display's x-y matrix of pixels.

[0130] In some implementations, the driver controller **29**, the array driver **22**, and the display array **30** are appropriate for any of the types of displays described herein. For example, the driver controller **29** can be a conventional display controller or a bi-stable display controller (e.g., an IMOD controller). Additionally, the array driver **22** can be a conventional driver or a bi-stable display driver (e.g., an IMOD display driver). Moreover, the display array **30** can be a conventional display array or a bi-stable display array (e.g., a display including an array of IMODs). In some implementations, the driver controller **29** can be integrated with the array driver **22**. Such an implementation is common in highly integrated systems such as cellular phones, watches and other small-area displays.

[0131] In some implementations, the input device **48** can be configured to allow, e.g., a user to control the operation of the display device **40**. The input device **48** can include a keypad, such as a QWERTY keyboard or a telephone keypad, a button, a switch, a rocker, a touch-sensitive screen, or a pressure- or heat-sensitive membrane. The microphone **46** can be

configured as an input device for the display device **40**. In some implementations, voice commands through the microphone **46** can be used for controlling operations of the display device **40**.

[0132] The power supply **50** can include a variety of energy storage devices as are well known in the art. For example, the power supply **50** can be a rechargeable battery, such as a nickel-cadmium battery or a lithium-ion battery. The power supply **50** also can be a renewable energy source, a capacitor, or a solar cell, including a plastic solar cell or solar-cell paint. The power supply **50** also can be configured to receive power from a wall outlet.

[0133] In some implementations, control programmability resides in the driver controller **29** which can be located in several places in the electronic display system. In some other implementations, control programmability resides in the array driver **22**. The above-described optimization may be implemented in any number of hardware and/or software components and in various configurations.

[0134] The various illustrative logics, logical blocks, modules, circuits and algorithm steps described in connection with the implementations disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. The interchangeability of hardware and software has been described generally, in terms of functionality, and illustrated in the various illustrative components, blocks, modules, circuits and steps described above. Whether such functionality is implemented in hardware or software depends upon the particular application and design constraints imposed on the overall system.

[0135] The hardware and data processing apparatus used to implement the various illustrative logics, logical blocks, modules and circuits described in connection with the aspects disclosed herein may be implemented or performed with a general purpose single- or multi-chip processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, or, any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a

combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. In some implementations, particular steps and methods may be performed by circuitry that is specific to a given function.

[0136] In one or more aspects, the functions described may be implemented in hardware, digital electronic circuitry, computer software, firmware, including the structures disclosed in this specification and their structural equivalents thereof, or in any combination thereof. Implementations of the subject matter described in this specification also can be implemented as one or more computer programs, i.e., one or more modules of computer program instructions, encoded on a computer storage media for execution by, or to control the operation of, data processing apparatus.

[0137] Various modifications to the implementations described in this disclosure may be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other implementations without departing from the spirit or scope of this disclosure. Thus, the disclosure is not intended to be limited to the implementations shown herein, but is to be accorded the widest scope consistent with the claims, the principles and the novel features disclosed herein. The word “exemplary” is used exclusively herein to mean “serving as an example, instance, or illustration.” Any implementation described herein as “exemplary” or provided as examples is not necessarily to be construed as preferred or advantageous over other implementations. Additionally, a person having ordinary skill in the art will readily appreciate, the terms “upper” and “lower” are sometimes used for ease of describing the figures, and indicate relative positions corresponding to the orientation of the figure on a properly oriented page, and may not reflect the proper orientation of the IMOD as implemented.

[0138] Certain features that are described in this specification in the context of separate implementations also can be implemented in combination in a single implementation. Conversely, various features that are described in the context of a single implementation also can be implemented in multiple implementations separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination can in some

cases be excised from the combination, and the claimed combination may be directed to a subcombination or variation of a subcombination.

[0139] Similarly, while operations are depicted in the drawings in a particular order, this should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results. Further, the drawings may schematically depict one more example processes in the form of a flow diagram. However, other operations that are not depicted can be incorporated in the example processes that are schematically illustrated. For example, one or more additional operations can be performed before, after, simultaneously, or between any of the illustrated operations. In certain circumstances, multitasking and parallel processing may be advantageous. Moreover, the separation of various system components in the implementations described above should not be understood as requiring such separation in all implementations, and it should be understood that the described program components and systems can generally be integrated together in a single software product or packaged into multiple software products. Additionally, other implementations are within the scope of the following claims. In some cases, the actions recited in the claims can be performed in a different order and still achieve desirable results.

CLAIMS

What is claimed is:

1. An electromechanical device, comprising:

a substrate;

a partially reflective optical stack disposed on the substrate; and

a movable mechanical layer positioned so that the partially reflective optical stack is between the mechanical layer and the substrate, the mechanical layer including a reflective layer, a conductive layer, and a supporting layer that is disposed between the reflective layer and the conductive layer, wherein the supporting layer is anchored on the optical stack in an optically non-active anchor region and extends from the anchor region away from the optical stack spacing the mechanical layer from the optical stack to define a collapsible gap between the mechanical layer and the optical stack,

wherein the mechanical layer is movable to an actuated position and a relaxed position by applying a voltage across the mechanical layer and a stationary electrode disposed between the substrate and the collapsible gap, and wherein the collapsible gap is in a collapsed state when the mechanical layer is in the actuated position and the gap is in a non-collapsed state when the mechanical layer is in the relaxed position.

2. The device of claim 1, wherein the mechanical layer further includes a kink disposed adjacent to the anchor region and in at least a portion of an optically non-active region.

3. The device of claim 2, wherein the kink in the mechanical layer includes a rising portion extending away from the gap and a falling portion extending towards the gap.

4. The device of claim 1, wherein the reflective layer and the conductive layer include aluminum alloys.

5. The device of claim 1, wherein the supporting layer includes a dielectric material.

6. The device of claim 5, wherein the supporting layer includes silicon oxynitride (SiON).

7. The device of claim 5, wherein a portion of the supporting layer extends past the reflective layer and towards the optical stack, and wherein the supporting layer contacts the optical stack in the anchor region.

8. The device of claim 1, wherein the supporting layer is between about 500 Å and about 8000 Å thick.

9. The device of claim 1, further comprising a dielectric layer disposed on the mechanical layer such that the mechanical layer is between the dielectric layer and the collapsible gap.

10. The device of claim 9, wherein the dielectric layer is between about 500 Å and about 4000 Å thick.

11. The device of claim 1, wherein the reflective layer includes an aluminum-copper (AlCu) layer having a thickness of between about 200 Å and about 500 Å.

12. The device of claim 11, wherein the conductive layer includes an AlCu layer having a thickness of between about 200 Å and about 500 Å.

13. The device of claim 1, wherein a height dimension of the kink is between about 400 Å and about 5000 Å.

14. The device of claim 13, where a width dimension of the kink is between about 0.2 μm and about 5μm.

15. The device of claim 1, wherein the optical stack includes the stationary electrode.

16. The device of claim 1, wherein the optical stack, the reflective layer of the mechanical layer, and the collapsible gap form an interferometric modulator.

17. The device of claim 1, further comprising:

a display including the substrate, the optical stack, and the mechanical layer;

a processor that is configured to communicate with the display, the processor being configured to process image data; and

a memory device that is configured to communicate with the processor.

18. The device of claim 17, further comprising a driver circuit configured to send at least one signal to the display.

19. The device of claim 18, further comprising a controller configured to send at least a portion of the image data to the driver circuit.

20. The device of claim 17, further comprising an image source module configured to send the image data to the processor.

21. The device of claim 20, wherein the image source module includes at least one of a receiver, transceiver, and transmitter.

22. The device of claim 17, further comprising an input device configured to receive input data and to communicate the input data to the processor.

23. A device, comprising:

a substrate;

means for partially reflecting light disposed on the substrate; and

movable means for reflecting light including a means for supporting the movable reflecting means, the supporting means anchored on the partially reflecting means in an optically non-active anchor region, wherein the supporting means extends from the anchor region away from the partially reflecting means spacing the movable reflecting means from the partially reflecting means to define a collapsible gap between the movable reflecting means and the partially reflecting means,

wherein the movable reflecting means is movable to an actuated position and a relaxed position by applying a voltage across the movable reflecting means and a stationary electrode disposed between the substrate and the collapsible gap, and wherein the collapsible gap is in a collapsed state when the movable reflecting means is in the actuated position and the gap is in a non-collapsed state when the movable reflecting means is in the relaxed position.

24. The device of claim 23, wherein the partially reflecting means includes an optical stack, and the optical stack includes the stationary electrode.

25. The device of claim 24, wherein the movable reflecting means includes a reflective layer and a conductive layer, wherein the supporting means includes a support layer comprising a dielectric material, and wherein the support layer is disposed between the reflective layer and the conductive layer.

26. The device of claim 25, wherein a portion of the support layer in the anchor region extends past the reflective layer and towards the optical stack, and the optical layer contacts the optical stack in the anchor region.

27. The device of claim 23, further comprising a dielectric layer disposed on the movable reflecting means.

28. A method of forming a mechanical layer in an electromechanical device, the method comprising:

providing a substrate;

forming an optical stack over the substrate;

providing a sacrificial layer over the optical stack;

removing a portion of the sacrificial layer that is disposed over an anchoring region;

forming a mechanical layer over the sacrificial layer and the anchoring region, wherein forming the mechanical layer includes providing a reflective layer over the sacrificial layer, removing a portion of the reflective layer that is disposed over the anchoring region, providing a supporting layer over the reflective layer such that a portion of the supporting layer contacts the anchoring region, and providing a conductive layer over the supporting layer; and

removing the sacrificial layer to form a collapsible gap between the mechanical layer and the substrate.

29. The method of claim 28, further comprising depositing a shaping layer over at least a portion of the substrate adjacent to the anchoring region, the shaping layer including at least one protrusion that extends away from the substrate, wherein the optical stack is formed over the shaping layer.

30. The method of claim 29, wherein providing the sacrificial layer includes forming the sacrificial layer as a conformal layer over the shaping layer including over the at least one protrusion, and wherein forming the mechanical layer further includes forming the mechanical layer over the sacrificial layer and the shaping layer, including the at least one protrusion, as a conformal layer such that a kink is formed in a portion of the mechanical layer over the at least one protrusion.

31. The method of claim 30, further comprising depositing a black mask over at least a portion of the substrate, wherein a portion of the shaping layer and a portion of the black mask overlap so as to define a height dimension of the protrusion.

32. The method of claim 28, wherein the supporting layer includes a dielectric material.

33. The method of claim 28, wherein the supporting layer directly contacts the optical stack over the anchoring region.

34. The method of claim 28, wherein the supporting layer has a thickness of between about 500 Å and about 8000 Å.

35. The method of claim 28, wherein the conductive layer includes an AlCu layer having a thickness of between about 200 Å and about 500 Å.

36. The method of claim 28 further comprising depositing a dielectric layer over the conductive layer.

37. The method of claim 36, wherein the dielectric layer has a thickness of between about 500 Å to about 4000 Å.

38. The method of claim 28, wherein the shaping layer includes a buffer oxide layer having a thickness of about 500 Å to about 6000 Å

39. The method of claim 31, further comprising depositing an aluminum oxide layer on the substrate before depositing the black mask.

40. The method of claim 39, wherein the aluminum oxide layer has a thickness of between about 50 Å and about 250 Å.

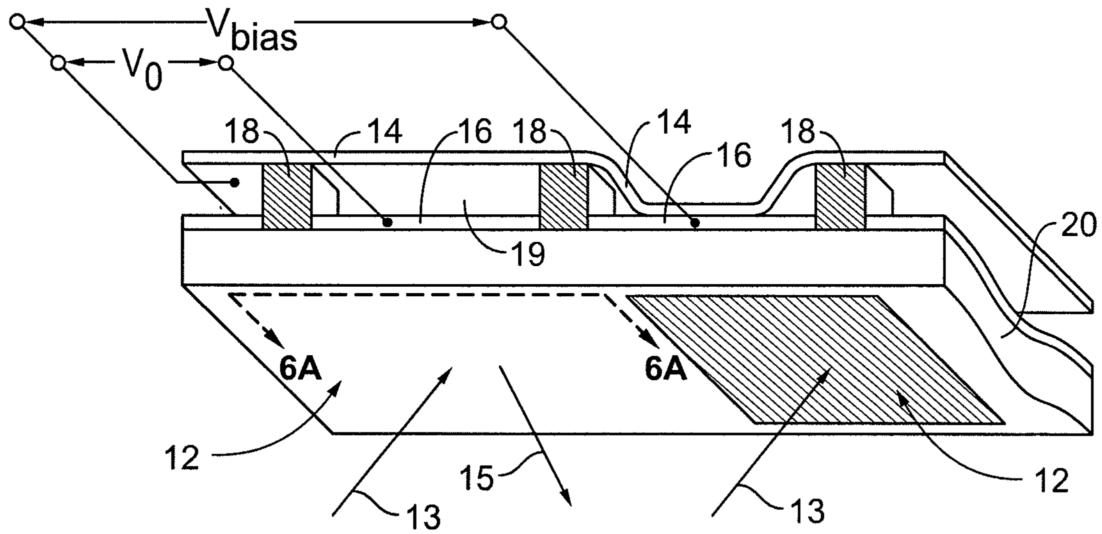

Figure 1

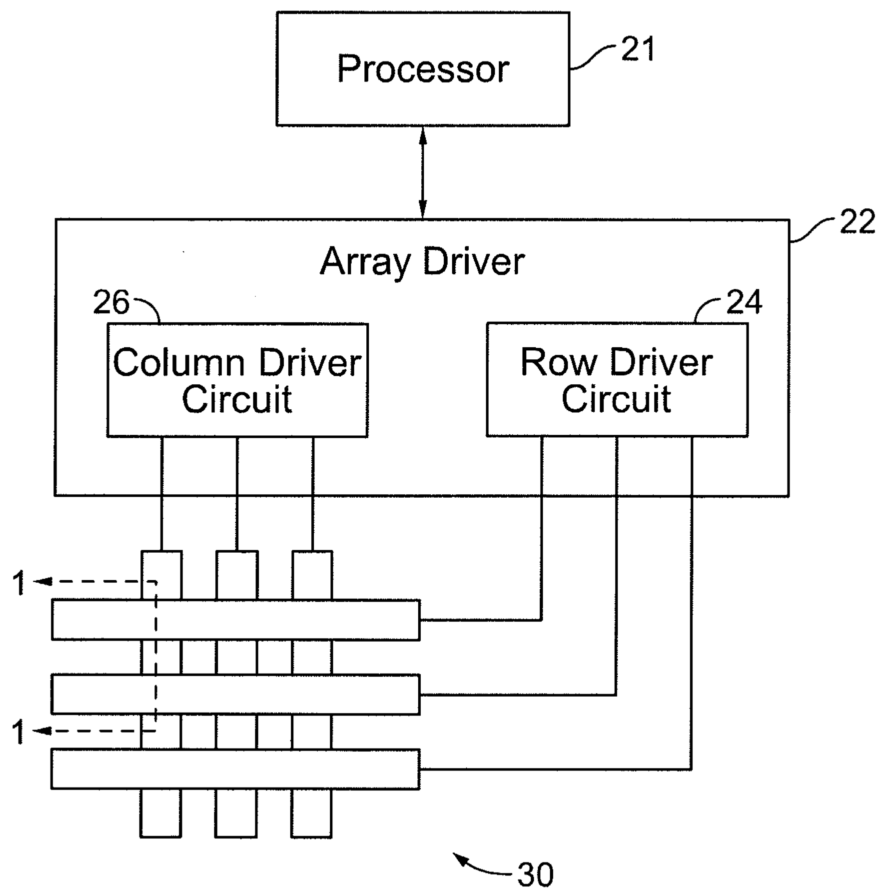

Figure 2

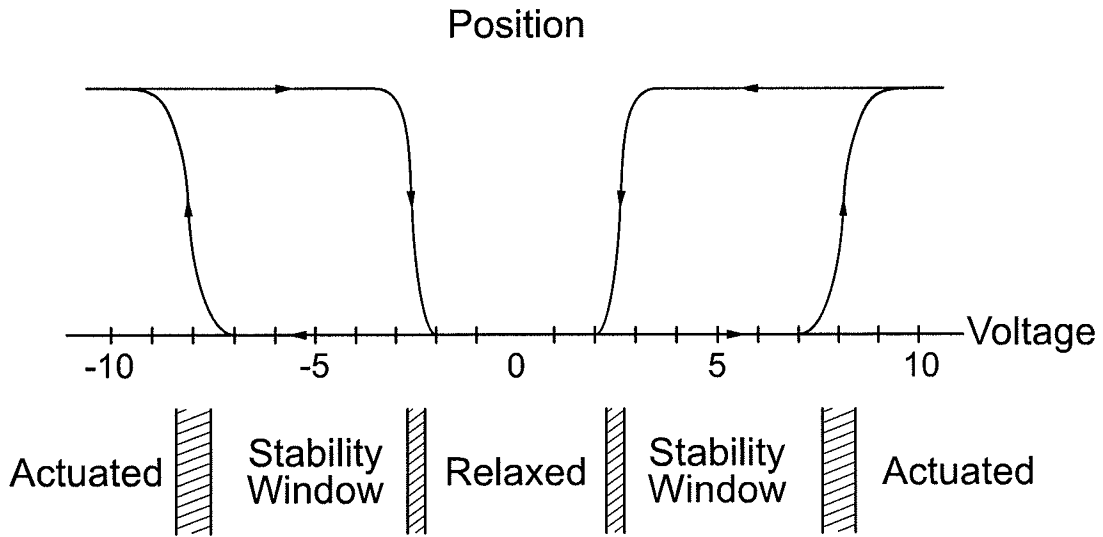

Figure 3

Common Voltages

Segment Voltages	VC_{ADD_H}	VC_{HOLD_H}	VC_{REL}	VC_{HOLD_L}	VC_{ADD_L}
VS_H	Stable	Stable	Relax	Stable	Actuate
VS_L	Actuate	Stable	Relax	Stable	Stable

Figure 4

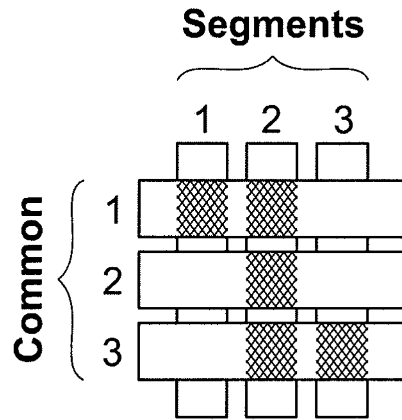

Figure 5A

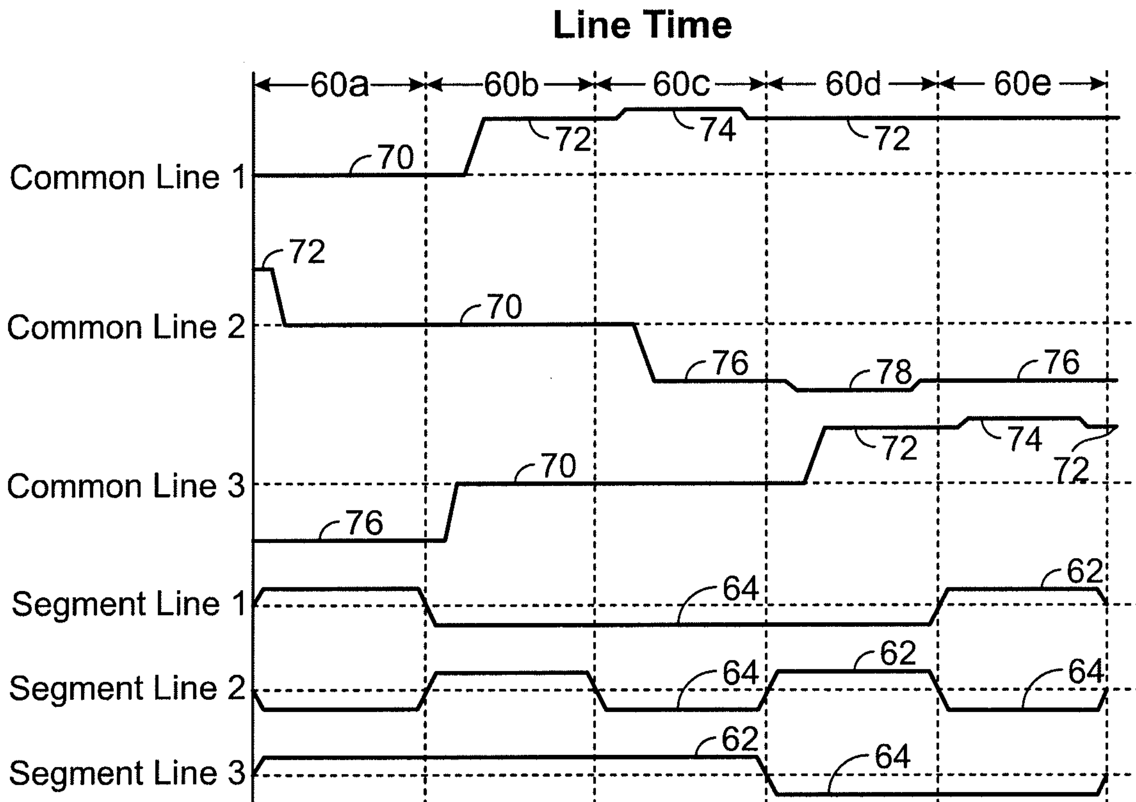

Figure 5B

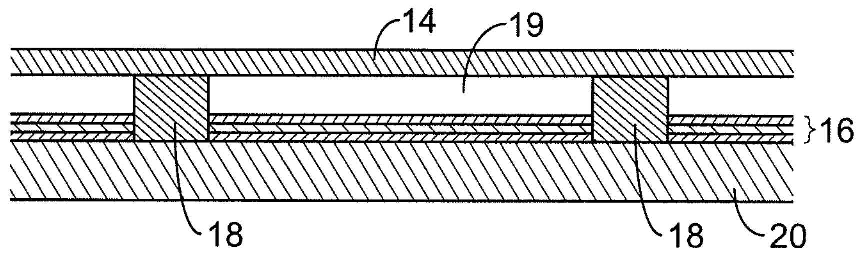

Figure 6A

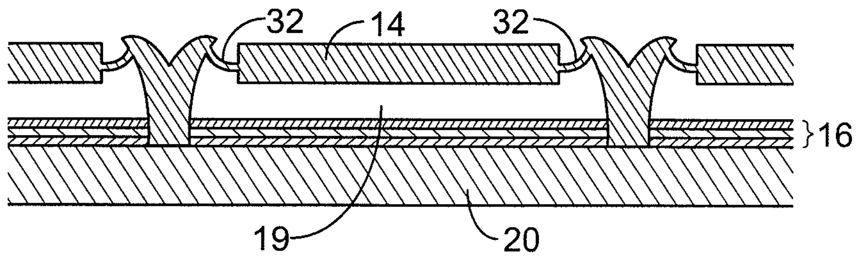

Figure 6B

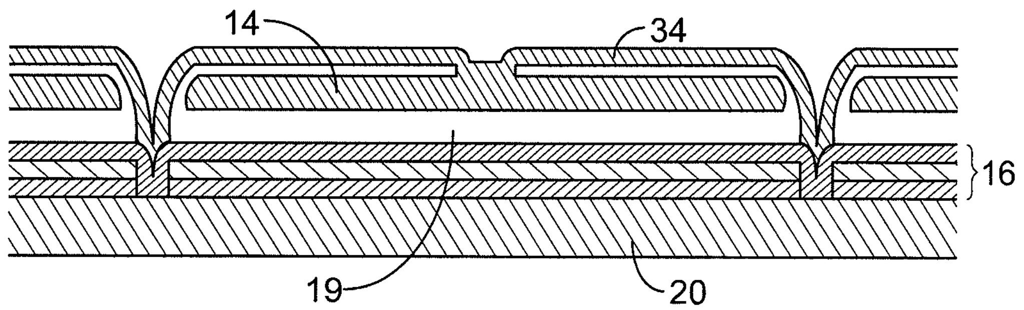

Figure 6C

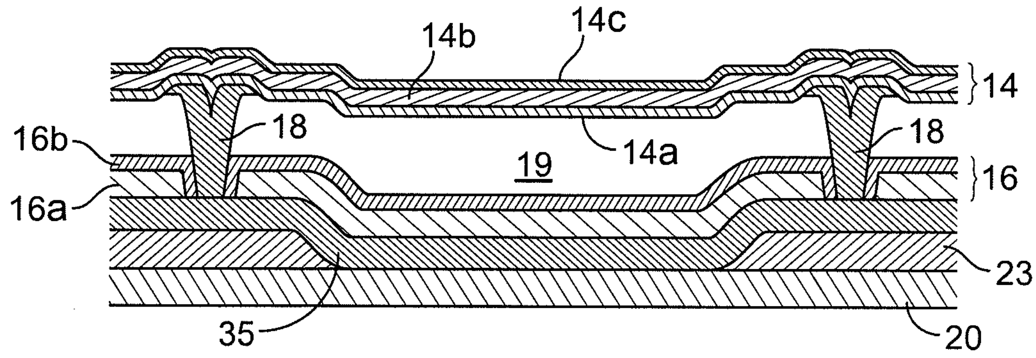

Figure 6D

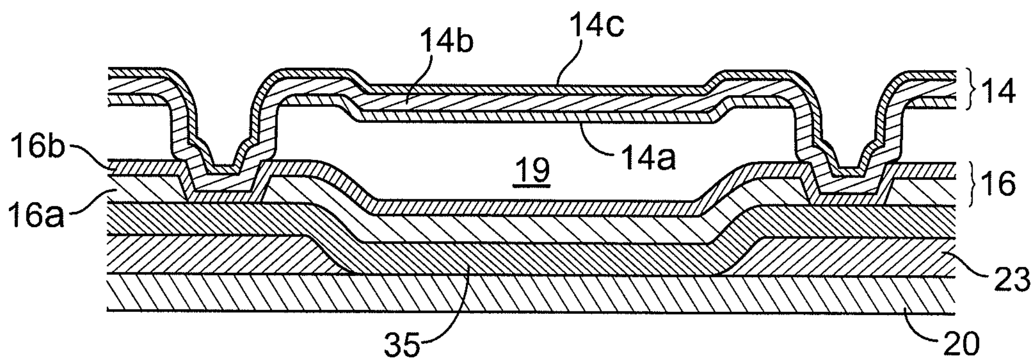

Figure 6E

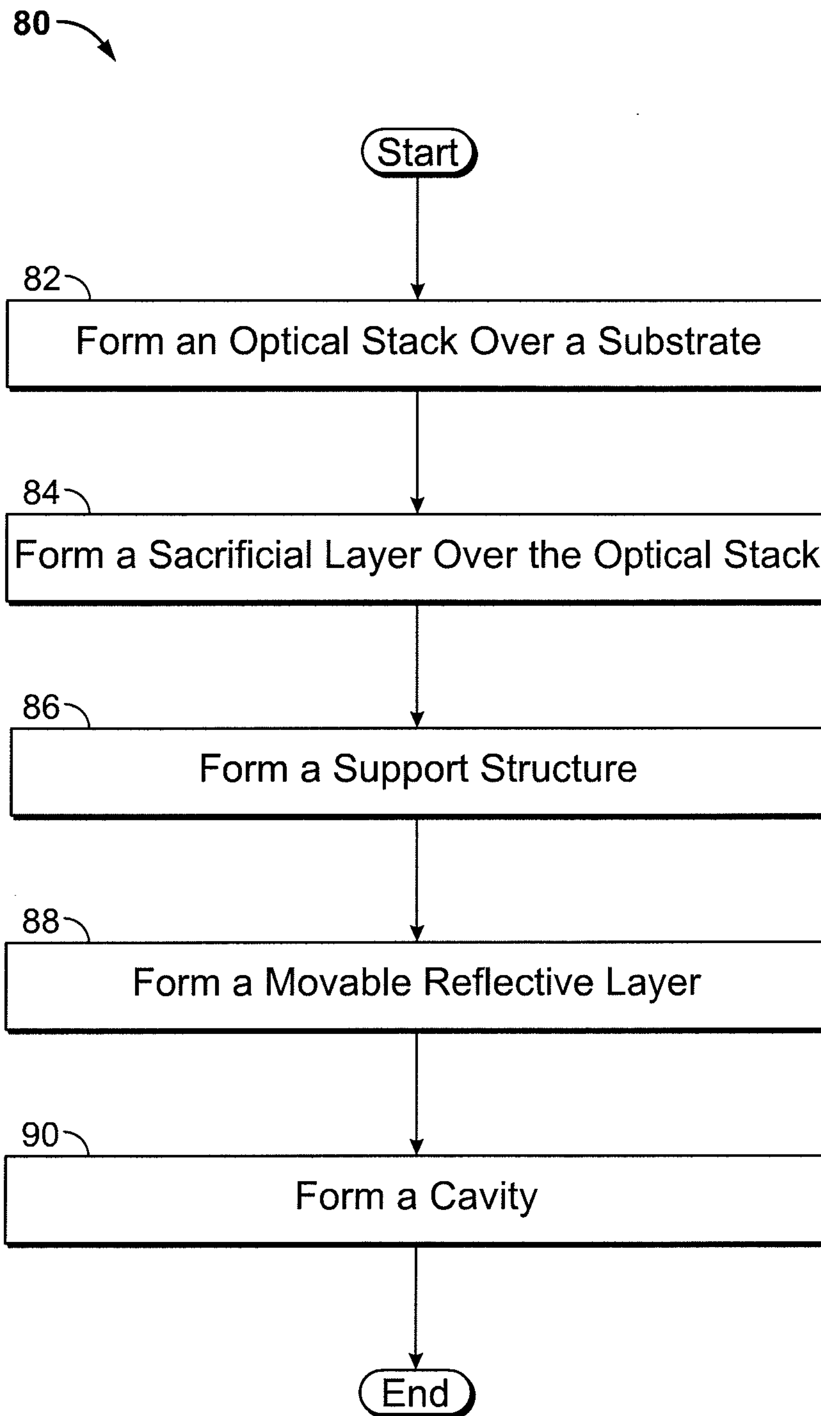

Figure 7

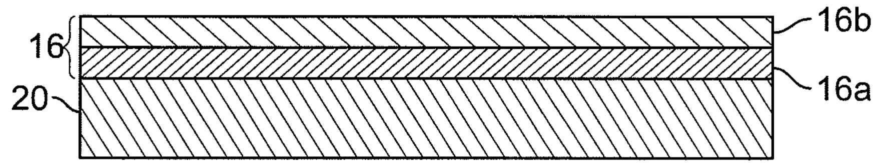

Figure 8A

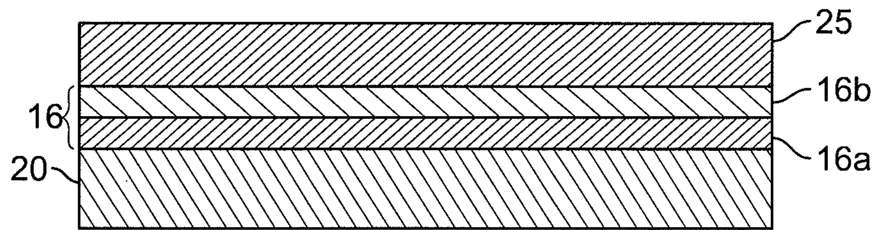

Figure 8B

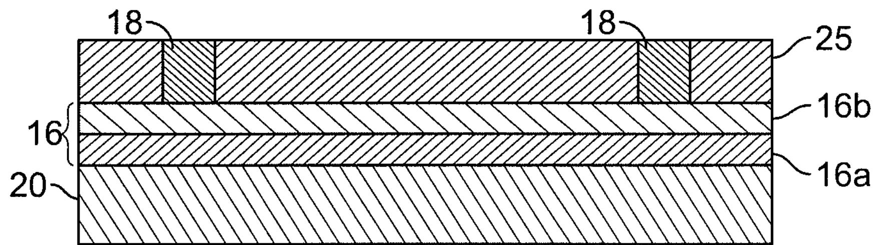

Figure 8C

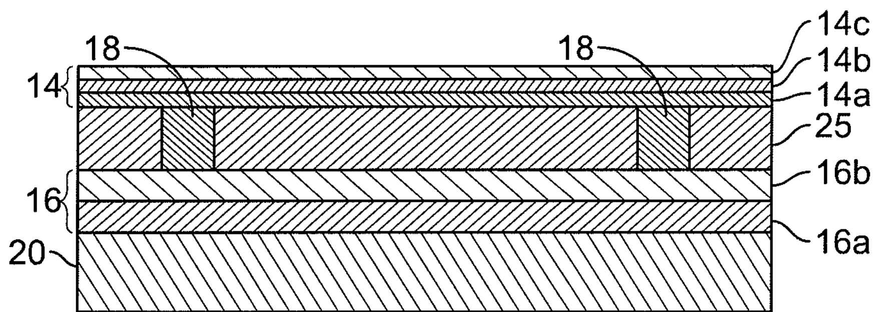

Figure 8D

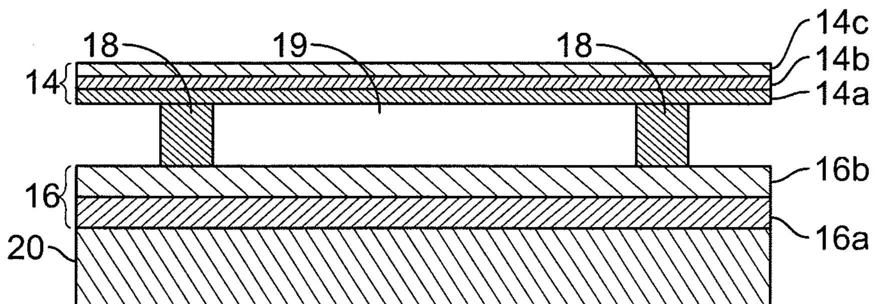

Figure 8E

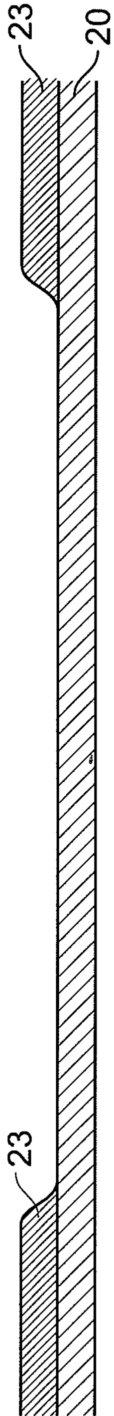

Figure 9A

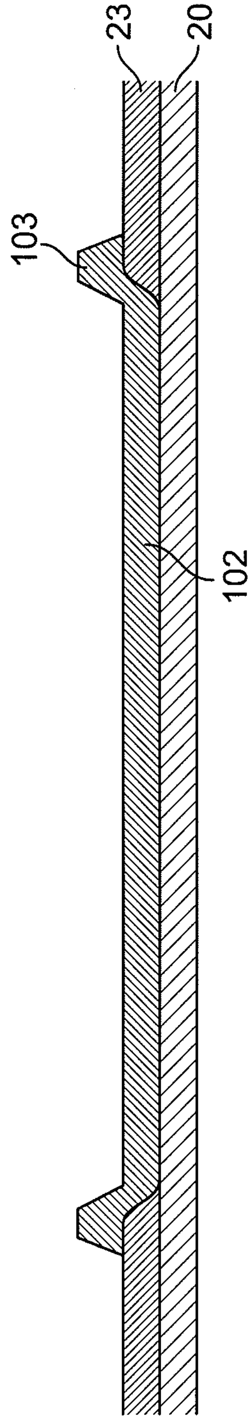

Figure 9B

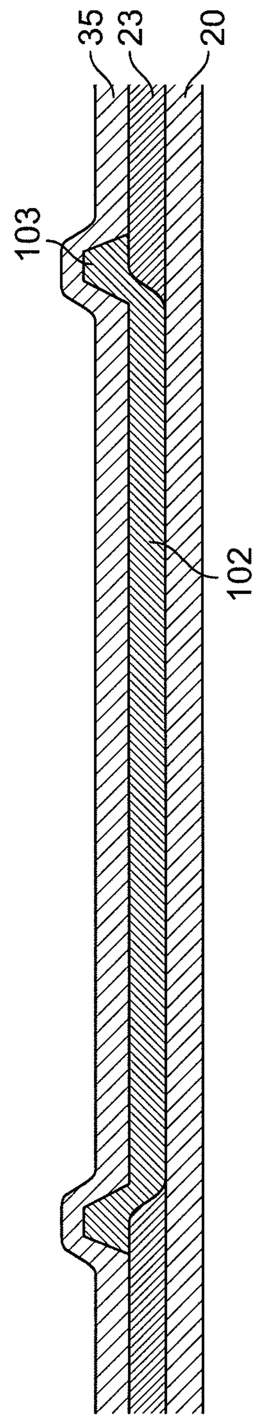

Figure 9C

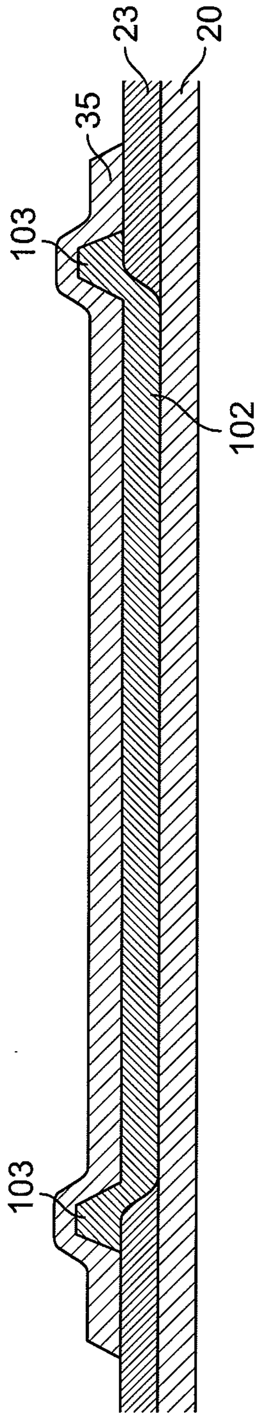

Figure 9D

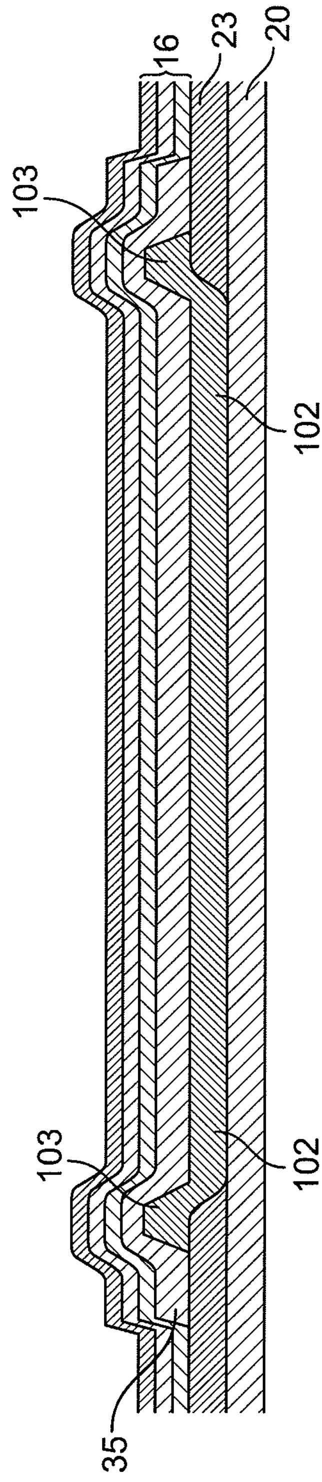

Figure 9E

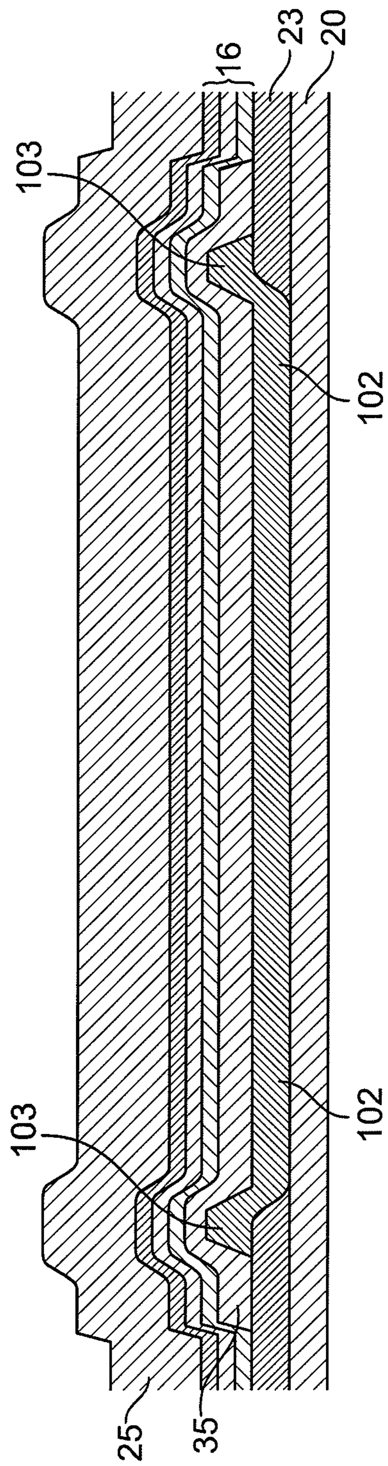

Figure 9F

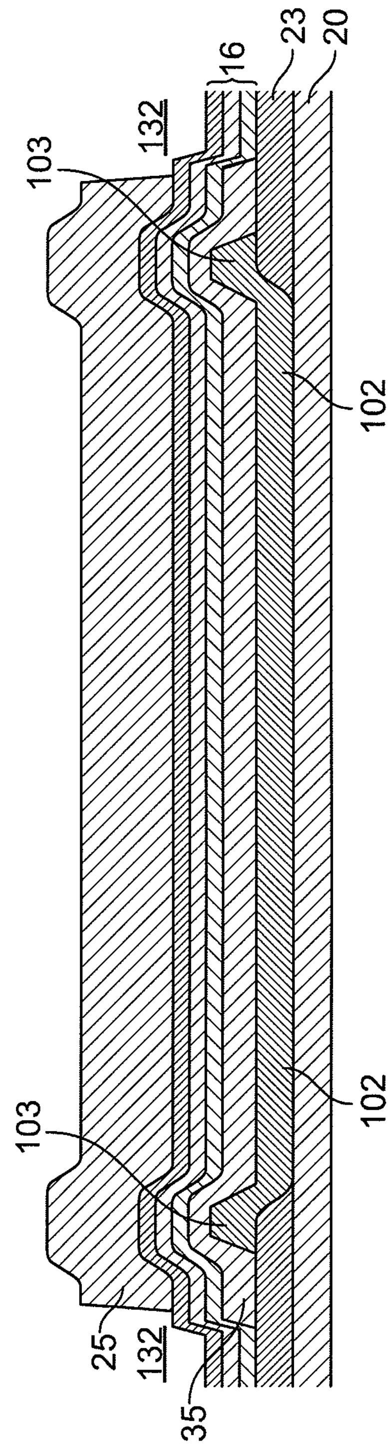

Figure 9G

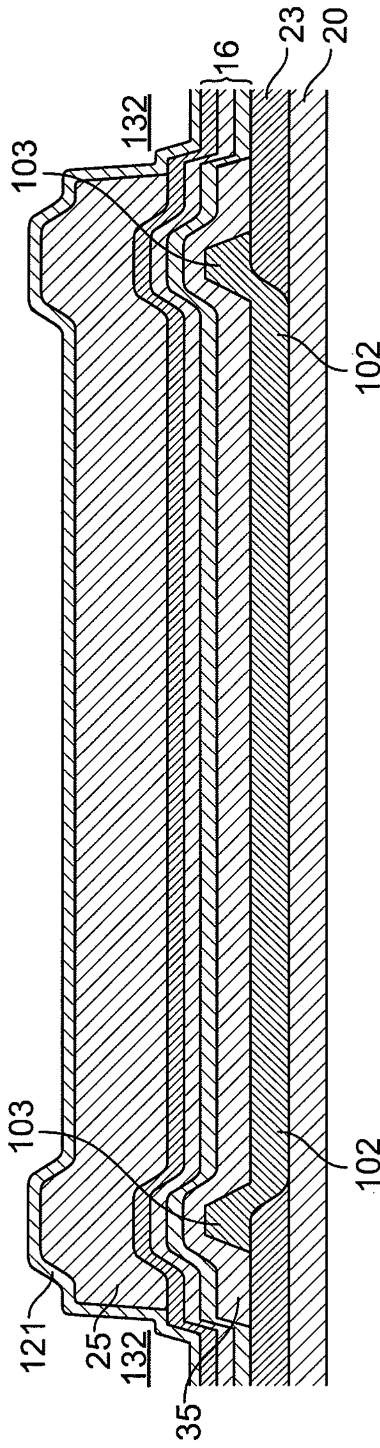

Figure 9H

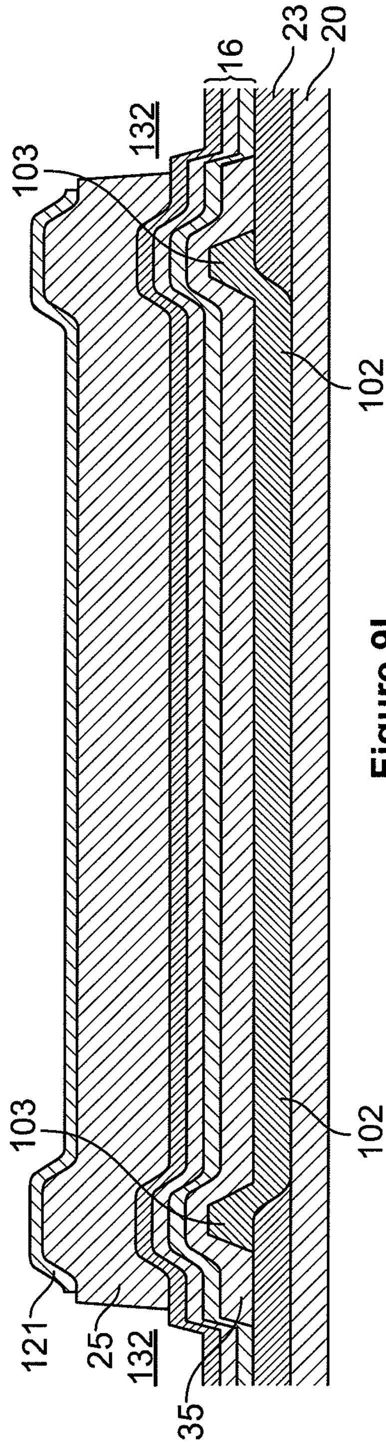

Figure 9I

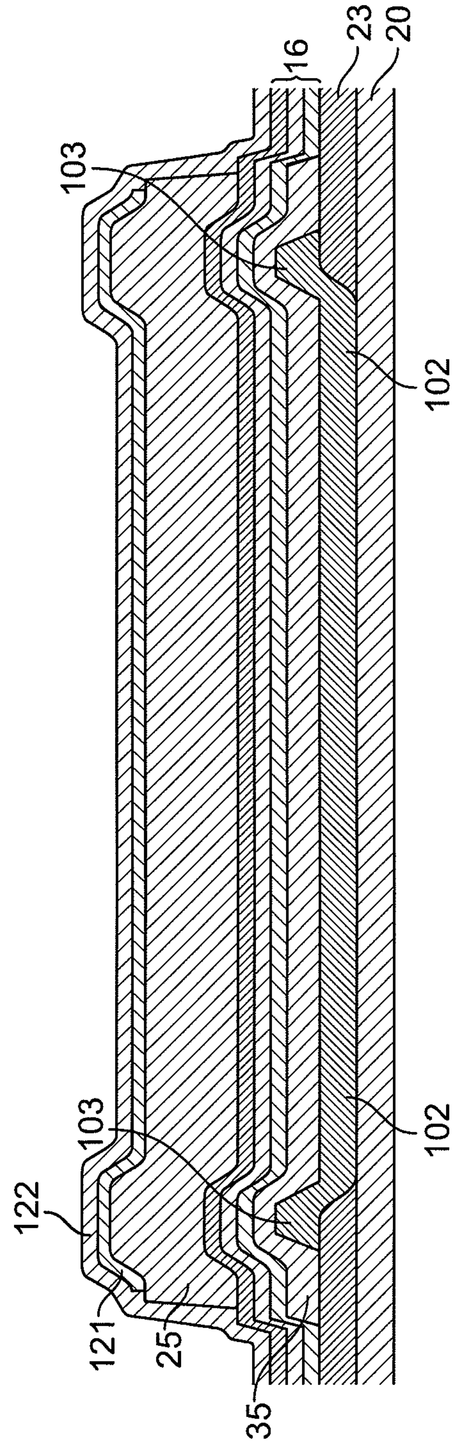

Figure 9J

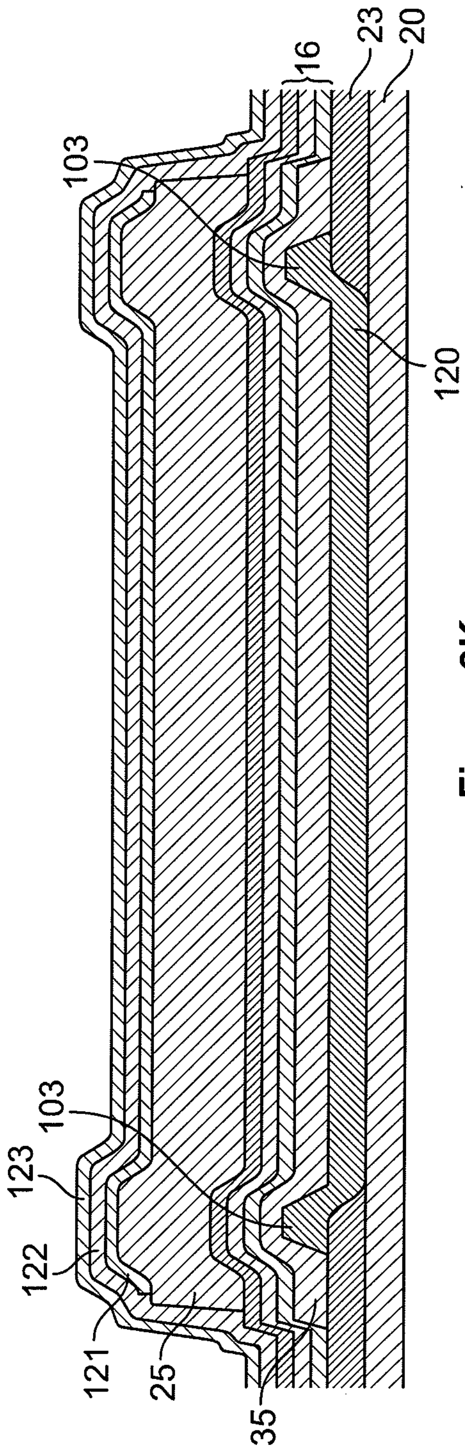

Figure 9K

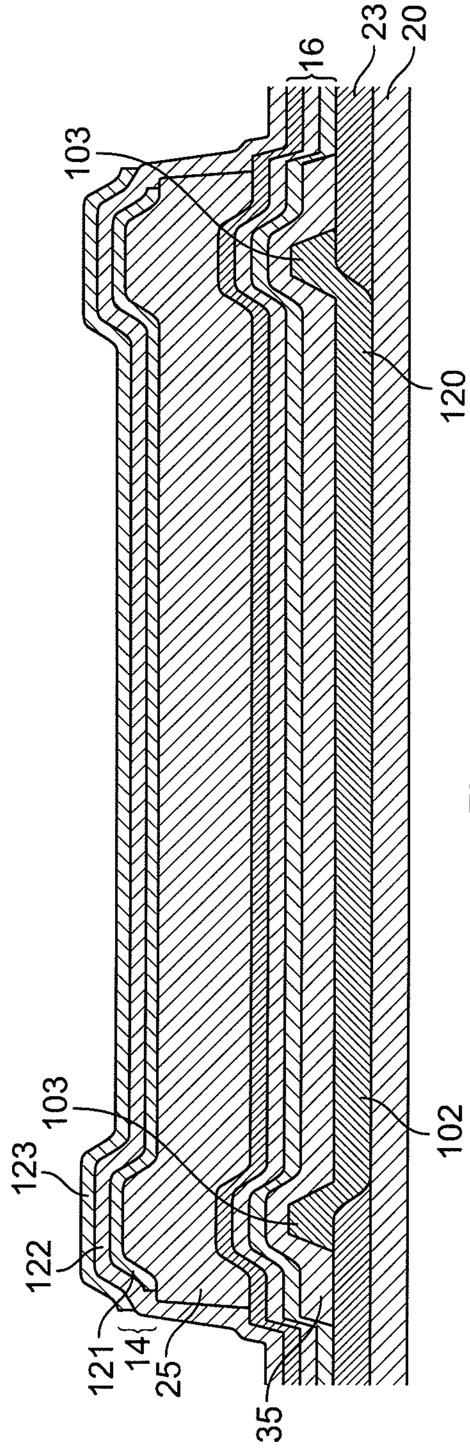

Figure 9L

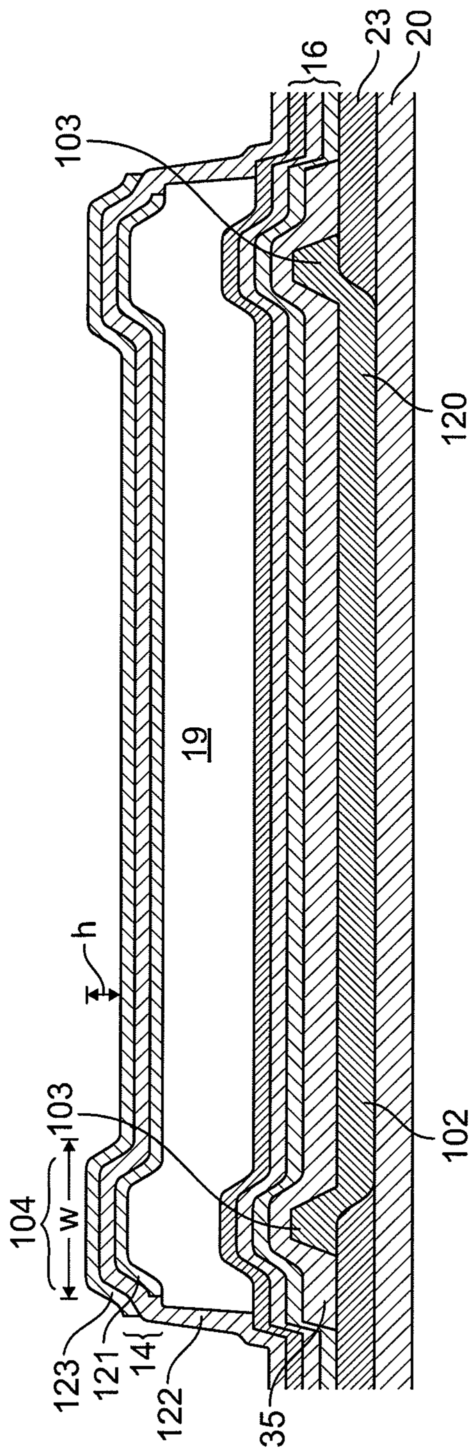

Figure 9M

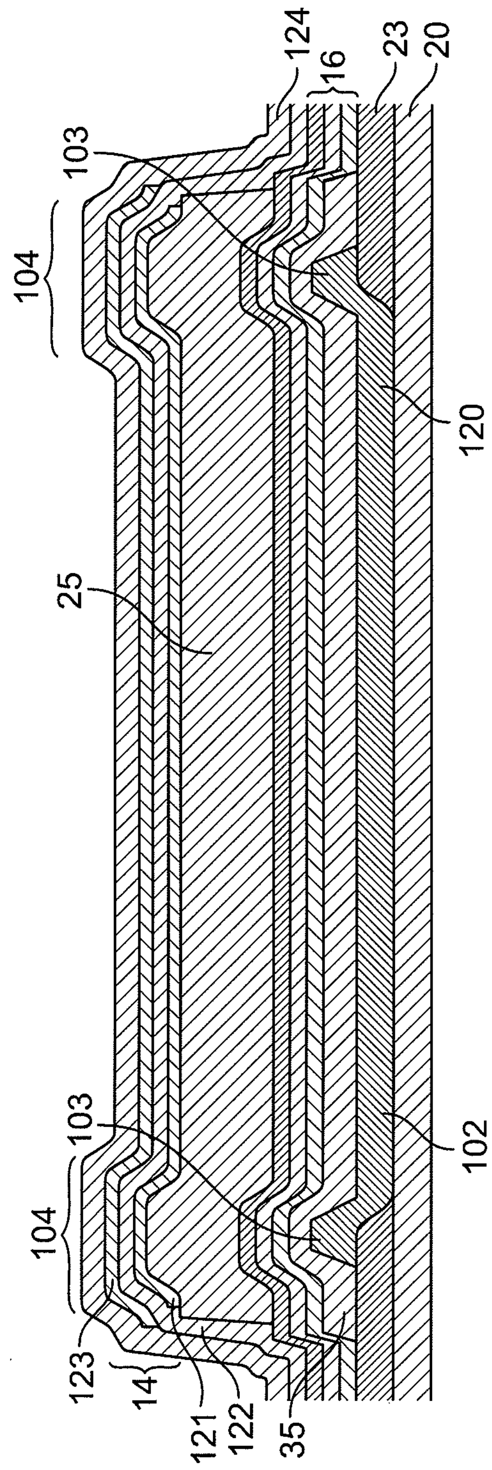

Figure 9N

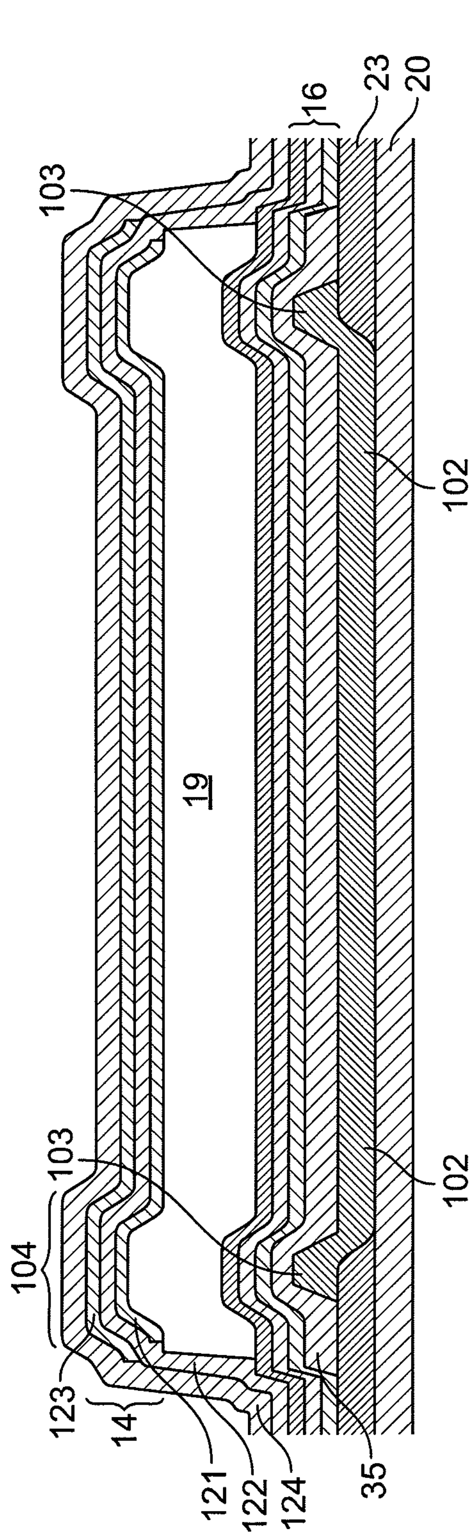

Figure 9O

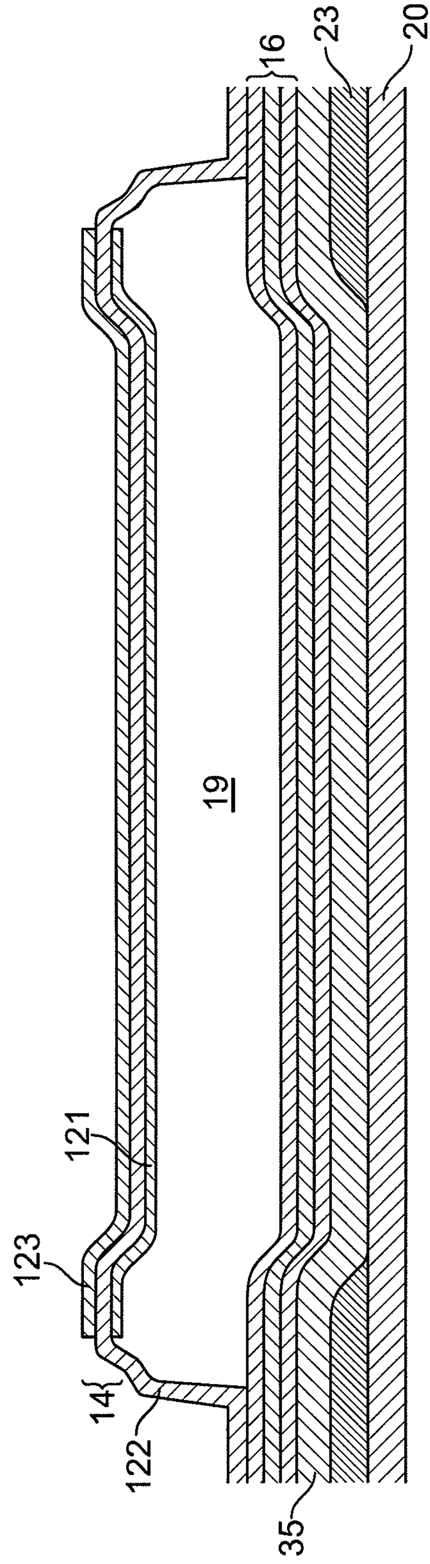

Figure 9P

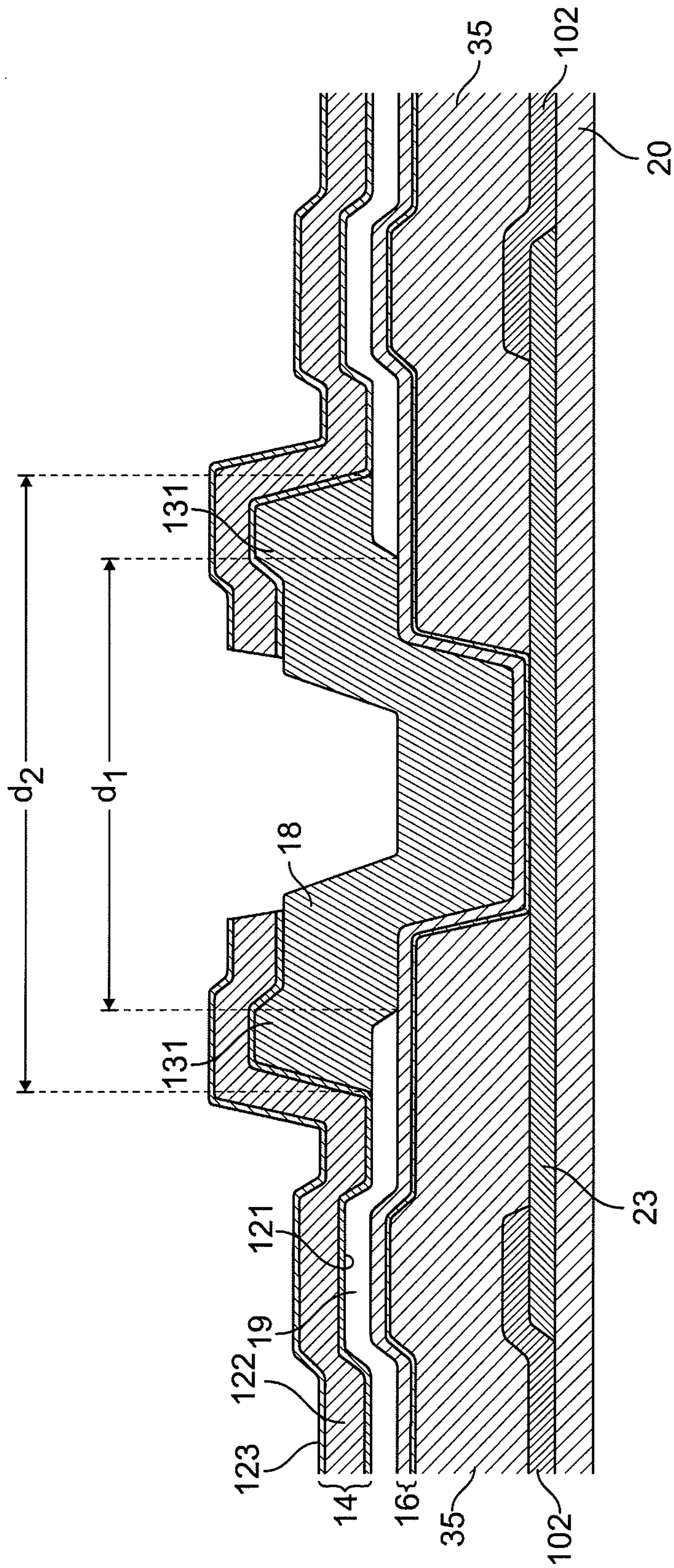

Figure 10A

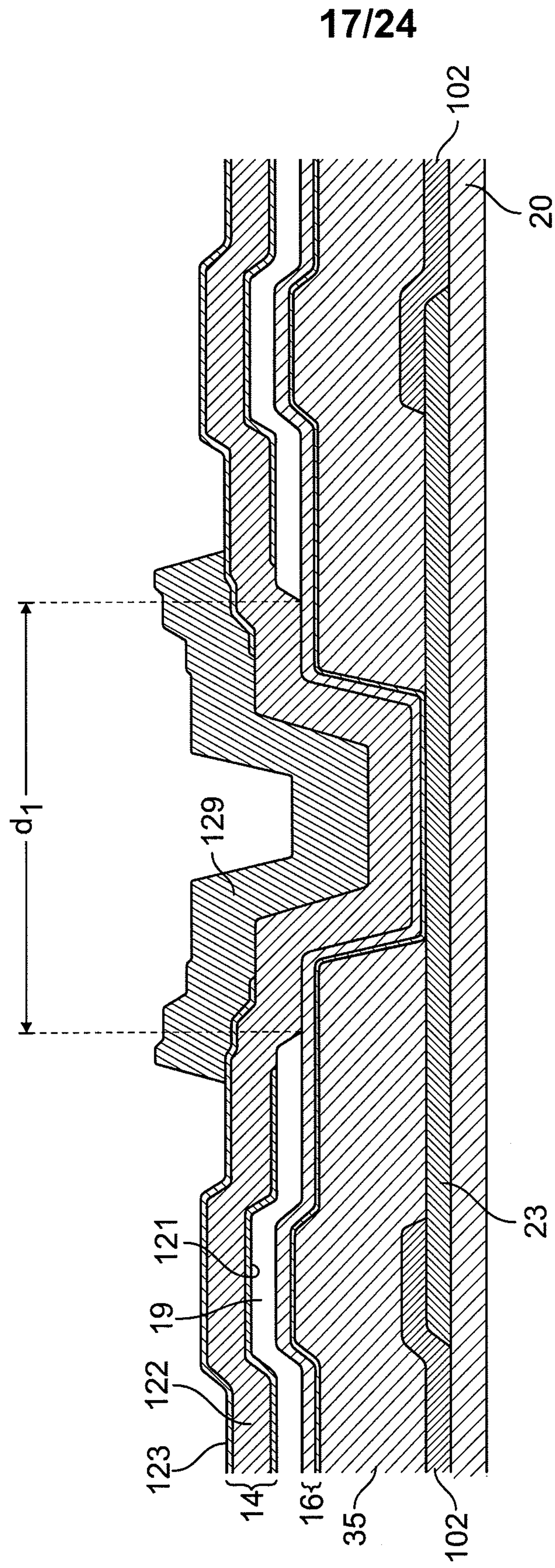

Figure 10B

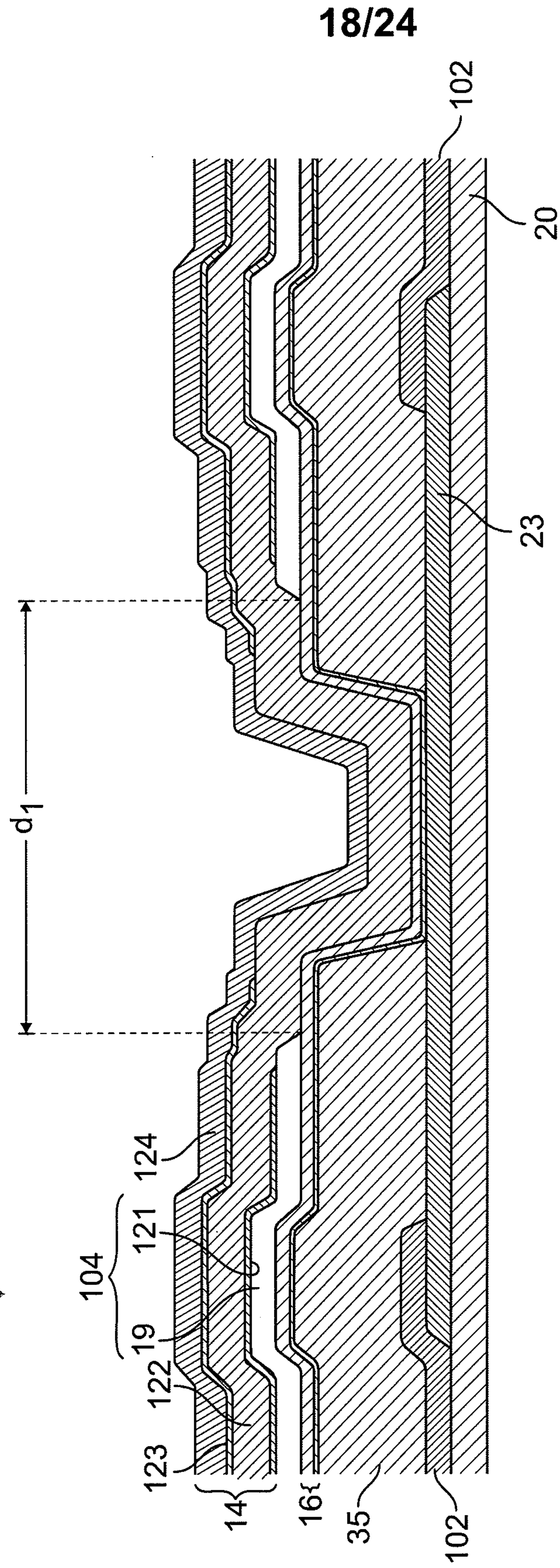

Figure 10C

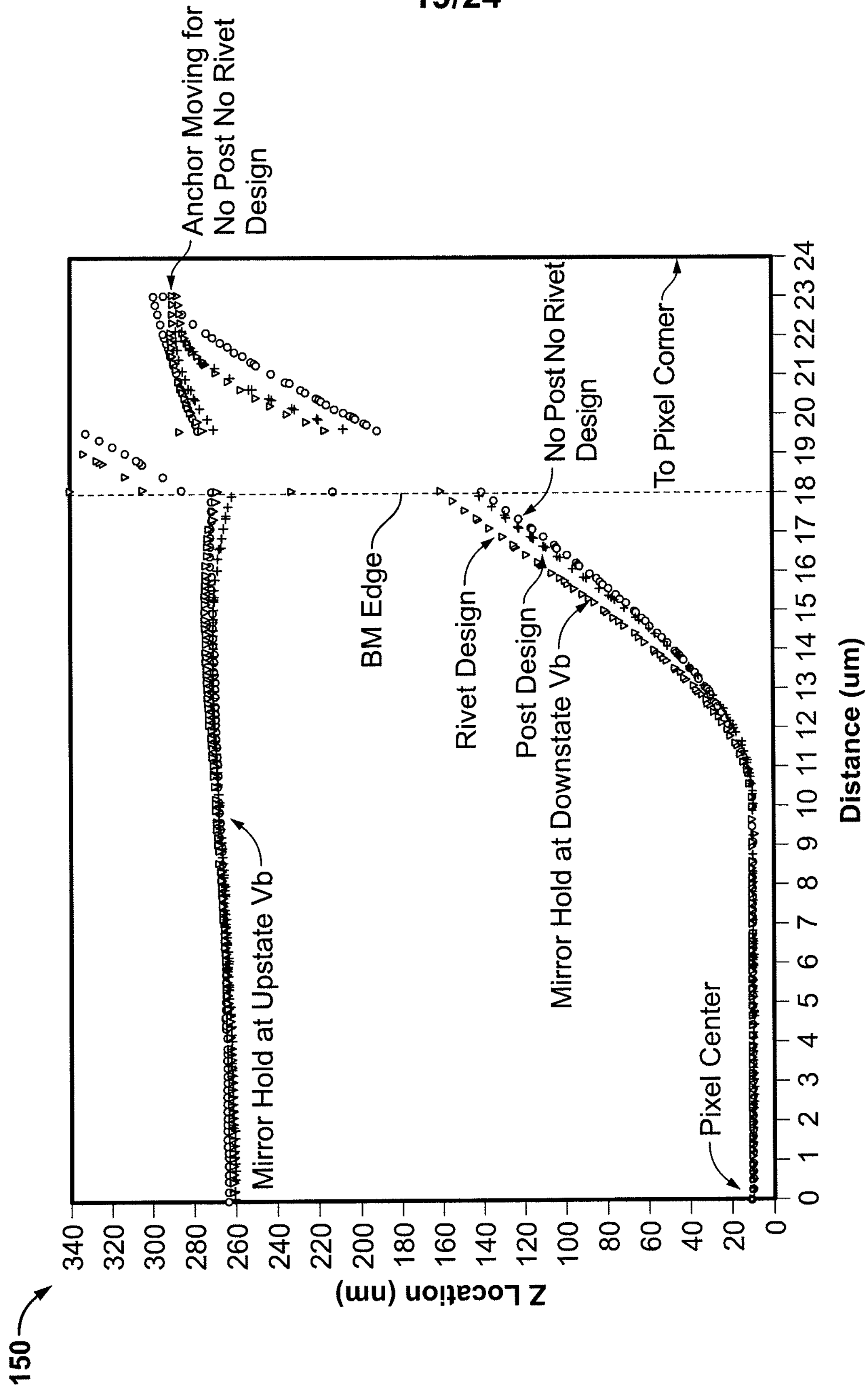

Figure 11

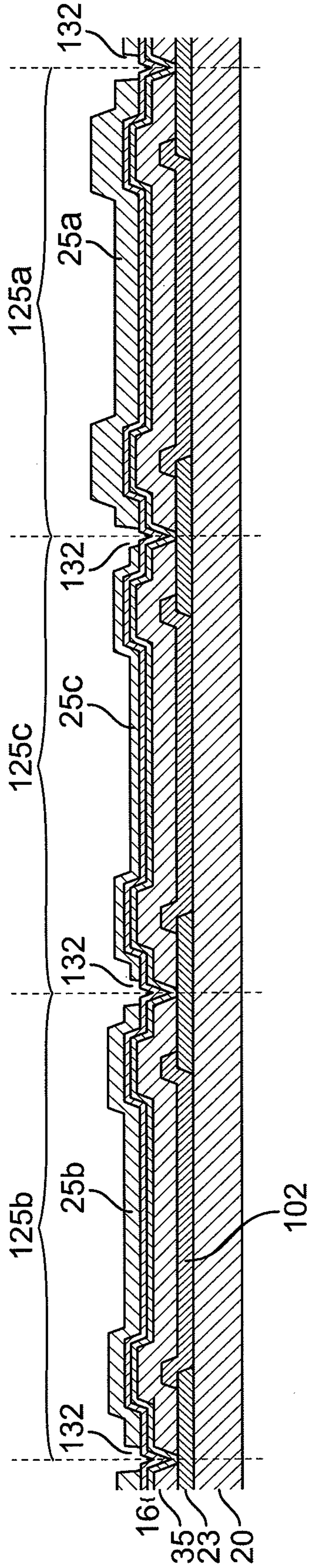

Figure 12A

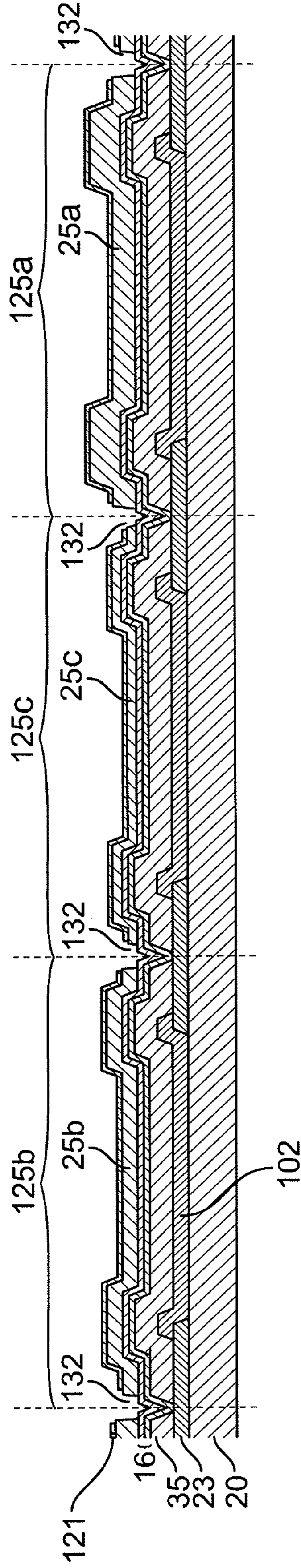

Figure 12B

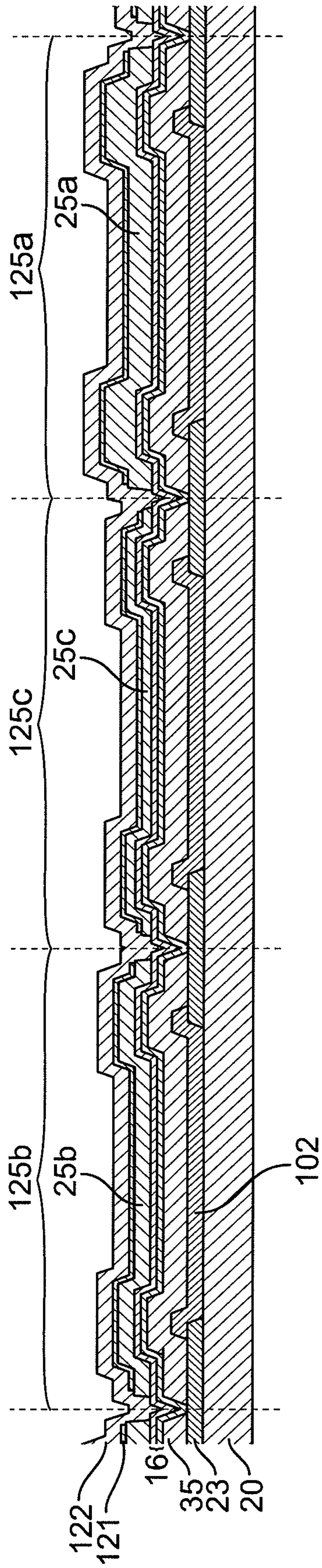

Figure 12C

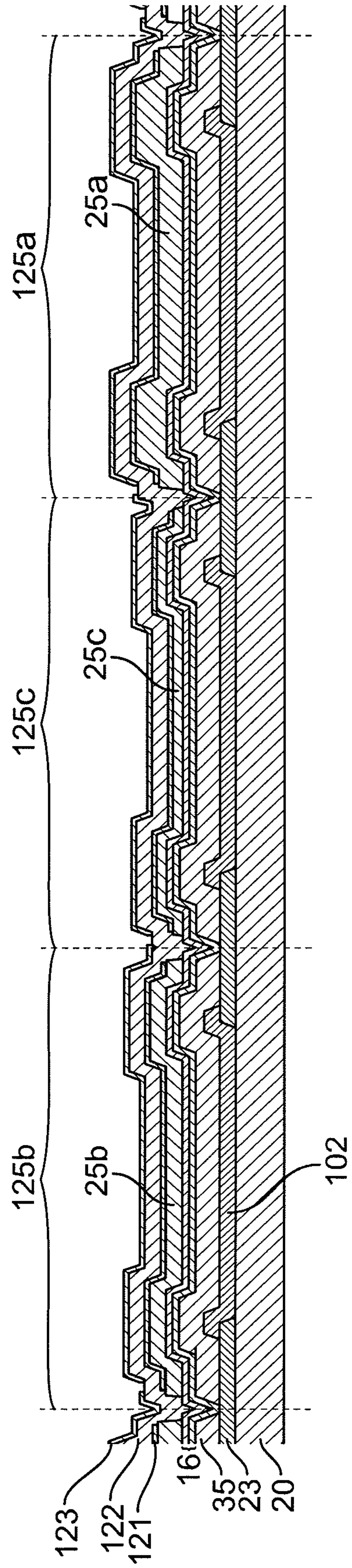

Figure 12D

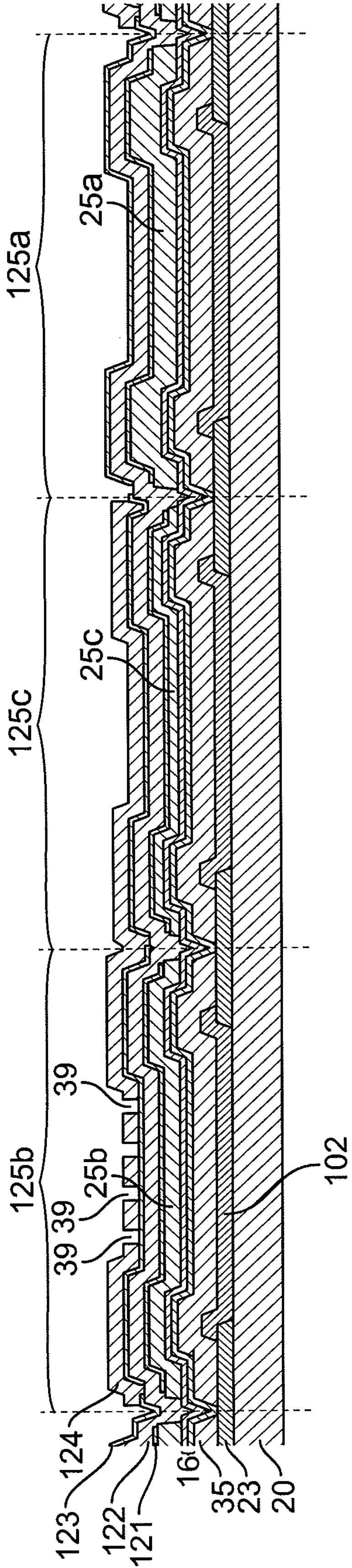

Figure 12E

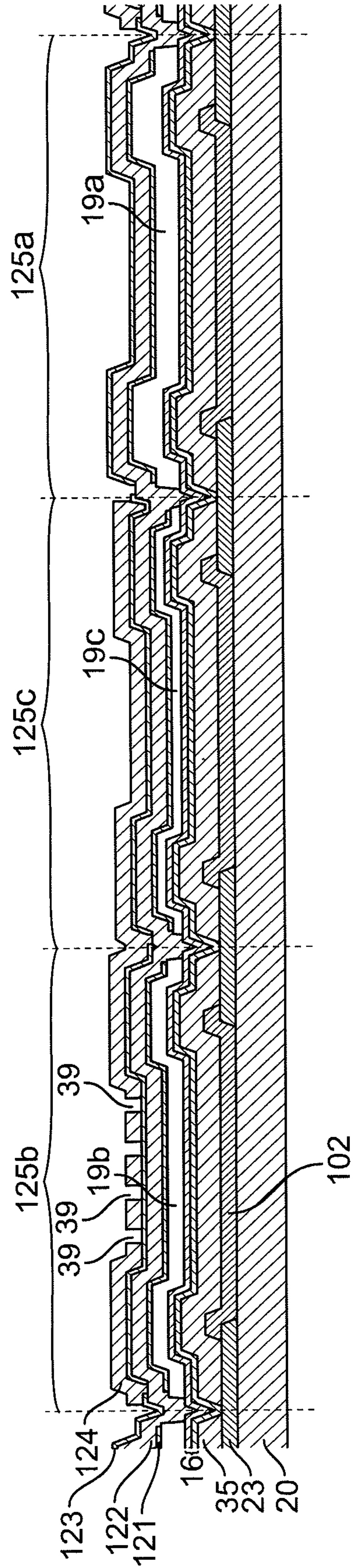

Figure 12F

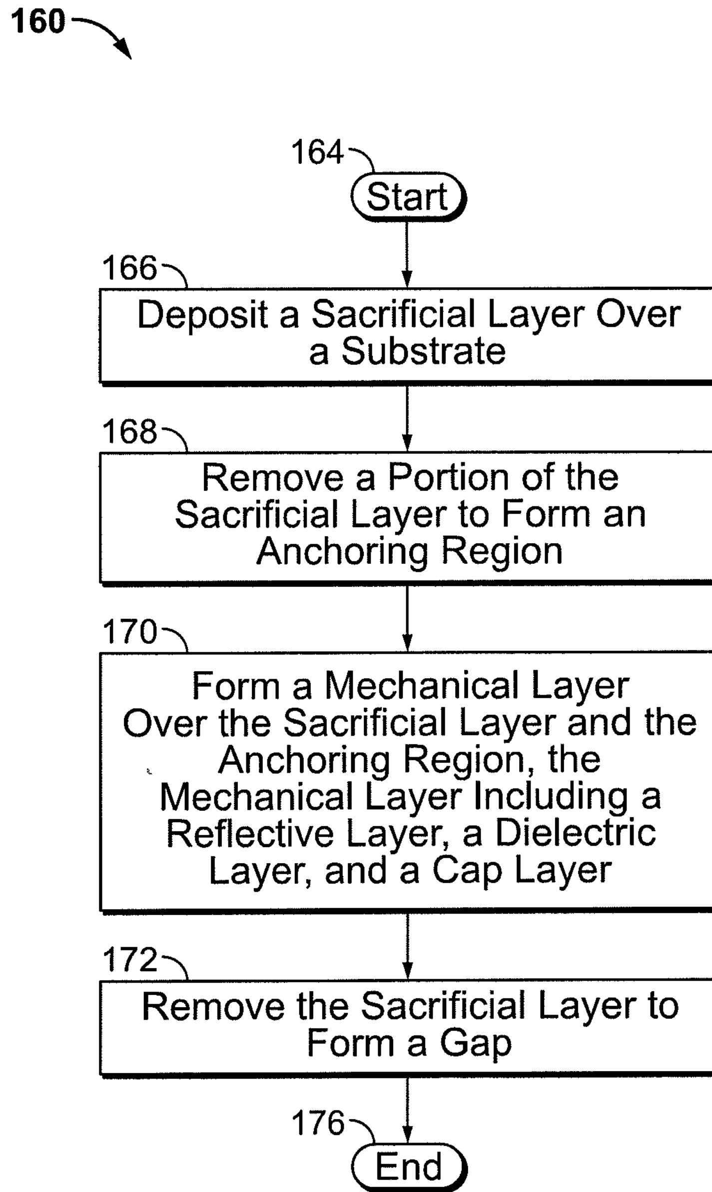

Figure 13

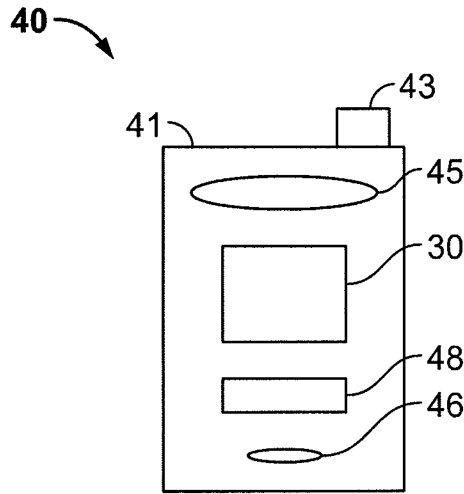

Figure 14A

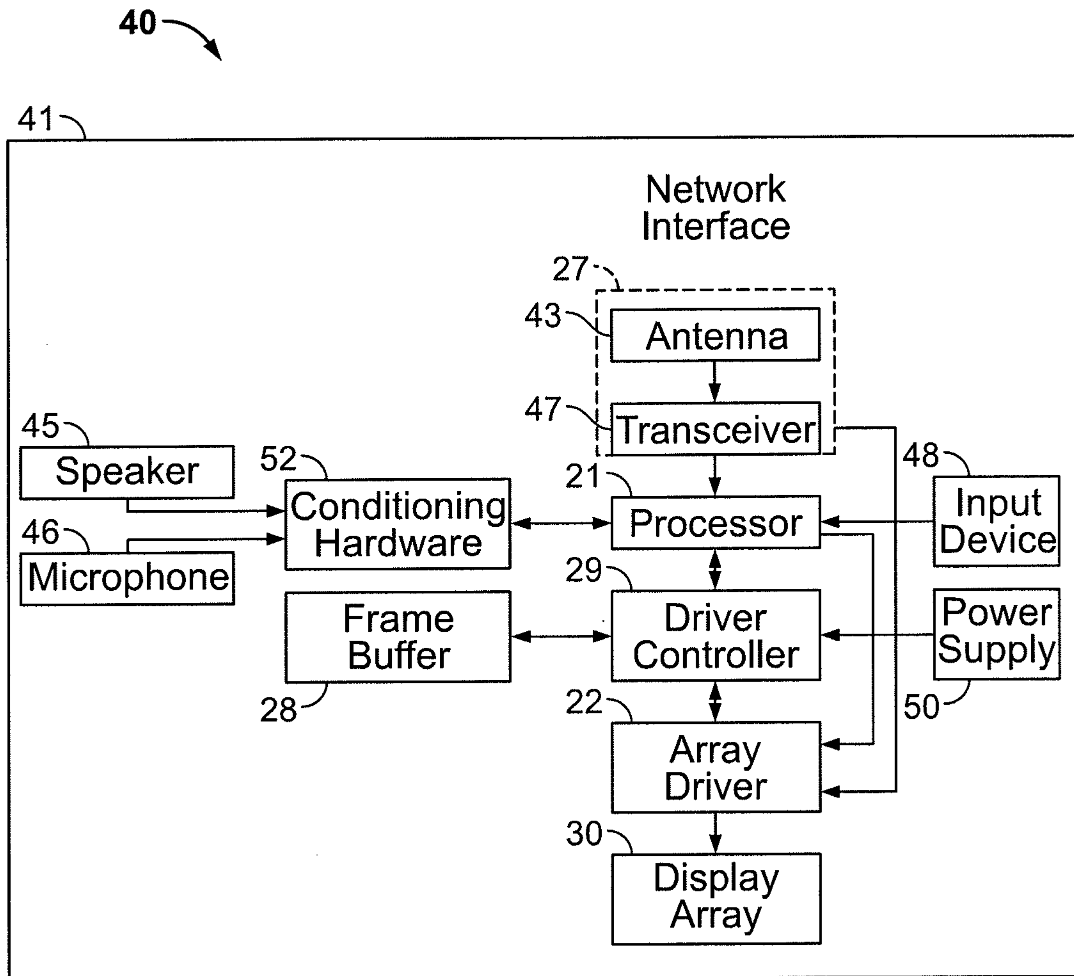

Figure 14B

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2011/031010

A. CLASSIFICATION OF SUBJECT MATTER
INV. G02B26/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G02B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 835 255 A (MILES MARK W [US]) 10 November 1998 (1998-11-10) column 13, line 59 - line 64 column 20, line 12 - column 21, line 65 column 17, line 64 - column 20, line 4 figures 20c,25-28	1-40
X	US 6 574 033 B1 (CHUI CLARENCE [US] ET AL) 3 June 2003 (2003-06-03) column 4, line 64 - column 5, line 30 figure 6	1,28
X	WO 99/52006 A2 (ETALON INC [US]; MILES MARK W [US]) 14 October 1999 (1999-10-14) page 9, line 11 - line 26 figure 1a	1,28
	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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Date of the actual completion of the international search	Date of mailing of the international search report
1 June 2011	14/06/2011

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2011/031010

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