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10-0399034
2003 09 08

(21) 10-2000-0023569
(22) 2000 05 02

(65)
(43)

2001-0104499
2001 11 26

(73) 373-1

(72) 3 860-1 2 413

103 905

(74)
:

(54)

1

1 (PARTIAL SEGMENT ACTIVATION)

2 (ADAPTIVE WINDOW CONTROL)

3a 3b 가

4

가

가

RC

(T.Sugibayashi, et al., "A 30ns 256-Mb DRAM with a Multi divided Array Structure" IEEE Journal of Solid State Circuit, pp1092~1098.Nov.,1993 /T Murotani, et al., "Hierarchical Word Line Architecture for Large Capacity DRAM" IEICE Trans. Electron., pp550~556, Apr.,1997)

(SRAM)

가

(EDRAM:Enhanced DRAM)

(CDRAM:Cache DRAM)

DRAM

가

가

가

1

1 64Mb, 128Mb, 256Mb SDRAM(

x8,4Bank)

(OPERATING CURRENT)

[1]

x8,4Bank	Row Add	Bank Add	Col Add	Operating Current*
64Mb	RA0 - RA11	BA0 ,BA1	CA0 - CA8	95mA - 115mA
128Mb	RA0 - RA11	BA0 ,BA1	CA0 - CA9	115mA - 150mA
256Mb	RA0 - RA12	BA0 ,BA1	CA0 - CA9	115mA - 140mA

1

가

가

가가

가

ACTIVATION), (ADAPTIVE WINDOW CONTROL),
(ENHANCED BANK INTERLEAVING)

(PARTIAL SEGMENT
(ASSOCIATIVE MAPPING),

1 (PARTIAL SEGMENT ACTIVATION)
1 N+1 (14)
N+1 (12), (22), (12)
(22) 가 (10) 2 (12) (14)

(10) 2 (12) (20) (22)

(20) 가 (10)

(20)가 (20)

2 (ADAPTIVE WINDOW CONTROL)

2 (44,46,47) 45 (Power Margin)가 가 5

5 가 40 가 46 5

(PAGE MISS) 가 2 4 (44,45,46,47 45,46,47,48)

44 가 3 (44,46,47) 40

(ACCESS)가 2 a b , 가 가 , 40

가 55 (WINDOW HIT)가

(HISTORY BIT) 가 가 90%

E-CHARGE) 가 가 40 (PR

가

3b 가

(PRE-FETCH)

가 1/N 가 N

3b 2 3a (65) (60,61,62,63)

가 4 3b

가

가 가

가 (INTERLEAVING) 가

DRAM 가 가

1 가

2 가

가 가

가 가

3

가

가 가

가 가

4

가

4

64MB/128MB/256MB

PC

(WINDO

(H/W)
W BOOTING)

(EXCEL)

(SDRAM)

30%

2% - 7%

5%

가

가

4

가

2

[2]

	Simulation (×8)			
	Scheme	64Mb	128Mb	256Mb
A	SDRAM	4K, 4Bank	8K, 4Bank	8K, 4Bank
B	PSA	2K, 4Bank	2K, 4Bank	2K, 4Bank
C	PSA + EBI(50%)		2K, 8Bank	2K, 8Bank
D	PSA + EBI(100%)	2K, 8Bank	2K, 16Bank	2K, 16Bank
E	PSA + AWC + EBI(50%)		2K, 8Bank	2K, 8Bank
F	PSA + AWC + EBI(100%)	2K, 8Bank	2K, 16Bank	2K, 16Bank

가

64MB DRAM

(PSA),

(AWC),

(EBI),

(ASM)

(EML)

DRAM

(DDR DRAM)

(RDRAM INTERFACE)

가

(57)

1.

가

가

1

2

3

2.

가

가

3.

2

4.

2

5.

1

4

가

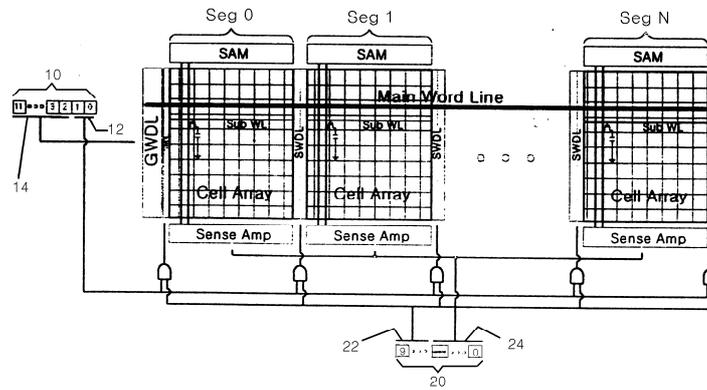
6.

7.

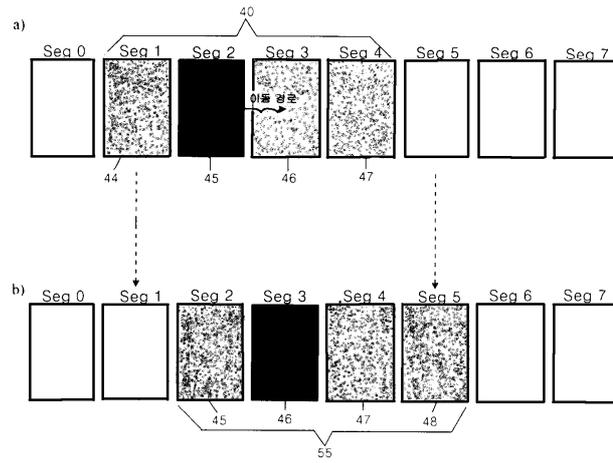
8.

9.

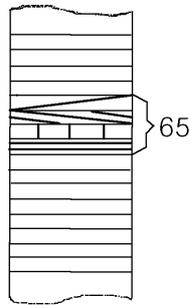
1



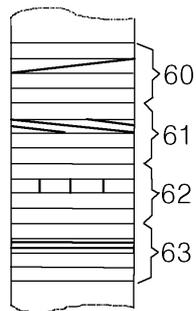
2



3a



3b



4

