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(54) **ELECTROLESS DEPOSITION PROCESSES AND COMPOSITIONS FOR FORMING INTERCONNECTS**

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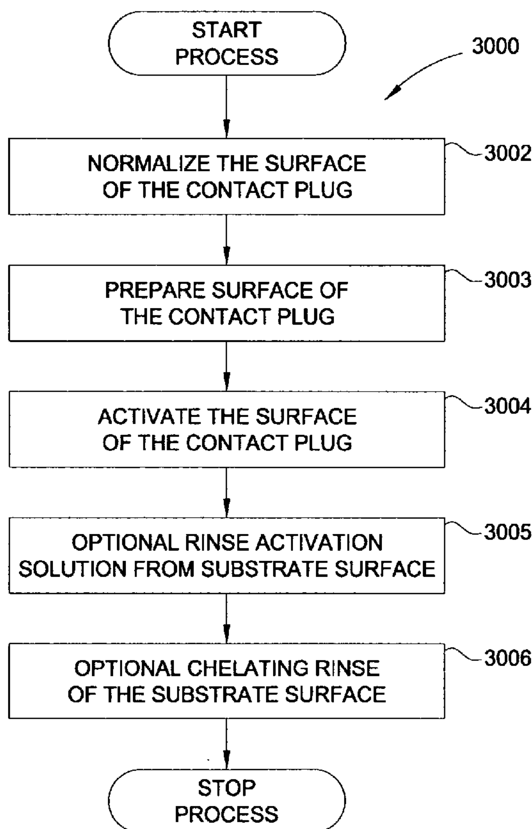
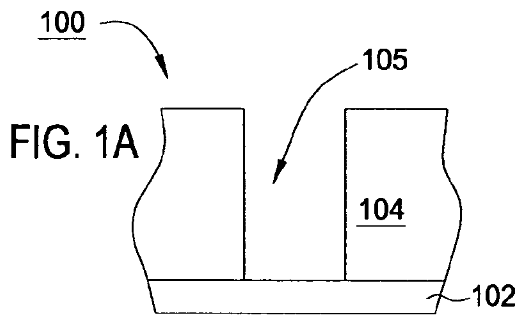
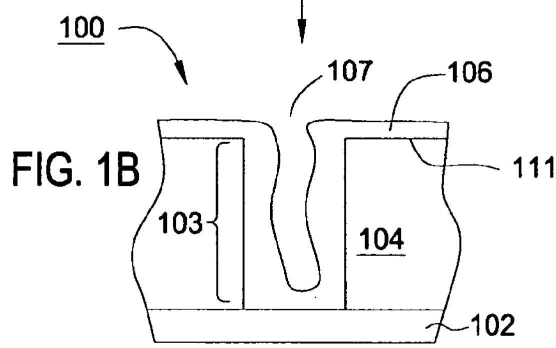
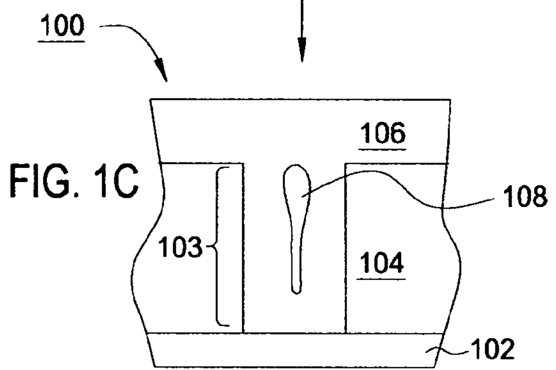
(57) **ABSTRACT**

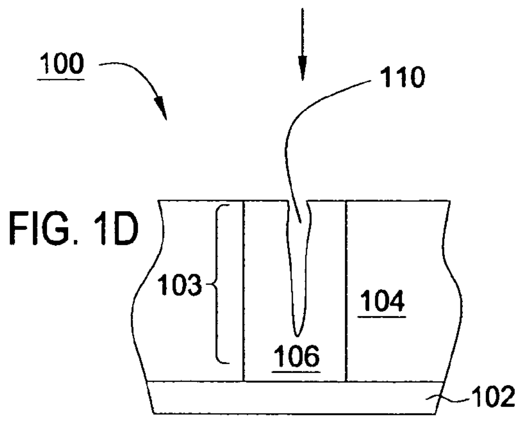
In one embodiment, a method for depositing a material on a substrate is provided which includes positioning a substrate containing a contact within a process chamber, exposing the substrate to at least one pretreatment step and depositing a fill the contact vias by an electroless deposition process. The pretreatment step contains multiple processes for exposing the substrate to a wet-clean solution, a hydrogen fluoride solution, a tungstate solution, a palladium activation solution, an acidic rinse solution, a complexing agent solution or combinations thereof. Generally, the HARC via contains a tungsten oxide surface and the shallow contact via may contain a tungsten silicide surface. In some example, the substrate is pretreated such that both vias are filled at substantially the same time by a nickel-containing material through an electroless deposition process.

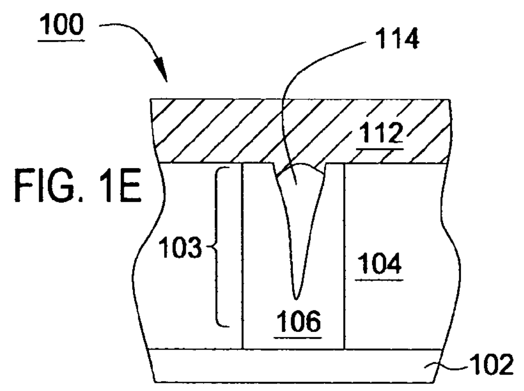


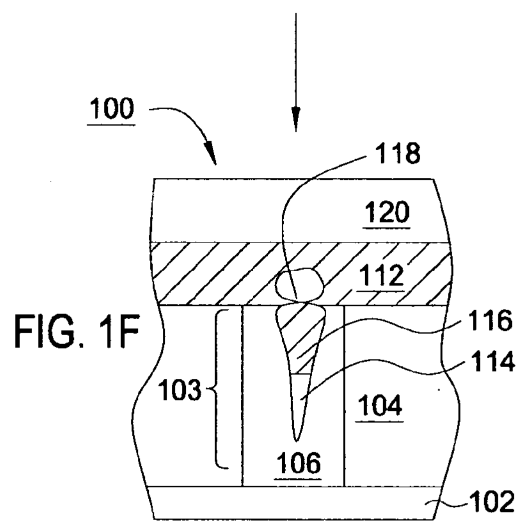












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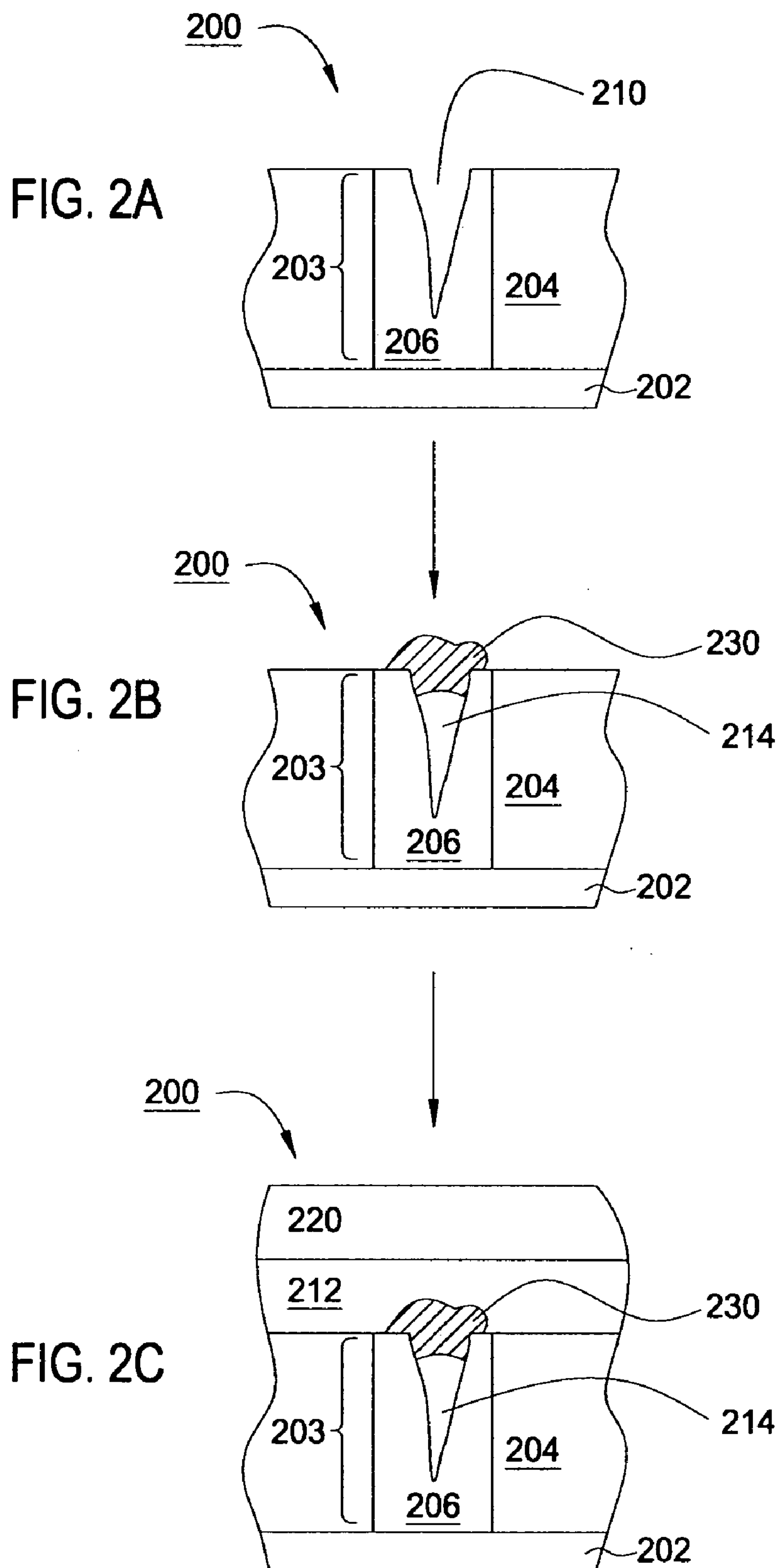
200
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FIG. 2A
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FIG. 2B
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FIG. 2C
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202

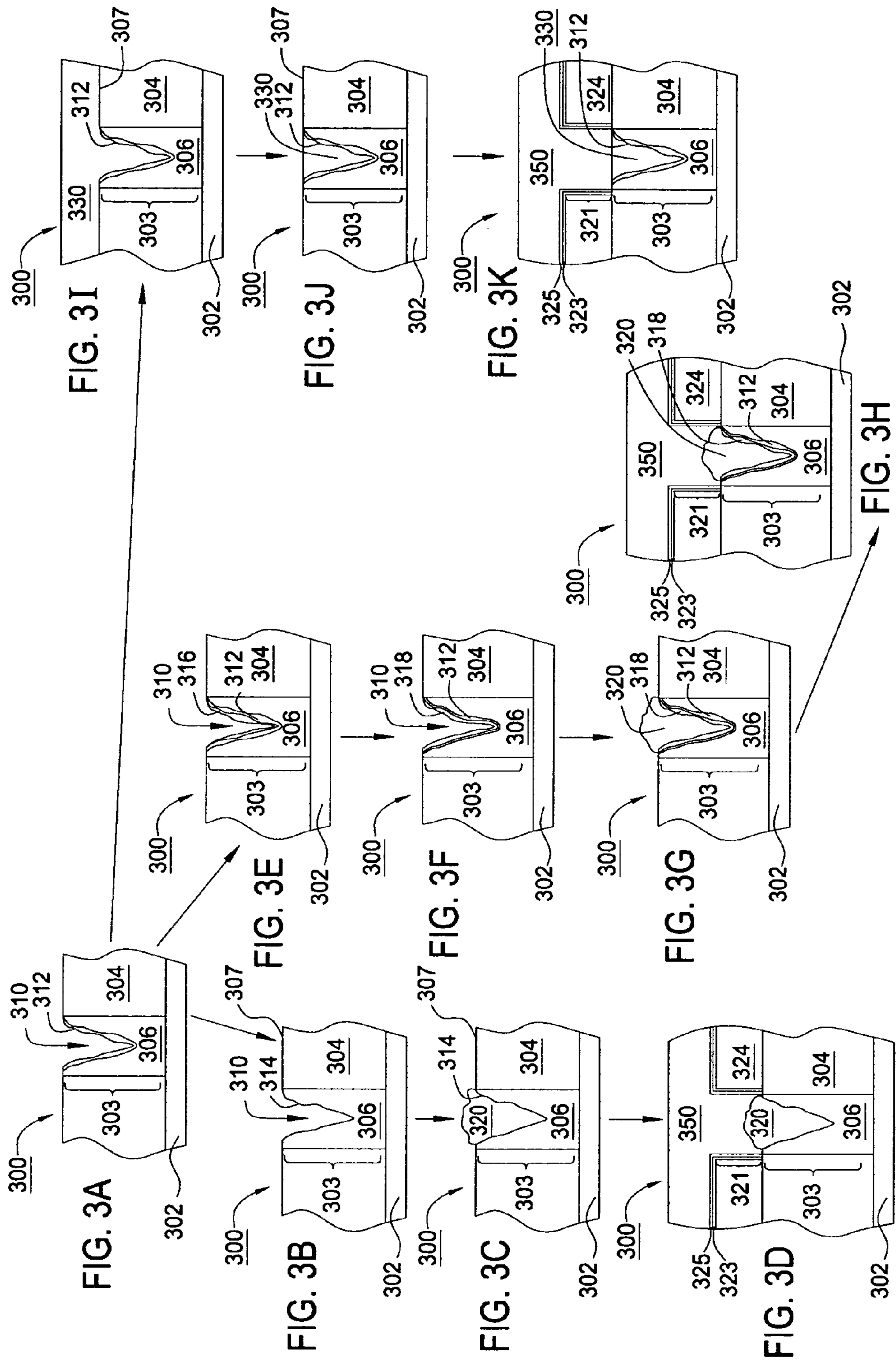
FIG. 3A
FIG. 3B
FIG. 3C
FIG. 3D
FIG. 3E
FIG. 3F
FIG. 3G
FIG. 3H
FIG. 3I
FIG. 3J
FIG. 3K
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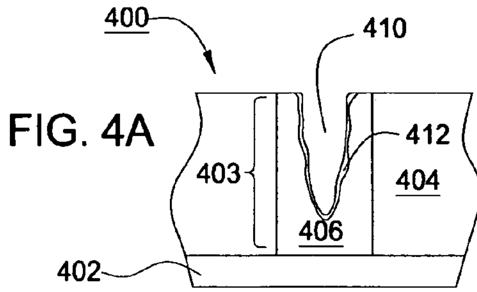

FIG. 4A

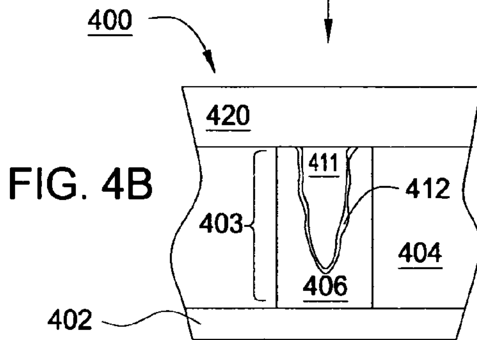

FIG. 4B

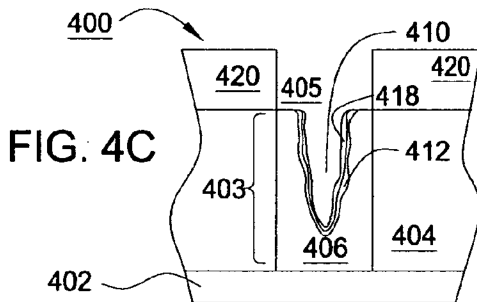

FIG. 4C

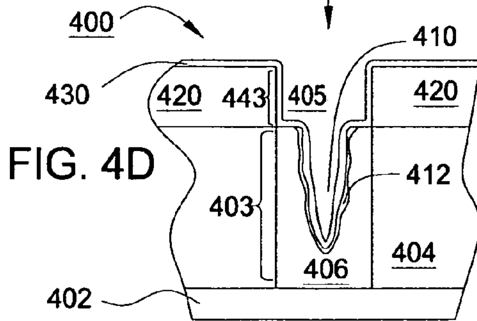

FIG. 4D

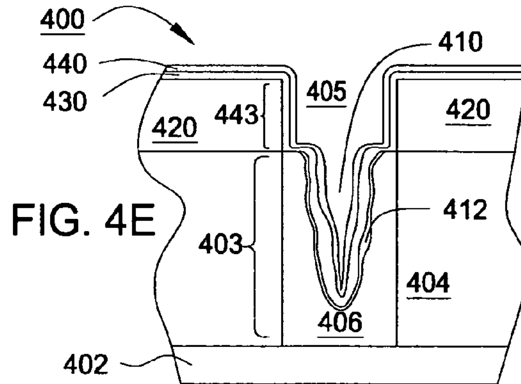

FIG. 4E

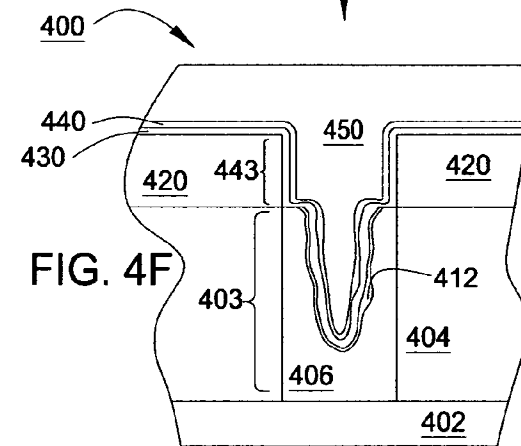

FIG. 4F

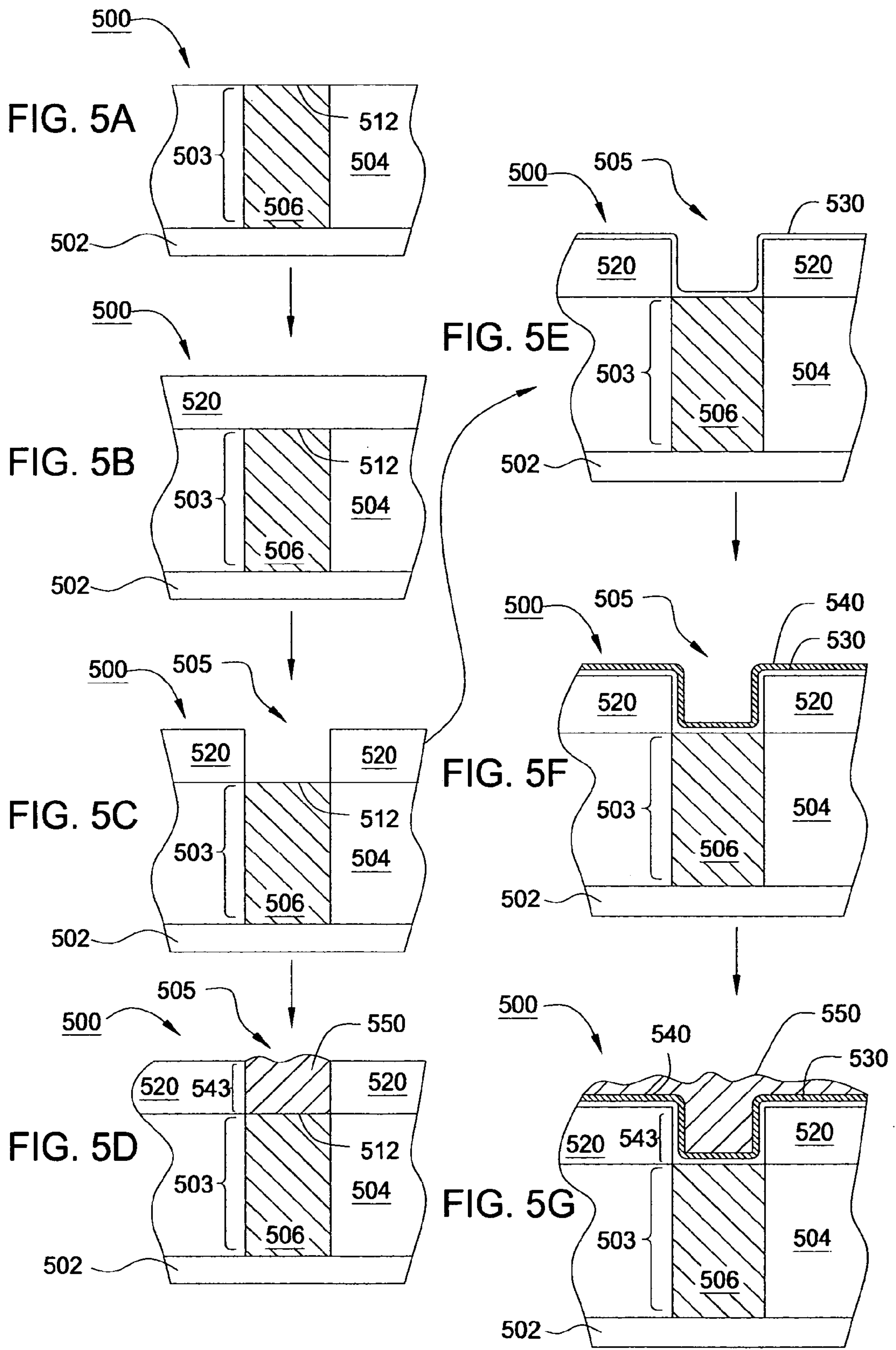
FIG. 5A
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FIG. 5E
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FIG. 5G
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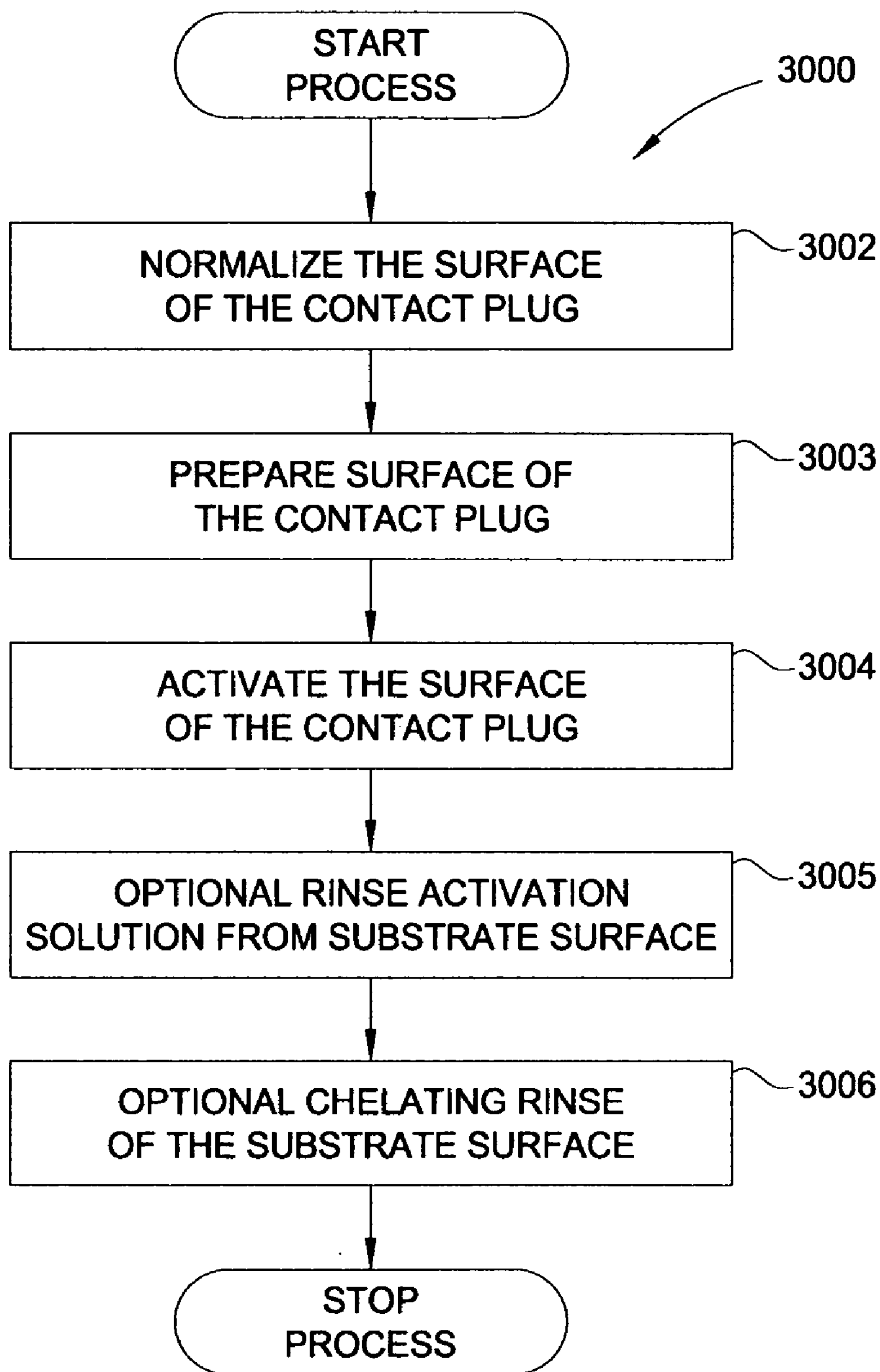

FIG. 6

ELECTROLESS DEPOSITION PROCESSES AND COMPOSITIONS FOR FORMING INTERCONNECTS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims benefit of U.S. Provisional Patent Application Ser. No. 60/663,493, filed Mar. 18, 2005 [APPM 9916L], U.S. Provisional Patent Application Ser. No. 60/683,599, filed May 23, 2005 [APPM 9916L02], U.S. Provisional Patent Application Ser. No. 60/703,538, filed Jul. 29, 2005 [APPM 9916L03], U.S. Provisional Patent Application Ser. No. 60/703,633, filed Jul. 29, 2005 [APPM 9916L04], U.S. Provisional Patent Application Ser. No. 60/709,564, filed Aug. 19, 2005 [APPM 9916L05], and U.S. Provisional Patent Application Ser. No. 60/754,230, filed Dec. 27, 2005 [APPM 9916L06], which are all herein incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] Embodiments of the invention generally relate to methods for depositing materials on substrates, and more specifically to methods of forming metal interconnects.

[0004] 2. Description of the Related Art

[0005] Multilevel, 45 nm node metallization is one of the key technologies for the next generation of very large scale integration (VLSI). The multilevel interconnects that lie at the heart of this technology possess high aspect ratio features, including contacts, vias, lines and other apertures. Reliable formation of these features is very important for the success of VLSI and the continued effort to increase quality and circuit density on individual substrates. Therefore, there is a great amount of ongoing effort being directed to the formation of void-free features having high aspect ratios of 10:1 (height:width) or greater.

[0006] Tungsten is a choice metal for filling VLSI features, such as sub-micron high aspect ratio contact (HARC) on a substrate. Contacts are formed by depositing a conductive interconnect material, such as tungsten into an aperture (e.g., via) on the surface of insulating material disposed between two spaced-apart conductive layers. A high aspect ratio of such an opening may inhibit deposition of a conductive interconnect material to fill an aperture. Although tungsten is a popular interconnect material, vapor deposition processes for depositing tungsten may suffer by forming a void or a seam within the contact plug, as illustrated in **FIG. 1C**.

[0007] **FIG. 1A** depicts a schematic cross-sectional view of an integrated circuit device on substrate **100** containing a via or aperture **105** formed in dielectric layer **104** to expose contact layer **102** (e.g., source region, drain region, polysilicon gate). During a vapor deposition process that may include chemical vapor deposition (CVD) or atomic layer deposition (ALD), a tungsten layer **106** is deposited on dielectric layer **104** and within aperture **105**, including on contact layer **102** and the sidewalls of dielectric layer **104**, to form the plug **103**, as illustrated in **FIG. 1B**. Near the opening **107** of plug **103**, tungsten layer **106** may pinch off, depicted in **FIG. 1C**, so that plug **103** maintains a gap, seam, or void (i.e., gap **108**) therein. During a subsequent chemical mechanical polishing (CMP) process, which removes a portion of tungsten layer **106** and dielectric layer **104** from the field region **111** of substrate **100**, the void **108** may be exposed to form a gap **110** within plug **103**, as illustrated in **FIG. 1D**. **FIG. 1E** illustrates a void **114** that is formed when the conductive layer **112** deposited over the gap **110** on the substrate **100**. The conductive layer **112**, as shown in **FIG. 1E**, can be a portion of a via, trench or bit line. Substrate **100** may contain additional layers deposited thereon, such as layer **120** (e.g., interlayer dielectrics (ILD)).

[0008] Defects, such as a seam or a void **114**, may cause a series of problems during the fabrication of electronic devices depicted herein. The resistance to current flow through the plug **103** is impaired due to the lack of tungsten material in the void **114**. However, a more serious obstacle during fabrication is the displacement of voids from one layer to the next. For example, subsequent fabrication processes of substrate **100** may include the deposition of layer **120** (e.g., dielectric layer) on conductive layer **112**. During subsequent thermal processing, such as an annealing process, the material **116** from conductive layer **112** may diffuse into void **114** and form a void **118** within conductive layer **112**. As illustrated in **FIG. 1F**, material **116** may not diffuse completely to the bottom of void **114**. The defect formed in the conductive layer **112**, such as void **118**, will increase the resistance of the circuit containing the defect and thus affect device performance. Ultimately, the defects in the conductive layer **112** can affect the device yield of the fabricated substrate.

[0009] Therefore, a need exists for a method to form an interconnect on a contact plug that is free of voids. If a void is present, then selected materials are deposited to cap or fill the voids and prevent subsequent displacement of conductive layers deposited thereon.

SUMMARY OF THE INVENTION

[0010] The present invention generally provide a method of forming an electrical contact on a silicon substrate, comprising providing a substrate containing an exposed tungsten-containing contact plug exposed that has an exposed gap formed therein, exposing the substrate to a pretreatment process, wherein the pretreatment process is adapted to remove an oxide layer from a surface of the exposed tungsten-containing contact plug, filling the exposed gap with a fill material.

[0011] Embodiments of the invention further provide a method of forming an electrical contact on a silicon substrate, comprising providing a silicon substrate having a first dielectric layer which is disposed on a surface of the silicon substrate and a first aperture formed in the first dielectric layer, wherein a doped silicon containing region of the silicon substrate is exposed at the bottom of the first aperture, filling the first aperture formed in the first dielectric layer with a tungsten containing layer, wherein the tungsten containing layer is in electrical communication with the doped silicon containing region, removing an amount of the tungsten containing layer disposed on the first dielectric layer, wherein a gap formed in the tungsten containing layer during the step of filling the first aperture is exposed, and depositing a material on the surface of the silicon substrate to substantially cover the gap formed in the tungsten containing layer.

[**0012**] Embodiments of the invention further provide a method of forming an electrical contact on a silicon substrate, comprising providing a substrate containing first dielectric layer that contains at least one tungsten-containing contact plug that has an exposed surface, forming a second dielectric layer over the first dielectric layer and the tungsten-containing contact plug, forming a second aperture in the second dielectric layer that is in communication with the exposed surface of the tungsten-containing contact plug, and selectively filling the second aperture with a fill material.

[**0013**] Embodiments of the invention further provide a method of forming an interconnect on a silicon substrate, comprising providing a substrate having an aperture formed in a dielectric layer disposed on a surface of the substrate, wherein the aperture is in communication with an exposed surface of a tungsten-containing contact plug, dispensing a clean solution on an the exposed surface of the tungsten-containing contact plug, wherein the clean solution comprises hydrogen fluoride, disposing a preparation solution on the exposed surface of the tungsten-containing contact plug, wherein the preparation solution comprises a tungstate source, depositing a initiation layer on the exposed surface of the tungsten-containing contact plug using an activation solution, activating the initiation layer using a rinse activation solution, and selectively filling the second aperture with a fill material.

BRIEF DESCRIPTION OF THE DRAWINGS

[**0014**] So that the manner in which the above recited features of the invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[**0015**] **FIGS. 1A-1F** illustrate schematic cross-sectional views of an integrated circuit formed by a process described in the art;

[**0016**] **FIGS. 2A-2C** illustrate schematic cross-sectional views of an integrated circuit formed by a process to cap a defect within a contact plug described within an embodiment herein;

[**0017**] **FIGS. 3A-3K** illustrate schematic cross-sectional views of an integrated circuits formed by processes to fill defects within contact plugs described within embodiments herein;

[**0018**] **FIGS. 4A-4F** illustrate schematic cross-sectional views of an integrated circuit formed by another process to fill a defect within a contact plug described within an embodiment herein;

[**0019**] **FIGS. 5A-5G** illustrate schematic cross-sectional views of a method of forming an interconnect layer on a contact plug that is described within an embodiment herein;

[**0020**] **FIG. 6** is a flow chart depicting a pretreatment process as described within an embodiment herein.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[**0021**] Embodiments of the invention provide methods of forming a device over a tungsten-containing contact plug. In one aspect, a process of capping and filling defects formed in a tungsten-containing contact plug that have been exposed during a subsequent chemical mechanical polishing (CMP) process is performed. Defects that are present in the tungsten-containing contact plug may include gaps, voids, and/or seams (hereafter gaps). In one embodiment, gaps are plugged or capped with a material that will be able to withstand subsequent thermal processing and inhibit displacement of the formed void therein. Gaps may be filled, or plugged, by employing selective deposition process that include chemical vapor deposition (CVD), atomic layer deposition (ALD), and electroless deposition processes. Preferably, the material used to fill the gaps or voids may include nickel, cobalt, tungsten and alloys thereof. In another embodiment, the method may include the steps of pretreating and then subsequently filling the gap by use of a CVD, ALD or electroless process using a conductive material such as nickel, ruthenium, cobalt, tungsten and alloys thereof.

[**0022**] In an alternative embodiment, a gap may be filled with a dielectric material. In one example, a spin-on-glass (SOG) is deposited by a spin coating process. SOG materials typically include silicon dioxide (SiO_2) or doped SiO_2 materials. In another example, hafnium silicate is deposited by a vapor deposition process.

[**0023**] In another embodiment, the gaps within a tungsten plug are filled during a later process. For example, the gap is temporally ignored, a dielectric layer is deposited on the substrate surface covering the gap and a second aperture is formed therein by an etching process over the tungsten plug and revealing the gap. A barrier layer (e.g., tantalum-containing) and a seed layer (e.g., copper) are sequential deposited by vapor deposition processes, such as physical vapor deposition (PVD) process.

Capping Process

[**0024**] Gaps within a tungsten-containing contact plug may be filled with a material that will be stable during subsequent semiconductor fabrication processes and inhibit the creation voids in the subsequent deposited metal layers. Gaps may be capped by employing selective vapor deposition processes (e.g., CVD or ALD) or liquid deposition processes (e.g., electroless) to deposit a capping material, such as nickel, cobalt, tungsten and alloys thereof.

[**0025**] **FIG. 2A** illustrates a cross-sectional view of substrate **200** following a CMP process, as discussed above while forming a tungsten-containing contact plug depicted in **FIGS. 1A-1D**. Substrate **200** contains contact layer **202** (e.g., MOS device source region, drain region, or gate region), dielectric layer **204** and plug **203** that includes tungsten layer **206** and gap **210** therein. The gap **210**, which may be a seam, void or other defect, is created in tungsten layer **206** during the formation of the plug **203** (e.g., tungsten CVD process) and is then exposed during the subsequent CMP process.

[**0026**] Dielectric layer **204** may contain a semiconductor material that includes silicon or silicon-containing materials. Dielectric layer **204** may be an insulating material such as silicon dioxide, silicon nitride, silicon-on-insulator (SOI), silicon oxynitride and/or carbon-doped silicon oxides, such as SiO_xC_y, for example, BLACK DIAMOND™ low-k dielectric, available from Applied Materials, Inc., located in

Santa Clara, Calif. Contact layer **202** may contain a doped silicon layer. Tungsten layer **206** may contain tungsten, tungsten alloys or a tungsten-containing material that includes tungsten and oxygen, nitrogen, boron, silicon or combinations thereof. Due to the exposure to the atmospheric environment, the surface of the tungsten layer **206** may contain contaminates or oxides thereon.

[**0027**] **FIG. 2B** depicts a capping layer **230** deposited on substrate **200** that covers gap **210** to form void **214**. Capping layer **230** may be composed of a conductive material or a dielectric material that will withstand subsequent thermal processing and inhibit displacement of void **214** into the subsequently deposited layers. Preferably, capping layer **230** contains a metal deposited by a liquid deposition process or a vapor deposition process. In one example, capping layer **230** is a nickel-containing layer deposited by an electroless deposition solution. In another example, capping layer **230** is a cobalt-containing layer (e.g., CoW-alloy) deposited by an electroless deposition solution. In another example, capping layer **230** is a nickel-containing layer deposited by a CVD process. In a further example, capping layer **230** is a dielectric material, such as a hafnium silicate layer deposited by a CVD process.

[**0028**] Conductive layer **212** is deposited on the surface of substrate **200** containing capping layer **230** and dielectric layer **204**, as depicted in **FIG. 2C**. Layer **220** is deposited on conductive layer **212**. Conductive layer **212** may contain copper, tungsten, aluminum or an alloy thereof, while layer **220** may contain a dielectric material (e.g., silicon-containing) or an additional conductive material. Preferably, conductive layer **212** contains copper and layer **220** is a dielectric layer. Preferably, the capping layer **230** is formed from a material that does not readily deform, form an alloy with the conductive layer **212**, or change state so that the physical properties or electrical properties of the material in the capping layer **230** remain unchanged after subsequent semiconductor processing steps have been performed on the substrate. In one aspect, the materials used to form the capping layer **230** and conductive layer **212** are selected so that they resist migration of the deposited material into the void **214** and the integrity of conductive layer **212** is preserved. Capping layer **230** is composed of a material that withstands being exposed to a temperature of about 500° C. or higher, preferably about 700° C. or higher.

[**0029**] In other embodiments, substrate **200** may contain additional layers of material depending on the overall architecture of the electronic device. For example, dielectric layer **204** may contain a barrier layer (not shown) thereon prior to the deposition of conductive layer **212** and/or conductive layer **212** may also contain a barrier layer (not shown) thereon prior to the deposition of layer **220**.

[**0030**] In one aspect, a CMP process may be performed on the substrate **200** to planarize the dielectric layer **204**, capping layer **230** and tungsten layer **206**. A planar surface may improve the device performance and reduce device to device variability due to the reduction in thickness variation of the conductive layer **212** near the capping layer **230**, if the conductive layer **212** and capping layer **230** are formed from different materials.

[**0031**] A capping layer **230** containing a cobalt-tungsten alloy or a nickel-containing material may be deposited by an electroless process that utilizes either a pre-mixed solution or an in-line mixing process that combines solution components to generate the electroless solution. In one example, an electroless solution used to deposit a cobalt-tungsten alloy may contain a cobalt source, a tungsten source, a citrate source, a hypophosphite source, a borane reductant and other additives. In another example, an electroless solution used to deposit a nickel-containing material may contain a nickel source, a citrate source, a borane reductant and other complexing agents and additives. Other electroless deposition solutions and processes useful for depositing cobalt-tungsten alloys are further described in the commonly assigned U.S. patent application Ser. No. 10/967,919, entitled, "Selective Self-initiating Electroless Capping of Copper with Cobalt-containing Alloys," filed on Oct. 18, 2004, which is incorporated by reference to the extent not inconsistent with the claimed aspects and description herein. Examples of cobalt-tungsten alloys that may electrolessly deposited include, but are not limited to cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), derivatives thereof, or combinations thereof. Examples of nickel alloys that may electrolessly deposited include, but are not limited to nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), nickel rhenium boride (NiReB), derivatives thereof, or combinations thereof. In one aspect, the capping layer **230** preferably has a resistivity below about 10 microohm-cm and thus will have a resistivity similar to the material deposited in the tungsten layer **206**. The resistance (R) of a circuit is equal to the resistivity (ρ) of the conductive material through which the current passes times the length (L) of the feature divided by the cross-sectional area (A) of the circuit through which the current passes (i.e., $R=\rho(L/A)$). Therefore, the addition of a capping layer **230** that is conductive, preferably metallic, will reduce the resistance of the circuit that utilizes the plug **203** (i.e., increase the effective cross-sectional area of the plug **203**).

Filling Process

[**0032**] In an alternative embodiment, to fill a gap formed within a tungsten-containing contact plug, the gap may be pretreated and filled with a material prior to depositing a conductive layer thereon (e.g., element **350** in **FIG. 3H**). The fill material inhibits void displacement that may otherwise occur by migration of material from a conductive layer deposited over the gap, as depicted in **FIG. 1F**. The gap(s) may be plugged by employing selective vapor deposition processes (e.g., CVD or ALD), liquid deposition processes (e.g., electroless- or electroplating) or spin coating processes. Materials useful to fill the gap(s) may include conductive materials, such as nickel, ruthenium, cobalt, tungsten and alloys thereof, as well as dielectric materials, such as spin-on-glass (SOG).

[**0033**] **FIG. 3A** illustrates a cross-sectional view of substrate **300** following a CMP process, as discussed above while forming a tungsten-containing contact plug depicted in **FIG. 1D**. Substrate **300** contains contact layer **302** (e.g., MOS device source or drain regions), dielectric layer **304** and plug **303** that includes tungsten layer **306** and gap **310**

formed therein. The gap **310**, which may be a seam, void or other defect, is created in tungsten layer **306** during the formation of the plug **303** (e.g., tungsten CVD process) and is generally exposed during the subsequent CMP process. During the CMP process or during a later exposure to oxidizing component(s), such as, components found in an ashing process, a wet clean process or ambient conditions, a tungsten oxide surface **312** will form on the tungsten layer **306**. Tungsten oxide surface **312** may be continuous or discontinuous across tungsten layer **306** and include a surface terminate with oxygen, hydrogen, hydroxides, metals and combinations thereof.

[**0034**] **FIGS. 3A-3D** illustrate cross-sectional views of an electronic device at different stages of an interconnect fabrication sequence incorporating one embodiment of the invention to pretreat and subsequently fill the gap **310** with a conductive material. **FIG. 3B** illustrates substrate **300** after performing a pretreatment process to remove the tungsten oxide surface **312** and expose the metallic tungsten-containing surface **314**. In one aspect of the embodiment, tungsten oxide surface **312** is chemically reduced to tungsten metal. For example, tungsten oxide surface **312** is exposed to a hydrogen plasma to remove the oxides and form a metallic tungsten-containing surface **314**. In another aspect, the tungsten oxide surface **312** is exposed to vapor deposition process containing diborane to remove the oxides and form metallic tungsten-containing surface **314** containing tungsten boride. In another aspect, the tungsten oxide surface **312** is exposed to wet clean process to further oxidize and remove tungstate ions while leaving behind a metallic tungsten-containing surface **314**. Additives, such as surface chelators, may be used within the wet clean solution that adhere to the freshly prepared metallic tungsten-containing surface **314** and inhibit oxidization.

[**0035**] A plasma pretreatment process is conducted for a predetermined time to reduce tungsten oxide surface **312** and form a metallic tungsten-containing surface **314**. A plasma pretreatment process may occur for about 5 minutes or less, preferably in a range from about 1 second to about 60 seconds, more preferably from about 5 seconds to about 30 seconds. During the pretreatment process, the substrate is maintained at a temperature in a range from about 20° C. to about 150° C., preferably from about 50° C. to about 100° C. The process chamber is maintained at a pressure in a range from about 0.1 Torr to about 750 Torr, preferably from about 1 Torr to about 100 Torr, and more preferably from about 10 Torr to about 30 Torr.

[**0036**] The plasma treatment process may be conducted in a process chamber capable of plasma vapor deposition techniques. For example, the substrate may be placed into a plasma enhanced ALD (PE-ALD), a plasma enhanced CVD (PE-CVD) or high density plasma CVD (HDP-CVD) chamber, such as the ULTIMA HDP-CVD™, available from Applied Materials Inc., located in Santa Clara, Calif. An inductively coupled plasma generating device, capacitively coupled plasma generating device, or combination thereof may be used in a plasma chamber to carryout the plasma treatment process. During processing the tungsten oxide surface **312** is exposed to a reducing plasma containing a reductant to form the metallic tungsten-containing surface **314**. The reductant may be diluted in a carrier gas and include hydrogen, diborane, silane, disilane, phosphine, derivatives thereof and combinations thereof. In one aspect, a carrier gas is delivered to the process chamber during the plasma pretreatment process. Carrier gases may be selected so as to also act as a purge gas for the removal of volatile reactants and/or by-products from the process chamber. Carrier gases or purge gases include helium, argon, hydrogen, forming gas and combinations thereof. The carrier gas may be provided at a flow rate in a range from about 100 sccm to about 5,000 sccm, preferably from about 500 sccm to about 2,500 sccm. The reductant may be provided at a flow rate in a range from about 5 sccm to about 500 sccm, preferably from about 10 sccm to about 100 sccm. The plasma may be formed using an RF power delivered to the plasma generating devices (e.g., showerhead in a capacitively coupled chamber or a substrate support) utilized in the plasma chamber where the RF power ranges from 100 W to 10,000 W at an RF frequency between about 0.4 kHz and about 10 GHz. In one aspect, the plasma is formed using a showerhead RF power setting and a substrate support RF power setting that is in a range from about 500 W to about 5,000 W at a frequency of about 13.56 MHz.

[**0037**] In an exemplary plasma pretreatment process, a substrate containing tungsten oxide is heated to about 50° C. and the process chamber is maintained at a pressure of about 10 Torr. A reducing plasma is exposed to the substrate containing hydrogen at a flow rate of about 1,000 sccm. The substrate is exposed to the reducing plasma for about 30 seconds to form a treated and reduced tungsten-containing layer.

[**0038**] In another exemplary plasma pretreatment process, a substrate containing tungsten oxide is heated to about 50° C. and the process chamber is maintained at a pressure of about 10 Torr. A reducing plasma is exposed to the substrate at a flow rate of about 500 sccm, whereas the reducing plasma contains diborane at a flow rate of about 50 sccm and a helium carrier gas at the flow rate of about 450 sccm. The substrate is exposed to the reducing plasma for about 30 seconds to form a treated and reduced tungsten-containing layer.

[**0039**] In another embodiment, the tungsten oxide surface **312** is exposed to a reducing vapor to form metallic tungsten-containing surface **314** to perform a vapor deposition process type pretreatment process. The reductant may include borane, diborane, borane-alkylsulfides, such as borane-dimethylsulfide ($BH_3.(CH_3)_2S$), alkyboranes (e.g., ethylborane), phosphine, alkylposphines (e.g., dimethylphosphine), silane, disilane, trisilane, alkylsilanes (e.g., methylsilane), ammonia, hydrazine, hydrogen, derivatives thereof or combinations thereof. Preferably, the reductant is diborane, phosphine, silane, hydrazine, hydrogen or combinations thereof. In one aspect of the pretreatment process, the tungsten oxide surface **312** is exposed to a reducing vapor process for a predetermined time to form metallic tungsten-containing surface **314**. The reducing vapor process may occur for about 5 minutes or less, preferably in a range from about 1 second to about 120 seconds, more preferably from about 5 seconds to about 90 seconds. During the reducing vapor process, the substrate is maintained at a temperature in a range from about 20° C. to about 150° C., preferably from about 50° C. to about 100° C. The process chamber is maintained at a pressure in a range from about 0.1 Torr to about 750 Torr, preferably from about 1 Torr to about 100 Torr, and more preferably from about 10 Torr to about 30 Torr. In one aspect, a reductant may be exposed to

tungsten oxide surface **312** directly or diluted in a carrier gas. During the reducing vapor process, a carrier gas flow is established within the process chamber and exposed to the substrate. Carrier gases may be selected so as to also act as a purge gas for the removal of volatile reactants and/or by-products from the process chamber. Carrier gases or purge gases include helium, argon, nitrogen, hydrogen, forming gas and combinations thereof. The carrier gas may be provided at a flow rate in a range from about 100 sccm to about 5,000 sccm, preferably from about 500 sccm to about 2,500 sccm. The reductant may be provided at a flow rate in a range from about 5 sccm to about 500 sccm, preferably from about 10 sccm to about 100 sccm.

[**0040**] The reducing vapor process may be conducted in a process chamber capable of vapor deposition, such as an ALD process chamber or a CVD process chamber. A process chamber useful for ALD during the reducing vapor process is described in commonly assigned U.S. Pat. Nos. 6,916,398 and 6,878,206, which are both incorporated herein by reference.

[**0041**] In another embodiment of the pretreatment process, the tungsten oxide surface **312** is exposed to wet clean process to further oxidize and remove tungstate ion while leaving behind a metallic tungsten-containing surface **314**. During a typical wet clean process a wet clean solution is dispensed across or sprayed on the surface of substrate **300**. The wet clean process may be an in situ process performed in the same processing cell as a subsequent electroless deposition process. Alternatively, substrate **300** may be wet cleaned in a separate processing cell from the subsequent electroless deposition processing cell. The wet clean process usually includes an acidic wet clean solution with a pH of about 4 or less, preferably, in a range from about 1.5 to about 3. The tungsten oxide surface **312** typically requires an aggressive cleaning at low pH values. The pH of the wet clean solution is usually adjusted by adding an acid or a base to the predetermined value. The acid may include hydrochloric acid (HCl), hydrogen fluoride (HF), sulfuric acid (H_2SO_4), nitric acid (HNO_3), phosphoric acid (HPO_4), derivatives thereof and combinations thereof. The base may include a hydroxide salt, ammonia or an amine, such as diethanolamine (DEA), triethanolamine (TEA), derivatives thereof, salts thereof and combinations thereof. The wet clean solution also contains at least one chelator or complexing agent, such as a carboxylic acid or carboxylate, for example, a citrate, oxalic acid, glycine, salts thereof and combinations thereof. In one example, the wet clean solution contains about 0.05 M to about 0.5 M of citric acid and optionally up to about 0.25 M of methanesulfonic acid.

[**0042**] In one embodiment, the pretreatment process is used to etch and remove a portion of the tungsten oxide surface **312** to increase the size of the gap **310** in an effort to improve the ability of the subsequent deposition process steps (discussed below) to access and fill the gap **310**. In one aspect, the process of increasing the gap **310** is performed using a wet clean process for a desired period of time.

[**0043**] Once tungsten oxide surface **312** is removed or reduced to reveal metallic tungsten-containing surface **314** by the processes described herein, a fill material **320** may be deposited thereon to fill the gap **310**, as illustrated in **FIG. 3C**. The fill material **320** may be composed of a conductive material or a dielectric material. Preferably, fill material **320** contains a metal deposited by a liquid deposition process or a vapor deposition process. In one example, fill material **320** is a nickel-containing layer deposited by an electroless deposition solution. In another example, fill material **320** is a cobalt-containing layer (e.g., CoW-alloy) deposited by an electroless deposition solution. In another example, fill material **320** is a nickel-containing layer deposited by a CVD process. Preferably, the capping layer **320** is formed from a material that does not readily deform, form an alloy with the conductive layer **350**, or change state so that the physical properties or electrical properties of the material in the capping layer **320** remain unchanged after subsequent semiconductor processing steps have been performed on the substrate. It is generally desirable to fill the gap **310** so that no gaps or voids are formed in the plug **303** or plug **321**, and thus integrity of conductive layer **350** is preserved during subsequent semiconductor processing steps. In one aspect, the material used to form the fill material **320** is selected so that it can withstands exposure to temperature of about 500° C. or higher, preferably about 700° C. or higher.

[**0044**] **FIG. 3D** depicts substrate **300** after several fabrication processes have been performed on its surface to form the subsequent metal interconnect layer (e.g., M1 layer). As shown in **FIG. 3D**, a dielectric layer **324** was deposited on the surface of substrate **300** and etched to reveal fill material **320** and an upper surface tungsten layer **306**. Then a barrier layer **323** was deposited on dielectric layer **324** and seed/adhesion layer **325** is deposited on barrier layer **323**, each by a vapor deposition process, such as a PVD process or an ALD process. The barrier layer **323** typically will contain metals, such as titanium, titanium nitride, titanium silicon nitride, tantalum, tantalum nitride, tantalum silicon nitride, alloys thereof, derivatives thereof or combinations thereof. The seed/adhesion layer **325** typically will contain metals, such as tungsten, copper, ruthenium, titanium, tantalum, alloys thereof or combinations thereof. In one aspect, as shown in **FIG. 3D**, the barrier layer **323** and seed/adhesion layer **325** were removed from the surface of the fill material **320** and an upper surface tungsten layer **306** by use of a re-sputtering process that is typically performed in the PVD or PECVD processing chambers. The removal of the barrier layer **323** and seed/adhesion layer **325** will help reduce the resistance of the circuit formed in the shown device, since the barrier layer **323** and seed/adhesion layer **325** are usually contain materials that have a resistivity higher than typical interconnect metals (e.g., conductive layer **350**), such as copper.

[**0045**] Next a conductive layer **350** is deposited onto substrate **300** to form a plug **321** (or via) that is in electrical contact with plug **303**. Conductive layer **350** may contain copper, tungsten, aluminum or an alloy thereof. Preferably, conductive layer **350** contains copper or a copper alloy. Conductive layer **350** may be deposited by a vapor deposition process (e.g., CVD or PVD) or a liquid deposition process (e.g., electroless or electroplating).

[**0046**] In one aspect, a CMP process may be performed on the substrate **300** to planarize the dielectric layer **304**, capping layer **330** and tungsten layer **306**. A planar surface may improve the device performance and reduce device to device variability.

[**0047**] In one aspect, a fill material **320** containing a cobalt-tungsten alloy or nickel alloy may be deposited by an

electroless process that exposes the substrate to an electroless solution within a process chamber. An example of an electroless solution for depositing a cobalt-tungsten alloy may contain a cobalt source, a tungsten source, a citrate source, a hypophosphite source, a borane reductant and other additives. Examples of cobalt-tungsten alloys that may electrolessly deposited include, but are not limited to cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), derivatives thereof, or combinations thereof. Examples of nickel alloys that may electrolessly deposited include, but are not limited to nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), nickel rhenium boride (NiReB), derivatives thereof, or combinations thereof. Other electroless deposition solutions for cobalt-tungsten alloys are further described in the commonly assigned U.S. patent application Ser. No. 10/967,919, entitled, "Selective Self-initiating Electroless Capping of Copper with Cobalt-containing Alloys," filed on Oct. 18, 2004, which is incorporated by reference to the extent not inconsistent with the claimed aspects and description herein. In another example, an electroless solution to deposit a nickel-containing material may contain a nickel source, a citrate source, a borane reductant and other complexing agents and additives. An exemplary electroless deposition process cell that may be one or more of the electroless deposition processes described herein is further described in the commonly assigned and copending U.S. patent application Ser. No. 10/996,342, filed Nov. 22, 2004 and U.S. patent application Ser. No. 11/175,251, filed Jul. 6, 2005, which are both incorporated by reference in their entirety.

[0048] In one aspect, the fill material **320** preferably has a resistivity below about 10 microohm-cm and thus will have a resistivity similar to the material deposited in the tungsten layer **306**. The resistance (R) of a circuit is equal to the resistivity (p) of the conductive material through which the current passes times the length (L) of the feature divided by the cross-sectional area (A) of the circuit through which the current passes (i.e., $R=\rho(L/A)$). Therefore, the addition of a fill material **320** that is conductive, preferably metallic, will reduce the resistance of the circuit that utilizes the plug **303** (i.e., increase the effective cross-sectional area of the plug **303**) and thus improve the device performance and reliability (e.g., reduces resistive heating effects).

Ruthenium Containing Layer Deposition Process Sequence

[0049] In an alternative embodiment, **FIGS. 3A**, and **3**E-**3**H illustrate cross-sectional views of an electronic device at different stages of an interconnect fabrication sequence that are used to pretreat and subsequently fill gap **310** with a fill material **320**. **FIG. 3E** illustrates substrate **300** after a pretreatment process has been performed on the substrate **300** shown in **FIG. 3A**. In one aspect of the pretreatment process, a ruthenium oxide layer **316** is deposited on the tungsten oxide surface **312** using a ruthenium tetroxide (RuO_4) containing gas. Thereafter, ruthenium oxide layer **316** may be chemically reduced to form ruthenium-containing layer **318** on tungsten oxide surface **312**, as illustrated in **FIG. 3F**.

[0050] Ruthenium tetroxide may be delivered to the substrate in a vapor deposition process, such as an ozone generation process, or in a liquid deposition process, such as an aqueous solution or suspension. Preferably, ruthenium tetroxide is generated by exposing a ruthenium-containing source to an oxidizing gas. Ruthenium tetroxide is a strong oxidant and therefore readily reacts with any exposed tungsten and/or tungsten oxide layers to form a consistent and catalytic active layer of ruthenium oxide or metallic ruthenium. An example of an exemplary process used to form ruthenium tetraoxide and deposit a ruthenium containing layer on the surface of the substrate is further described in the commonly assigned U.S. patent application Ser. No. 11/228,425, filed Sep. 15, 2005, which is incorporated by reference in its entirety. In one example, ruthenium tetroxide is formed by flowing an ozone containing gas, preferably >12 vol % ozone, across a metallic ruthenium source material (e.g., powdered ruthenium metal). The formed ruthenium tetraoxide is then delivered and separated from the other components in the ruthenium tetraoxide containing gas by use of a cold trap. Thereafter, the cold trap is purged of the unwanted gases and then warmed to a temperature to sublime the ruthenium tetroxide while a flow of inert gas is passed therethrough. The vaporized ruthenium tetroxide saturates the inert gas to form a ruthenium tetraoxide deposition gas. In an exemplary vapor deposition process, a deposition gas containing ruthenium tetroxide is delivered to a substrate having a tungsten oxide layer formed thereon. During the process, the substrate is maintained at a temperature between of about 100° C. and about 450° C., and more preferably a temperature between about 200° C. and about 400° C. A ruthenium containing layer can be selectively or non-selectively deposited on certain preferred materials by adjusting the temperature of the substrate during processing (e.g., <180° C. (selective); >200 (non-selective)). After exposing the tungsten oxide layer to the ruthenium tetroxide containing gas for about 30 seconds, a ruthenium oxide layer is formed on the tungsten oxide layer.

[0051] In **FIG. 3F**, the ruthenium oxide layer **316** is exposed to a reductant forming ruthenium-containing layer **318**. In this step the ruthenium oxide is chemically reduced to ruthenium metal. For example, ruthenium oxide layer **316** is exposed to a hydrogen plasma to remove the oxygen and form metallic ruthenium-containing layer **318**. In another example, ruthenium oxide layer **316** is exposed to a vapor deposition process containing diborane to remove oxygen and form ruthenium-containing layer **318** containing ruthenium boride. In another example, ruthenium oxide layer **316** is exposed to phosphine through a vapor deposition process to remove oxygen and form ruthenium-containing layer **318** containing ruthenium phosphide.

[0052] Next the fill material **320** is deposited on the ruthenium-containing layer **318** to fill gap **310** as illustrated in **FIG. 3G**. The deposition processes and the compositions of fill material **320** are described above in conjunction with **FIG. 3C**. Also, **FIG. 3H** depicts substrate **300** after several subsequent fabrication processes have been formed on the substrate, which is similarly described above in conjunction with **FIG. 3D**.

Dielectric Gap Fill Process

[0053] In an alternative embodiment, the gap **310** is filled with a dielectric material as illustrated by cross-sectional

views shown in FIGS. 3A, 3I-3K. **FIG. 3A** depicts substrate **300** with plug **303** that contains tungsten material **306**, tungsten oxide surface **312** and gap **310** therein. Optionally, a pretreatment process to remove tungsten oxide surface **312** and reveal the surface of tungsten material **306**, as described in conjunction with **FIG. 3B**, may be performed before depositing a dielectric fill material **330** into the gap **310**. Preferably, a pretreatment process is not conducted and dielectric fill material **330** is deposited on substrate **300** to fill gap **310**, as depicted in **FIG. 3I**. Dielectric material **330** may be deposited on substrate **300** by a spin-coating process or by a vapor deposition process.

[**0054**] In one example, dielectric fill material **330** is spin-on-glass (SOG) deposited by a spin-coating process. Dielectric fill material **330** containing SOG is formed by a polymerization reaction of precursor compounds that are dissolved in an organic solution. The isolated dielectric compound is useful to fill gap **310**. Preferably, dielectric fill material **330** is a silicate or a polysiloxane and may contain a metal such as titanium, zirconium hafnium and/or vanadium. Therefore, the composition of a SOG used as dielectric fill material **330** may include silicon, carbon, oxygen, titanium, zirconium, hafnium, vanadium or combinations thereof. Substrate **300** is generally exposed to a thermal annealing, or curing, process following the SOG deposition process. Additional compositions of SOG and processes to deposit SOG into vias or trenches is described in J. W. Lutze et al., "Spin-on-glass for 200 nm trench isolation structures, "*J. Micromech. Microeng*, vol. 1, pp. 46-51 (1991), which is herein incorporated by reference.

[**0055**] In another example, dielectric fill material **330** is a silicon-containing material or a metal-containing material deposited by an ALD process or a CVD process. Examples of dielectric fill material **330** deposited by vapor deposition processes include silicon oxide, silicon oxynitride, aluminum oxide, tantalum oxide, hafnium oxide, hafnium silicate, zirconium oxide, zirconium silicate, titanium oxide, titanium silicate, derivates thereof and combinations thereof. Additional compositions of dielectric fill material **330** and vapor deposition processes to deposit dielectric fill material **330** is described the commonly assigned U.S. patent application Ser. No. 10/406,833, entitled, "Method for Hafnium Silicon Oxynitride Deposition," filed Apr. 4, 2003, and published as U.S. Publication No. 20030235961 and U.S. patent application Ser. No. 11/127,767, entitled, "Apparatuses and Methods for Atomic Layer Deposition of Hafnium-Containing High-K Materials," filed May 12, 2005, which are both herein incorporated by reference.

[**0056**] A planarization process, such as a chemical mechanical polishing (CMP) process or etching process may be performed to remove an excess dielectric fill material **330** deposited on the surface of substrate **300** (i.e., field region **307**) and expose the upper surface tungsten layer **306**, as depicted in **FIG. 3J**. Therefore, gap **310** remains filled with dielectric fill material **330** while substantially flush with the surface substrate **300**.

[**0057**] **FIG. 3K** depicts substrate **300** after several fabrication processes. Dielectric layer **324** is deposited on the surface of substrate **300** and etched to reveal fill dielectric fill material **330** and an upper surface tungsten layer **306**. Barrier layer **323** is deposited on dielectric layer **324** and seed/adhesion layer **325** is deposited on barrier layer **323**, each by a vapor deposition process, such as a PVD process or an ALD process. In one aspect, as shown in **FIG. 3K**, the barrier layer **323** and seed/adhesion layer **325** were removed from the surface of the dielectric layer **324** and an upper surface tungsten layer **306** by use of a re-sputtering process that is typically performed in the PVD or PECVD processing chambers. Conductive layer **350** is deposited onto substrate **300** forming plug **321** in contact with plug **303**.

[**0058**] Preferably, the dielectric fill material **330** is formed from a material that does not readily deform, form an alloy with the conductive layer **350**, or change state so that the physical properties or electrical properties of the material in the dielectric fill material **330** remain unchanged after subsequent semiconductor processing steps have been performed on the substrate. It is generally desirable to fill the gap **310** so that no gaps or voids are formed in the plug **303** or plug **321**, and thus integrity of conductive layer **350** is preserved during subsequent semiconductor processing steps. In one aspect, the material used to form the dielectric fill material **330** is selected so that it can withstands exposure to temperature of about 500° C. or higher, preferably about 700° C. or higher, and more preferably about 1,000° C. or higher.

[**0059**] The process steps illustrated in **FIGS. 3A-3K** are not intended to be limiting as to the scope of the invention, since substrate **300** may contain one or more additional or intermediate layers of material without varying from the basic scope of the invention described herein. For example, the sidewalls of the gap **310** formed in the dielectric layer **304** may be covered by a barrier layer or an adhesion layer (not shown) prior to the deposition of tungsten layer **306**.

Interconnect Formation Process

[**0060**] In another embodiment, a process is used to initiate on a tungsten containing contact plug to form an interconnect feature (see item #**321** in **FIGS. 3H and 3K** and item #**443** in **FIG. 4F**). As shown in **FIGS. 4A-4F**, an interconnect plug **443** is formed over the plug **403** so that an electrical connection can be made between the contact layer **402**, the interconnect plug **443** and any subsequently deposited layers, such as the M2 and above interconnects (not shown). In this case, any gaps formed within a tungsten-containing contact plug is postponed until the subsequent metal layer(s) are formed over the plug **403** (see **FIG. 4A**). While **FIGS. 4A-4F** illustrates a tungsten-containing contact plug that has a gap **410** formed therein, this configuration is not intended to be limiting as to the scope of the invention since the methods described herein may be useful to create an interconnect feature over a tungsten-containing contact plug that does not contain this type of defect. In general this process requires the deposition of dielectric layer over the plug **403** formed on the substrate **400**. Then various conventional lithographic patterning and etching techniques are used to form an aperture **405** (or via) so that an interconnect layer can be deposited on the plug **403**. In one aspect, various materials may be used to fill the gap **410** and aperture **405**, which may include conductive materials, such as copper, nickel, ruthenium, cobalt, tungsten and alloys thereof.

[**0061**] **FIG. 4A** illustrates a cross-sectional view of substrate **400** following a CMP process, as discussed above during processes forming a tungsten-containing contact plug depicted in **FIG. 1D**. Substrate **400** contains contact layer

402, dielectric layer **404** and plug **403** that includes tungsten layer **406** formed in the gap **410**. The gap **410**, which may be a seam, void or other defect, is created in tungsten layer **406** during the formation of the plug **403** (e.g., tungsten CVD process) and is then exposed during the subsequent CMP process. The surface of the tungsten layer **406** may contain a tungsten oxide layer **412** that is formed by atmospheric oxidation or exposure to an oxidizer, such as during an ashing process. The tungsten oxide layer **412** may be continuous or discontinuous across tungsten layer **406** and include a surface terminated with oxygen, hydrogen, hydroxides and combinations thereof. Optionally, the tungsten oxide layer **412** may be removed by a reduction process or a pre-clean process as described above to form a metallic tungsten-containing surface (not shown), substantially free of tungsten oxide layer **412**.

[**0062**] **FIG. 4B** illustrates substrate **400** after a dielectric layer **420** has been formed on the dielectric layer **404** and plug **403**. Generally, a void **411** will be formed as the deposited dielectric layer **420** seals off the gap **410** formed in the plug **403**. In some cases the dielectric layer **420** may coat the inside surface of void **411** forming dielectric surface **418**. In other cases the gap **410** may be completely filled by dielectric material **420** and thus void **411** does not exist (not shown).

[**0063**] The dielectric layer **420** and the dielectric surface **418** are composed of a dielectric material that may include silicon dioxide, silicon nitride, SOI, silicon oxynitride and/or carbon-doped silicon oxides, such as SiO_xC_y, for example, BLACK DIAMOND™ low-k dielectric, available from Applied Materials, Inc., located in Santa Clara, Calif. The dielectric material forming dielectric layer **420** and dielectric surface **418** may be deposited by a vapor deposition process such as CVD or plasma-enhanced-CVD (PE-CVD). In one example, a TEOS CVD process, utilizing the precursor tetraethyl orthosilicate ($Si(OC_2H_5)_4$ or TEOS), is conducted to deposit a silicon oxide material at about 700° C. In another example, a TEOS PE-CVD process is conducted to deposit a silicon oxide material at about 500° C.

[**0064**] **FIG. 4C** illustrates substrate **400** after the dielectric layer **420** has been masked and etched, using conventional techniques, to form a via or aperture **405** to reveal plug **403** and gap **410**. In one aspect, the gap **410** may contain a dielectric coating, or dielectric surface **418**, as shown. Alternatively, dielectric surface **418** may be removed during the etching process to remove dielectric layer **420** (not shown). In this case a wet or dry etching process(es) may be performed to remove the dielectric surface **418** material from the surface of the gap **410**.

[**0065**] In one embodiment, not shown in **FIGS. 4A-4F**, a pretreatment process is performed to remove the tungsten oxide surface **412** after the dielectric surface **418** has been removed, but prior to depositing the barrier layer **430**. In this case the tungsten oxide surface **412** is removed to expose a metallic tungsten-containing surface (e.g., similar to the item **314** in **FIG. 3B**). In one aspect, tungsten oxide surface **412** is chemically reduced to tungsten metal. For example, tungsten oxide surface **412** is exposed to a hydrogen plasma to remove the oxides and form a metallic tungsten-containing surface. In another aspect, the tungsten oxide surface **412** is exposed to vapor deposition process containing diborane to remove the oxides and form metallic tungsten-containing surface containing tungsten boride. In another aspect, the tungsten oxide surface **412** is exposed to wet clean process to further oxidize and remove tungstate ions while leaving behind a metallic tungsten-containing surface. Processes that may be used to perform the pretreatment process are discussed above in conjunction with **FIGS. 3A-3C**.

[**0066**] Thereafter, as illustrated in **FIG. 4D**, barrier layer **430** is deposited on substrate **400**, including on dielectric layer **420**, aperture **405** and the gap **410**. Barrier layer **430** may contain a material that acts as an adhesion and/or diffusion barrier layer for the subsequently deposited materials deposited thereon, such as copper. Materials to form barrier layer **430** may include tantalum, tantalum nitride, tantalum silicon nitride, titanium, titanium nitride, titanium silicon nitride, ruthenium, alloys thereof, derivatives thereof or combinations thereof. Barrier layer **430** may be deposited by vapor deposition process that includes PVD, ALD or CVD. Preferably, barrier layer **430** is a tantalum-containing compound deposited by a PVD process. In one aspect, not shown, the barrier layer **430** may be removed from the surface of the plug **403** by use of a re-sputtering process that is typically performed in the PVD or PECVD processing chambers.

[**0067**] **FIG. 4E** illustrates the substrate **400** after an optional seed layer **440** has been deposited on barrier layer **430** and into gap **410**. The optional seed layer **440** may increase adhesion or promote nucleation sites for subsequently deposited bulk-fill materials. The seed layer **440** may be a continuous layer or a non-continuous layer across the surface of barrier layer **430**. Therefore, barrier layer **430** may be exposed if seed layer **440** is a non-continuous layer. Seed layer **440** may contain a metal, such as, copper, tungsten, tantalum, titanium, ruthenium, alloys thereof, derivatives thereof or combinations thereof. Seed layer **440** may be deposited by a vapor deposition process that includes PVD, ALD and CVD or a liquid deposition process that includes electroless or electroplating. Preferably, seed layer **440** is a copper-containing compound deposited by a PVD process.

[**0068**] **FIG. 4F** illustrates substrate **400** after a bulk fill layer **450** has been deposited on seed layer **440**, thus filling gap **410** and aperture **405**. The deposition of bulk fill layer **450** completes the formation of interconnect plug **443** that is in electrical contact to plug **403**. Bulk fill layer **450** may contain a conductive metal that includes copper (Cu), tungsten (W), aluminum (Al), ruthenium (Ru), nickel (Ni), cobalt (Co), alloys thereof, derivatives thereof or combinations thereof. Bulk fill layer **450** may be deposited by a vapor deposition process that includes PVD and CVD or a liquid deposition process that includes electroless or electroplating. In one example, bulk fill layer **450** is a copper-containing compound deposited by a PVD process. In another example, bulk fill layer **450** is a tungsten-containing compound deposited by a CVD process. In another example, bulk fill layer **450** is a nickel-containing compound deposited by an electroless deposition process. In another example, bulk fill layer **450** is a cobalt-tungsten alloy deposited by an electroless deposition process. In another example, bulk fill layer **450** is a copper-containing compound deposited by an electroless deposition process. In another example, bulk fill layer **450** is a copper-containing compound deposited by an electroplating process. An exemplary electroplating deposition process

and apparatus that may be in one or more of the electroplating deposition processes described herein is further described in the commonly assigned and copending U.S. patent application Ser. No. 10/268,284 [APPM 7669], filed Oct. 9, 2002 and U.S. patent application Ser. No. 110/616, 284 [APPM 7669P1], filed Jul. 8, 2003, which are both incorporated by reference in their entirety.

Alternate Interconnect Formation Process

[0069] In another embodiment, a process is used to initiate on a tungsten containing contact plug to form an interconnect feature **505**. **FIGS. 5A-5G** illustrate the process of forming an interconnect plug **543** (See **FIGS. 5D and 5G**) over the plug **503** so that an electrical connection can be made between the contact layer **502**, the interconnect plug **543** and any subsequently deposited layers, such as the M2 interconnect layers (not shown). In general this process starts by depositing a dielectric layer over the plug **503** that was previously formed on the substrate **500**. Then various conventional lithographic patterning and etching techniques are used to form an aperture **505** (or via) so that an interconnect layer (i.e., bulk fill layer **550**) can be deposited on the plug **503**.

[0070] **FIG. 5A** illustrates a cross-sectional view of substrate **500** after a CMP process has been performed on a tungsten-containing contact plug. Substrate **500** contains contact layer **502**, dielectric layer **504** and plug **503** that includes tungsten layer **506**. The surface **512** of the tungsten layer **506** may contain a tungsten oxide layer that is formed by atmospheric oxidation or exposure to an oxidizer, such as during an ashing process. The tungsten oxide layer may be continuous or discontinuous across tungsten layer **506** and include a surface terminated with oxygen, hydrogen, hydroxides and combinations thereof. Optionally, the tungsten oxide layer may be removed by a reduction process or a pre-clean process as described above to form a metallic tungsten-containing surface (not shown), substantially free of tungsten oxide layer.

[0071] **FIG. 5B** illustrates substrate **500** after a dielectric layer **520** has been formed on the dielectric layer **504** and plug **503**. The dielectric layer **520** may be composed of a dielectric material that may include silicon dioxide, silicon nitride, SOI, silicon oxynitride and/or carbon-doped silicon oxides, such as SiO_xC_y, for example, BLACK DIAMOND™ low-k dielectric, available from Applied Materials, Inc., located in Santa Clara, Calif. The dielectric material forming dielectric layer **520** may be deposited by a vapor deposition process such as CVD or plasma-enhanced-CVD (PE-CVD). In one example, a TEOS CVD process, utilizing the precursor tetraethyl orthosilicate ($Si(OC_2H_5)_4$ or TEOS), is conducted to deposit a silicon oxide material at about 700° C. In another example, a TEOS PE-CVD process is conducted to deposit a silicon oxide material at about 500° C.

[0072] **FIG. 5C** illustrates substrate **500** after the dielectric layer **520** has been masked and etched, using conventional techniques, to form a via or aperture **505** to reveal plug **503**. In general, it is desirable to assure that all of the dielectric layer **520** is removed from the exposed regions of the surface **512** of the plug **503**.

[0073] In one embodiment, not shown in **FIGS. 5A-5F**, a pretreatment process is performed to remove the tungsten oxide layer on the surface **512** after the dielectric material has been removed, but prior to depositing the barrier layer **530** or bulk fill layer **550**. In this case the tungsten oxide on the surface **512** is removed to expose a metallic tungsten-containing surface (e.g., similar to the item **314** in **FIG. 3B**). In one aspect, tungsten oxide is chemically reduced to tungsten metal. For example, tungsten oxide is exposed to a hydrogen plasma to remove the oxides and form a metallic tungsten-containing surface. In another aspect, the tungsten oxide is exposed to vapor deposition process containing diborane to remove the oxides and form metallic tungsten-containing surface containing tungsten boride. In another aspect, the tungsten oxide is exposed to wet clean process to further oxidize and remove tungstate ions while leaving behind a metallic tungsten-containing surface. Processes that may be used to perform the pretreatment process are discussed above in conjunction with **FIGS. 3A-3C**.

Pretreatment Process Example

[0074] In one embodiment of the pretreatment process, various processing steps **3000** (see **FIG. 6**) are used to prepare the surface of the substrate prior to depositing the bulk fill layer **550**. In one embodiment, the processing steps **3000** generally includes 1) an oxide removal step, 2) a surface preparation step, 3) an activation step, 4) an optional activation rinse step, and 5) an optional chelating rinse step. Each of the steps will be discussed in turn.

[0075] In the first step of the pretreatment process, or step **3002**, the surface **512** is exposed to a clean solution to remove leftover etch residues from the formation of the interconnect feature **505** and/or any left over dielectric material (Item #**520FIG. 5B**). In one aspect, the clean solution may be useful to remove some of the tungsten oxides formed on the surface **512**, but cleaning solutions that are too aggressive will aggressively attack commonly used dielectric layer **520** materials. The preparation of the surface **512** typically requires a clean solution that has a low pH. The pH of the clean solution is usually adjusted by adding an acid or a base (e.g., DEA, TEA) to the predetermined value. The clean process usually includes an acidic clean solution with a pH of about 4 or less, preferably, in a range from about 1.5 to about 3. The acid may include hydrochloric acid (HCl), hydrogen fluoride (HF), sulfuric acid (H_2SO_4), nitric acid (HNO_3), phosphoric acid (HPO_4), derivatives thereof and combinations thereof. In one aspect, the clean solution contains between about 0.1 wt % and about 5 wt % of hydrofluoric acid (HF). Preferably, the clean solution contains about 0.5 wt % of hydrofluoric acid (HF). During a typical clean process a clean solution is dispensed across or sprayed on the surface of substrate **500** at a temperature at or near room temperature. The time the clean solution is in contact with the surface of the substrate to achieve a desired result may depend on the prior processing steps the substrate has gone through and the concentration of the clean solution components. For example, an aqueous solution that contains about 0.5 wt % of hydrofluoric acid (HF) may only require about a 30 second exposure to the substrate surface.

[0076] In the second step of the pretreatment process, or step **3003**, the surface **512** is exposed to surface preparation step that is adapted to further normalize the surface **512** prior to performing the subsequent deposition steps. It is believed that exposure of the surface **512** to a tungstate source will tend to normalize the activity of all the exposed regions across the substrate surface so that they all behave similarly

in the subsequent processing steps. In this step a preparation solution containing tungstic acid (H_2WO_4) and/or various tungstate salts, or other water soluble WO_4^{2-} sources, hydrates thereof, derivatives thereof or combinations thereof are dispensed on the substrate surface to promote the bonding of the subsequent layers to the substrate surface. In one aspect, the preparation solution contains tungstic acid in a concentration between about 0.002 M and about 0.1 M, and has an adjusted pH of between about 12 and about 13 by the addition of a base (e.g., TMAH). Preferably, the tungstic acid concentration in the preparation solution is between about 0.06 and about 0.1 M and the pH is about 12.5. In one aspect, the preparation solution is dispensed on the surface of the substrate at a temperature at or near room temperature (e.g., ~20° C.). The time the preparation solution is in contact with the surface of the substrate to achieve a desired result may depend on the prior processing steps the substrate has gone through and the concentration of the processing solution components. For example, an aqueous solution that contains about 10 g/l of tungstic acid and has adjusted pH of about 12.5 may only require between about a 30 second and about a 45 second exposure to the substrate surface.

[**0077**] In the third step of the pretreatment process, or step **3004**, prior to the deposition of the bulk fill layer **550** the surface **512** is activated using an activation solution. During this step, an initiation layer (not shown) may be formed on the surface **512** by displacement plating of a catalytic metal such a palladium, platinum, ruthenium, osmium, rhodium or iridium. Typical procedures for cleaning and displacement plating of tungsten with palladium employ dilute aqueous acid solutions of palladium salts such as palladium chloride, palladium nitrate or palladium sulfate. An example of a suitable acidic activation solution is one prepared by addition of about 4 ml of a 10 wt % $Pd(NO_3)_2$ in 10% nitric acid to 1 liter of deionized water. In another example, an activation solution contains about 120 ppm palladium chloride and sufficient hydrochloric acid to provide a pH in a range from about 1.5 to about 3. Substrates to be activated are exposed to the activation solution for about 30 seconds at room or ambient temperature.

[**0078**] Next an optional rinse process (step **3005**) is used to activate the initiation layer, clean the substrate surface and/or remove remaining contaminants from any of the early processes. In this step a rinse activation solution is dispensed on the substrate surface to activate the initiation layer formed in the third step. In one aspect, the rinse activation solution is a reducing solution (e.g., DMAB, glyoxylic acid) that is delivered to the substrate surface for wetting, cleaning and thermally equilibrating the substrate surface. In one aspect, one liter of a rinse activation solution containing about 1.2 g DMAB and about 3.3 g of 50% H_3PO_2 to DI water at ambient temperature, and enough 25% TMAH to adjust the pH to about 9.25, is dispensed on the substrate surface. In another aspect, a rinse activation solution may contain about 1.2 g/L DMAB, 7.2 g/L of citric acid, 0.1 g/L of hydroxypyridine (a stabilizer), and about 3.3 g/L of 50% H_3PO_2, DI water, and then adding 25% TMAH to adjust the pH to about 9.25. In one aspect, the rinse activation solution contains DMAB in a concentration from about 1 mM to about 200 mM, and preferably, about 20 mM. In one example, the rinse process may be for about 30 seconds.

[**0079**] Next an optional chelating process (step **3006**) that uses a chelating solution is dispensed on the substrate surface to clean the substrate surface and/or remove remaining contaminants from any of the early processes. The chelating solution is used to remove and prevent particles from forming on the activated surface. In one aspect, a room temperature chelating solution containing about 0.1 M of citric acid is dispensed on and/or remains in contact with the substrate surface for about 30 seconds.

[**0080**] One will note that a rinse process will general follow each process steps described above, to reduce the interaction of the various chemicals. The rinse process includes rinsing the substrate surface with deionized water at or near room temperature. The substrate will be rinsed for a period from about 1 second to about 30 seconds, preferably from about 5 seconds to about 10 seconds.

[**0081**] Referring to **FIG. 5D**, a bulk fill layer **550** is then deposited on the surface **512** of the plug **503** to fill the aperture **505**. In this configuration the bulk fill layer **550** may be selectively deposited so that the plug **543** is filled from the bottom up, thus preventing defects from being formed in the plug **543** from the growth of the film on the side walls of the aperture **505** (e.g., typically described as "pinch off"). In one aspect, the bulk fill layer **550** may be selectively deposited on the surface **512** by use of a vapor deposition process that includes ALD or CVD. Preferably, the bulk fill layer **550** is selectively deposited using an electroless deposition process. In one aspect, electrolessly deposited films are preferred, since they will not contain the amount of carbon that CVD and ALD deposited films contain due to the incorporation of the CVD or ALD precursor materials in the deposited film. The incorporation of carbon in the deposited film will affect the resistivity and adhesion of the deposited layer to prior or subsequently deposited layers. Electrolessly deposited films are also favored over PVD deposited films, since PVD deposited films will tend to "pinch off" at the top of the aperture **505**, since PVD it is a line-of-sight type deposition process. Electroless deposition processes are also useful to form metal layers that have two or more metal components contained therein. In one aspect, it may be desirable to varying composition of the electrolessly deposited layer that contains two or more metal components. An exemplary process and hardware that may be used to form a metal layer having a varying composition is described in the commonly assigned U.S. patent application Ser. No. 11/040,962 [APPM 8926], filed Jan. 22, 2005, which is incorporated by reference herein in its entirety. The bulk fill layer **550** may contain a conductive metal that includes copper (Cu), tungsten (W), aluminum (Al), ruthenium (Ru), nickel (Ni), cobalt (Co), alloys thereof, derivatives thereof or combinations thereof. In one aspect, the bulk fill layer **550** may include cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), and nickel rhenium boride (NiReB), derivatives thereof or combinations thereof. Preferably, bulk fill layer **550** is a nickel boride compound deposited by an electroless deposition process.

[**0082**] In another embodiment, as shown in **FIG. 5E**, after forming the aperture **505** (see **FIG. 5C**) a barrier layer **530**

is deposited on substrate **500**, including on dielectric layer **520**, and aperture **505**. Barrier layer **530** may contain a material that acts as an adhesion and/or diffusion barrier layer for the subsequently deposited materials deposited thereon, such as copper. Materials to form barrier layer **530** may include tantalum, tantalum nitride, tantalum silicon nitride, titanium, titanium nitride, titanium silicon nitride, ruthenium, alloys thereof, derivatives thereof or combinations thereof. Barrier layer **530** may be deposited by vapor deposition process that includes PVD, ALD or CVD. Preferably, barrier layer **530** is a tantalum-containing compound deposited by a PVD process. In one aspect, not shown, the barrier layer **530** may be removed from the surface of the plug **503** by use of a re-sputtering process that is typically performed in the PVD or PECVD processing chambers.

[**0083**] **FIG. 5F** illustrates the substrate **500** after an optional seed layer **540** has been deposited on barrier layer **530**. The optional seed layer **540** may increase adhesion or promote nucleation sites for subsequently deposited bulk-fill layer **550**. The seed layer **540** may be a continuous layer or a non-continuous layer across the surface of barrier layer **530**. Therefore, barrier layer **530** may be exposed if seed layer **540** is a non-continuous layer. Seed layer **540** may contain a metal, such as, copper, tungsten, tantalum, titanium, ruthenium, alloys thereof, derivatives thereof or combinations thereof. Seed layer **540** may be deposited by a vapor deposition process that includes PVD, ALD and CVD or a liquid deposition process that includes electroless or electroplating. Preferably, seed layer **540** is a copper-containing compound deposited by a PVD process.

[**0084**] **FIG. 5G** illustrates substrate **500** after a bulk fill layer **550** has been deposited on seed layer **540**, thus the aperture **505**. The deposition of bulk fill layer **550** completes the formation of interconnect plug **543** that is in electrical contact to plug **503**. Bulk fill layer **550** may contain a conductive as described above. Bulk fill layer **550** may be deposited by a vapor deposition process that includes PVD and CVD or a liquid deposition process that includes electroless or electroplating. In one embodiment, the bulk fill layer **550** is a copper-containing compound deposited by a PVD process. In another example, bulk fill layer **550** is a tungsten-containing compound deposited by a CVD process. In another example, bulk fill layer **550** is a nickel-containing compound deposited by an electroless deposition process. In another example, bulk fill layer **550** is a cobalt-tungsten alloy deposited by an electroless deposition process. In another example, bulk fill layer **550** is a copper-containing compound deposited by an electroless deposition process. In another example, bulk fill layer **550** is a copper-containing compound deposited by an electroplating process.

Examples of Electroless Process Solutions

[**0085**] The following are a examples of various electroless chemistries and processes that may be used to form the fill material **230**, fill material **320**, seed/adhesion layer **325**, conductive layer **350**, seed layer **440**, bulk fill layer **450**, seed layer **540**, and/or bulk fill layer **550**.

Electroless Nickel Deposition Chemistries and Processes

[**0086**] In one example, an electroless deposition solution useful to form nickel-containing material contains a nickel source, a reductant, at least one complexing agent, a pH adjusting agent, water and optional additives and surfactants. Nickel-containing material may be deposited by an electroless process utilizing either a pre-mixed electroless deposition solution or an in-line mixing process that combines solution components to generate the electroless solution.

[**0087**] The nickel source within the electroless deposition solution may have a concentration within a range from about 20 mM to about 200 mM, preferably from about 40 mM to about 80 mM, and more preferably from about 50 mM to about 70 mM, such as about 60 mM. Nickel sources provide nickel ions (e.g., Ni^{2+}) dissolved within the electroless solution and later reduced out as the deposited nickel-containing material. Useful nickel sources include nickel sulfate, nickel chloride, nickel acetate, nickel phosphate, derivatives thereof, hydrates thereof or combinations thereof. In a preferred embodiment, nickel sulfate hexahydrate ($NiSO_4.6H_2O$) is used in the electroless solution to deposit nickel-containing materials.

[**0088**] The reductant within the electroless deposition solution may have a concentration within a range from about 1 mM to about 100 mM, preferably from about 2 mM to about 50 mM, and more preferably from about 5 mM to about 20 mM, such as about 14 mM. Reductants provide electrons to induce chemical reduction of the nickel ions that form and deposit the nickel-containing material. Reductants may include organic reductants (e.g., formaldehyde or glyoxylic acid), hydrazine, organic hydrazines (e.g., methyl hydrazine), hypophosphite sources (e.g., hypophosphorous acid (H_3PO_2), ammonium hypophosphite ($(NH_4)_{4-x}H_xPO_2$) and salts thereof), borane sources (e.g., dimethylamine borane complex ($(CH_3)_2NH.BH_3$), DMAB), trimethylamine borane complex ($(CH_3)_3N.BH_3$), TMAB), tert-butylamine borane complex ($^tBuNH_2.BH_3$), tetrahydrofuran borane complex ($THF.BH_3$), pyridine borane complex ($C_5H_5N.BH_3$), ammonia borane complex ($NH_3.BH_3$), borane (BH_3), diborane (B_2H_6), derivatives thereof, complexes thereof or combinations thereof. In a preferred embodiment, DMAB is used as a reductant in the electroless solution for depositing nickel-containing materials.

[**0089**] Chelators or complexing agents are in the electroless solution to complex nickel ions thereby stabilizing the solubility and reduction of nickel ions. The complexing agents may have a concentration within a range from about 50 mM to about 2 M, preferably from about 100 mM to about 1 M, and more preferably from about 200 mM to about 500 mM. Complexing agents generally may have functional groups, such as carboxylic acids, dicarboxylic acids, polycarboxylic acids, amino acids, amines, diamines, polyamines, alkylamines, alkanolamines and alkoxyamines. Complexing agents may include citric acid, citrates, glycolic acid, glycine, malonic acid, maleic acid, lactic acid, ethylenediaminetetraacetic acid (EDTA), ethylenediamine (EDA), triethylene tetramine (TETA), diaminoethane, monoethanolamine, diethanolamine (DEA), triethanolamine (TEA), hydroxylamine hydrochloride, ammonia, ammonium chloride, derivatives thereof, salts thereof or combinations thereof. Usually, the electroless solution contains more than one complexing agent. Preferably, the electroless solution contains at least citric acid or citrate salts, more preferably, the electroless solution also contains DEA, glycine and/or lactic acid. In one example, the electroless solution contains about 60 mM of citric acid, 60 mM of DEA, 15 mM of glycine and 120 mM of lactic acid.

[0090] A pH adjusting agent is added to adjust the electroless solution to a pH value within a range from about 8 to about 11, preferably from about 9 to about 10, and more preferably from about 8.0 to about 8.5, such as about 8.5. The pH adjusting agent may be an acidic compound to decrease the pH value of the electroless solution and include hydrochloric acid, sulfuric acid, phosphoric acid, derivatives thereof or combinations thereof. Alternatively, the pH adjusting agent may be a basic compound to increase the pH value of the electroless solution and include metal hydroxides, tetraalkylammonium hydroxides (e.g., tetramethylammonium hydroxide ($(CH_3)_4NOH$, TMAH) or tetraethylammonium hydroxide ($(CH_3CH_2)_4NOH$, TEAH)), ammonium hydroxide, DEA, TEA, derivatives thereof or combinations thereof. The pH adjusting agent may be dissolved in water prior to adjusting the pH value of the electroless solution. In one example, a 25 wt % aqueous solution of TMAH is used as a pH adjusting agent. In another example, both TMAH and DEA are used to adjust the pH value of an electroless solution.

[0091] The optional additives may include levelers, accelerators and suppressors. Levelers within the electroless solution are used to achieve different deposition thickness as a function of leveler concentration and feature geometry while depositing nickel-containing materials. The leveler within the electroless deposition solution may have a concentration within a range from about 20 ppb to about 600 ppm, preferably from about 100 ppb to about 100 ppm. Examples of levelers that may be employed in an electroless solution include, but are not limited to alkylpolyimines and organic sulfonates, such as 1-(2-hydroxyethyl)-2-imidazolidinethione (HIT), 4-mercaptopyridine, 2-mercaptothiazoline, ethylene thiourea, thiourea or derivatives thereof. The electroless deposition solution may contain brighteners or accelerators and suppressors as alternative additives to provide further control of the deposition process. The role of accelerators is to achieve a smoothly deposited surface of the nickel-containing material. The accelerator within the electroless deposition solution has a concentration within a range from about 20 ppb to about 600 ppm, preferably from about 100 ppb to about 100 ppm. Accelerators that are useful in an electroless solution for depositing nickel-containing materials may include sulfur-based compounds such as bis(3-sulfopropyl)disulfide (SPS), 3-mercapto-1-propane sulfonic acid (MPSA), aminoethane sulfonic acids, thiourea, derivatives thereof, combinations thereof. Suppressors are used to suppress nickel deposition by initially adsorbing onto underlying catalytic surfaces and therefore blocking access to the catalyst of the reaction. Suppressors generally may include polyethylene glycol (PEG), polypropylene glycol (PPG), polyoxyethylene-polyoxypropylene copolymer (POCP), benzotriazole (BTA), dipyridyl, dimethyl dipyridyl, derivatives thereof or combinations thereof. The suppressor within the electroless deposition solution may have a concentration within a range from about 20 ppb to about 600 ppm, preferably from about 100 ppb to about 100 ppm.

[0092] The electroless solution may contain boric acid as an additional additive. Boric acid is added to provide additional buffering and to stabilize the composition of the solution. Boric acid is an oxidation by-product from the chemical reactions of borane reductants (e.g., DMAB). Therefore, an electroless solution containing boric acid is more normalized at the start of the deposition process since a less steep dissipation gradient exist as additional boric acid is formed from the borane reductant. Boric acid is preferably within the electroless deposition solution at concentration within a range from about 1 mM to about 50 mM, preferably from about 2 mM to about 20 M, and more preferably from about 3 mM to about 15 mM, such as about 5 mM.

[0093] Also, an optional surfactant may be added to the electroless solution. The surfactant is a wetting agent to reduce the surface tension between the electroless solution and the substrate surface. Surfactants are generally added to the electroless solution at a concentration of about 1,000 ppm or less, preferably about 800 ppm or less, such as from about 20 ppb to about 600 ppm. The surfactant may have ionic or non-ionic characteristics. A preferred surfactant includes dodecyl sulfates, such as sodium dodecyl sulfate (SDS). Other surfactants that may be used in the electroless deposition solution include glycol ether based surfactants (e.g., polyethylene glycol). For example, a glycol ether based surfactants may contain polyoxyethylene units, such as TRITON® 100, available from Dow Chemical Company. A nonylphenol ethoxylate surfactant is useful in the electroless deposition solution, such as TERGITOL®, available from Dow Chemical Company or IGEPAL-630, available from GAF Corporation. Other useful surfactants may contain phosphate units, for example, sodium poly(oxyethylene)phenyl ether phosphate, such as RHODAFAC® RE-610, available from Rhodia, Inc. The surfactants may be single compounds or a mixture of compounds of molecules containing varying length of hydrocarbon chains.

[0094] An electroless process to deposit nickel-containing materials may utilize an in-line mixing process to form the electroless solution. The process may contain the addition of two, three, four or more componential solutions to form the electroless solution. In one example, the electroless solution is formed by combining a buffered cleaning solution, a nickel-containing solution, a reducing solution and water, where each solution is a concentrate and water is added to reach a predetermined concentration of the final solution. In another example, the electroless solution is formed by combining a buffered cleaning solution, a nickel-containing solution and a reducing solution, where each of the solutions are pre-diluted and therefore do not require additional water. In another example, the electroless solution is formed by combining a buffered nickel-containing solution, a reducing solution and water, where a buffered cleaning solution and a nickel-containing solution are combined to form the buffered nickel-containing solution. Further details of in-line mixing processes and componential solutions are further described in the commonly assigned, U.S. patent application Ser. No. 10/967,919, entitled, "Selective Self-initiating Electroless Capping of Copper with Cobalt-containing Alloys," filed on Oct. 18, 2004, and published as US 2005-0136193, which is incorporated by reference to the extent not inconsistent with the claimed aspects and description herein.

[0095] A buffered cleaning solution usually contains water, at least one complexing agent, additives and a pH adjusting agent. The complexing agent within the buffered cleaning solution is at a concentration from about 0.2 M to about 3 M, preferably from about 0.5 M to about 2 M. The additive within the buffered cleaning solution is at a concentration from about 10 mM to about 1 M, preferably from about 50 mM to about 500 mM. The pH adjusting agent is at a concentration to provide the buffered cleaning solution with a pH value in a range from about 7.5 to about 11,

preferably from about 8 to about 10, and more preferably from about 9.2 to about 9.6, such as about 9.4. In one example, a buffered cleaning solution contains water, about 1.15 M of DEA, about 375 mM of citric acid, about 300 mM of glycine, about 100 mM of boric acid and a concentration of TMAH to adjust the pH value to about 9.4. In another example, a buffered cleaning solution contains water, about 330 mM of DEA, about 300 mM of citric acid, about 150 mM of glycine, about 50 mM of boric acid and a concentration of TMAH to adjust the pH value to about 9.4.

[0096] A nickel-containing solution usually contains water, a nickel source, at least one complexing agent and a pH adjusting agent. The nickel source within the nickel-containing solution is at a concentration from about 50 mM to about 1 M, preferably from about 100 mM to about 500 mM, such as about 300 mM. The complexing agent within the nickel-containing solution is at a concentration from about 0.2 M to about 2 M, preferably from about 0.5 M to about 1 M. The pH adjusting agent is at a concentration to provide the nickel-containing solution with a pH value in a range from about 8 to about 11, preferably from about 9 to about 10, and more preferably from about 8.0 to about 8.5, such as about 8.5. In one example, a nickel-containing solution contains water, about 100 mM of citric acid, about 300 mM of nickel sulfate, about 600 mM of 85% lactic acid and a concentration of TMAH to adjust the pH value to about 9.4.

[0097] A reducing solution usually contains water, at least one reductant, at least one complexing agent and a pH adjusting agent. The reductant within the reducing solution is at a concentration from about 10 mM to about 500 mM, preferably from about 50 mM to about 100 mM, such as about 70 mM. The complexing agent within the reducing solution is at a concentration from about 1 mM to about 50 mM, preferably from about 5 mM to about 15 mM, such as about 10 mM. The pH adjusting agent is at a concentration to provide the reducing solution with a pH value in a range from about 8 to about 11, preferably from about 9 to about 10, and more preferably from about 8.0 to about 8.5, such as about 8.5. In one example, a reducing solution contains water, about 10 mM of citric acid, about 70 mM of DMAB and a concentration of TMAH to adjust the pH value to about 9.4.

[0098] The electroless solution is preferably formed by in-line mixing process that combines various volumetric ratios of the buffered cleaning solution, the nickel-containing solution, the reducing solution and water. In one example, 1 volumetric equivalent of a buffered cleaning solution, 4 volumetric equivalents of a nickel-containing solution, 4 volumetric equivalents of a reducing solution and 11 volumetric equivalents of deionized water are in-line mixed to form an electroless solution. That is, the volumetric ratio of the buffered cleaning solution, the nickel-containing solution, the reducing solution and the deionized water is 1:4:4:11 (5%, 20%, 20%, 55% of electroless solution). In other examples of an electroless solution, a volumetric ratio of the buffered cleaning solution, the nickel-containing solution, the reducing solution and the water is 1:2:2:5 (10%, 20%, 20%, 50% of electroless solution) and 1:1:1:3 (16.7%, 16.7%, 16.7%, 50% of electroless solution).

[0099] In one embodiment, an electroless solution contains: nickel sulfate with a concentration in a range from about 20 mM to about 200 mM, preferably from about 40 mM to about 80 mM, and more preferably from about 50 mM to about 70 mM, such as about 60 mM; DMAB with a concentration in a range from about 1 mM to about 100 mM, preferably from about 2 mM to about 50 mM, and more preferably from about 5 mM to about 20 mM, such as about 14 mM; citric acid with a concentration in a range from about 5 mM to about 500 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 40 mM to about 80 mM, such as about 60 mM; DEA with a concentration in a range from about 5 mM to about 500 mM, preferably from about 10 mM to about 200 mM, such as about 60 mM; glycine with a concentration in a range from about 1 mM to about 150 mM, preferably from about 2 mM to about 80 mM, and more preferably from about 5 mM to about 50 mM, such as about 15 mM; boric acid with a concentration in a range from about 1 mM to about 100 mM, preferably from about 2 mM to about 50 mM, and more preferably from about 3 mM to about 20 mM, such as about 5 mM; lactic acid with a concentration in a range from about 10 mM to about 500 mM, preferably from about 50 mM to about 200 mM, and more preferably from about 100 mM to about 140 mM, such as about 120 mM; TMAH with a concentration to adjust the electroless solution to a have pH value in a range from about 8 to about 11, preferably from about 9 to about 10, and more preferably from about 98.0 to about 8.5, such as about 8.5.

[0100] In one embodiment, citrate is a preferred complexing agent and is present in each componential solution, such as the buffered cleaning solution, the nickel-containing solution and the reducing solution. Citrate may be added as citric acid and/or as a citrate salt. Citrate plays an important role of buffering each of the individual componential solutions while being combined to form the plating solution. Citrates generally have poor solubility in water at high concentrations, while the componential solutions may have relatively concentrated solutions. If a substantial citrate concentration of the final electroless solution is desired, a single componential solution may not be capable of completely containing all the dissolved citrate. Therefore, the citrate may be dissolved in each componential solution to assure no formation of citrate precipitate, and subsequently combined with water forming the electroless solution at a final concentration.

[0101] The electroless deposition process may be conducted at a temperature in a range from about 35° C. to about 120° C., preferably from about 60° C. to about 100° C. In one example, the temperature is from about 80° C. to about 85° C. In another example, the temperature is from about 65° C. to about 70° C. The water may be degassed, preheated and/or deionized water. Degassing the water reduces the oxygen concentration of the subsequently formed electroless solution. An electroless solution with a low oxygen concentration (e.g., less than about 100 ppm) may be used during the deposition process. Preheated water allows forming the electroless solution at a predetermined temperature just below the temperature used to initiate the deposition process, thereby shortening the process time.

[0102] The substrate may be exposed to a chemical mechanical polishing (CMP) process prior to the pretreatment and deposition processes described herein. Usually, the CMP process is conducted in a first process chamber, the nickel-containing layer or cobalt-tungsten alloy layer is

deposited in a second process chamber and the first and second process chambers are on the same CMP tool. In one example, the second process chamber is in fluid communication to an in-line mixing system that combines stock solutions used in the pretreatment process and/or the electroless deposition processes.

[0103] A "substrate surface" as used herein refers to any substrate or material surface formed on a substrate upon which film processing is performed. For example, a substrate surface on which processing may be performed include materials such as monocrystalline, polycrystalline or amorphous silicon, strained silicon, silicon on insulator (SOI), doped silicon, silicon germanium, germanium, gallium arsenide, glass, sapphire, silicon oxide, silicon nitride, silicon oxynitride and/or carbon doped silicon oxides, such as SiO_xC_y, for example, BLACK DIAMOND™ low-k dielectric, available from Applied Materials, Inc., located in Santa Clara, Calif. Substrates may have various dimensions, such as 200 mm or 300 mm diameter wafers, as well as, rectangular or square panes. Embodiments of the processes described herein deposit nickel-containing materials on many types of substrates and surfaces. Substrates on which embodiments of the invention may be useful include, but are not limited to semiconductor wafers, such as crystalline silicon (e.g., Si<100> or Si<111>), silicon oxide, strained silicon, silicon germanium, doped or undoped polysilicon, doped or undoped silicon wafers, and patterned or non-patterned wafers. Substrates made of glass or plastic, which, for example, are commonly used to fabricate flat panel displays and other similar devices, are also included.

[0104] A chamber useful to conduct an electroless deposition process for depositing a cobalt-tungsten material, a cobalt-nickel material or a nickel-containing material is the electroless deposition process cell, further described in the commonly assigned U.S. patent application Ser. No. 10/965,220, entitled "Apparatus for Electroless Deposition," filed on Oct. 14, 2004, and published as US 2005-0081785, U.S. patent application Ser. No. 10/996,342, entitled, "Apparatus for Electroless Deposition of Metals on Semiconductor Wafers," filed on Nov. 22, 2004, U.S. patent application Ser. No. 11/043,442, entitled, "Apparatus for Electroless Deposition of Metals onto Semiconductor Substrates," filed on Jan. 26, 2005, and U.S. patent application Ser. No. 11/040,962, entitled "Method and Apparatus for Selectively Changing Thin Film Composition During Electroless Deposition in a Single Chamber," filed on Jan. 22, 2005, which are each incorporated by reference to the extent not inconsistent with the claimed aspects and description herein.

Examples of Cobalt and Nickel Electroless Deposition Chemistries

Cobalt

[0105] In one embodiment, an electroless solution for depositing metallic cobalt contains: cobalt ions (Co^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; hydrazine hydrate with a concentration in a range from about 100 mM to about 2 M, preferably from about 200 mM to about 1 M, and more preferably from about 300 mM to about 700 mM, such as about 500 mM; citric acid or citrate salt with a citrate concentration in a range from about 5 mM to about 200 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 30 mM to about 70 mM, such as about 50 mM; and an optional pH adjusting agent (e.g., TMAH) with a concentration to adjust the electroless solution to a have pH value in a range from about 10 to about 14, preferably from about 11.5 to about 13, and more preferably from about 12.2 to about 12.8, such as about 12.5. In one example, a pH value is about 11.5 or higher, preferably, about 12.0 or higher, and more preferably, about 12.5 or higher. The electroless deposition process to deposit metallic cobalt may be conducted at a temperature within a range from about 35° C. to about 100° C., preferably from about 60° C. to about 90° C., and more preferably from about 70° C. to about 80° C., such as about 75° C.

Cobalt Boride

[0106] In one embodiment, an electroless solution for depositing cobalt boride contains: cobalt ions (Co^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; DMAB with a concentration in a range from about 1 mM to about 200 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 30 mM to about 50 mM, such as about 40 mM; citric acid or citrate salt with a citrate concentration in a range from about 5 mM to about 500 mM, preferably from about 30 mM to about 300 mM, and more preferably from about 50 mM to about 150 mM, such as about 100 mM; and an optional pH adjusting agent (e.g., TMAH) with a concentration to adjust the electroless solution to a have pH value in a range from about 8 to about 11, preferably from about 8 to about 10, and more preferably from about 8.5 to about 9.5, such as about 8.9. The electroless deposition process to deposit cobalt boride may be conducted at a temperature within a range from about 35° C. to about 100° C., preferably from about 60° C. to about 80° C., and more preferably from about 65° C. to about 75° C., such as about 70° C.

Cobalt Tungsten Boride

[0107] In one embodiment, an electroless solution for depositing cobalt tungsten boride contains: cobalt ions (Co^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; tungstic acid or tungstate salt with a tungstate concentration in a range from about 0.1 mM to about 10 mM, preferably from about 0.5 mM to about 5 mM, and more preferably from about 1 mM to about 3 mM, such as about 2 mM; DMAB with a concentration in a range from about 1 mM to about 200 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 30 mM to about 50 mM, such as about 40 mM; citric acid or citrate salt with a citrate concentration in a range from about 5 mM to about 500 mM, preferably from about 30 mM to about 300 mM, and more preferably from about 50 mM to about 150 mM, such as about 100 mM; and an optional pH adjusting agent (e.g., TMAH) with a concentration to adjust the electroless solution to a have pH value in a range from about 8 to about 11, preferably from about 8 to about 10, and more preferably from about 8.5 to about 9.5, such as about 8.9. The electroless deposition process to deposit cobalt tungsten boride may be conducted at a temperature within a range from about 35° C. to about 100° C., preferably from about 60° C. to about 80° C., and more preferably from about 65° C. to about 75° C., such as about 70° C.

Nickel Boride

[0108] In one embodiment, an electroless solution for depositing nickel boride contains: nickel ions (Ni^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 80 mM, such as about 60 mM; DMAB with a concentration in a range from about 1 mM to about 200 mM, preferably from about 10 mM to about 50 mM, such as about 28 mM; citric acid or citrate salt with a citrate concentration in a range from about 5 mM to about 300 mM, preferably from about 10 mM to about 60 mM, such as about 58 mM; boric acid with a concentration in a range from about 1 mM to about 100 mM, preferably from about 2 mM to about 50 mM, and more preferably from about 3 mM to about 20 mM, such as about 5 mM; lactic acid or lactate salt with a lactate concentration in a range from about 5 mM to about 300 mM, preferably from about 10 mM to about 150 mM, such as about 120 mM; glycine with a concentration in a range from about 1 mM to about 150 mM, preferably from about 2 mM to about 80 mM, and more preferably from about 5 mM to about 50 mM, such as about 15 mM; diethanolamine (DEA) with a concentration in a range from about 5 mM to about 300 mM, preferably from about 10 mM to about 150 mM, such as about 58 mM and an optional pH adjusting agent (e.g., TMAH) with a concentration to adjust the electroless solution to a have pH value in a range from about 8 to about 11, preferably from about 8 to about 10, and more preferably from about 8.0 to about 8.5, such as about 8.5. The electroless deposition process to deposit nickel boride may be conducted at a temperature within a range from about 35° C. to about 100° C., preferably from about 60° C. to about 80° C., and more preferably from about 65° C. to about 75° C., such as about 70° C.

Nickel Tungsten Boride

[0109] In one embodiment, an electroless solution for depositing nickel tungsten boride contains: nickel ions (Ni^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; tungstic acid or tungstate salt with a tungstate concentration in a range from about 0.1 mM to about 10 mM, preferably from about 0.5 mM to about 5 mM, and more preferably from about 1 mM to about 3 mM, such as about 2 mM; DMAB with a concentration in a range from about 1 mM to about 200 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 30 mM to about 50 mM, such as about 40 mM; citric acid or citrate salt with a citrate concentration in a range from about 5 mM to about 300 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 40 mM to about 60 mM, such as about 50 mM; lactic acid or lactate salt with a lactate concentration in a range from about 5 mM to about 300 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 40 mM to about 60 mM, such as about 50 mM; and an optional pH adjusting agent (e.g., TMAH) with a concentration to adjust the electroless solution to a have pH value in a range from about 8 to about 11, preferably from about 8 to about 10, and more preferably from about 8.5 to about 9.5, such as about 8.9. The electroless deposition process to deposit nickel tungsten boride may be conducted at a temperature within a range from about 35° C. to about 100° C., preferably from about 60° C. to about 80° C., and more preferably from about 65° C. to about 75° C., such as about 70° C.

Cobalt Nickel Boride

[0110] In one embodiment, an electroless solution for depositing cobalt nickel boride contains: cobalt ions (Co^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; nickel ions (Ni^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; DMAB with a concentration in a range from about 1 mM to about 200 mM, preferably from about 10 mM to about 100 mM, and more preferably from about 30 mM to about 50 mM, such as about 40 mM; citric acid or citrate salt with a citrate concentration in a range from about 5 mM to about 500 mM, preferably from about 30 mM to about 300 mM, and more preferably from about 50 mM to about 150 mM, such as about 100 mM; and an optional pH adjusting agent (e.g., TMAH) with a concentration to adjust the electroless solution to a have pH value in a range from about 8 to about 11, preferably from about 8 to about 10, and more preferably from about 8.5 to about 9.5, such as about 8.9. The electroless deposition process to deposit cobalt nickel boride may be conducted at a temperature within a range from about 35° C. to about 100° C., preferably from about 60° C. to about 80° C., and more preferably from about 65° C. to about 75° C., such as about 70° C.

Cobalt Nickel

[0111] In one embodiment, an electroless solution for depositing cobalt nickel contains: cobalt ions (Co^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; nickel ions (Ni^{2+}) with a concentration in a range from about 1 mM to about 100 mM, preferably from about 5 mM to about 50 mM, and more preferably from about 10 mM to about 20 mM, such as about 15 mM; hydrazine hydrate with a concentration in a range from about 100 mM to about 2 M, preferably from about 200 mM to about 1 M, and more preferably from about 300 mM to about 700 mM, such as about 500 mM; citric acid or citrate salt with a citrate concentration in a range from about 5 mM to about 500 mM, preferably from about 30 mM to about 300 mM, and more preferably from about 50 mM to about 150 mM, such as about 100 mM; and an optional pH adjusting agent (e.g., TMAH) with a concentration to adjust the electroless solution to a have pH value in a range from about 10 to about 14, preferably from about 11.5 to about 13, and more preferably from about 12.2 to about 12.8, such as about 12.5. The electroless deposition process to deposit cobalt nickel may be conducted at a temperature within a range from about 35° C. to about 100° C., preferably from about 60° C. to about 90° C., and more preferably from about 70° C. to about 80° C., such as about 75° C.

[0112] While foregoing is directed to the preferred embodiment of the invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

1. A method of forming an interconnect on a silicon substrate, comprising:

providing a substrate containing an exposed tungsten-containing contact plug exposed that has an exposed gap formed therein;

exposing the substrate to a pretreatment process, wherein the pretreatment process is adapted to remove an oxide layer from a surface of the exposed tungsten-containing contact plug; and

filling the exposed gap with a fill material.

2. The method of claim 1, wherein the pretreatment process comprises exposing the substrate to a wet-clean solution having a pH value of less than about 5.

3. The method of claim 2, wherein the wet-clean solution has a hydrogen fluoride concentration within a range from about 0.1 wt % to about 2 wt %.

4. The method of claim 2, wherein the wet-clean solution further comprises a complexing agent that is selected from the group consisting of citric acid, EDTA, EDA, carboxylic acids, amines, salts thereof, derivatives thereof and combinations thereof.

5. The method of claim 1, wherein the step of filling the exposed gap is completed using an electroless deposition process, wherein the fill material is selected from the group consisting of cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), and nickel rhenium boride (NiReB).

6. The method of claim 1, wherein the fill material is selected from the group consisting of copper, cobalt, nickel and tungsten.

7. The method of claim 1, wherein the fill material is a dielectric material.

8. The method of claim 1, further comprising removing a portion of the exposed tungsten-containing contact plug to increase the size of the exposed gap.

9. The method of claim 8, wherein the step of removing a portion of the exposed tungsten-containing contact plug is performed using a wet-clean solution having a pH value of less than about 5.

10. A method of forming an interconnect on a silicon substrate, comprising:

providing a silicon substrate having a first dielectric layer which is disposed on a surface of the silicon substrate and a first aperture formed in the first dielectric layer, wherein a doped silicon containing region of the silicon substrate is exposed at the bottom of the first aperture;

filling the first aperture formed in the first dielectric layer with a tungsten containing layer, wherein the tungsten containing layer is in electrical communication with the doped silicon containing region;

removing an amount of the tungsten containing layer disposed on the first dielectric layer, wherein a gap formed in the tungsten containing layer during the step of filling the first aperture is exposed; and

depositing a material on the surface of the silicon substrate to substantially cover the gap formed in the tungsten containing layer.

11. The method of claim 10, further comprising exposing the substrate to a pretreatment process, wherein the pretreatment process is adapted to remove an oxide layer from a surface of the exposed tungsten containing layer.

12. The method of claim 11, wherein the pretreatment process further comprises exposing the substrate to a wet-clean solution having a pH value of less than about 5.

13. The method of claim 12, wherein wet-clean solution further comprises a complexing agent that is selected from the group consisting of citric acid, EDTA, EDA, carboxylic acids, amines, salts thereof, derivatives thereof and combinations thereof.

14. The method of claim 10, wherein the material is selected from the group consisting of metallic nickel (Ni), metallic cobalt (Co), cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), and nickel rhenium boride (NiReB).

15. The method of claim 10, further comprising;

forming a second dielectric layer over the first dielectric layer and the tungsten containing layer disposed in the first aperture; and

forming a second aperture in the second dielectric layer that is in communication with the tungsten containing layer disposed in the first aperture, wherein the step of forming the second aperture is formed before the step of depositing a material on the surface of the silicon containing substrate is performed.

16. A method of forming an interconnect on a silicon substrate, comprising:

providing a substrate containing first dielectric layer that contains at least one tungsten-containing contact plug that has an exposed surface;

forming a second dielectric layer over the first dielectric layer and the tungsten-containing contact plug;

forming a second aperture in the second dielectric layer that is in communication with the exposed surface of the tungsten-containing contact plug; and

selectively filling the second aperture with a fill material.

17. The method of claim 16, further comprising depositing a first metal layer over the exposed surface of the tungsten-containing contact plug and the second aperture before selectively filling the second aperture.

18. The method of claim 16, wherein the tungsten-containing contact plug has an exposed gap that comprises a portion of the exposed surface of the tungsten-containing contact plug, wherein the second aperture is in communication with the exposed surface and the exposed gap.

19. The method of claim 16, further comprising exposing the substrate to a pretreatment process, wherein the pretreatment process is performed after forming the second aperture

and is adapted to remove an oxide layer from the exposed surface of the tungsten-containing contact plug.

20. The method of claim 17, further comprising removing the second dielectric layer from the surface of the tungsten-containing contact plug before depositing the first metal layer.

21. The method of claim 16, further comprising exposing the substrate to a pretreatment process, wherein the pretreatment process is adapted to remove an oxide layer from a surface of the exposed tungsten-containing contact plug before selectively filling the second aperture with the fill material.

22. The method of claim 16, wherein the pretreatment process further comprises exposing the substrate to a wet-clean solution having a pH value of less than about 5.

23. The method of claim 22, wherein wet-clean solution further comprises a complexing agent that is selected from the group consisting of citric acid, EDTA, EDA, carboxylic acids, amines, salts thereof, derivatives thereof and combinations thereof.

24. The method of claim 17, wherein the first metal layer is contains a metal selected from the group consisting of metallic nickel (Ni), metallic cobalt (Co), cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), and nickel rhenium boride (NiReB).

25. The method of claim 16, wherein the fill material is selected from the group consisting of metallic nickel (Ni), metallic cobalt (Co), cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), and nickel rhenium boride (NiReB).

26. The method of claim 16, wherein the fill material is electrolessly deposited on the exposed surface of the tungsten-containing contact plug and is generally in contact with the second dielectric layer.

27. The method of claim 26, wherein the fill material contains a metal selected from the group consisting of cobalt and nickel.

28. The method of claim 18, further comprising filing the exposed gap with a second layer that contains a metal selected from the group consisting of metallic nickel (Ni), metallic cobalt (Co), cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), and nickel rhenium boride (NiReB).

29. A method of forming an interconnect on a silicon substrate, comprising:

providing a substrate having an aperture formed in a dielectric layer disposed on a surface of the substrate, wherein the aperture is in communication with an exposed surface of a tungsten-containing contact plug;

dispensing a clean solution on an the exposed surface of the tungsten-containing contact plug, wherein the clean solution comprises hydrogen fluoride;

disposing a preparation solution on the exposed surface of the tungsten-containing contact plug, wherein the preparation solution comprises a tungstate source;

depositing a initiation layer on the exposed surface of the tungsten-containing contact plug using an activation solution; and

selectively filling the second aperture with a fill material.

30. The method of claim 29, wherein the clean solution is an aqueous solution that has a hydrofluoric acid concentration in a range from about 0.1 wt % to about 0.5 wt %.

31. The method of claim 29, wherein the preparation solution is an aqueous solution that comprises a tungstate source that is selected from the group consisting of ammonium tungsten oxide, tungstic acid, water soluble WO_4^{2-} sources, derivatives thereof and combinations thereof.

32. The method of claim 29, wherein the preparation solution is an aqueous solution that has a tungstic acid concentration in a range from about 2 mM to about 100 mM.

33. The method of claim 29, further comprising dispensing a chelating solution on the exposed surface of the substrate, wherein the chelating solution comprises citric acid that is in a concentration between about 50 mM and about 300 mM.

34. The method of claim 29, wherein the initiation layer is deposited using an activation solution that contains a palladium source.

35. The method of claim 29, wherein the fill material contains a metal selected from the group consisting of cobalt and nickel.

36. The method of claim 29, wherein the fill material contains a metal selected from the group consisting of metallic nickel (Ni), metallic cobalt (Co), cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), nickel boride (NiB), nickel phosphide (NiP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel molybdenum phosphide (NiMoB), nickel molybdenum phosphide (NiMoP), nickel rhenium phosphide (NiReP), and nickel rhenium boride (NiReB).

37. The method of claim 29, further comprising activating the initiation layer using a rinse activation solution before selectively filling the second aperture with a fill material.

38. The method of claim 37, wherein rinse activation solution has a borane reductant concentration in a range from about 1 mM to about 200 mM.

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