(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

PCT

(43) International Publication Date
10 November 2011 (10.11.2011)

(10) International Publication Number
WO 2011/140033 A2

(51) International Patent Classification:
G11C 7/10 (2006.01) *G11C 11/401* (2006.01) *G11C 8/14* (2006.01)

(21) International Application Number:
PCT/US2011/034924

(22) International Filing Date:
3 May 2011 (03.05.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/332,037 6 May 2010 (06.05.2010) US
13/031,906 22 February 2011 (22.02.2011) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: TECHNIQUES FOR REFRESHING A SEMICONDUCTOR MEMORY DEVICE

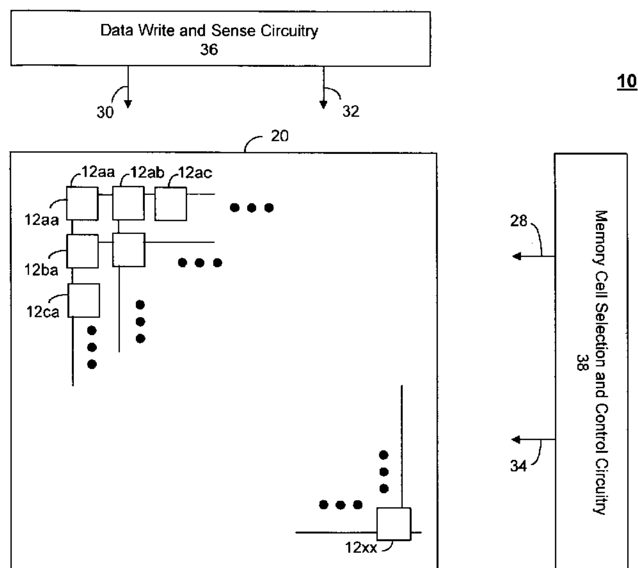

FIGURE 1

(57) Abstract: Techniques for refreshing a semiconductor memory device are disclosed. In one particular exemplary embodiment, the techniques may be realized as a semiconductor memory device including a plurality of memory cells arranged in an array of rows and columns. Each memory cell may include a first region coupled to a source line and a second region coupled to a carrier injection line. Each memory cell may also include a body region capacitively coupled to at least one word line and disposed between the first region and the second region and a decoupling resistor coupled to at least a portion of the body region.

WO 2011/140033 A2

WO 2011/140033 A2

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

TECHNIQUES FOR REFRESHING A SEMICONDUCTOR MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

This patent application claims priority to U.S. Provisional Patent Application No. 61/332,037, filed May 6, 2010, which is hereby incorporated by reference herein in its entirety.

FIELD OF THE DISCLOSURE

The present disclosure relates generally to semiconductor memory devices and, more particularly, to techniques for refreshing a semiconductor memory device.

BACKGROUND OF THE DISCLOSURE

The semiconductor industry has experienced technological advances that have permitted increases in density and/or complexity of semiconductor memory devices. Also, the technological advances have allowed decreases in power consumption and package sizes of various types of semiconductor memory devices. There is a continuing trend to employ and/or fabricate advanced semiconductor memory devices using techniques, materials, and devices that improve performance, reduce leakage current, and enhance overall scaling. Silicon-on-insulator (SOI) and bulk substrates are examples of materials that may be used to fabricate such semiconductor memory devices. Such semiconductor memory devices may include, for example, partially depleted (PD) devices, fully depleted (FD) devices, multiple gate devices (e.g., double, triple gate, or surrounding gate), and Fin-FET devices.

A semiconductor memory device may include a memory cell having a memory transistor with an electrically floating body region wherein electrical charge may be stored. When excess majority electrical charges carriers are stored in the

electrically floating body region, the memory cell may store a logic high (e.g., binary "1" data state). When the electrical floating body region is depleted of majority electrical charge carriers, the memory cell may store a logic low (e.g., binary "0" data state). Also, a semiconductor memory device may be fabricated on silicon-on-insulator (SOI) substrates or bulk substrates (e.g., enabling body isolation). For example, a semiconductor memory device may be fabricated as a three-dimensional (3-D) device (e.g., a multiple gate device, a Fin-FET device, and a vertical pillar device).

In one conventional technique, the memory cell of the semiconductor memory device may be read by applying bias signals to a source/drain region and a gate of the memory transistor. As such, a conventional reading technique may involve sensing an amount of current provided/generated by/in the electrically floating body region of the memory cell in response to the application of the source/drain region and gate bias signals to determine a data state of the memory cell. For example, the memory cell may have two or more different current states corresponding to two or more different logical states (e.g., two different current conditions/states corresponding to two different logic states: a binary "0" data state and a binary "1" data state).

In another conventional technique, the memory cell of the semiconductor memory device may be written to by applying bias signals to the source/drain region(s) and the gate of the memory transistor. As such, a conventional writing technique may result in an increase/decrease of majority charge carriers in the electrically floating body region of the memory cell which, in turn, determines the data state of the memory cell. Such an excess of majority charge carriers may result from channel impact ionization, band-to-band tunneling (gate-induced drain leakage "GIDL"), or direct injection. Majority charge carriers may be removed via drain region hole removal,

source region hole removal, or drain and source region hole removal, for example, using back gate pulsing.

Often, conventional reading and/or writing operations may lead to relatively large power consumption and large voltage potential swings which may cause disturbance to unselected memory cells in the semiconductor memory device. Also, pulsing between positive and negative gate biases during read and write operations may reduce a net quantity of majority charge carriers in the electrically floating body region of the memory cell, which, in turn, may result in an inaccurate determination of the data state of the memory cell. Furthermore, in the event that a bias signal having a voltage potential that is below a threshold voltage potential of the memory transistor is applied to the gate of the memory transistor, a channel of minority charge carriers beneath the gate may be eliminated. However, some of the minority charge carriers may remain "trapped" in interface defects. Some of the trapped minority charge carriers may combine with majority charge carriers, which may be attracted to the gate as a result of the applied bias signal. As a result, the net quantity of majority charge carriers in the electrically floating body region may be reduced. This phenomenon, which is typically characterized as charge pumping, is problematic because the net quantity of majority charge carriers may be reduced in the electrically floating body region of the memory cell, which, in turn, may result in an inaccurate determination of the data state of the memory cell.

In view of the foregoing, it may be understood that there may be significant problems and shortcomings associated with conventional techniques for operating a semiconductor memory device.

SUMMARY OF THE DISCLOSURE

Techniques for refreshing a semiconductor memory device are disclosed. In one particular exemplary embodiment, the techniques may be realized as a semiconductor memory device comprising a plurality of memory cells arranged in an array of rows and columns. Each memory cell may comprise a first region coupled to a source line and a second region coupled to a carrier injection line. Each memory cell may also comprise a body region capacitively coupled to at least one word line and disposed between the first region and the second region and a decoupling resistor coupled to at least a portion of the body region.

In accordance with other aspects of this particular exemplary embodiment, the first region may be an N-doped region and the second region may be a P-doped region.

In accordance with further aspects of this particular exemplary embodiment, the body region may be an undoped region.

In accordance with additional aspects of this particular exemplary embodiment, the body region may comprise a first portion and a second portion.

In accordance with other aspects of this particular exemplary embodiment, the first portion of the body region and the second portion of the body region may be different portions of the body region.

In accordance with further aspects of this particular exemplary embodiment, the decoupling resistor may be coupled to the second portion of the body region.

In accordance with additional aspects of this particular exemplary embodiment, the decoupling resistor may be coupled to the second portion of the body region via a bit line.

In accordance with other aspects of this particular exemplary embodiment, a plurality of word lines may be capacitively coupled to the body region.

In accordance with further aspects of this particular exemplary embodiment, the plurality of word lines may be capacitively coupled to a plurality of side portions of the body region.

5 In accordance with additional aspects of this particular exemplary embodiment, each of the plurality of word lines may be capacitively coupled to different portions on a common side of the body region.

In accordance with other aspects of this particular 10 exemplary embodiment, each of the plurality of word lines may be capacitively coupled to opposite side portions of the body region.

In accordance with further aspects of this particular exemplary embodiment, the plurality of word lines may comprise 15 a first word line and a second word line.

In accordance with additional aspects of this particular exemplary embodiment, the first word line may be capacitively coupled to a first portion of the body region and the second word line may be capacitively coupled to a second portion of 20 the body region.

In accordance with other aspects of this particular exemplary embodiment, the decoupling resistor may have a resistance that causes a current flow through the decoupling resistor between a current that may represent a logic low and 25 a current that may represent a logic high.

In another particular exemplary embodiment, the techniques may be realized as a method for biasing a semiconductor memory device comprising the steps of applying a plurality of voltage potentials to a plurality of memory cells 30 arranged in an array of rows and columns. The method may also comprise applying a first voltage potential to a first region via a respective source line of the array and applying a second voltage potential to a second region via a respective carrier injection line of the array. The method may further

comprise applying a third voltage potential to a first portion of a body region via at least one respective word line of the array that is capacitively coupled to the body region and applying a fourth voltage potential to a second portion of the body region via a respective bit line of the array and a decoupling resistor.

In accordance with other aspects of this particular exemplary embodiment, the respective source line may be coupled to an electrical ground.

In accordance with further aspects of this particular exemplary embodiment, the fourth voltage potential applied to the second portion of the body region may be a constant voltage potential.

In accordance with additional aspects of this particular exemplary embodiment, the method may further comprise increasing the third voltage potential applied to the at least one respective word line during a hold operation in order to perform a write logic low operation.

In accordance with other aspects of this particular exemplary embodiment, the method may further comprise maintaining the second voltage potential applied to the respective carrier injection line during a hold operation in order to perform a write logic low operation.

In accordance with further aspects of this particular exemplary embodiment, the method further comprise increasing the second voltage potential applied to the respective carrier injection line and the third voltage potential applied to the at least one respective word line during a hold operation in order to perform a write logic high operation.

In accordance with additional aspects of this particular exemplary embodiment, the method further comprise increasing the second voltage potential applied to the respective carrier injection line and the third voltage potential applied to the at least one respective word line during a hold operation in

order to perform a read operation.

In accordance with other aspects of this particular exemplary embodiment, the decoupling resistor and the respective bit line may be coupled to the respective carrier injection line.

In accordance with further aspects of this particular exemplary embodiment, the method may further comprise increasing the third voltage potential applied to the at least one respective word line during a hold operation in order to perform a write logic low operation.

In accordance with additional aspects of this particular exemplary embodiment, the method may further comprise maintaining the second voltage potential applied to the respective carrier injection line during a hold operation in order to perform a write logic low operation.

In accordance with other aspects of this particular exemplary embodiment, the method may further comprise increasing the second voltage potential applied to the respective carrier injection line and the third voltage potential applied to the at least one respective word line during a hold operation in order to perform a write logic high operation.

In accordance with further aspects of this particular exemplary embodiment, the method may further comprise increasing the second voltage potential applied to the respective carrier injection line and the third voltage potential applied to the at least one respective word line during a hold operation in order to perform a read operation.

In accordance with additional aspects of this particular exemplary embodiment, the second voltage potential applied to the second region may be a constant voltage potential.

In accordance with other aspects of this particular exemplary embodiment, the method may further comprise increasing the third voltage potential applied to the at least

one respective word line and the fourth voltage potential applied to the respective bit line during a hold operation in order to perform a write logic low operation.

In accordance with further aspects of this particular exemplary embodiment, the method may further comprise maintaining the fourth voltage potential applied to the respective bit line during a hold operation in order to perform a write logic high operation.

In accordance with additional aspects of this particular exemplary embodiment, the method may further comprise increasing the third voltage potential applied to the at least one respective bit line during a hold operation to perform a write logic high operation.

In accordance with other aspects of this particular exemplary embodiment, the method may further comprise increasing the third voltage potential applied to the at least one respective word line and the fourth voltage potential applied to the respective bit line during a hold operation in order to perform a read operation.

In accordance with further aspects of this particular exemplary embodiment, the method may further comprise increasing the second voltage potential applied to the respective carrier injection line, the third voltage potential applied to the at least one respective word line, and the fourth voltage potential applied to the respective bit line during a hold operation in order to perform a write logic low operation.

In accordance with additional aspects of this particular exemplary embodiment, the method may further comprise increasing the second voltage potential applied to the respective carrier injection line and the third voltage potential applied to the at least one respective word line during a hold operation in order to perform a write logic high operation.

In accordance with other aspects of this particular exemplary embodiment, the method may further comprise increasing the second voltage potential applied to the respective carrier injection line and the third voltage potential applied to the at least one respective word line during a hold operation in order to perform a write logic high operation.

In accordance with further aspects of this particular exemplary embodiment, the method may further comprise increasing the second voltage potential applied to the respective carrier injection line, the third voltage potential applied to the at least one respective word line, and the fourth voltage potential applied to the respective bit line during a hold operation in order to perform a read operation.

The present disclosure will now be described in more detail with reference to exemplary embodiments thereof as shown in the accompanying drawings. While the present disclosure is described below with reference to exemplary embodiments, it should be understood that the present disclosure is not limited thereto. Those of ordinary skill in the art having access to the teachings herein will recognize additional implementations, modifications, and embodiments, as well as other fields of use, which are within the scope of the present disclosure as described herein, and with respect to which the present disclosure may be of significant utility.

BRIEF DESCRIPTION OF THE DRAWINGS

In order to facilitate a fuller understanding of the present disclosure, reference is now made to the accompanying drawings, in which like elements are referenced with like numerals. These drawings should not be construed as limiting the present disclosure, but are intended to be exemplary only.

Figure 1 shows a block diagram of a semiconductor memory device including a memory cell array, data write and sense

circuitry, and memory cell selection and control circuitry in accordance with an embodiment of the present disclosure.

Figure 2 shows a cross-sectional view of a memory cell of the memory cell array in accordance with an embodiment of the present disclosure.

Figure 3 shows a cross-sectional view of a memory cell of the memory cell array in accordance with an alternative embodiment of the present disclosure.

Figure 4 shows a schematic diagram of a memory cell of the memory cell array in accordance with an embodiment of the present disclosure.

Figure 5 shows a schematic diagram of at least a portion of a memory cell array having a plurality of memory cells as shown in Figure 4 in accordance with an embodiment of the present disclosure.

Figure 6 shows control signal voltage waveforms for performing various operations on memory cells as shown in Figure 5 in accordance with an embodiment of the present disclosure.

Figure 7 shows a schematic diagram of a memory cell of the memory cell array in accordance with an alternate embodiment of the present disclosure.

Figure 8 shows a schematic diagram of at least a portion of a memory cell array having a plurality of memory cells as shown in Figure 7 in accordance with an alternate embodiment of the present disclosure.

Figure 9 shows control signal voltage waveforms for performing various operations on memory cells as shown in Figure 8 in accordance with an embodiment of the present disclosure.

Figure 10 shows a schematic diagram of a memory cell of the memory cell array in accordance with an alternate embodiment of the present disclosure.

Figure 11 shows a schematic diagram of at least a portion

of a memory cell array having a plurality of memory cells as shown in Figure 10 in accordance with an alternative embodiment of the present disclosure.

Figure 12 shows control signal voltage waveforms for performing various operations on memory cells as shown in Figure 11 in accordance with an alternate embodiment of the present disclosure.

Figure 13 shows a schematic diagram of a memory cell of the memory cell array in accordance with an alternate embodiment of the present disclosure.

Figure 14 shows a schematic diagram of at least a portion of a memory cell array having a plurality of memory cells as shown in Figure 13 in accordance with an alternative embodiment of the present disclosure.

Figure 15 shows control signal voltage waveforms for performing various operations on memory cells as shown in Figure 14 in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

Referring to Figure 1, there is shown a block diagram of a semiconductor memory device 10 comprising a memory cell array 20, data write and sense circuitry 36, and memory cell selection and control circuitry 38 in accordance with an embodiment of the present disclosure. The memory cell array 20 may comprise a plurality of memory cells 12 each coupled to the memory cell selection and control circuitry 38 via a word line (WL) 28 and a carrier injection line (EP) 34, and to the data write and sense circuitry 36 via a bit line (CN) 30 and a source line (EN) 32. It may be appreciated that the bit line (CN) 30 and the source line (EN) 32 are designations used to distinguish between two signal lines and they may be used interchangeably.

The data write and sense circuitry 36 may read data from

and may write data to selected memory cells 12. In an exemplary embodiment, the data write and sense circuitry 36 may include a plurality of data sense amplifier circuits. Each data sense amplifier circuit may receive at least one bit line (CN) 30 and a current or voltage reference signal. For example, each data sense amplifier circuit may be a cross-coupled type sense amplifier to sense a data state stored in a memory cell 12. The data write and sense circuitry 36 may include at least one multiplexer that may couple to a data sense amplifier circuit to at least one bit line (CN) 30. In an exemplary embodiment, the multiplexer may couple a plurality of bit lines (CN) 30 to a data sense amplifier circuit.

Each data sense amplifier circuit may employ voltage and/or current sensing circuitry and/or techniques. In an exemplary embodiment, each data sense amplifier circuit may employ current sensing circuitry and/or techniques. For example, a current sense amplifier may compare current from a selected memory cell 12 to a reference current (e.g., the current of one or more reference cells). From that comparison, it may be determined whether the selected memory cell 12 stores a logic high (e.g., binary "1" data state) or a logic low (e.g., binary "0" data state). It may be appreciated by one having ordinary skill in the art that various types or forms of the data write and sense circuitry 36 (including one or more sense amplifiers, using voltage or current sensing techniques, to sense a data state stored in a memory cell 12) may be employed to read data stored in the memory cells 12.

The memory cell selection and control circuitry 38 may select and/or enable one or more predetermined memory cells 12 to facilitate reading data therefrom by applying control signals on one or more word lines (WL) 28 and/or carrier injection lines (EP) 34. The memory cell selection and control circuitry 38 may generate such control signals from

address signals, for example, row address signals. Moreover, the memory cell selection and control circuitry 38 may include a word line decoder and/or driver. For example, the memory cell selection and control circuitry 38 may include one or more different control/selection techniques (and circuitry therefrom) to select and/or enable one or more predetermined memory cells 12. Notably, all such control/selection techniques, and circuitry therefrom, whether now known or later developed, are intended to fall within the scope of the present disclosure.

In an exemplary embodiment, the semiconductor memory device 10 may implement a two step write operation whereby all the memory cells 12 in a row of memory cells 12 may be written to a predetermined data state by first executing a "clear" or a logic low (e.g., binary "0" data state) write operation, whereby all of the memory cells 12 in the row of memory cells 12 are written to logic low (e.g., binary "0" data state). Thereafter, selected memory cells 12 in the row of memory cells 12 may be selectively written to the predetermined data state (e.g., a logic high (binary "1" data state)). The semiconductor memory device 10 may also implement a one step write operation whereby selected memory cells 12 in a row of memory cells 12 may be selectively written to either a logic high (e.g., binary "1" data state) or a logic low (e.g., binary "0" data state) without first implementing a "clear" operation. The semiconductor memory device 10 may employ any of the exemplary writing, preparation, holding, refresh, and/or reading techniques described herein.

The memory cells 12 may comprise N-type, P-type and/or both types of transistors. Circuitry that is peripheral to the memory cell array 20 (for example, sense amplifiers or comparators, row and column address decoders, as well as line drivers (not illustrated herein)) may also include P-type and/or N-type transistors. Regardless of whether P-type or N-

type transistors are employed in memory cells 12 in the memory cell array 20, suitable voltage potentials (for example, positive or negative voltage potentials) for reading from the memory cells 12 will be described further herein.

5 Referring to Figure 2, there is shown a cross-sectional view of a memory cell 12 of the memory cell array 20 in accordance with an embodiment of the present disclosure. The memory cell 12 may be implemented in a vertical configuration having various regions. For example, the memory cell 12 may 10 comprise an N+ source region 120, a P- body region 122, and a P+ drain region 124. The N+ source region 120, the P- body region 122, and/or the P+ drain region 124 may be disposed in a sequential contiguous relationship, and may extend vertically from a plane defined by a P- substrate 130. In an 15 exemplary embodiment, the P- body region 122 may be an electrically floating body region of the memory cell 12 configured to accumulate/store charges, and may be spaced apart from and capacitively coupled to the plurality of word lines (WL) 28.

20 The N+ source region 120 of the memory cell 12 may be coupled to a corresponding source line (EN) 32. In an exemplary embodiment, the N+ source region 120 may be formed of a semiconductor material (e.g., silicon) comprising donor impurities. For example, the N+ source region 120 may be 25 formed of a silicon material doped with phosphorous or arsenic impurities. In an exemplary embodiment, the N+ source region 120 may be formed of a silicon material doped with phosphorous or arsenic having a concentration of 10^{20} atoms/cm^3.

In an exemplary embodiment, the source line (EN) 32 may 30 be formed of a metal material. In another exemplary embodiment, the source line (EN) 32 may be formed of a polycide material (e.g., a combination of a metal material and a silicon material). In other exemplary embodiments, the source line (EN) 32 may be formed of an N+ doped silicon

layer. The source line (EN) 32 may provide a predetermined voltage potential to the memory cells 12 of the memory cell array 20. For example, the source line (EN) 32 may be coupled to a plurality of memory cells 12 (e.g., a column or a row of memory cell array 20). The source line (EN) 32 may be configured on sides of the N+ source region 120.

The P- body region 122 of the memory cell 12 may be capacitively coupled to a corresponding word lines (WL) 28. In an exemplary embodiment, the P- body region 122 may have a first portion and a second portion formed of an undoped semiconductor material (e.g., intrinsic silicon). In an exemplary embodiment, the P- body region 122 may be formed of a semiconductor material (e.g., silicon) comprising acceptor impurities. The P- body region 122 may be formed of a silicon material doped with boron impurities. In an exemplary embodiment, the P- body region 122 may be formed of a silicon material with acceptor impurities having a concentration of 10^{15} atoms/cm^3.

The word lines (WL) 28 may be capacitively coupled the P-body region 122. The word lines (WL) 28 may be oriented in a row direction of the memory cell array 20 and coupled to a plurality of memory cells 12. The word lines (WL) 28 may be arranged on the sides of the memory cells 12 (e.g., memory cells 12 located on a row direction of the memory cell array 20). The word lines (WL) 28 may be capacitively coupled to the first portion of the P- body region 122. The first portion and the second portion of the P- body region 122 may be different portions of the P- body region 122. For example, the word lines (WL) 28 may be arranged on at least two side portions of the memory cells 12.

For example, the word lines (WL) 28 may be formed of a polycide material (e.g., a combination of a metal material and a silicon material), a metal material, and/or a combination of a polycide material and a metal material. In another

exemplary embodiment, the word lines (WL) 28 may be formed of a P+ doped silicon material. In an exemplary embodiment, each of the word lines (WL) 28 may include a plurality of layers formed of different materials. For example, each of the word lines (WL) 28 may include a layer formed above the polycide layer to couple the polycide layer to a voltage/current source of the memory cell selection and control circuitry 38.

The bit line (CN) 30 may be coupled to a second portion of the P- body region 122. The bit line (CN) 30 may be formed of a metal material. In another exemplary embodiment, the bit line (CN) 30 may be formed of a polycide material (e.g., a combination of a metal material and a silicon material). In other exemplary embodiments, the bit line (CN) 30 may be formed of an N+ doped silicon layer. For example, the source line (EN) 32 may be coupled to a plurality of memory cells 12. The bit line (CN) 30 may be configured on sides of the second portion of the P- body region 122.

The P+ drain region 124 of the memory cell 12 may be coupled to a corresponding carrier injection line (EP) 34. In an exemplary embodiment, the P+ drain region 124 of the memory cell 12 may be formed of a semiconductor material (e.g., silicon) comprising acceptor impurities. For example, the P+ drain region 124 may be formed of a silicon material doped with boron impurities. In an exemplary embodiment, the P+ drain region 124 may be doped with acceptor impurities having a concentration of 10^{20} atom/cm^3.

In an exemplary embodiment, the carrier injection line (EP) 34 may be formed of a polycide material. In another exemplary embodiment, the carrier injection line (EP) 34 may be formed of a metal material. The carrier injection line (EP) 34 may extend vertically in a column direction of the memory cell array 20 and may couple to a plurality of memory cells 12 (e.g., a column of memory cells 12). The carrier injection line (EP) 34 may be formed of a metal material. In

another exemplary embodiment, the carrier injection line (EP) 34 may be formed of a polycide material (e.g., a combination of a metal material and a silicon material). In other exemplary embodiments, the carrier injection line (EP) 34 may be formed of an N+ doped silicon layer.

In an exemplary embodiment, the P- substrate 130 may be made of a semiconductor material (e.g., silicon) comprising acceptor impurities and may form a base of the memory cell array 20. For example, the P- substrate 130 may be made of a semiconductor material comprising boron impurities. In an exemplary embodiment, the P- substrate 130 may be made of silicon comprising boron impurities having a concentration of 10^{15} atoms/cm^3. In alternative exemplary embodiments, a plurality of P- substrates 130 may form the base of the memory cell array 20 or a single P- substrate 130 may form the base of the memory cell array 20. Also, the P- substrate 130 may be made in the form of a P-well substrate.

Referring to Figure 3, there is shown a cross-sectional view of a memory cell 12 of the memory cell array 20 in accordance with an alternative embodiment of the present disclosure. The memory cell 12 may comprise an N+ source region 120 coupled to a corresponding source line (EN) 32, a P- body region 122 capacitively coupled to a plurality of word lines (WL) 28, and a P+ drain region 124 coupled to a corresponding carrier injection line (EP) 34. The N+ source region 120, the P- body region 122, and/or the P+ drain region 124 may be disposed in a sequential contiguous relationship, and may extend vertically from a plane defined by a P- substrate 130. In an exemplary embodiment, the P- body region 122 may be an electrically floating body region of the memory cell 12 configured to accumulate/store charges, and may be spaced apart from and capacitively coupled to the plurality of word lines (WL) 28.

The N+ source region 120 of the memory cell 12 may be

coupled to a corresponding source line (EN) 32. In an exemplary embodiment, the N+ source region 120 may be formed of a semiconductor material (e.g., silicon) comprising donor impurities. For example, the N+ source region 120 may be formed of a silicon material doped with phosphorous or arsenic impurities. In an exemplary embodiment, the N+ source region 120 may be formed of a silicon material doped with phosphorous or arsenic having a concentration of 10^{20} atoms/cm^3.

In an exemplary embodiment, the source line (EN) 32 may be formed of a metal material. In another exemplary embodiment, the source line (EN) 32 may be formed of a polycide material (e.g., a combination of a metal material and a silicon material). In other exemplary embodiments, the source line (EN) 32 may be formed of an N+ doped silicon layer. The source line (EN) 32 may provide a predetermined voltage potential to the memory cells 12 of the memory cell array 20. For example, the source line (EN) 32 may be coupled to a plurality of memory cells 12 (e.g., a column or a row of memory cell array 20). The source line (EN) 32 may be configured on sides of the N+ source region 120.

The P- body region 122 of the memory cell 12 may be capacitively coupled to a plurality of corresponding word lines (WL) 28. In an exemplary embodiment, the P- body region 122 may have a first portion and a second portion formed of an undoped semiconductor material (e.g., intrinsic silicon). In an exemplary embodiment, the P- body region 122 may be formed of a semiconductor material (e.g., silicon) comprising acceptor impurities. The P- body region 122 may be formed of a silicon material doped with boron impurities. In an exemplary embodiment, the P- body region 122 may be formed of a silicon material with acceptor impurities having a concentration of 10^{15} atoms/cm^3.

The plurality of word lines (WL) 28 may be capacitively coupled the P- body region 122. The plurality of word lines

(WL) 28 may be oriented in a row direction of the memory cell array 20 and coupled to a plurality of memory cells 12. The plurality of word lines (WL) 28 may include a first word line (WL1) 28a capacitively coupled to a first portion of the P- body region 122 and a second word line (WL2) 28b capacitively coupled to a second portion of the P- body region 122. The first portion and the second portion of the P- body region 122 may be different portions of the P- body region 122. The plurality of word lines (WL) 28 may be arranged on a side portion of the memory cells 12 (e.g., memory cells 12 located on a row direction of the memory cell array 20). In an exemplary embodiment, the first word line (WL1) 28a and the second word line (WL2) 28b may be configured on the same side of the P- body region 122. In another exemplary embodiment, the first word line (WL1) 28a and the second word line (WL2) 28b may be configured on opposite sides of the P- body region 122.

For example, the word lines (WL) 28 may be formed of a polycide material (e.g., a combination of a metal material and a silicon material), a metal material, and/or a combination of a polycide material and a metal material. In another exemplary embodiment, the word lines (WL) 28 may be formed of a P+ doped silicon material. In an exemplary embodiment, each of the word lines (WL) 28 may include a plurality of layers formed of different materials. For example, each of the word lines (WL) 28 may include a layer formed above the polycide layer to couple the polycide layer to a voltage/current source of the memory cell selection and control circuitry 38.

The bit line (CN) 30 may be coupled to a second portion of the P- body region 122. The bit line (CN) 30 may be configured on a side of the second portion of the P- body region 122. For example, the bit line (CN) 30 may be configured on the opposite side of the second portion of the P- body region 122 from the second word line (WL2) 28b. The

bit line (CN) 30 may be formed of a metal material. In another exemplary embodiment, the bit line (CN) 30 may be formed of a polycide material (e.g., a combination of a metal material and a silicon material). In other exemplary embodiments, the bit line (CN) 30 may be formed of an N+ doped silicon layer. For example, the source line (EN) 32 may be coupled to a plurality of memory cells 12.

The P+ drain region 124 of the memory cell 12 may be coupled to a corresponding carrier injection line (EP) 34. In an exemplary embodiment, the P+ drain region 124 of the memory cell 12 may be formed of a semiconductor material (e.g., silicon) comprising acceptor impurities. For example, the P+ drain region 124 may be formed of a silicon material doped with boron impurities. In an exemplary embodiment, the P+ drain region 124 may be doped with acceptor impurities having a concentration of 10^{20} atom/cm^3.

In an exemplary embodiment, the carrier injection line (EP) 34 may be formed of a polycide material. In another exemplary embodiment, the carrier injection line (EP) 34 may be formed of a metal material. The carrier injection line (EP) 34 may extend vertically in a column direction of the memory cell array 20 and may couple to a plurality of memory cells 12 (e.g., a column of memory cells 12). The carrier injection line (EP) 34 may be formed of a metal material. In another exemplary embodiment, the carrier injection line (EP) 34 may be formed of a polycide material (e.g., a combination of a metal material and a silicon material). In other exemplary embodiments, the carrier injection line (EP) 34 may be formed of an N+ doped silicon layer.

In an exemplary embodiment, the P- substrate 130 may be made of a semiconductor material (e.g., silicon) comprising acceptor impurities and may form a base of the memory cell array 20. For example, the P- substrate 130 may be made of a semiconductor material comprising boron impurities. In an

exemplary embodiment, the P- substrate 130 may be made of silicon comprising boron impurities having a concentration of 10^{15} atoms/cm^3. In alternative exemplary embodiments, a plurality of P- substrates 130 may form the base of the memory cell array 20 or a single P- substrate 130 may form the base of the memory cell array 20. Also, the P- substrate 130 may be made in the form of a P-well substrate.

Referring to Figure 4, there is shown a schematic diagram of a memory cell 12 of the memory cell array 20 in accordance with an embodiment of the present disclosure. The memory cell 12 may comprise a first bipolar transistor 14a and a second bipolar transistor 14b coupled to each other. For example, the first bipolar transistor 14a and/or the second bipolar transistor 14b may be an NPN bipolar transistor or a PNP bipolar transistor. The first bipolar transistor 14a may be an NPN bipolar transistor and the second bipolar transistor 14b may be a PNP bipolar transistor. In another exemplary embodiment, the first memory transistor 14a may be a PNP bipolar transistor and the second memory transistor 14b may be an NPN bipolar transistor. The memory cell 12 may be coupled to a respective word line (WL) 28, a respective bit line (CN) 30, a respective source line (EN) 32, and/or a respective carrier injection line (EP) 34. Data may be written to or read from a selected memory cell 12 by applying suitable control signals to a selected word line (WL) 28, a selected bit line (CN) 30, a selected source line (EN) 32, and/or a selected carrier injection line (EP) 34. In an exemplary embodiment, the word line (WL) 28 may extend horizontally parallel to the carrier injection line (EP) 34.

The respective bit line (CN) 30 may be coupled to a data sense amplifier circuit of the data write and sense circuitry 36 and/or a constant power source 402 (e.g., a voltage potential source and a current source). For example, the respective bit line (CN) 30 may be coupled to the data write

and sense circuitry 36 via a decoupling resistor 40. The decoupling resistor 40 may have a predetermined resistance in order to lower a barrier voltage potential of the junction between the second portion of the P- body region 122 and the P+ drain region 124 during various operations (e.g., read or write operations). In an exemplary embodiment, the decoupling resistor 40 may have a predetermined resistance to generate a current between a current that may represent a logic low (e.g., binary "0" data state) and a current that may represent a logic high (e.g., binary "0" data state). In another exemplary embodiment, the decoupling resistor 40 may have a predetermined resistance to generate a 0.5 voltage potential drop. One or more control signals may be applied to one or more selected memory cells 12 via a selected word line (WL) 28, a selected bit line (CN) 30, a selected source line (EN) 32, and/or a selected carrier injection line (EP) 34. A voltage potential and/or a current may be generated by the one or more selected memory cells 12 and outputted to the data sense amplifier circuit of the data write and sense circuitry 36 via a corresponding bit line (CN) 30 and the decoupling resistor 40.

Also, a data state may be written to one or more selected memory cells 12 by applying one or more control signals via one or more corresponding word line (WL) 28, source line (EN) 32, and/or carrier injection line (EP) 34. The one or more control signals applied via the corresponding word line (WL) 28 and/or carrier injection line (EP) 34 may control the second bipolar transistor 14b of the memory cell 12 in order to write a desired data state to the memory cell 12. In the event that a data state is read from and/or written to the memory cell 12 via the word line (WL) and/or the carrier injection line (EP) 34, then the bit line (CN) 30 may be coupled to the data sense amplifier circuit of the data write and sense circuitry 36 while the source line (EN) 32 may be

separately coupled to an electrical ground (Vss) of the data write and sense circuitry 36. In an exemplary embodiment, the data sense amplifier circuit of the data write and sense circuitry 36 and the voltage/current source of the data write and sense circuitry 36 may be configured on opposite sides of the memory cell array 20. In another exemplary embodiment, the data write and sense circuitry 36 may include a plurality of data sense amplifier circuits configured on opposite sides of the memory cell array 20.

Referring to Figure 5, there is shown a schematic diagram of at least a portion of a memory cell array 20 having a plurality of memory cells 12 as shown in Figure 4 in accordance with an embodiment of the present disclosure. As discussed above, the memory cell 12 may comprise a first bipolar transistor 14a and a second bipolar transistor 14b coupled to each other. The first bipolar transistor 14a may be an NPN bipolar transistor and the second bipolar transistor 14b may be a PNP bipolar transistor. The memory cell 12 may be coupled to a respective word line (WL) 28, a respective bit line (CN) 30, a respective source line (EN) 32, and/or a respective carrier injection line (EP) 34. The respective bit line (CN) 30 may be coupled to a data sense amplifier circuit of the data write and sense circuitry 36. For example, the respective bit line (CN) 30 may be coupled to the data write and sense circuitry 36 via a decoupling resistor 40.

As illustrated in Figure 5, the plurality of memory cells 12 may be coupled to a constant power source 402 (e.g., voltage potential source or current source) via the bit line (CN) 30 and the decoupling resistor 40. In an exemplary embodiment, a plurality of rows and columns of memory cells 12 of the memory cell array 20 may be coupled to the constant power source 402. It may be appreciated by one skilled in the art that the number of rows and columns of memory cells 12 coupled to the constant power source 402 may vary, for example

symmetrical, but not limited to, four rows by four columns, sixteen rows by sixteen columns, thirty-two rows by thirty-two columns, sixty-four rows by sixty-four columns, etc. Also, the number of rows and columns of memory cells 12 coupled to 5 the constant power source 402 may be asymmetrical, for example, but not limited to, four rows by two columns, eight rows by four columns, sixteen rows by thirty-two columns, etc.

In an exemplary embodiment, memory cells 12 may be written using a two step operation wherein a given row of 10 memory cells 12 are written to a first predetermined data state by first executing a "clear" operation (e.g., all the memory cells 12 of a selected row are written or programmed to logic low (binary "0" date state)). In particular, the first portion of the P- body region 122 of each memory cell 12 of a 15 selected row is controlled to store a majority charge carrier having a concentration that corresponds to a logic low (binary "0" data state). Thereafter selected memory cells 12 may be written to a second predetermined data state (e.g., a selective write operation to the second predetermined data 20 state, logic high (binary "1" data state)). For example, the first portion of the P- body region 122 of the memory cell 12 may be controlled to store a majority charge carrier having a concentration that corresponds to a logic high (e.g., binary "1" data state).

25 Referring to Figure 6, there are shown control signal voltage waveforms for performing various operations on memory cells 12 as shown in Figure 5 in accordance with an embodiment of the present disclosure. For example, the various operations may include control signals configured to perform a 30 write logic low (e.g., binary "0" data state) operation, a read operation, a write logic high (e.g., binary "1" data state) operation, and/or a refresh operation. Prior to performing various operations, the control signals may be configured to perform a hold operation in order to maintain a

data state (e.g., a logic high (binary "1" data state) or a logic low (binary "0" data state)) stored in the memory cell 12. In particular, the control signals may be configured to perform a hold operation in order to maximize a retention time of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in the memory cell 12. Also, the control signals for the hold operation may be configured to eliminate or reduce activities or field (e.g., electrical fields between junctions which may lead to leakage of charges) within the memory cell 12. In an exemplary embodiment, during a hold operation, a negative voltage potential may be applied to the word line (WL) 28 that may be capacitively coupled to one or more portions of the P- body region 122 of the memory cell 12 while a constant voltage potential may be applied to the second portion of the P- body region 122 via the bit line (CN) 30 and the decoupling resistor 40. The voltage potentials applied to other regions (e.g., the N+ source region 120 and/or P+ drain region 124) may be maintained at 0V.

For example, the negative voltage potential applied to the word line (WL) 28 (e.g., capacitively coupled to the P- region 122 of the memory cell 12) may be -2.0V. The constant voltage potential applied to the second portion of the P- body region 122 via the bit line (CN) 30 and the decoupling resistor 40 may be 1.4V. During the hold operation, the junction between the N+ source region 120 and first portion of the P- body region 122 and the junction between the P+ drain region 124 and the second portion of the P- body region 122 may be reverse biased in order to retain a data state (e.g., a logic high (binary "1" data state) or a logic low (binary "0" data state)) stored in the memory cell 12.

In an exemplary embodiment, control signals may be configured to perform one or more write logic low (e.g., binary "0" data state) operations to one or more selected

memory cells 12. For example, the write logic low (e.g., binary "0" data state) operation may be performed to one or more selected memory cells 12 in order to deplete charge carriers that may have accumulated/stored in the P- body regions 122 of the one or more selected memory cells 12. Various voltage potentials may be applied to the various regions of the memory cell 12. In an exemplary embodiment, the voltage potentials applied to the N+ source region 120 may be coupled to an electrical ground (Vss) and the P+ drain region 124 may be maintained at 0V. The constant voltage potential of 1.4V may be applied to the second portion of the P- body region 122 via the decoupling resistor 40. The voltage potential applied to the word line (WL) 28 that may be capacitively coupled to a first portion of the P- body region 122 may be raised from a voltage potential applied during the hold operation. In an exemplary embodiment, the voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be raised to 0.5V.

Under such biasing, the junction between the N+ source region 120 and the first portion of the P- body region 122 and the junction between the first portion of the P- body region 122 and the second portion of the P- body region 122 may be forward biased. The junction between the second portion of the P- body region 122 and the P+ drain region 124 may be reverse biased. The majority charge carriers (e.g., holes) that may have accumulated/stored in the first portion of the P- body region 122 may flow to the second portion of the P- body region 122 and lower a voltage potential barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124. Also, the majority charge carrier (e.g., holes) that may have accumulated/stored in the first portion of the P- body region 122 may flow to the N+ source region 120. Thus, the majority charge carriers (e.g.,

hole) that may have accumulated/stored in first portion of the P- body region 122 may be depleted via the second portion of the P- body region 122 and/or the N+ source region 120. By removing the majority charge carriers that may have accumulated/stored in first portion of the P- body region 122, a logic low (e.g., binary "0" data state) may be written to the memory cell 12.

In an exemplary embodiment, control signals may be configured to perform a read operation of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in one or more selected memory cells 12 of one or more selected rows of the memory cell array 20. The controls signals may be also configured to perform a refresh operation of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in one or more selected memory cells 12 of the one or more selected rows of the memory cell array 20. In an exemplary embodiment, the control signals may be configured to perform a read operation and a refresh operation simultaneously.

The control signals may be configured to a predetermined voltage potential to implement a read operation via the bit line (CN) 30 and/or a refresh operation. In an exemplary embodiment, the N+ source region 120 may be coupled to an electrical ground (Vss) via the source line (EN) 32 and the constant voltage potential applied to bit line (CN) 30 to the second portion of the P- body region 122 via the decoupling resistor 40 (e.g., a 0.5V drop) may be maintained at 1.4V. The voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 and the voltage potential applied to the P+ drain region 124 may be raised from the voltage potentials applied during the hold operation. In an exemplary embodiment, the voltage potential applied to the word line

(WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be raised to -1.0V. The voltage potential applied to the P+ drain region 124 via the carrier injection line (EP) 34 may be raised to 1.4V.

5 Under such biasing, when a logic low (e.g., binary "0" data state) is stored in the memory cell 12, the predetermined amount of majority charge carriers (e.g., holes) accumulated/stored in the first portion of the P- body region 122 may flow toward the second portion of the P- body region 10 122. The predetermined amount of majority charge carriers flown to the second portion of the P- body region 122 may lower a voltage potential at the second portion of the P- body region 122. Also, the predetermined amount of majority charge carriers flown to the second portion of the P- body region 122 15 may lower the voltage potential barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124. However, the junction between the second portion of the P- body region 122 and the P+ drain region 124 may remain reverse biased or become weakly forward biased 20 (e.g., above a reverse bias voltage and below a forward bias threshold voltage potential). A small amount of voltage potential and current or no voltage potential and current (e.g., compared to a reference voltage potential or current) may be generated when the junction between the second portion 25 of the P- body region 122 and the P+ drain region 124 is reverse biased or weakly forward biased. A data sense amplifier in the data write and sense circuitry 36 may detect the small amount of voltage potential or current (e.g., compared to a reference voltage potential or current) or no 30 voltage potential or current via the bit line (CN) 30 coupled to the second portion of the P- body region 122.

Simultaneously to the read operation, the control signals may be configured to perform a refresh operation. Under the biasing during the read operation, the junction between the

first portion of the P- body region 122 and the N+ source region 120 may be forward biased. A predetermined amount of residual majority charge carriers (e.g., holes) accumulated/stored in the first portion of the P- body region 122 may be depleted from the first portion of the P- body region 122. Also, as discussed above, a predetermined amount of majority charge carriers (e.g., holes) accumulated/stored in the first portion of the P- body region 122 may flow from the first portion of the P- body region 122 to the second portion of the P- body region 122 and thus lowering the voltage potential at the second portion of the P- body region 122. Thus, the majority charge carriers (e.g., holes) accumulated/stored in the first portion of the P- body region 122 may be depleted from the first portion of the P- body region 122 and a logic low (e.g., binary "0" data state) may be refreshed.

In an exemplary embodiment, control signals may be configured to write a logic high (e.g., binary "1" data state) to one or more selected memory cells 12 of one or more selected rows of the memory cell array 20. For example, the write logic high (e.g., binary "1" data state) operation may be performed on one or more selected rows of the memory cell array 20 or the entire memory cell array 20. In another exemplary embodiment, a write logic high (e.g., binary "1" data state) operation may have control signals configured to cause accumulation/storage of majority charge carriers in the P- body region 122.

In an exemplary embodiment, a voltage potential applied to the N+ source region 120 of the memory cell 12 may be coupled to an electrical ground (Vss) via the source line (EN) 32 and a constant voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 of the memory cells 12 via the decoupling resistor 40 (e.g., 0.5V drop) may be maintained at the same voltage potential as the

voltage potential during the hold operation. For example, a voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 may be maintained at 1.4V.

5 The voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 and the voltage potential applied to P+ drain region 124 may be raised from the voltage potentials applied during the hold operation. For example, the voltage 10 potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be raised to 0.5V from -2.0V. The voltage potential applied to the P+ drain region 124 via the carrier injection line (EP) 34 may be raised to 1.4V from 0V.

15 Under such biasing, the junction between the N+ source region 120 and the first portion of the P- body region 122, the junction between the first portion of the P- body region 122 and the second portion of the P- body region 122, and the junction between the second portion of the P- body region 122 20 and the P+ drain region 124 may become forward biased. For example, the majority charge carriers (e.g., holes) at the first portion of the P- body region 122 may flow toward the second portion of the P- body region 122. The flow of majority charge carriers to the second portion of the P- body 25 region 122 may lower a voltage potential at the second portion of the P- body region 122 and thus lowering a voltage potential barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124. The junction between the second portion of the P- body region 122 30 and the P+ drain region 124 may become forward biased (e.g., above a forward bias threshold voltage potential). Additional majority charge carriers (e.g., holes) may flow through the forward biased junction between the P+ drain region 124 and the second portion of the P- body region 122 toward the first

portion of the P- body region 122. Subsequently, the voltage potential applied on the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be lowered to -2.0V from 0.5V. Thu, a predetermined amount of majority charge carriers (e.g., holes) may be accumulated/stored in the first portion of the P- body region 122 via the P+ drain region 124 and the second portion of the P- body region 122. The predetermined amount of charge carriers accumulated/stored in the first portion (e.g., capacitively coupled to word line (WL) 28) of the P- body region 122 may represent that a logic high (e.g., binary "1" data state) may be written in the memory cell 12.

Again, the control signals may be configured to perform a second read operation of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in one or more selected memory cells 12 of one or more selected rows of the memory cell array 20. The controls signals may be also configured to perform a refresh operation of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in one or more selected memory cells 12 of the one or more selected rows of the memory cell array 20. In an exemplary embodiment, the control signals may be configured to perform a read operation and a refresh operation simultaneously.

The control signals may be configured to a predetermined voltage potential to implement a read operation via the bit line (CN) 30 and/or a refresh operation. In an exemplary embodiment, the N+ source region 120 may be coupled to an electrical ground (Vss) via the source line (EN) 32 and the constant voltage potential applied to the bit line (CN) 30 to second portion of the P- body region 122 via the decoupling resistor 40 (e.g., a 0.5V drop) may be maintained at 1.4V. The voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P-

body region 122 and the voltage potential applied to the P+ drain region 124 may be raised from the voltage potentials applied during the hold operation. In an exemplary embodiment, the voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be raised to -1.0V. The voltage potential applied to the P+ drain region 124 via the carrier injection line (EP) 34 may be raised to 1.4V.

Under such biasing, when a logic high (e.g., binary "1" data state) is stored in the memory cell 12, the predetermined amount of majority charge carriers (e.g., that may represent a logic high (e.g., binary "1" data state)) accumulated/stored in the first portion of the P- body region 122 may flow toward the second portion of the P- body region 122. The predetermined amount of majority charge carriers flown to the second portion of the P- body region 122 may lower a voltage potential at the second portion of the P- body region 122. The predetermined amount of majority charge carriers flown to the second portion of the P- body region 122 may lower the voltage potential barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124. The junction between the second portion of the P- body region 122 and the P+ drain region 124 may be forward biased (e.g., above a forward bias threshold voltage potential). A predetermined amount of voltage potential and/or current may be generated when the junction between the second portion of the P- body region 122 and the P+ drain region 124 is forward biased. A data sense amplifier in the data write and sense circuitry 36 may detect the generated voltage potential or current (e.g., compared to a reference voltage potential or current) via the bit line (CN) 30 and the decoupling resistor 40 coupled to the second portion of the P- body region 122.

Simultaneously to the read operation, the control signals may be configured to perform a refresh operation. Under the

biasing during the read operation, the junction between the second portion of the P- body region 122 and the P+ drain region 124 may be forward biased. A predetermined amount of majority charge carriers (e.g., holes) may flow from the P+ drain region 124 to the first portion of the P- body region 122 via the second portion of the P- body region 122. The flow of predetermined amount of majority charge carriers from the P+ drain region 124 may gradually lower the voltage potential at the P+ drain region 124. Also, the junction between first portion of the P- body region 122 and the N+ source region 120 may be forward biased and thus a predetermined amount of electrons may flow from the N+ source region 120 to the first portion of the P- body region 122. The flow of electrons may facilitate the flow of majority charge carriers (e.g., holes) to the first portion of the P- body region 122. The voltage potential applied to the word line (WL) 28 (e.g., that may be capacitively coupled to the first portion of the P- body region 122) may be lowered from -1.0V to -2.0V and thus a predetermined amount of majority charge carriers may be accumulated/stored in the first portion of the P- body region 122. Thus, the predetermined amount of majority charge carriers (e.g., holes) accumulated/stored in the first portion of the P- body region 122 may be restored to the first portion of the P- body region 122 and a logic low (e.g., binary "0" data state) may be refreshed.

Referring to Figure 7, there is shown a schematic diagram of a memory cell 12 of the memory cell array 20 in accordance with an alternate embodiment of the present disclosure. The memory cell 12 illustrated in Figure 7 may be similar to the memory cell 12 illustrated in Figure 4, except that the bit line (CN) 30 may be coupled to the carrier injection line (EP) 34 via the decoupling resistor 40. The voltage potential applied to the bit line (CN) 30 may be associated with the voltage potential applied to the carrier injection line (EP)

34. For example, the voltage potential applied to the bit line (CN) 30 may be equal to the voltage potential applied to the carrier injection line (EP) 34 minus the voltage potential drop at the decoupling resistor (R0) 40.

5 The respective bit line (CN) 30 may be coupled to a data sense amplifier circuit of the data write and sense circuitry 36. For example, the respective bit line (CN) 30 may be coupled to the data write and sense circuitry 36 via a decoupling resistor 40. The decoupling resistor 40 may have a 10 predetermined resistance in order to lower a barrier voltage potential of the junction between the second portion of the P- body region 122 and the P+ drain region 124 during various operations (e.g., read or write operations). In an exemplary embodiment, the decoupling resistor 40 may have a resistance 15 so that the voltage potential and/or current generated by the selected memory cells 12 may lower an energy barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124.

Referring to Figure 8, there is shown a schematic diagram 20 of at least a portion of a memory cell array 20 having a plurality of memory cells 12 as shown in Figure 7 in accordance with an alternative embodiment of the present disclosure. The memory cell array 20 illustrated in Figure 8 may be similar to the memory cell array 20 illustrated in 25 Figure 5, except that the bit line (CN) 30 may be coupled to the carrier injection line (EP) 34 via the decoupling resistor 40. As discussed above, the memory cell 12 may be coupled to a respective word line (WL) 28, a respective bit line (CN) 30, a respective source line (EN) 32, and/or a respective carrier 30 injection line (EP) 34. The respective bit line (CN) 30 may be coupled to a data sense amplifier circuit of the data write and sense circuitry 36. For example, the respective bit line (CN) 30 may be coupled to the data write and sense circuitry 36 via the decoupling resistor 40.

As illustrated in Figure 8, the plurality of memory cells 12 configured in a column direction of the memory cell array 20 may be coupled to the respective carrier injection line (EP) 34. The bit lines (CN) 30 of the plurality of memory cells 12 configured in a column direction of the memory cell array 20 may be coupled to a respective carrier injection line (EP) 34 via the respective decoupling resistors 40.

Referring to Figure 9, there are shown control signal voltage waveforms for performing various operations on memory cells 12 as shown in Figure 8 in accordance with an embodiment of the present disclosure. For example, the various operations may include control signals configured to perform a write logic low (e.g., binary "0" data state) operation, a read operation, a write logic high (e.g., binary "1" data state) operation, and/or a refresh operation. Prior to performing various operations, the control signals may be configured to perform a hold operation in order to maintain a data state (e.g., a logic high (binary "1" data state) or a logic low (binary "0" data state)) stored in the memory cell 12. In particular, the control signals may be configured to perform a hold operation in order to maximize a retention time of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in the memory cell 12. Also, the control signals for the hold operation may be configured to eliminate or reduce activities or field (e.g., electrical fields between junctions which may lead to leakage of charges) within the memory cell 12. In an exemplary embodiment, during a hold operation, a negative voltage potential may be applied to the word line (WL) 28 that may be capacitively coupled to one or more portions of the P- body region 122 of the memory cell 12 while a constant voltage potential may be applied to the bit line (CN) 30 to the second portion of the P- body region 122 via the decoupling resistor 40. The voltage potentials applied to other regions (e.g.,

the N+ source region 120 and/or P+ drain region 124) may be maintained at 0V.

For example, the negative voltage potential applied to the word line (WL) 28 (e.g., capacitively coupled to the P- region 122 of the memory cell 12) may be -2.0V. The constant voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 may be 1.4V. During the hold operation, the junction between the N+ source region 120 and first portion of the P- body region 122 and the junction between the P+ drain region 124 and the second portion of the P- body region 122 may be reverse biased in order to retain a data state (e.g., a logic high (binary "1" data state) or a logic low (binary "0" data state)) stored in the memory cell 12.

In an exemplary embodiment, control signals may be configured to perform one or more write logic low (e.g., binary "0" data state) operations to one or more selected memory cells 12. For example, the write logic low (e.g., binary "0" data state) operation may be performed to one or more selected memory cells 12 in order to deplete charge carriers that may have accumulated/stored in the P- body regions 122 of the one or more selected memory cells 12. Various voltage potentials may be applied to the various regions of the memory cell 12. In an exemplary embodiment, the voltage potentials applied to the N+ source region 120 may be coupled to an electrical ground (Vss) and voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 and the P+ drain region 124 may be maintained the same as the voltage potential applied during the hold operation. The voltage potential applied to the word line (WL) 28 that may be capacitively coupled to a first portion of the P- body region 122 may be raised from a voltage potential applied during the hold operation. In an exemplary embodiment, the voltage potential applied to the P+ drain

region 124 and the bit line (CN) 30 to the second portion of the P- body region 122 may be maintained at 0V. The voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be raised to 0.5V from -2.0V.

Under such biasing, the junction between the N+ source region 120 and the first portion of the P- body region 122 and the junction between the first portion of the P- body region 122 and the second portion of the P- body region 122 may be forward biased. The junction between the second portion of the P- body region 122 and the P+ drain region 124 may be reverse biased. The majority charge carriers (e.g., holes) that may have accumulated/stored in the first portion of the P- body region 122 may flow to the second portion of the P- body region 122 and lower a voltage potential barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124. Also, the majority charge carrier (e.g., holes) that may have accumulated/stored in the first portion of the P- body region 122 may flow to the N+ source region 120. Thus, the majority charge carriers (e.g., hole) that may have accumulated/stored in first portion of the P- body region 122 may be depleted via the second portion of the P- body region 122 and/or the N+ source region 120. By removing the majority charge carriers that may have accumulated/stored in first portion of the P- body region 122, a logic low (e.g., binary "0" data state) may be written to the memory cell 12.

In an exemplary embodiment, control signals may be configured to perform a read operation of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in one or more selected memory cells 12 of one or more selected rows of the memory cell array 20. The controls signals may be also configured to perform a refresh operation of a data state (e.g., a logic low (binary

"0" data state) and/or a logic high (binary "1" data state)) stored in one or more selected memory cells 12 of the one or more selected rows of the memory cell array 20. In an exemplary embodiment, the control signals may be configured to perform a read operation and a refresh operation simultaneously.

The control signals may be configured to a predetermined voltage potential to implement a read operation via the bit line (CN) 30 and/or a refresh operation. In an exemplary embodiment, the N+ source region 120 may be coupled to an electrical ground (Vss) via the source line (EN) 32. The voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122, the voltage potential applied to the P+ drain region 124, the voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 may be raised from the voltage potentials applied during the hold operation. The voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 via the decoupling resistor 40 may be based at least in part on the voltage potential applied to the P+ drain region 124. In an exemplary embodiment, the voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be raised to -1.0V. The voltage potential applied to the P+ drain region 124 via the carrier injection line (EP) 34 may be raised to 1.4V. The voltage potential applied to the bit line (CN) 30 may be 1.4V or 0.9V at the second portion of the P- body region 122 after a 0.5V drop across the decoupling resistor 40.

Under such biasing, when a logic low (e.g., binary "0" data state) is stored in the memory cell 12, the predetermined amount of majority charge carriers (e.g., holes) accumulated/stored in the first portion of the P- body region

122 may flow toward the second portion of the P- body region 122. The predetermined amount of majority charge carriers (e.g., represent a logic low (e.g., binary "0" data state)) flown to the second portion of the P- body region 122 may lower a voltage potential at the second portion of the P- body region 122. Also, the predetermined amount of majority charge carriers flown to the second portion of the P- body region 122 may lower the voltage potential barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124. However, the junction between the second portion of the P- body region 122 and the P+ drain region 124 may remain reverse biased or become weakly forward biased (e.g., above a reverse bias voltage and below a forward bias threshold voltage potential). A small amount of voltage potential and current or no voltage potential and current (e.g., compared to a reference voltage potential or current) may be generated when the junction between the second portion of the P- body region 122 and the P+ drain region 124 is reverse biased or weakly forward biased. A data sense amplifier in the data write and sense circuitry 36 may detect the small amount of voltage potential or current (e.g., compared to a reference voltage potential or current) or no voltage potential or current via the bit line (CN) 30 coupled to the second portion of the P- body region 122.

Simultaneously to the read operation, the control signals may be configured to perform a refresh operation. Under the biasing during the read operation, the junction between the first portion of the P- body region 122 and the N+ source region 120 may be forward biased. A predetermined amount of residual majority charge carriers (e.g., holes) accumulated/stored in the first portion of the P- body region 122 may be depleted from the first portion of the P- body region 122 via the N+ source region 120. Also, as discussed above, a predetermined amount of majority charge carriers

(e.g., holes) accumulated/stored in the first portion of the P- body region 122 may flow from the first portion of the P- body region 122 to the second portion of the P- body region 122 and thus lowering the voltage potential at the second portion of the P- body region 122. Thus, the majority charge carriers (e.g., holes) accumulated/stored in the first portion of the P- body region 122 may be depleted from the first portion of the P- body region 122 and a logic low (e.g., binary "0" data state) may be refreshed.

In an exemplary embodiment, control signals may be configured to write a logic high (e.g., binary "1" data state) to one or more selected memory cells 12 of one or more selected rows of the memory cell array 20. For example, the write logic high (e.g., binary "1" data state) operation may be performed on one or more selected rows of the memory cell array 20 or the entire memory cell array 20. In another exemplary embodiment, a write logic high (e.g., binary "1" data state) operation may have control signals configured to cause accumulation/storage of majority charge carriers in the P- body region 122.

In an exemplary embodiment, a voltage potential applied to the N+ source region 120 of the memory cell 12 may be coupled to an electrical ground (Vss) via the source line (EN) 32. The voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122, the voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122, the voltage potential applied to P+ drain region 124 may be raised from the voltage potentials applied during the hold operation. For example, the voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be raised to 0.5V from -2.0V. The voltage potential applied to the P+ drain region 124 via the carrier injection line (EP) 34 may be

raised to 1.4V from 0V. The voltage potential applied to the bit line (CN) 30 may be raised to 1.4V or 0.9V at the second portion of the P- body region 122 after a 0.5V drop across the decoupling resistor 40.

5 Under such biasing, the junction between the N+ source region 120 and the first portion of the P- body region 122, the junction between the first portion of the P- body region 122 and the second portion of the P- body region 122 and the junction between the second portion of the P- body region 122 10 and the P+ drain region 124 may become forward biased. For example, the majority charge carriers (e.g., holes) at the first portion of the P- body region 122 may flow toward the second portion of the P- body region 122. The flow of majority charge carriers to the second portion of the P- body 15 region 122 may lower a voltage potential at the second portion of the P- body region 122 and thus lowering a voltage potential barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124. The junction between the second portion of the P- body region 122 20 and the P+ drain region 124 may become forward biased (e.g., above a forward bias threshold voltage potential). Additional majority charge carriers (e.g., holes) may flow through the forward biased junction between the P+ drain region 124 and the second portion of the P- body region 122 toward the first 25 portion of the P- body region 122. Subsequently, the voltage potential applied on the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be lowered to -2.0V from 0.5V. Thu, a predetermined amount of majority charge carriers (e.g., holes) 30 may be accumulated/stored in the first portion of the P- body region 122 via the P+ drain region 124 and the second portion of the P- body region 122. The predetermined amount of charge carriers accumulated/stored in the first portion of the P- body region 122 may represent that a logic high (e.g., binary

"1" data state) may be written in the memory cell 12.

Again, the control signals may be configured to perform a second read operation of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in one or more selected memory cells 12 of one or more selected rows of the memory cell array 20. The controls signals may be also configured to perform a refresh operation of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in one or more selected memory cells 12 of the one or more selected rows of the memory cell array 20. In an exemplary embodiment, the control signals may be configured to perform a read operation and a refresh operation simultaneously.

The control signals may be configured to a predetermined voltage potential to implement a read operation via the bit line (CN) 30 and/or a refresh operation. In an exemplary embodiment, the N+ source region 120 may be coupled to an electrical ground (Vss) via the source line (EN) 32. The voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122, the voltage potential applied to the P+ drain region 124, and the voltage potential applied to the first portion of the P- body region 122 may be raised from the voltage potentials applied during the hold operation. In an exemplary embodiment, the voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be raised to -1.0V. The voltage potential applied to the P+ drain region 124 via the carrier injection line (EP) 34 may be raised to 1.4V. The voltage potential applied to the bit line (CN) 30 may be raised to 1.4V or 0.9V at the second portion of the P- body region 122 after a 0.5V drop across the decoupling resistor 40.

Under such biasing, when a logic high (e.g., binary "1"

data state) is stored in the memory cell 12, the predetermined amount of majority charge carriers (e.g., that may represent a logic high (e.g., binary "1" data state)) accumulated/stored in the first portion of the P- body region 122 may flow toward the second portion of the P- body region 122. The predetermined amount of majority charge carriers flown to the second portion of the P- body region 122 may lower a voltage potential at the second portion of the P- body region 122. The predetermined amount of majority charge carriers flown to the second portion of the P- body region 122 may lower the voltage potential barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124. The junction between the second portion of the P- body region 122 and the P+ drain region 124 may be forward biased (e.g., above a forward bias threshold voltage potential). A predetermined amount of voltage potential and/or current may be generated when the junction between the second portion of the P- body region 122 and the P+ drain region 124 is forward biased. A data sense amplifier in the data write and sense circuitry 36 may detect the generated voltage potential or current (e.g., compared to a reference voltage potential or current) at the second portion of the P- body region 122 via the bit line (CN) 30 and the decoupling resistor 40 coupled to the second portion of the P- body region 122.

Simultaneously to the read operation, the control signals may be configured to perform a refresh operation. Under the biasing during the read operation, the junction between the second portion of the P- body region 122 and the P+ drain region 124 may be forward biased. A predetermined amount of majority charge carriers (e.g., holes) may flow from the P+ drain region 124 to the first portion of the P- body region 122 via the second portion of the P- body region 122. The flow of predetermined amount of majority charge carriers from the P+ drain region 124 may gradually lower the voltage

potential at the P+ drain region 124. The voltage potential at the second portion of the P- body region 122 may be also gradually lowered. Also, the junction between first portion of the P- body region 122 and the N+ source region 120 may be forward biased and thus a predetermined amount of electrons may flow from the N+ source region 120 to the first portion of the P- body region 122. The flow of electrons may facilitate the flow of majority charge carriers (e.g., holes) to the first portion of the P- body region 122. The voltage potential applied to the word line (WL) 28 (e.g., that may be capacitively coupled to the first portion of the P- body region 122) may be lowered from -1.0V to -2.0V and thus a predetermined amount of majority charge carriers may be accumulated/stored in the first portion of the P- body region 122. Thus, the predetermined amount of majority charge carriers (e.g., holes) accumulated/stored in the first portion of the P- body region 122 may be restored to the first portion of the P- body region 122 and a logic low (e.g., binary "0" data state) may be refreshed.

Referring to Figure 10, there is shown a schematic diagram of a memory cell 12 of the memory cell array 20 in accordance with an alternate embodiment of the present disclosure. The memory cell 12 illustrated in Figure 10 may be similar to the memory cell 12 illustrated in Figure 4, except that the carrier injection line (EP) 34 may be coupled to a constant power source 1002 (e.g., a voltage potential source and/or a current source). Various control signals may be applied to the memory cell 12 via the bit line (CN) 30 and the decoupling resistor 40 in order to properly bias the memory cell 12 to perform various operations (e.g., read or write operations).

The respective bit line (CN) 30 may be coupled to a data sense amplifier circuit of the data write and sense circuitry 36. For example, the respective bit line (CN) 30 may be

coupled to the data write and sense circuitry 36 via a decoupling resistor 40. The decoupling resistor 40 may have a predetermined resistance in order to lower a barrier voltage potential of the junction between the second portion of the P- body region 122 and the P+ drain region 124 during various operations (e.g., read or write operations). In an exemplary embodiment, the decoupling resistor 40 may have a resistance so that the voltage potential and/or current generated by the selected memory cells 12 may lower an energy barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124.

Referring to Figure 11, there is shown a schematic diagram of at least a portion of a memory cell array 20 having a plurality of memory cells 12 as shown in Figure 10 in accordance with an alternative embodiment of the present disclosure. The memory cell array 20 illustrated in Figure 11 may be similar to the memory cell array 20 illustrated in Figure 5, except that the carrier injection line (EP) 34 may be coupled to the constant power source 1002. In an exemplary embodiment, a plurality of rows and columns of memory cells 12 of the memory cell array 20 may be coupled to the constant power source 1002. It may be appreciated by one skilled in the art that the number of rows and columns of memory cells 12 coupled to the constant power source 1002 may vary, for example symmetrical, but not limited to, four rows by four columns, sixteen rows by sixteen columns, thirty-two rows by thirty-two columns, sixty-four rows by sixty-four columns, etc. Also, the number of rows and columns of memory cells 12 coupled to the constant power source 1002 may be asymmetrical, for example, but not limited to, four rows by two columns, eight rows by four columns, sixteen rows by thirty-two columns, etc.

As discussed above, the memory cell 12 may be coupled to a respective word line (WL) 28, a respective bit line (CN) 30,

a respective source line (EN) 32, and/or a respective carrier injection line (EP) 34. The respective bit line (CN) 30 may be coupled to a data sense amplifier circuit of the data write and sense circuitry 36. For example, the respective bit line (CN) 30 may be coupled to the data write and sense circuitry 36 via the decoupling resistor 40. Also, various control signals may be applied to the memory cells 12 via the bit line (CN) 30 in order to properly bias the memory cells 12 to perform various operations.

Referring to Figure 12, there are shown control signal voltage waveforms for performing a refresh operation on memory cells 12 as shown in Figure 11 in accordance with an alternate embodiment of the present disclosure. For example, the refresh operation may include control signals configured to perform one or more operations. In an exemplary embodiment, the refresh operation may include control signals to perform a write logic low (e.g., binary "0" data state) operation, a read operation, a write logic high (e.g., binary "1" data state) operation, and/or a read operation. Prior to performing a refresh operation, the control signals may be configured to perform a hold operation in order to maintain a data state (e.g., a logic high (binary "1" data state) or a logic low (binary "0" data state)) stored in the memory cell 12. In particular, the control signals may be configured to perform a hold operation in order to maximize a retention time of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in the memory cell 12. Also, the control signals for the hold operation may be configured to eliminate or reduce activities or field (e.g., electrical fields between junctions which may lead to leakage of charges) within the memory cell 12. In an exemplary embodiment, during a hold operation, a negative voltage potential may be applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P-

body region 122 of the memory cell 12, while a positive voltage potential may be applied to the bit line (CN) 30 to the second portion of the P- body region 122 and/or the P+ drain region 124. The voltage potentials applied to the N+ 5 source region 120 may be coupled to an electrical ground (Vss). For example, the negative voltage potential applied to the word line (WL) 28 (e.g., capacitively coupled to the P- region 122 of the memory cell 12) may be -2.0V. The positive voltage potential applied to the first portion of the P- body 10 region 122 may be 1.4V. Also, the positive voltage potential applied to the P+ drain region 124 may be 1.4V. During the hold operation, the junction between the N+ source region 120 and first portion of the P- body region 122 and the junction between the P+ drain region 124 and the second portion of the 15 P- body region 122 may be reverse biased in order to retain a data state (e.g., a logic high (binary "1" data state) or a logic low (binary "0" data state)) stored in the memory cell 12.

In an exemplary embodiment, control signals may be 20 configured to perform one or more write logic low (e.g., binary "0" data state) operations to one or more selected memory cells 12. For example, the write logic low (e.g., binary "0" data state) operation may be performed to one or more selected memory cells 12 in order to deplete majority 25 charge carriers that may have accumulated/stored in the P- body regions 122 of the one or more selected memory cells 12. Various voltage potentials may be applied to the various regions of the memory cell 12. The voltage potential applied to the N+ source region 120 may be maintained at the holding 30 operation voltage potential (e.g., electrical ground (Vss)). The voltage potential applied to the P+ drain region 124 may be maintained at a constant voltage potential by the constant power source 1002 (e.g., at 1.4V). The voltage potential applied to the word line (WL) 28 that may be capacitively

coupled to a first portion of the P- body region 122 may be raised from a voltage potential applied during the hold operation. The voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 may be raised from a voltage potential applied during the hold operation. In an exemplary embodiment, the voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be raised to 0.5V from -2.0V. The voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 may be raised to 2.0V from 1.4V.

Under such biasing, the junction between the N+ source region 120 and the first portion of the P- body region 122 and the junction between the first portion of the P- body region 122 and the second portion of the P- body region 122 may be forward biased. The junction between the second portion of the P- body region 122 and the P+ drain region 124 may be reverse biased. The majority charge carriers (e.g., holes) that may have accumulated/stored in the first portion of the P- body region 122 may flow to the second portion of the P- body region 122 and lower a voltage potential barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124. Also, the majority charge carrier (e.g., holes) that may have accumulated/stored in the first portion of the P- body region 122 may flow to the N+ source region 120. Thus, the majority charge carriers (e.g., hole) that may have accumulated/stored in the first portion of the P- body region 122 may be depleted via the second portion of the P- body region 122 and/or the N+ source region 120. By removing the majority charge carriers that may have accumulated/stored in first portion of the P- body region 122, a logic low (e.g., binary "0" data state) may be written to the memory cell 12.

In an exemplary embodiment, control signals may be

configured to perform a read operation of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in one or more selected memory cells 12 of one or more selected rows of the memory cell array 20. The controls signals may be also configured to perform a refresh operation of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in one or more selected memory cells 12 of the one or more selected rows of the memory cell array 20. In an exemplary embodiment, the control signals may be configured to perform a read operation and a refresh operation simultaneously.

The control signals may be configured to a predetermined voltage potential to implement a read operation via the bit line (CN) 30 and/or a refresh operation. In an exemplary embodiment, the N+ source region 120 may be coupled to an electrical ground (Vss) via the source line (EN) 32 and the constant voltage potential applied to the P+ drain region 124 may be maintained at 1.4V. The voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 and the voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 may be raised from the voltage potentials applied during the hold operation. In an exemplary embodiment, the voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be raised to -1.0V from -2.0V. The voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 via the decoupling resistor 40 may be raised to 2.0V from 1.4V.

Under such biasing, when a logic low (e.g., binary "0" data state) is stored in the memory cell 12, the predetermined amount of majority charge carriers (e.g., holes) accumulated/stored in the first portion of the P- body region

122 may flow toward the second portion of the P- body region 122. The predetermined amount of majority charge carriers flown to the second portion of the P- body region 122 may lower a voltage potential at the second portion of the P- body region 122. Also, the predetermined amount of majority charge carriers flown to the second portion of the P- body region 122 may lower the voltage potential barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124. However, the junction between the second portion of the P- body region 122 and the P+ drain region 124 may remain reverse biased or become weakly forward biased (e.g., above a reverse bias voltage and below a forward bias threshold voltage potential). A small amount of voltage potential and current or no voltage potential and current (e.g., compared to a reference voltage potential or current) may be generated when the junction between the second portion of the P- body region 122 and the P+ drain region 124 is reverse biased or weakly forward biased. A data sense amplifier in the data write and sense circuitry 36 may detect the small amount of voltage potential or current (e.g., compared to a reference voltage potential or current) or no voltage potential or current via the bit line (CN) 30 coupled to the second portion of the P- body region 122.

Simultaneously to the read operation, the control signals may be configured to perform a refresh operation. Under the biasing during the read operation, the junction between the first portion of the P- body region 122 and the N+ source region 120 may be forward biased. A predetermined amount of residual majority charge carriers (e.g., holes) that may have accumulated/stored in the first portion of the P- body region 122 may be depleted from the first portion of the P- body region 122 via the N+ source region 120. Also, as discussed above, a predetermined amount of majority charge carriers (e.g., holes) accumulated/stored in the first portion of the

P- body region 122 may flow from the first portion of the P- body region 122 to the second portion of the P- body region 122 and thus lowering the voltage potential at the second portion of the P- body region 122. Thus, the majority charge carriers (e.g., holes) accumulated/stored in the first portion of the P- body region 122 may be depleted from the first portion of the P- body region 122 and a logic low (e.g., binary "0" data state) may be refreshed.

In an exemplary embodiment, control signals may be configured to write a logic high (e.g., binary "1" data state) to one or more selected memory cells 12 of one or more selected rows of the memory cell array 20. For example, the write logic high (e.g., binary "1" data state) operation may be performed on one or more selected rows of the memory cell array 20 or the entire memory cell array 20. In another exemplary embodiment, a write logic high (e.g., binary "1" data state) operation may have control signals configured to cause accumulation/storage of majority charge carriers in the P- body region 122.

In an exemplary embodiment, the N+ source region 120 of the memory cell 12 may be coupled to an electrical ground (Vss) via the source line (EN) 32 and a constant voltage potential applied to the P+ drain region 124 of the memory cells 12 via the carrier injection line (EP) 34 may be maintained at the same voltage potential as the voltage potential applied during the hold operation. For example, a voltage potential applied to the P+ drain region 124 may be maintained at 1.4V.

The voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be raised from the voltage potentials applied during the hold operation. For example, the voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body

region 122 may be raised to 0.5V from -2.0V. The voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 may be maintained at the same voltage potential as the voltage potential applied during the hold operation. For example, the voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 may be maintained at 1.4V.

Under such biasing, the junction between the N+ source region 120 and the first portion of the P- body region 122, the junction between the first portion of the P- body region 122 and the second portion of the P- body region 122, and the junction between the second portion of the P- body region 122 and the P+ drain region 124 may become forward biased. For example, the majority charge carriers (e.g., holes) at the first portion of the P- body region 122 may flow toward the second portion of the P- body region 122. The flow of majority charge carriers to the second portion of the P- body region 122 may lower a voltage potential at the second portion of the P- body region 122 and thus lowering a voltage potential barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124. The junction between the second portion of the P- body region 122 and the P+ drain region 124 may become forward biased (e.g., above a forward bias threshold voltage potential). Additional majority charge carriers (e.g., holes) may flow through the forward biased junction between the P+ drain region 124 and the second portion of the P- body region 122 toward the first portion of the P- body region 122. Subsequently, the voltage potential applied on the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be lowered to -2.0V from 0.5V. Thu, a predetermined amount of majority charge carriers (e.g., holes) may be accumulated/stored in the first portion of the P- body region 122 via the P+ drain region 124 and the second portion

of the P- body region 122. The predetermined amount of charge carriers accumulated/stored in the first portion (e.g., capacitively coupled to word line (WL) 28 of the P- body region 122 may represent that a logic high (e.g., binary "1" data state) may be written in the memory cell 12.

Again, the control signals may be configured to perform a second read operation of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in one or more selected memory cells 12 of one or more selected rows of the memory cell array 20. The controls signals may be also configured to perform a refresh operation of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in one or more selected memory cells 12 of the one or more selected rows of the memory cell array 20. In an exemplary embodiment, the control signals may be configured to perform a read operation and a refresh operation simultaneously.

The control signals may be configured to a predetermined voltage potential to implement a read operation via the bit line (CN) 30 and/or a refresh operation. In an exemplary embodiment, the N+ source region 120 may be coupled to an electrical ground (Vss) via the source line (EN) 32 and the constant voltage potential applied to the P+ drain region 124 via the carrier injection line (EP) 34 may be maintained at 1.4V. Also, the voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 may be maintained at 1.4V. The voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be raised from the voltage potentials applied during the hold operation. In an exemplary embodiment, the voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be raised to -1.0V. The voltage potential applied to the P+ drain region

124 via the carrier injection line (EP) 34 may be raised to 1.4V.

Under such biasing, when a logic high (e.g., binary "1" data state) is stored in the memory cell 12, the predetermined amount of majority charge carriers (e.g., that may represent a logic high (e.g., binary "1" data state)) accumulated/stored in the first portion of the P- body region 122 may flow toward the second portion of the P- body region 122. The predetermined amount of majority charge carriers flown to the second portion of the P- body region 122 may lower a voltage potential at the second portion of the P- body region 122. The predetermined amount of majority charge carriers flown to the second portion of the P- body region 122 may lower the voltage potential barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124. The junction between the second portion of the P- body region 122 and the P+ drain region 124 may be forward biased (e.g., above a forward bias threshold voltage potential). A predetermined amount of voltage potential and/or current may be generated when the junction between the second portion of the P- body region 122 and the P+ drain region 124 is forward biased. A data sense amplifier in the data write and sense circuitry 36 may detect the generated voltage potential or current (e.g., compared to a reference voltage potential or current) via the bit line (CN) 30 and the decoupling resistor 40 coupled to the second portion of the P- body region 122.

Simultaneously to the read operation, the control signals may be configured to perform a refresh operation. Under the biasing during the read operation, the junction between the second portion of the P- body region 122 and the P+ drain region 124 may be forward biased. A predetermined amount of majority charge carriers (e.g., holes) may flow from the P+ drain region 124 to the first portion of the P- body region 122 via the second portion of the P- body region 122. The

flow of predetermined amount of majority charge carriers from the P+ drain region 124 may cause a temporary lowering of the voltage potential at the P+ drain region 124. Also, the junction between first portion of the P- body region 122 and the N+ source region 120 may be forward biased and thus a predetermined amount of electrons may flow from the N+ source region 120 to the first portion of the P- body region 122. The flow of electrons may facilitate the flow of majority charge carriers (e.g., holes) to the first portion of the P- body region 122. The voltage potential applied to the word line (WL) 28 (e.g., that may be capacitively coupled to the first portion of the P- body region 122) may be lowered from -1.0V to -2.0V and thus a predetermined amount of majority charge carriers may be accumulated/stored in the first portion of the P- body region 122. Thus, the predetermined amount of majority charge carriers (e.g., holes) accumulated/stored in the first portion of the P- body region 122 may be restored to the first portion of the P- body region 122 and a logic low (e.g., binary "0" data state) may be refreshed.

Referring to Figure 13, there is shown a schematic diagram of a memory cell 12 of the memory cell array 20 in accordance with an alternate embodiment of the present disclosure. The memory cell 12 illustrated in Figure 13 may be similar to the memory cell 12 illustrated in Figure 4, except that the bit line (CN) 30 may be coupled to a variable power source via the decoupling resistor 40. For example, various control signals may be applied to the bit line (CN) 30 via the decoupling resistor 40 in order to properly bias the memory cells 12 to perform various operations.

The respective bit line (CN) 30 may be coupled to a data sense amplifier circuit of the data write and sense circuitry 36. For example, the respective bit line (CN) 30 may be coupled to the data write and sense circuitry 36 via a decoupling resistor 40. The decoupling resistor 40 may have a

predetermined resistance in order to lower a barrier voltage potential of the junction between the second portion of the P- body region 122 and the P+ drain region 124 during various operations (e.g., read or write operations). In an exemplary embodiment, the decoupling resistor 40 may have a resistance so that the voltage potential and/or current generated by the selected memory cells 12 may lower an energy barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124.

Referring to Figure 14, there is shown a schematic diagram of at least a portion of a memory cell array 20 having a plurality of memory cells 12 as shown in Figure 13 in accordance with an alternative embodiment of the present disclosure. The memory cell array 20 illustrated in Figure 14 may be similar to the memory cell array 20 illustrated in Figure 5, except that the bit line (CN) 30 may be coupled to a variable power source via the decoupling resistor 40. As discussed above, the memory cell 12 may be coupled to a respective word line (WL) 28, a respective bit line (CN) 30, a respective source line (EN) 32, and/or a respective carrier injection line (EP) 34. The respective bit line (CN) 30 may be coupled to a data sense amplifier circuit of the data write and sense circuitry 36. For example, the respective bit line (CN) 30 may be coupled to the data write and sense circuitry 36 via the decoupling resistor 40. The plurality of memory cells 12 configured in a row direction of the memory cell array 20 may be coupled to a respective carrier injection line (EP) 34.

Referring to Figure 15, there are shown control signal voltage waveforms for performing various operations on memory cells 12 as shown in Figure 14 in accordance with an embodiment of the present disclosure. For example, the various operations may include control signals configured to perform a write logic low (e.g., binary "0" data state)

operation, a write logic high (e.g., binary "1" data state) operation, a read operation, and/or a refresh operation. Prior to performing various operations, the control signals may be configured to perform a hold operation in order to maintain a data state (e.g., a logic high (binary "1" data state) or a logic low (binary "0" data state)) stored in the memory cell 12. In particular, the control signals may be configured to perform a hold operation in order to maximize a retention time of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in the memory cell 12. Also, the control signals for the hold operation may be configured to eliminate or reduce activities or field (e.g., electrical fields between junctions which may lead to leakage of charges) within the memory cell 12. In an exemplary embodiment, during a hold operation, a negative voltage potential may be applied to the word line (WL) 28 that may be capacitively coupled to one or more portions of the P- body region 122 of the memory cell 12. The voltage potentials applied to other regions (e.g., the N+ source region 120 and/or P+ drain region 124) may be maintained at 0V.

For example, the negative voltage potential applied to the word line (WL) 28 (e.g., capacitively coupled to the P- region 122 of the memory cell 12) may be -2.0V. During the hold operation, the junction between the N+ source region 120 and first portion of the P- body region 122 and the junction between the P+ drain region 124 and the second portion of the P- body region 122 may be reverse biased in order to retain a data state (e.g., a logic high (binary "1" data state) or a logic low (binary "0" data state)) stored in the memory cell 12.

Control signals may be configured to perform one or more write logic low (e.g., binary "0" data state) operations to one or more selected memory cells 12. In an exemplary

embodiment, a write logic low (e.g., binary "0" data state) operation may be performed on one or more selected rows of memory cells 12, whereby all of the memory cells 12 in the one or more selected rows of memory cells 12 are written to logic low (e.g., binary "0" data state). Thereafter, selected memory cells 12 in the one or more selected rows of memory cells 12 may be selectively written to a logic high (e.g., binary "1" data state).

For example, the write logic low (e.g., binary "0" data state) operation may be performed to one or more selected memory cells 12 in order to deplete charge carriers that may have accumulated/stored in the P- body regions 122 of the one or more selected memory cells 12. Various voltage potentials may be applied to the various regions of the memory cell 12. In an exemplary embodiment, the voltage potentials applied to the N+ source region 120 may be coupled to an electrical ground (Vss). The voltage potential applied to the word line (WL) 28 that may be capacitively coupled to a first portion of the P- body region 122 may be raised from a voltage potential applied during the hold operation. The voltage potential applied to the P+ drain region 124 and the voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 may be raised from a voltage potential applied during the hold operation. In an exemplary embodiment, the voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be raised to 0.5V from -2.0V. The voltage potential applied to the P+ drain region 124 and the voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 may be raised to 1.4V from 0V.

Under such biasing, the junction between the N+ source region 120 and the first portion of the P- body region 122 and the junction between the first portion of the P- body region

122 and the second portion of the P- body region 122 may be forward biased. The junction between the second portion of the P- body region 122 and the P+ drain region 124 may be reverse biased. The majority charge carriers (e.g., holes) that may have accumulated/stored in the first portion of the P- body region 122 may flow to the second portion of the P- body region 122 and lower a voltage potential barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124. Also, the majority charge carrier (e.g., holes) that may have accumulated/stored in the first portion of the P- body region 122 may flow to the N+ source region 120. Thus, the majority charge carriers (e.g., holes) that may have accumulated/stored in first portion of the P- body region 122 may be depleted via the second portion of the P- body region 122 and/or the N+ source region 120. By removing the majority charge carriers that may have accumulated/stored in first portion of the P- body region 122, a logic low (e.g., binary "0" data state) may be written to the memory cell 12.

Subsequent to performing a write logic low (e.g., binary "0" data state) operation, control signals may be configured to write a logic high (e.g., binary "1" data state) to one or more selected memory cells 12 of one or more selected rows of the memory cell array 20. In an exemplary embodiment, a write logic high (e.g., binary "1" data state) operation may have control signals configured to cause accumulation/storage of majority charge carriers in the P- body region 122.

In an exemplary embodiment, a voltage potential applied to the N+ source region 120 of the memory cell 12 may be coupled to an electrical ground (Vss) via the source line (EN) 32. The voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 and the voltage potential applied to P+ drain region 124 may be maintained as the same voltage

potentials applied during the write logic low (e.g., binary "0" data state) operation. For example, the voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be maintained at 0.5V. The voltage potential applied to the P+ drain region 124 via the carrier injection line (EP) 34 may be maintained at 1.4V. The voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 may be lowered from the voltage potential applied during the write logic low (e.g., binary "0" data state) operation. In an exemplary embodiment, the voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 may be lowered to 0V from 1.4V.

Under such biasing, the junction between the N+ source region 120 and the first portion of the P- body region 122, the junction between the first portion of the P- body region 122 and the second portion of the P- body region 122, and the junction between the second portion of the P- body region 122 and the P+ drain region 124 may become forward biased. For example, the majority charge carriers (e.g., holes) at the first portion of the P- body region 122 may flow toward the second portion of the P- body region 122. For example, majority charge carriers (e.g., holes) may flow through the forward biased junction between the P+ drain region 124 and the second portion of the P- body region 122 toward the first portion of the P- body region 122. Subsequently, the voltage potential applied on the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be lowered to -2.0V from 0.5V. Thu, a predetermined amount of majority charge carriers (e.g., holes) may be accumulated/stored in the first portion of the P- body region 122 via the P+ drain region 124 and the second portion of the P- body region 122. The predetermined amount of charge carriers accumulated/stored in the first portion of the P-

body region 122 may represent that a logic high (e.g., binary "1" data state) may be written in the memory cell 12.

In an exemplary embodiment, control signals may be configured to perform a read operation of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in one or more selected memory cells 12 of one or more selected rows of the memory cell array 20. The controls signals may be also configured to perform a refresh operation of a data state (e.g., a logic low (binary "0" data state) and/or a logic high (binary "1" data state)) stored in one or more selected memory cells 12 of the one or more selected rows of the memory cell array 20. In an exemplary embodiment, the control signals may be configured to perform a read operation and a refresh operation simultaneously.

The control signals may be configured to a predetermined voltage potential to implement a read operation via the bit line (CN) 30 and/or a refresh operation. In an exemplary embodiment, the N+ source region 120 may be coupled to an electrical ground (Vss) via the source line (EN) 32. The voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122, the voltage potential applied to the P+ drain region 124, the voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 may be raised from the voltage potentials applied during the hold operation. In an exemplary embodiment, the voltage potential applied to the word line (WL) 28 that may be capacitively coupled to the first portion of the P- body region 122 may be raised to -1.0V. The voltage potential applied to the P+ drain region 124 via the carrier injection line (EP) 34 may be raised to 1.4V. The voltage potential applied to the bit line (CN) 30 to the second portion of the P- body region 122 may be raised to 1.4V.

Under such biasing, when a logic low (e.g., binary "0" data state) is stored in the memory cell 12, the predetermined amount of majority charge carriers (e.g., holes) accumulated/stored in the first portion of the P- body region 122 may flow toward the second portion of the P- body region 122. The predetermined amount of majority charge carriers (e.g., represent a logic low (e.g., binary "0" data state)) flown to the second portion of the P- body region 122 may lower a voltage potential at the second portion of the P- body region 122. Also, the predetermined amount of majority charge carriers flown to the second portion of the P- body region 122 may lower the voltage potential barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124. However, the junction between the second portion of the P- body region 122 and the P+ drain region 124 may remain reverse biased or become weakly forward biased (e.g., above a reverse bias voltage and below a forward bias threshold voltage potential). A small amount of voltage potential and current or no voltage potential and current (e.g., compared to a reference voltage potential or current) may be generated when the junction between the second portion of the P- body region 122 and the P+ drain region 124 is reverse biased or weakly forward biased. A data sense amplifier in the data write and sense circuitry 36 may detect the small amount of voltage potential or current (e.g., compared to a reference voltage potential or current) or no voltage potential or current via the bit line (CN) 30 coupled to the second portion of the P- body region 122.

In another exemplary embodiment, when a logic high (e.g., binary "1" data state) is stored in the memory cell 12, the predetermined amount of majority charge carriers (e.g., that may represent a logic high (e.g., binary "1" data state)) accumulated/stored in the first portion of the P- body region 122 may flow toward the second portion of the P- body region

122. The predetermined amount of majority charge carriers flown to the second portion of the P- body region 122 may lower a voltage potential at the second portion of the P- body region 122. The predetermined amount of majority charge carriers flown to the second portion of the P- body region 122 may lower the voltage potential barrier at the junction between the second portion of the P- body region 122 and the P+ drain region 124. The junction between the second portion of the P- body region 122 and the P+ drain region 124 may be forward biased (e.g., above a forward bias threshold voltage potential). A predetermined amount of voltage potential and/or current may be generated when the junction between the second portion of the P- body region 122 and the P+ drain region 124 is forward biased. A data sense amplifier in the data write and sense circuitry 36 may detect the generated voltage potential or current (e.g., compared to a reference voltage potential or current) at the second portion of the P- body region 122 via the bit line (CN) 30 and the decoupling resistor 40 coupled to the second portion of the P- body region 122.

Simultaneously to the read operation, the control signals may be configured to perform a refresh operation. The refresh operation may refresh a data state (e.g., a logic low (e.g., binary "0" data state) or a logic high (e.g., binary "1" data state)) stored in the memory cell 12. In an exemplary embodiment, when a logic low is stored in the memory cell 12 and under the biasing during the read operation, the junction between the first portion of the P- body region 122 and the N+ source region 120 may be forward biased. A predetermined amount of residual majority charge carriers (e.g., holes) accumulated/stored in the first portion of the P- body region 122 may be depleted from the first portion of the P- body region 122 via the N+ source region 120. Also, as discussed above, a predetermined amount of majority charge carriers

(e.g., holes) accumulated/stored in the first portion of the P- body region 122 may flow from the first portion of the P- body region 122 to the second portion of the P- body region 122 and thus lowering the voltage potential at the second portion of the P- body region 122. Thus, the majority charge carriers (e.g., holes) accumulated/stored in the first portion of the P- body region 122 may be depleted from the first portion of the P- body region 122 and a logic low (e.g., binary "0" data state) may be refreshed.

In another exemplary embodiment, when a logic high (e.g., binary "1" data state) is stored in the memory cell 12 and under the biasing during the read operation, the junction between the second portion of the P- body region 122 and the P+ drain region 124 may be forward biased. A predetermined amount of majority charge carriers (e.g., holes) may flow from the P+ drain region 124 to the first portion of the P- body region 122 via the second portion of the P- body region 122. The flow of predetermined amount of majority charge carriers from the P+ drain region 124 may gradually lower the voltage potential at the P+ drain region 124. The voltage potential at the second portion of the P- body region 122 may be also gradually lowered. Also, the junction between first portion of the P- body region 122 and the N+ source region 120 may be forward biased and thus a predetermined amount of electrons may flow from the N+ source region 120 to the first portion of the P- body region 122. The flow of electrons may facilitate the flow of majority charge carriers (e.g., holes) to the first portion of the P- body region 122. The voltage potential applied to the word line (WL) 28 (e.g., that may be capacitively coupled to the first portion of the P- body region 122) may be lowered from -1.0V to -2.0V and thus a predetermined amount of majority charge carriers may be accumulated/stored in the first portion of the P- body region 122. Thus, the predetermined amount of majority charge

carriers (e.g., holes) accumulated/stored in the first portion of the P- body region 122 may be restored to the first portion of the P- body region 122 and a logic low (e.g., binary "0" data state) may be refreshed.

5 At this point it should be noted that providing techniques for refreshing a semiconductor memory device in accordance with the present disclosure as described above may involve the processing of input data and the generation of output data to some extent. This input data processing and 10 output data generation may be implemented in hardware or software. For example, specific electronic components may be employed in a semiconductor memory device or similar or related circuitry for implementing the functions associated with providing techniques for refreshing a semiconductor 15 memory device in accordance with the present disclosure as described above. Alternatively, one or more processors operating in accordance with instructions may implement the functions associated with providing techniques for refreshing a semiconductor memory device in accordance with the present 20 disclosure as described above. If such is the case, it is within the scope of the present disclosure that such instructions may be stored on one or more processor readable media (e.g., a magnetic disk or other storage medium), or transmitted to one or more processors via one or more signals 25 embodied in one or more carrier waves.

The present disclosure is not to be limited in scope by the specific embodiments described herein. Indeed, other various embodiments of and modifications to the present disclosure, in addition to those described herein, will be 30 apparent to those of ordinary skill in the art from the foregoing description and accompanying drawings. Thus, such other embodiments and modifications are intended to fall within the scope of the present disclosure. Further, although the present disclosure has been described herein in the

context of a particular implementation in a particular environment for a particular purpose, those of ordinary skill in the art will recognize that its usefulness is not limited thereto and that the present disclosure may be beneficially
5 implemented in any number of environments for any number of purposes. Accordingly, the claims set forth below should be construed in view of the full breadth and spirit of the present disclosure as described herein.

CLAIMS

1. A semiconductor memory device comprising:

a plurality of memory cells arranged in an array of rows and columns, each memory cell comprising:

5 a first region coupled to a source line;

a second region coupled to a carrier injection line;

a body region capacitively coupled to at least one word line and disposed between the first region and the second region; and

10 a decoupling resistor coupled to at least a portion of the body region.

2. The semiconductor memory device according to claim 1, wherein the first region is an N-doped region and the second
15 region is a P-doped region.

3. The semiconductor memory device according to claim 1, wherein the body region is an undoped region.

20 4. The semiconductor memory device according to claim 1, wherein the body region comprises a first portion and a second portion.

5. The semiconductor memory device according to claim 4,
25 wherein the first portion of the body region and the second portion of the body region are different portions of the body region.

6. The semiconductor memory device according to claim 4,
30 wherein the decoupling resistor is coupled to the second portion of the body region.

7. The semiconductor memory device according to claim 6, wherein the decoupling resistor is coupled to the second

portion of the body region via a bit line.

8. The semiconductor memory device according to claim 1, wherein a plurality of word lines are capacitively coupled to 5 the body region.

9. The semiconductor memory device according to claim 8, wherein the plurality of word lines are capacitively coupled to a plurality of side portions of the body region.

10

10. The semiconductor memory device according to claim 8, wherein each of the plurality of word lines are capacitively coupled to different portions on a common side of the body region.

15

11. The semiconductor memory device according to claim 8, wherein the each of the plurality of word lines are capacitively coupled to opposite side portions of the body region.

20

12. The semiconductor memory device according to claim 8, wherein the plurality of word lines comprise a first word line and a second word line.

25 13. The semiconductor memory device according to claim 12, wherein the first word line is capacitively coupled to a first portion of the body region and the second word line is capacitively coupled to a second portion of the body region.

30 14. The semiconductor memory device according to claim 1, wherein the decoupling resistor has a resistance that causes a current flow through the decoupling resistor between a current that represents a logic low and a current that represents a logic high.

15. A method for biasing a semiconductor memory device comprising the steps of:

applying a plurality of voltage potentials to a plurality of memory cells arranged in an array of rows and columns, wherein applying the plurality of voltage potentials to the plurality of memory cells comprises:

applying a first voltage potential to a first region via a respective source line of the array;

applying a second voltage potential to a second region via a respective carrier injection line of the array;

applying a third voltage potential to a first portion of a body region via at least one respective word line of the array that is capacitively coupled to the body region; and

applying a fourth voltage potential to a second portion of the body region via a respective bit line of the array and a decoupling resistor.

16. The method according to claim 15, wherein the respective source line is coupled to an electrical ground.

17. The method according to claim 16, wherein the fourth voltage potential applied to the second portion of the body region is a constant voltage potential.

18. The method according to claim 17, further comprising increasing the third voltage potential applied to the at least one respective word line during a hold operation in order to perform a write logic low operation.

19. The method according to claim 17, further comprising maintaining the second voltage potential applied to the respective carrier injection line during a hold operation in

order to perform a write logic low operation.

20. The method according to claim 17, further comprising increasing the second voltage potential applied to the respective carrier injection line and the third voltage potential applied to the at least one respective word line during a hold operation in order to perform a write logic high operation.

21. The method according to claim 17, further comprising increasing the second voltage potential applied to the respective carrier injection line and the third voltage potential applied to the at least one respective word line during a hold operation in order to perform a read operation.

22. The method according to claim 16, wherein the decoupling resistor and the respective bit line are coupled to the respective carrier injection line.

23. The method according to claim 22, further comprising increasing the third voltage potential applied to the at least one respective word line during a hold operation in order to perform a write logic low operation.

24. The method according to claim 22, further comprising maintaining the second voltage potential applied to the respective carrier injection line during a hold operation in order to perform a write logic low operation.

25. The method according to claim 22, further comprising increasing the second voltage potential applied to the respective carrier injection line and the third voltage potential applied to the at least one respective word line during a hold operation in order to perform a write logic high

operation.

26. The method according to claim 22, further comprising increasing the second voltage potential applied to the respective carrier injection line and the third voltage potential applied to the at least one respective word line during a hold operation in order to perform a read operation.

27. The method according to claim 16, wherein the second voltage potential applied to the second region is a constant voltage potential.

28. The method according to claim 27, further comprising increasing the third voltage potential applied to the at least one respective word line and the fourth voltage potential applied to the respective bit line during a hold operation in order to perform a write logic low operation.

29. The method according to claim 27, further comprising maintaining the fourth voltage potential applied to the respective bit line during a hold operation in order to perform a write logic high operation.

30. The method according to claim 27, further comprising increasing the third voltage potential applied to the at least one respective bit line during a hold operation to perform a write logic high operation.

31. The method according to claim 27, further comprising increasing the third voltage potential applied to the at least one respective word line and the fourth voltage potential applied to the respective bit line during a hold operation in order to perform a read operation.

32. The method according to claim 16, further comprising increasing the second voltage potential applied to the respective carrier injection line, the third voltage potential applied to the at least one respective word line, and the fourth voltage potential applied to the respective bit line during a hold operation in order to perform a write logic low operation.

33. The method according to claim 16, further comprising increasing the second voltage potential applied to the respective carrier injection line and the third voltage potential applied to the at least one respective word line during a hold operation in order to perform a write logic high operation.

34. The method according to claim 16, further comprising increasing the second voltage potential applied to the respective carrier injection line and the third voltage potential applied to the at least one respective word line during a hold operation in order to perform a write logic high operation.

35. The method according to claim 17, further comprising increasing the second voltage potential applied to the respective carrier injection line, the third voltage potential applied to the at least one respective word line, and the fourth voltage potential applied to the respective bit line during a hold operation in order to perform a read operation.

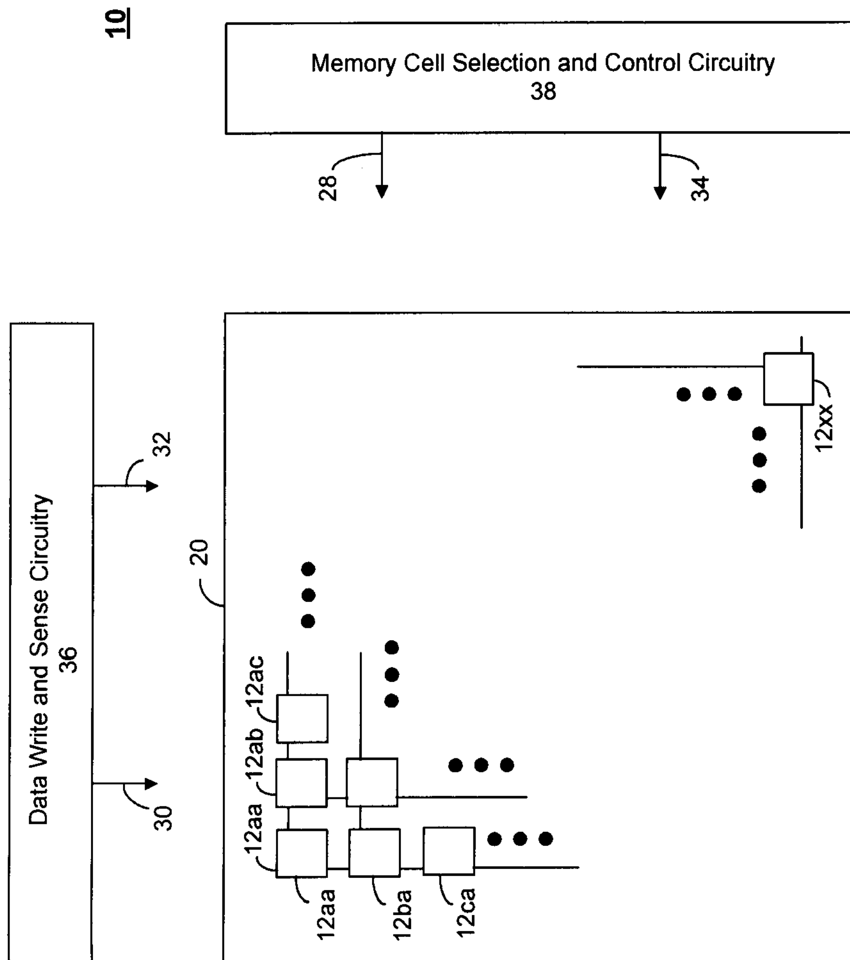

FIGURE 1

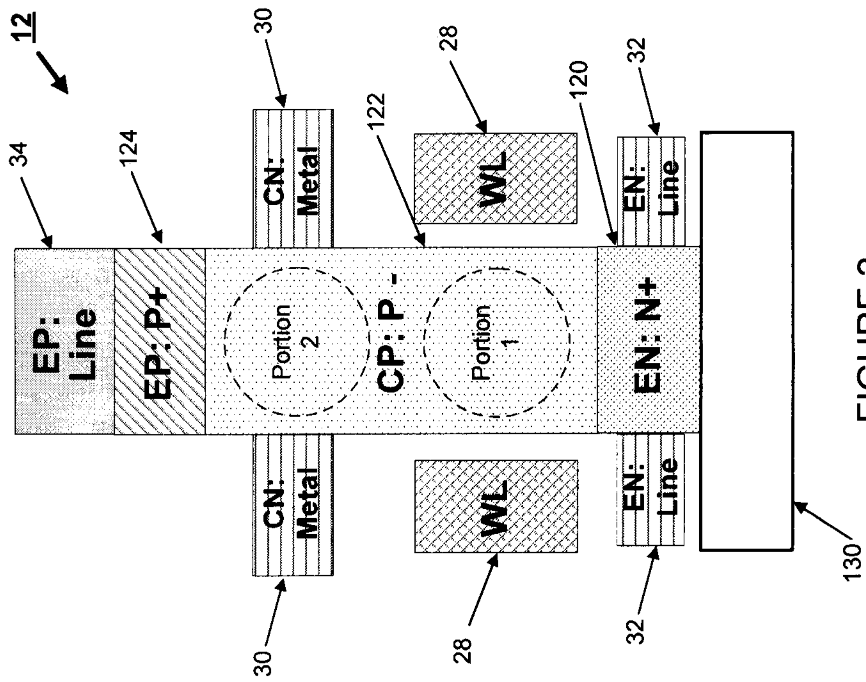

FIGURE 2

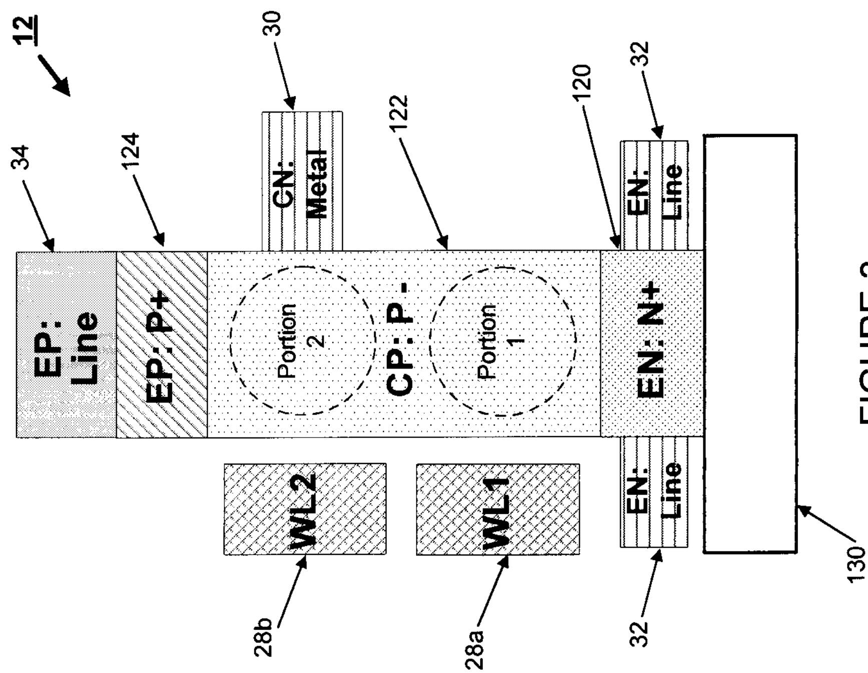

FIGURE 3

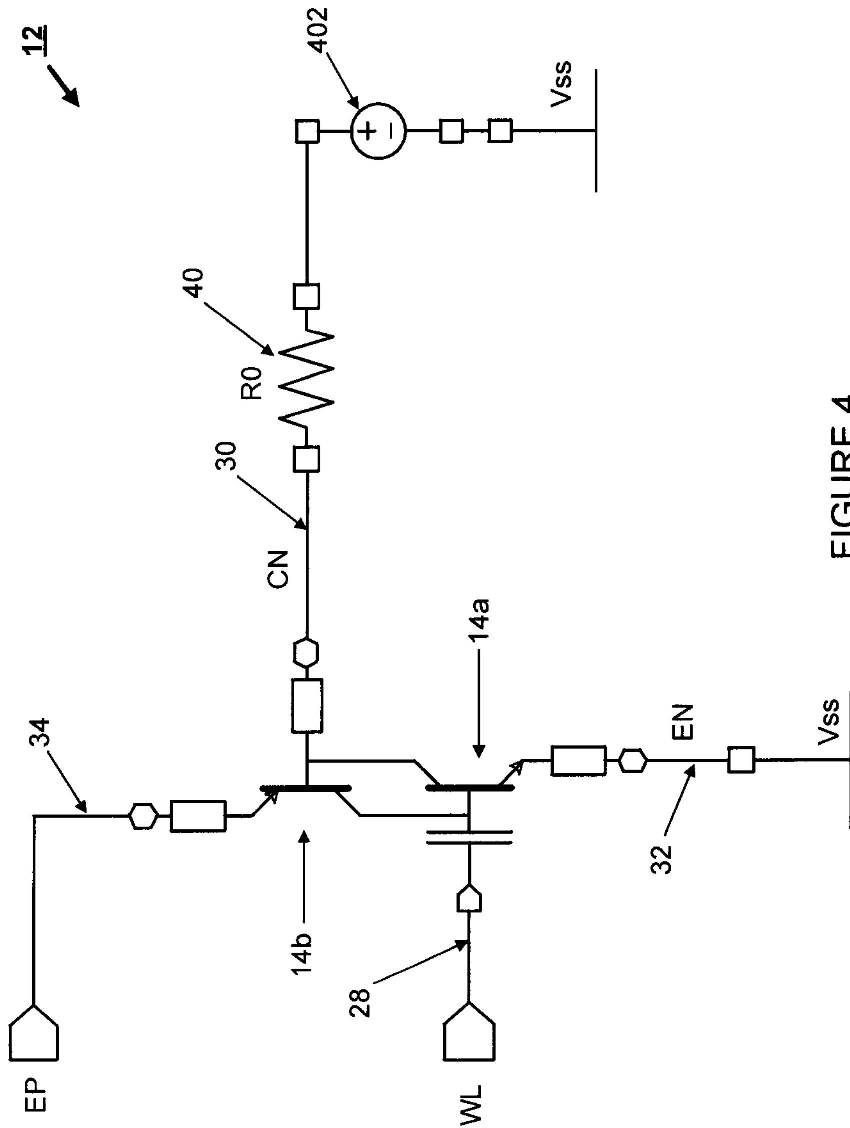

FIGURE 4

FIGURE 5

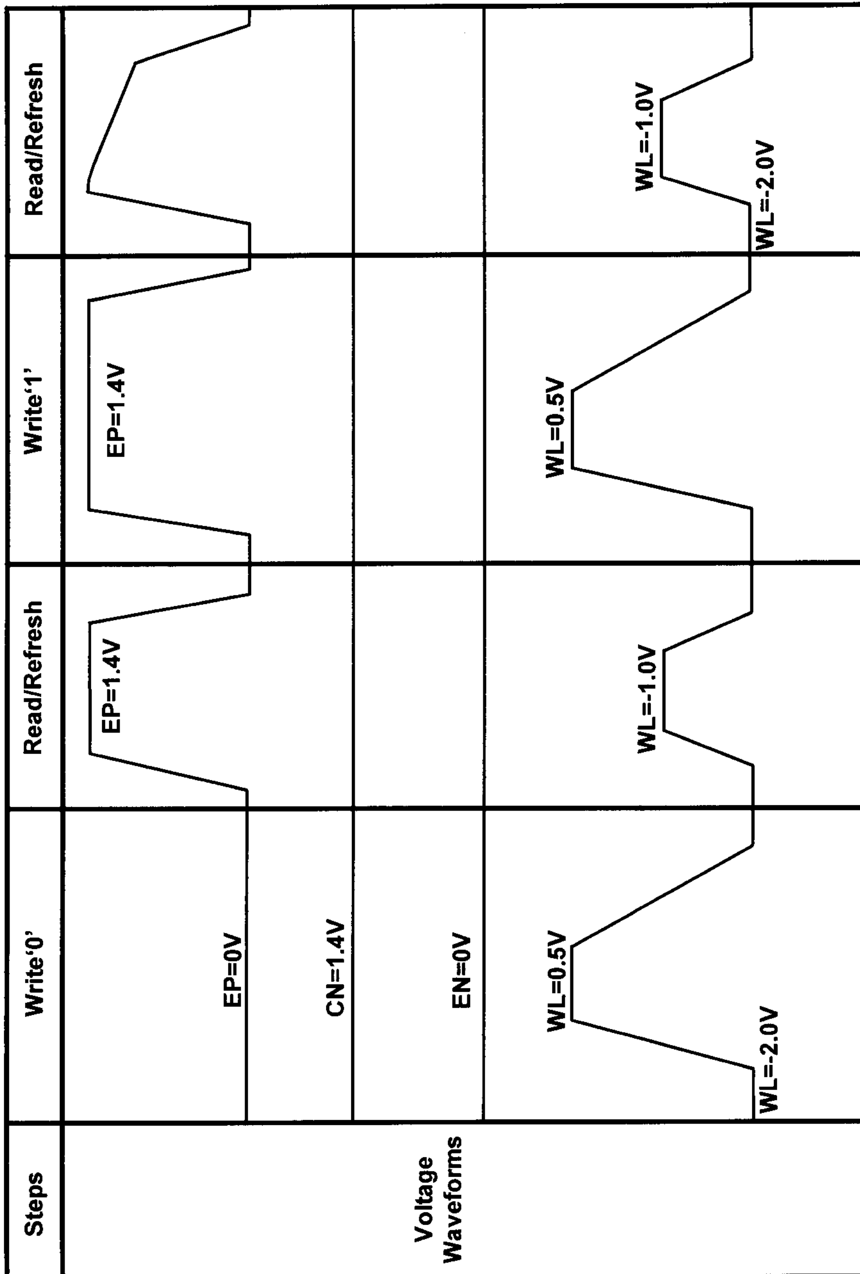

FIGURE 6

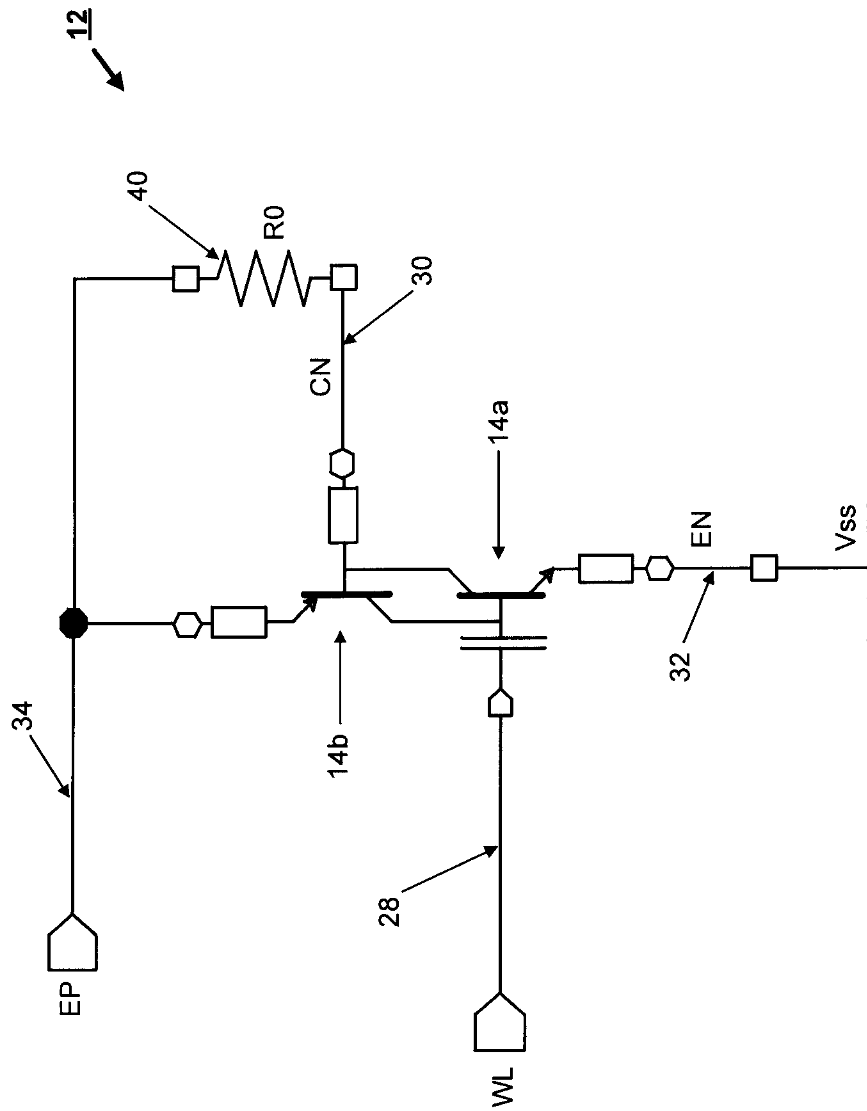

FIGURE 7

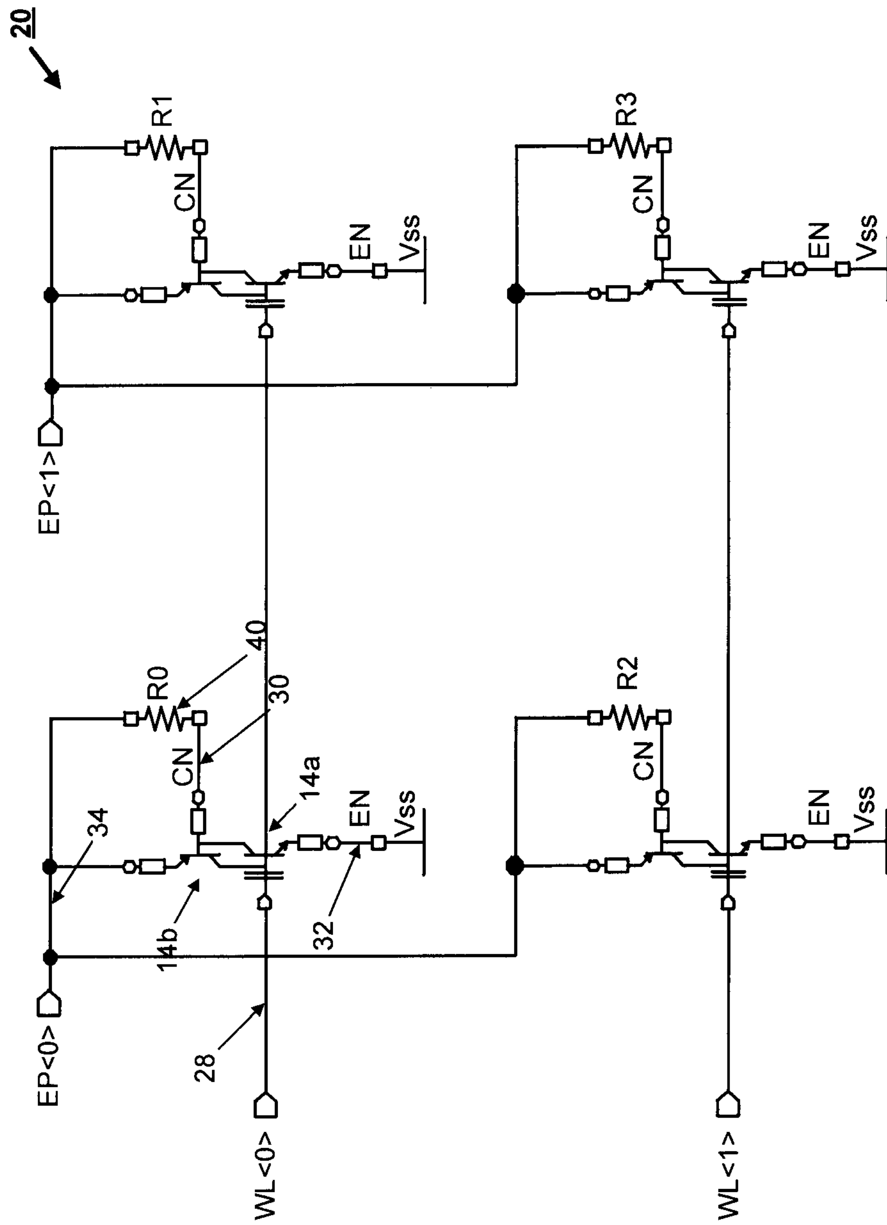

FIGURE 8

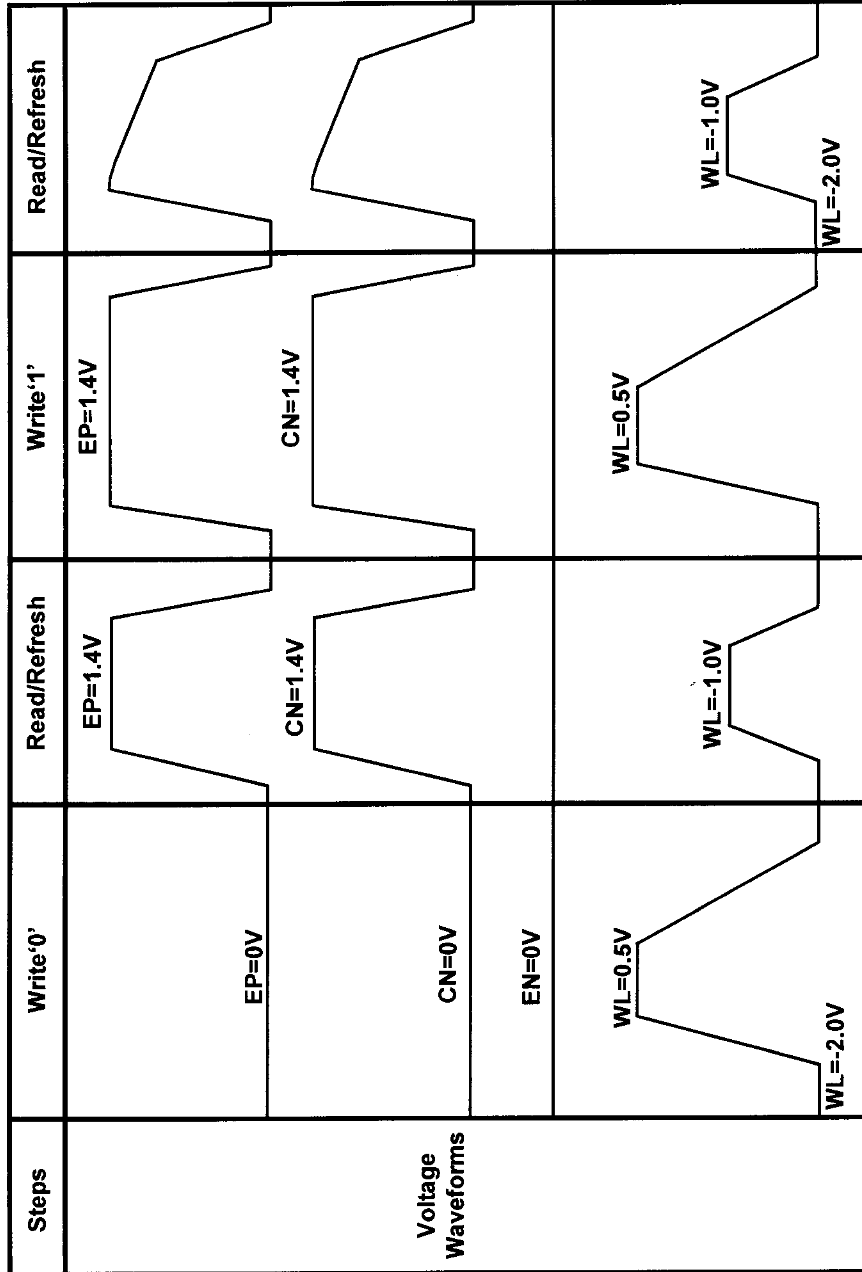

FIGURE 9

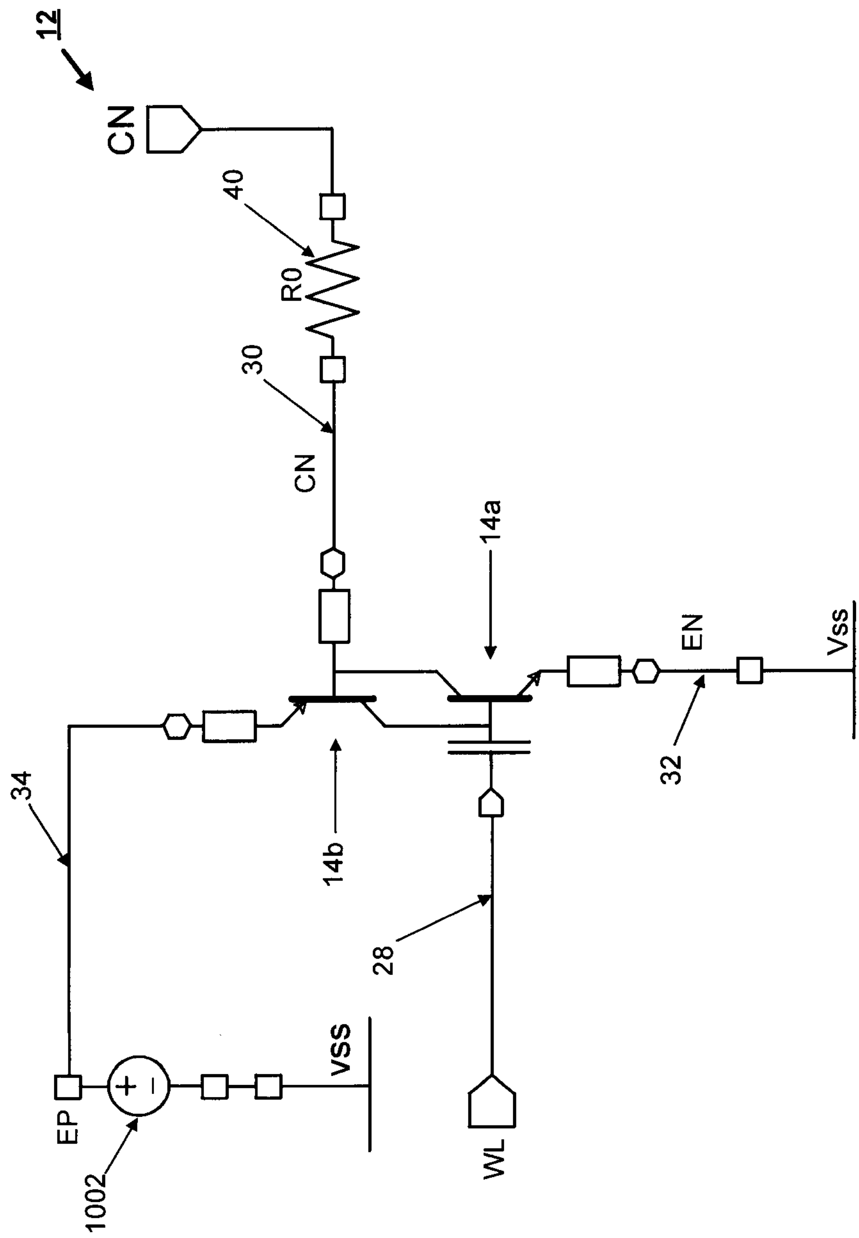

FIGURE 10

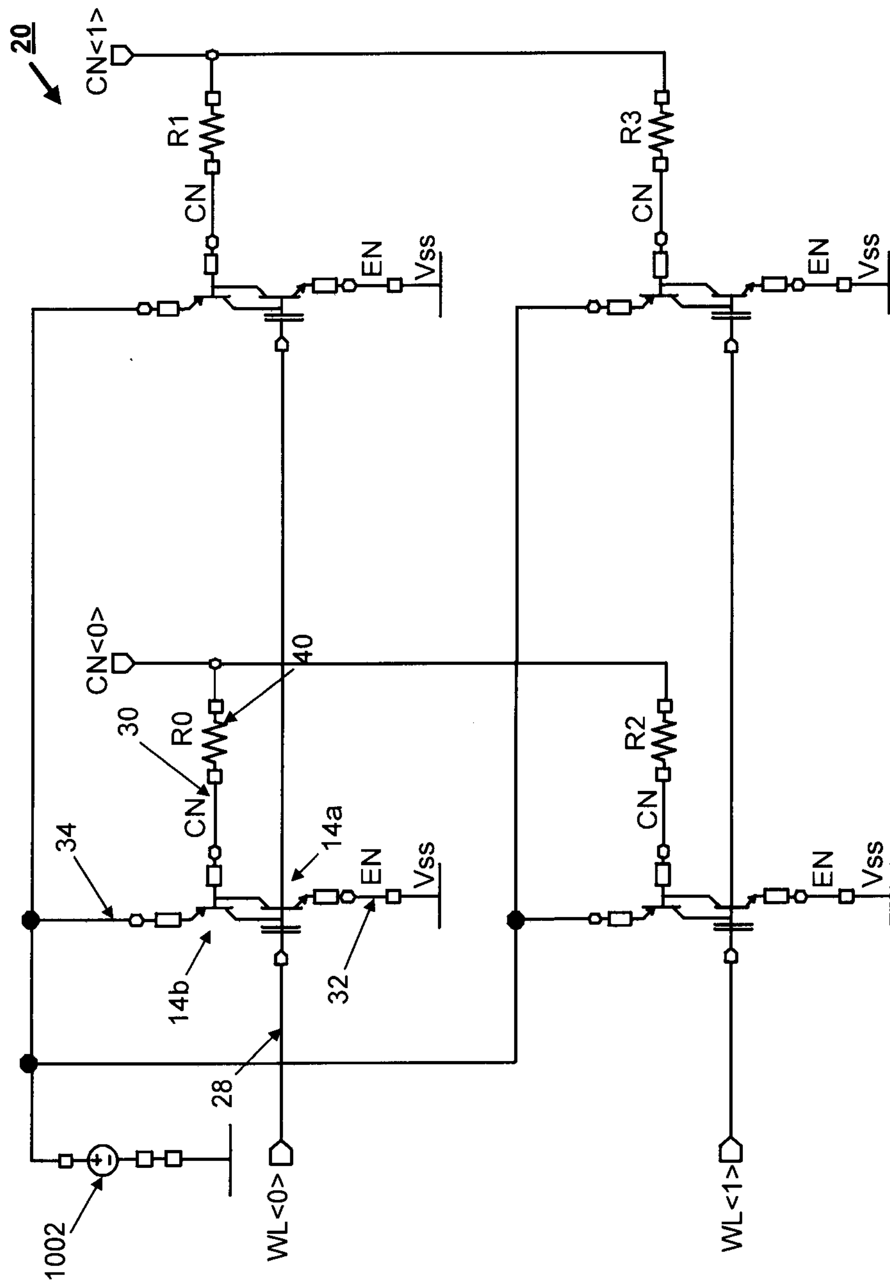

FIGURE 11

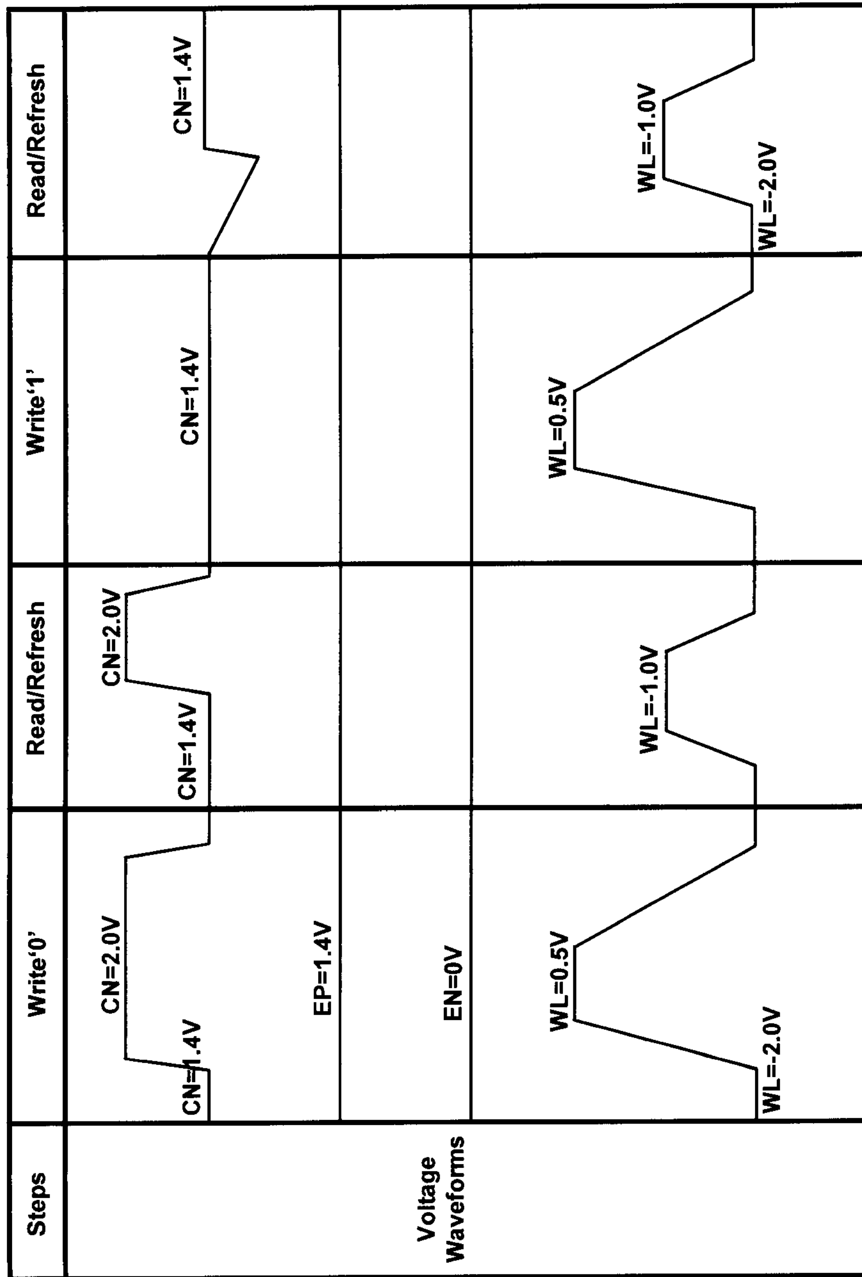

FIGURE 12

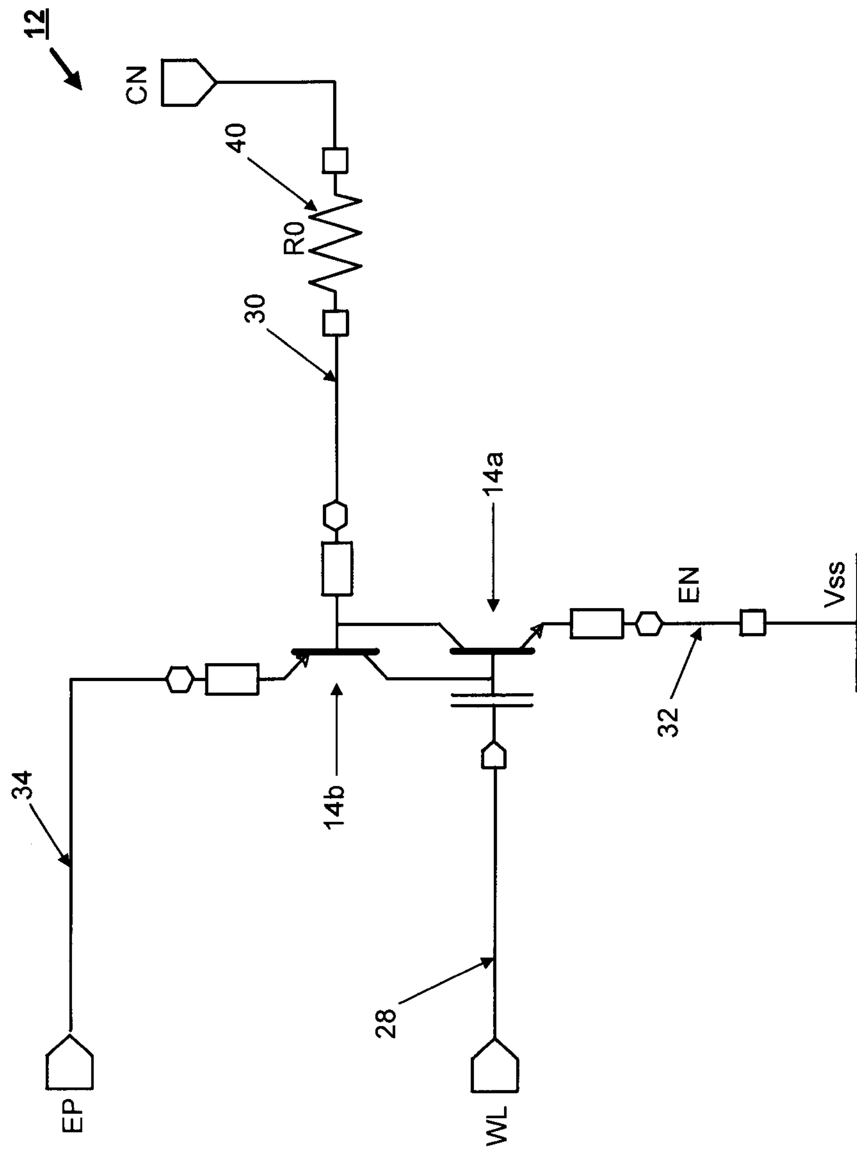

FIGURE 13

FIGURE 14

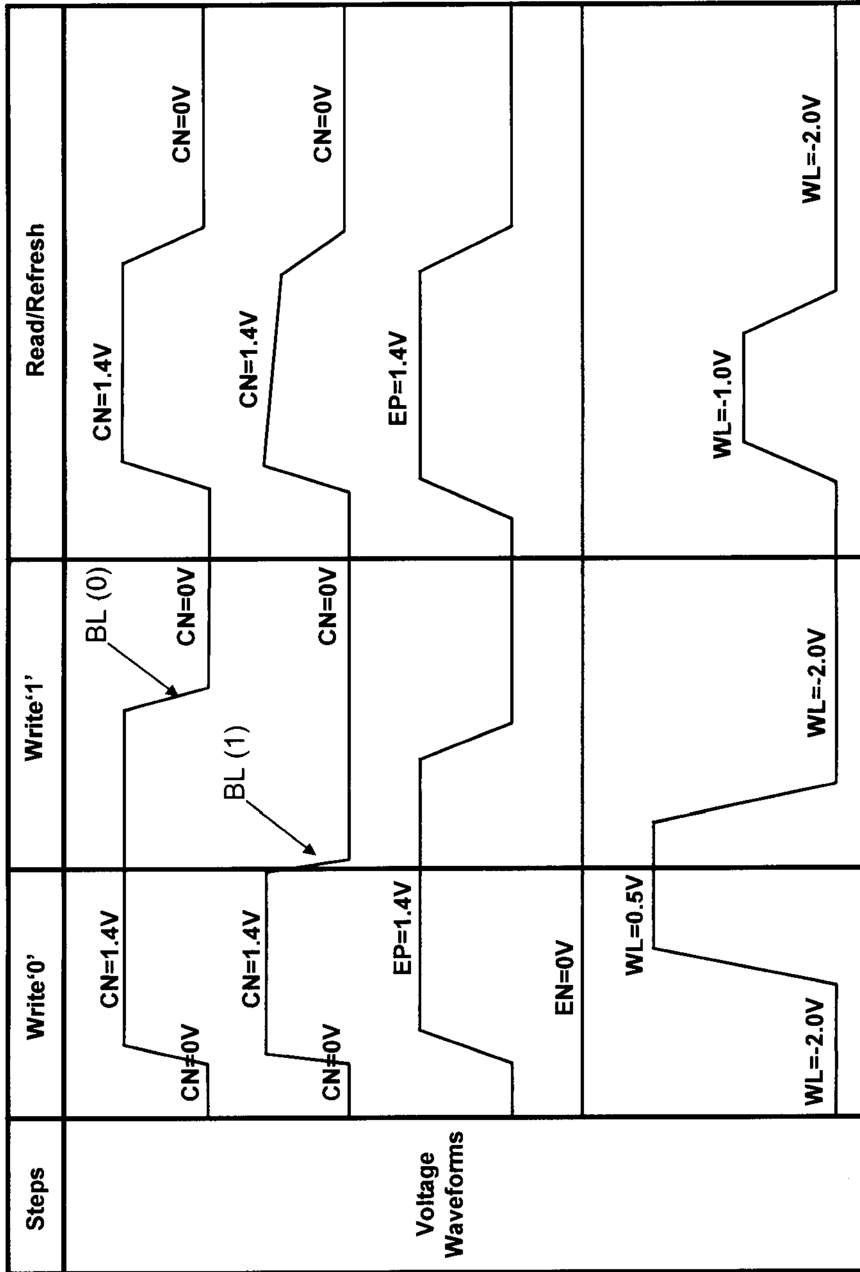

FIGURE 15