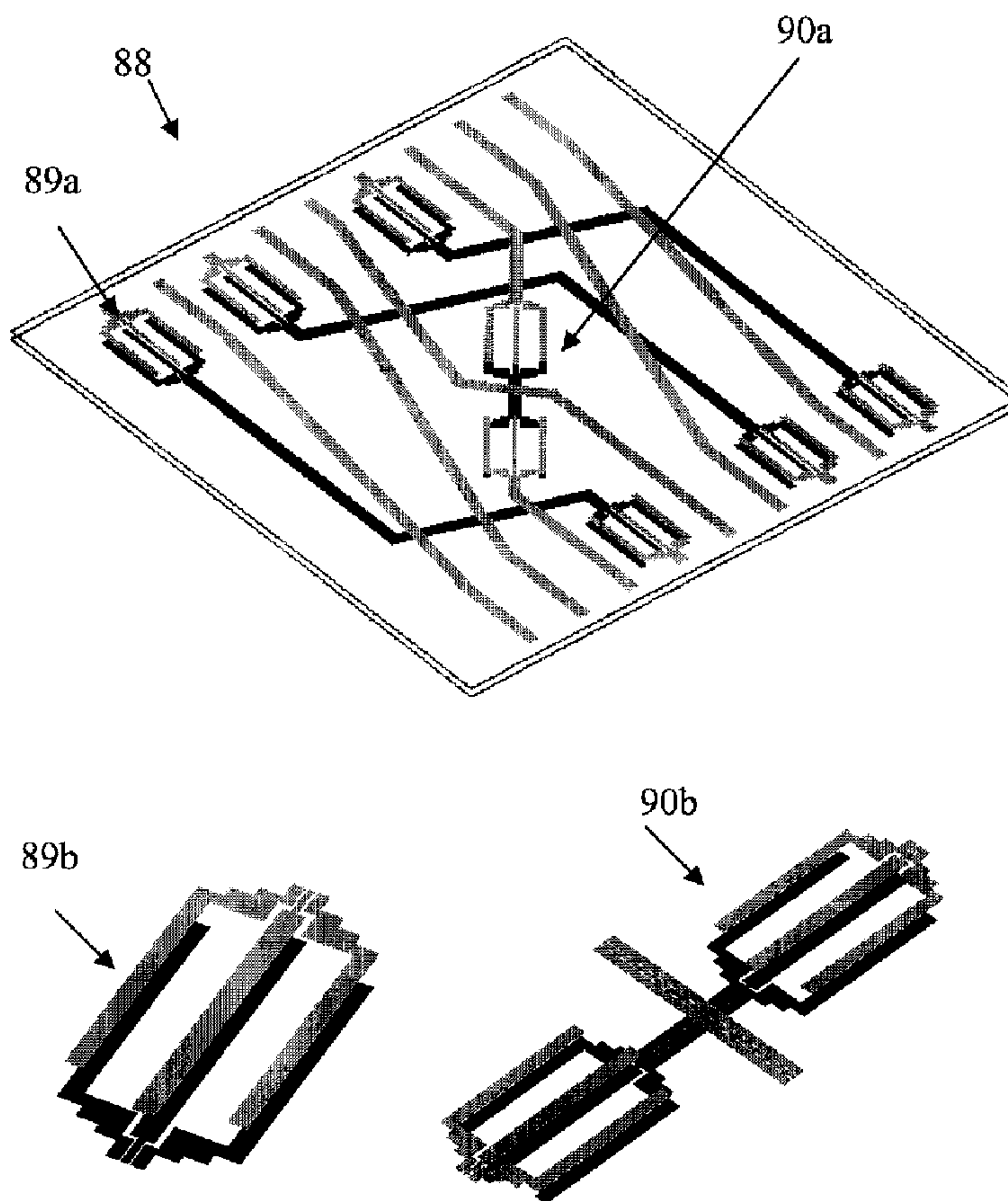




(22) Date de dépôt/Filing Date: 2007/04/05  
 (41) Mise à la disp. pub./Open to Public Insp.: 2007/10/05  
 (30) Priorités/Priorities: 2006/04/05 (US60/789,136);  
 2006/04/05 (US60/789,131)

(51) Cl.Int./Int.Cl. *B81B 3/00* (2006.01),  
*B81B 7/02* (2006.01), *H01P 1/10* (2006.01)  
 (71) Demandeurs/Applicants:  
 DANESHMAND, MOJGAN, CA;  
 MANSOUR, RAAFAT R., CA  
 (72) Inventeurs/Inventors:  
 DANESHMAND, MOJGAN, CA;  
 MANSOUR, RAAFAT R., CA  
 (74) Agent: SCHNURR, DARYL W.

(54) Titre : COMMUTATEURS MEMS RF MONOLITHIQUES MULTIACCES ET MATRICES DE COMMUTATION  
 (54) Title: MULTI-PORT MONOLITHIC RF MEMS SWITCHES AND SWITCH MATRICES



(57) **Abrégé/Abstract:**

A multi-port RF MEMS switch, a switch matrix having several multi-port RF MEMS switches and an interconnect network have a monolithic structure with clamped-clamped beams, cantilever beams or thermally operated actuators. A method of fabricating a monolithic switch has clamped-clamped beams or cantilever beams.

ABSTRACT

A multi-port RF MEMS switch, a switch matrix having several multi-port RF MEMS switches and an interconnect network have a monolithic structure with clamped-clamped beams, cantilever beams or thermally operated actuators. A method of fabricating a monolithic switch has clamped-clamped beams or cantilever beams.

### **Multi-Port Monolithic RF MEMS Switches and Switch Matrices**

This invention relates to RF MEMS microwave switches, a switch matrix and a method of fabricating a monolithic switch. More particularly, this invention relates to a multi-port RF MEMS switch having a monolithic structure with clamped-clamped beams, cantilever beams or  
5 thermally operated actuators.

Satellite beam linking systems vastly rely on switch matrix functionality to manage traffic routing and for optimum utilization of system bandwidth to enhance satellite capacity. A beam link system creates sub-channels for each uplink beam where the switch matrix provides the flexibility to independently direct the beams to the desired downlink channel. Switch matrices  
10 can also provide system redundancy for both receive and transmit subsystems and improve the reliability of the systems. In case of failure of any amplifiers, the switch matrix reroutes the signal to the spare amplifier and thus the entire system remains fully functional.

The two types of switches that can be currently used in the form of switch matrices are mechanical switches and solid state switches. Mechanical (coaxial and waveguide) switches  
15 show good RF performance up to couple of hundred gigahertz. However, mechanical switches are heavy and bulky as they employ motors for the actuation mechanism. This issue is more pronounced in the form of switch matrices where hundreds of multi-port switches are integrated together. Solid state switches, on the other hand, are relatively small in size, but they show poor RF performance especially in high frequency applications (100-200GHz) and they have DC  
20 power consumption.

RF MEMS switches are good candidates to substitute for the existing multi-port switches and switch matrices due to their good RF performance and miniaturized dimensions. However, by reducing the size and increasing the system density, signal transmission and isolation of the interconnect lines become an important issue.

25 The approach of the present invention provides the opportunity to implement the entire switch matrix structure on one chip and avoid hybrid integration of MEMS switches with thick-film multi-layer substrates.

The present invention proposes a method of realizing monolithic RF MEMS multi-port switches, all interconnects and switch matrices on a single layer substrate using thin film technology. Novel prototype units of C-type and R-type switches and switch matrices are demonstrated.

Novel configurations of monolithic C-type and R-type switches are demonstrated. C-type switch  
5 is a four port device with two operational states that can be used to integrate in the form of a redundancy switch matrix. An R-type switch is also a four port device that has an additional operating state compared to the C-type switch. This can considerably simplify switch matrix integration. In addition, a new technique to integrate multi-port switches in the form of switch matrices including all the interconnect lines monolithically is exhibited. These switches and  
10 switch matrices are employed for satellite and wireless communication.

An objective of the present invention is to show the feasibility of using MEMS technology to develop C-type and R-type RF MEMS switches.

It is also another objective to provision a technique that monolithically integrates multi-port RF MEMS switches with interconnect lines in the form of switch matrices over a single substrate.

15 A multi-port RF MEMS switch comprises a monolithic structure formed on a single substrate. The switch has at least one of clamped-clamped beams and cantilever beams. The switch has two connecting paths.

A switch matrix comprises several multi-port RF MEMS switches and an interconnect network for the switches. The switches in the interconnect network are integrated on a single substrate  
20 and form a building block for the matrix. Each switch comprises a monolithic structure having at least one of clamped-clamped beams and cantilever beams. The switch has at least two connecting paths.

A multi-port RF MEMS switch comprises a monolithic structure formed on a single substrate. The switch has at least two connecting paths with at least one thermally operated actuator that  
25 moves into contact and out of contact with the at least two connecting paths.

A switch matrix comprises several multi-port RF MEMS switches and an interconnect network for the switches. The switches and the interconnect network are integrated on a single substrate.

Each switch comprises a monolithic structure having at least one thermally operated actuator that moves into and out of contact with at least two conducting paths.

A method of fabricating a monolithic switch, said method comprising simultaneously forming interconnect lines and MEMS switches on a substrate, selecting a wafer as a base substrate, depositing a metallic film on a back side of said substrate, covering said metallic film with a protective layer, evaporating a resistive layer on a front side of said substrate, depositing a conductive film on said resistive layer, said conductive film being patterned to form a first layer, depositing a dielectric layer on said conductive layer, coating said dielectric layer with a sacrificial layer, forming contact dimples in said sacrificial layer, adding a thick layer of evaporated metal to said sacrificial layer, removing said sacrificial layer and removing said protective layer, forming said switch with at least one of clamped-clamped beams and cantilever beams.

Figure 1 is schematic view of a fabrication system for monolithic switches;

Figure 2(a) is a schematic view of a prior art C-switch in a first state;

Figure 2(b) is a prior art schematic view of a C-switch in a second state;

Figure 3(a) is a schematic view of a C-switch designed and fabricated in accordance with the process of the present invention;

Figure 3(b) shows a fabricated C-switch;

Figure 4(a) is a prior art schematic view of an R-switch in a first state;

Figure 4(b) is a prior art schematic view of an R-switch in a second state;

Figure 4(c) is a prior art schematic view of an R-switch in a third state;

Figure 5 is a fabricated R switch;

Figure 6 is a schematic view of a redundancy switch matrix having C-switches;

Figure 7 is a switch matrix having C-switches fabricated in accordance with the present invention;

Figure 8 is a schematic view of a switch matrix of R-switches;

Figure 9 is a switch matrix of R-switches fabricated in accordance with the present invention;

Figure 10(a) is a schematic view of a switch matrix having a pair wise connection;

Figure 10(b) is a schematic view of a large switch matrix;

Figure 11 is a view of an interconnect network of the present invention having a three by three switch matrix;

Figure 12 is a view of a single pole triple throw switch;

5 Figure 13(a) is a schematic top view of a single pole triple throw switch;

Figure 13(b) is a schematic top view of a nine by nine switch matrix;

Figure 14 shows a three by three interconnect network using single coupled and double coupled transitions;

Figure 15 is a schematic top view of the interconnect network of Figure 14;

10 Figure 16(a) and 16(b) are the measured results of the structure of the structure of Figures 14 and 15;

Figure 17 is a schematic top view of a switch matrix expanded to a 9 by 9 switch matrix;

Figure 18(a) shows a schematic top view of a two to four redundancy building block;

15 Figure 18(b) shows a building block that is composed of four single pole triple throw switches;

Figure 19(a) shows a single pole single throw switch:

Figure 19(b) shows a schematic view of a thermal actuator of a switch in Figure 19(a), the actuator being in a rest position;

20 Figure 19(c) shows a schematic top view of the actuator in an expanded position with the rest position version superimposed thereon in dotted lines;

Figure 20 is a perspective view of a single pole double throw switch having thermally operated actuators;

Figure 21 is a perspective view of a C-switch having thermal actuators; and

25 Figure 22 is a perspective view of an R-switch with a combination of thermal actuators and electrostatic actuators.

Figure 1 shows a preferred fabrication process that is used to develop monolithic switches and switch matrices. It is comprised of the simultaneous processing of all the interconnect lines and the MEMS switches within one substrate. An alumina wafer 1 is selected as the base substrate as  
30 it exhibits a good RF performance at high frequencies. Initially, a gold film 2 is deposited on the back side of the substrate. This film is patterned for the transitions and crossovers. Afterwards, a

back side is covered with a layer of Kapton tape or photoresist 3. The process continues with evaporating a resistive layer 4 for DC biasing as well as adhesion of the following film (gold 5a) in the front side. Gold film 5b is patterned to form the first layer. White gold is preferred, other metallic films are suitable. The fourth step is the deposition of the dielectric layer 6 (PECVD SiO<sub>2</sub> with adhesion layer of TiW). Then a sacrificial layer (photo resist 7) is spin coated. Initially, the resist is fully exposed through the fifth mask to pattern the anchors 8. Then the resist is followed by short exposure of the contact dimples 9 using another mask. The last layer is thick evaporated gold 10 as the structural layer and it is followed by oxygen plasma release which results in released beams 11. Then the protecting layer at the back is removed to have the final device 12.

Figure 2 is the operation schematic of a C-type switch. The switch functions in two states. State I (Figure 2(a)) is presented when port 14a is connected to port 15a and port 16a is connected to port 17a. State II (Figure 2(b)) is represented when port 14b is connected to port 17b and port 15a is connected to port 16a. Figure 3(a) shows the structure of the C-type switch designed and fabricated using the above mentioned process. It is a compact ( $750 \times 750 \mu\text{m}^2$ ) coplanar series switch, consisting of four actuating beams (18,19,20,21). One end of each beam is attached to a 50Ω coplanar transmission line, whereas the other end is suspended on top of another 50Ω coplanar transmission line to form a series-type contact switch. In state I, beams 18 and 20 are in contact mode while for state II, connection is established when beams 19 and 21 is pulled down. Figure 3(b) shows the fabricated preferred embodiment for the present invention.

Figure 4 shows the operational schematic of an R-type switch. In state I, shown in Figure 4(a), ports 23a and 24a, and ports 25a and 26a, are connected, while in state II (in Figure 4(b)), ports 23b and 26b, and ports 24b and 25b, are connected, and in state III only ports 23c and 25c, are connected. Figure 5 shows the fabricated R-type switch using thin film process shown in Figure 1. It consists of four ports 23d, 24d, 25d, 26d and five actuators 27, 28, 29, 30, 31. The additional state of the R-type switch compared to the C-type switch is represented when beam 29 is pulled down and provides a short circuit between ports 24d, and 26d. It should be noted that there are electrodes 32, 33, 34, 35, 36, 37 under the beams. The R-type switches provide a superior advantage in comparison to the C-type switches as they operate in one more state, which considerably reduces the number of building blocks in redundancy switch matrices and simplifies the overall topology.

In a typical satellite payload hundreds of switches, in the form of switch matrices, are used to provide the system redundancy and maintain the full functionality. This is achieved by rerouting the signal to the spare amplifier in case of any failure. The configuration shown in Figure 6 is a 5 to 7 redundancy switch matrix based on C-type switch 13 basic building blocks. Ports 37a to 41a is the input ports of the switch matrix 56a connected to amplifiers of 47 to 51. In case of any failure in these amplifiers, the switch matrix reroutes the signal in a way that spare amplifiers 52 and 53 are in the circuit and the entire system remains fully functional. Using the process presented in Figure 1 and based on C-type switches 13 the entire switch matrix is fabricated and the preferred embodiment is shown in Figure 7 which has 5 input ports (37, 38, 39, 40,41) and 7output ports ( 42,43, 44,45, 46, 54, 55). It uses Cr 4 layer as DC biasing lines 57 and air bridges for crossovers 58 in the interconnect lines. Further, switches are constructed to be operated to have a variable functionality. For example, an R-switch can be operated as an R-switch, a C-switch or a single pole double throw switch.

Figure 8 shows schematic of an R-type switch matrix 71a. This consists of five R-type switches 22b. The state that is shown in Figure 8 is for the case that there are two failures and the switch matrix reroutes the signal to its spare outputs 64a and 70a. Figure 9 shows a preferred embodiment for invented R-type switch matrix 71c. It has five inputs 59, 60, 61, 62, 63 and seven outputs 64, 65, 66, 67, 68, 69, 70. It can be clearly observed that using R-type switches 22c, the switch matrix is much smaller (only five elements 22c).

Figure 10(a) shows the schematic of another switch matrix 72a that has pair wise connection. This type of matrices 72 are used for signal routing and managing the traffic. In RF MEMS switch matrices that are small and dense, the signal transmission and maintaining a good isolation becomes more critical. This problem is even more pronounced for the larger structures such as shown in Figure 10(b) 75. Figure 11 presents a preferred embodiment for the interconnect network 72b of a 3 by 3 switch matrix that makes use of a backside 76 patterning. Single vertical transitions 77b and double vertical transitions 79b are used to transfer the signal from the top to the bottom side of the wafer. The vertical transitions are preferably conductive vias. A single vertical transition is a single conductive via and a double vertical transition is a double conductive via. The interconnect network can be integrated with multi-port switches to form a switch matrix. For instance, the 3 by 3 interconnect network 72b can be integrated by Single Pole Triple Throw switches (SP3T) 85. Figure 12 shows the preferred structure of this



switch. It has four ports 81, 82, 83, and 84 with three beams 80. It could present three states and connect input port of 81 to any output ports of 82, 83, and 84.

The smaller switch matrices can be easily expanded to larger one using different network connectivity such as Clos network 75. Figure 13(b) shows a preferred embodiment of the expanded switch matrix to 9 by 9, 87.

In addition to via transitions 77b, electromagnetically coupled transitions can be also used 89 (a). In this case, the signal is electromagnetically coupled from one side 76 of the substrate to the other side 78. Figure 14 shows the preferred embodiment of the present invention for 3 by 3 interconnect network 88 using single coupled transition 89 and double vertical coupled transitions 90. This is limited in bandwidth but it requires much simpler fabrication process. It is due to the fact that it avoids using vertical vias. This network can be simply integrated with SP3T switches 85c and form a switch matrix 91 as shown in Figure 15. The measured results of such a structure indicates excellent performance as presented in Figure 16. Figure 17 shows the expanded version of the present invention 92 in the form of a 9 by 9 switch matrix.

Figures 18(a) and (b) show another preferred embodiment 99a that is a small switch matrix or a type of multi-port switch with a special function such as 2 to 4 or 3 to 4 redundancy. The structure shown in Figure 18(a) 99a, represents a 2 to 4 redundancy building block. In normal operation, input ports, 95 and 96, are connected to the main amplifiers, 93 and 94. In case of failure of one of the main amplifiers, that port can be switched to the spare amplifiers 97 and 98. Figure 18(b) shows another building block 99b that is composed of the same structure (four SP3T switches 85d). This structure 99b can be used for 3 to 4 redundancy purposes using one spare amplifier. There are three input ports 103, 104, 105 that are connected to three main amplifiers 100, 101, 102 during the normal operation. In the case of amplifier failure, any of the input ports can be switched to the spare amplifier 106 to maintain the full functionality of the system.

Figures 19(a),(b) and (c) present another embodiment 107 of the present invention of switch that uses thermal actuators 113 to turn the switch ON and OFF. The actuator uses two thin and thick arms and different thermal expansion of the arms provides a forward movement and switching. The switch uses a dielectric layer 109 to separate the contact metal 108 with the actuator providing much better RF performance.

Figures 19(b) and 19(c) are schematic views of the thermal actuator of Figure 19(a). Figure 19(b) shows the actuator in the rest position and Figure 19(c) shows the actuator in the expanded or actuated position with the rest position superimposed thereon by dotted lines. The same reference numerals are used in Figure 19(c) as those used in Figure 19(b).

- 5 An SP2T switch 141 is presented in Figure 20. Figure 21 presents a C-type switch 118 developed using this concept. Actuators 113d and 113f move forward to provide connection between ports 121 to 119 and 122 to 120. For the other operating state, the actuators 113e and 113g move forward and make connection between ports 121 to 122 and 119 to 120.

10 Figure 22 is an R-switch 160. The same reference numerals are used in Figure 22 as those used in Figure 21 for those components that are identical. The R-switch 160 has four thermal actuators 113d, 113e, 113f, and 113g as well as one electrostatic cantilever actuator 162 that connects port 119 and port 122 when the thermal actuators are in the rest position and the electrostatic actuator 162 is activated. The electrostatic actuator 162 can be placed with another type of actuator. For example, the electrostatic actuator can be replaced by a thermal actuator.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A multi-port RF MEMS switch, said switch comprising a monolithic structure formed on a single substrate, said switch having at least one of clamped-clamped beams and cantilever beams, said switch having at least two connecting paths.
2. A switch matrix comprising several multi-port RF MEMS switches and an interconnect network for said switches, said switches and said interconnect network being integrated as a monolithic structure on a single substrate and forming a building block for said matrix, each switch comprising a monolithic structure having at least one of clamped-clamped beams and cantilever beams, said switch having at least two connecting paths.
3. A method of fabricating a monolithic switch, said method comprising simultaneously forming interconnect lines and MEMS switches on a substrate, selecting a wafer as a base substrate, depositing a metallic film on a back side of said substrate, covering said metallic film with a protective layer, evaporating a resistive layer on a front side of said substrate, depositing a conductive film on said resistive layer, said conductive film being patterned to form a first layer, depositing a dielectric layer on said conductive layer, coating said dielectric layer with a sacrificial layer, forming contact dimples in said sacrificial layer, adding a thick layer of evaporated metal to said sacrificial layer, removing said sacrificial layer and removing said protective layer, forming said switch with at least one of clamped-clamped beams and cantilever beams.
4. A multi-port RF MEMS switch, said switch comprising a monolithic structure formed on a single substrate, said switch having at least two connecting paths with at least one thermally operated actuator that moves into contact and out of contact with said at least two connecting paths.
5. A switch matrix comprising several multi-port RF MEMS switches and an interconnect network for said switches, said switches and said interconnect network being integrated on a single substrate, each switch comprising a monolithic structure having at least one thermally operated actuator that moves into and out of contact with said at least two connecting paths.

6. A switch as claimed in Claim 1 wherein the switch is a single pole double throw switch with three connecting paths of said at least two connecting paths.
7. A switch as claimed in Claim 1 wherein the switch is a C-switch with four connecting paths of said at least two connecting paths.
8. A switch as claimed in Claim 1 wherein said switch has two states.
9. A switch as claimed in Claim 1 wherein said switch is an R-switch, said R-switch having five connecting paths and five actuators.
10. A switch as claimed in Claim 1 wherein said switch has five connecting paths and three states.
11. A switch as claimed in Claim 1 wherein said switch has one or more actuators selected from the group of thermal, magnetic, electrostatic and a combination thereof.
12. A switch as claimed in Claim 1 wherein said switch has one or more electrostatic actuators.
13. A switch matrix as claimed in Claim 2 wherein said interconnect network ports are located on one side of each substrate.
14. A switch matrix as claimed in Claim 2 wherein said interconnect network ports are located on two sides of each substrate.
15. A switch matrix as claimed in Claim 2 wherein said interconnect network ports are located on more than two sides of each substrate.
16. A switch matrix as claimed in Claim 2 wherein said interconnect has at least one of conductive connectors and capacitative connectors.
17. A switch matrix as claimed in Claim 2 wherein there are several building blocks that are interconnected by an interconnect network.

18. A switch matrix as claimed in Claim 2 wherein there are several switch matrices that are constructed to provide redundancy and maintain full functionality of a system by being connected to reroute a signal to a spare amplifier in case of failure.
19. A switch matrix as claimed in Claim 2 wherein said switches are C-switches.
20. A switch matrix as claimed in Claim 2 wherein said switches are R-switches.
21. A switch matrix as claimed in Claim 2 wherein said switches and interconnect network are stripline or microstripline.
22. A switch matrix as claimed in Claim 2 wherein said matrix is constructed to have a variable functionality.
23. A switch matrix constructed to provide redundancy in the event of failure of part of the matrix.
24. A switch as claimed in Claim 4 wherein said switch has four connecting paths and is a C-switch with four ports, and each C-switch having four actuators that are connected to operate to connect ports 1 and 2 and ports 3 and 4 in a first state and ports 1 and 3 and ports 2 and 4 in a second state.
25. A switch as claimed in Claim 4 wherein said switch is a single pole double throw switch having ports 1, 2 and 3, ports 1 and 2 being connected when one of the actuators is activated and ports 1 and 3 being connected when another actuator is activated.
26. A switch as claimed in Claim 4 where said switch is a C-switch having four connecting paths and four actuators, said actuators being connected so that two actuators are activated simultaneously while the remaining two actuators are not activated and vice versa.
27. A switch as claimed in Claim 4 wherein said switch is an R-switch having ports 1, 2, 3 and 4, said switch having three states, one state occurring when ports 1 and 2 and ports 3 and 4 are connected, another state occurring when ports 1 and 3 and ports 2 and 4 are connected and a third state occurring when ports 1 and 4 are connected.

28. A method as claimed in Claim 3 wherein said method includes the step of using gold as said metallic layer.

29. A multi-port RF MEMS switch, said switch comprising a monolithic structure formed on a single substrate, said switch having at least one of clamped-clamped beams and cantilever beams, said switch having at least two connecting paths in at least one state that are connected simultaneously.

Application number / numéro de demande: \_\_\_\_\_

Figures: 3, 5, 7, 11, 12, 15, 19, 20, 21, 22

Pages: \_\_\_\_\_

Unscannable item(s)  
received with this application

To inquire if you can order a copy of the unscannable items, please visit the  
CIPO WebSite at [HTTP://CIPO.GC.CA](http://CIPO.GC.CA)

Item(s) ne pouvant être balayés

Documents reçus avec cette demande ne pouvant être balayés.

Pour vous renseigner si vous pouvez commander une copie des items ne  
pouvant être balayés, veuillez visiter le site web de l'OPIC au [HTTP://CIPO.GC.CA](http://CIPO.GC.CA)

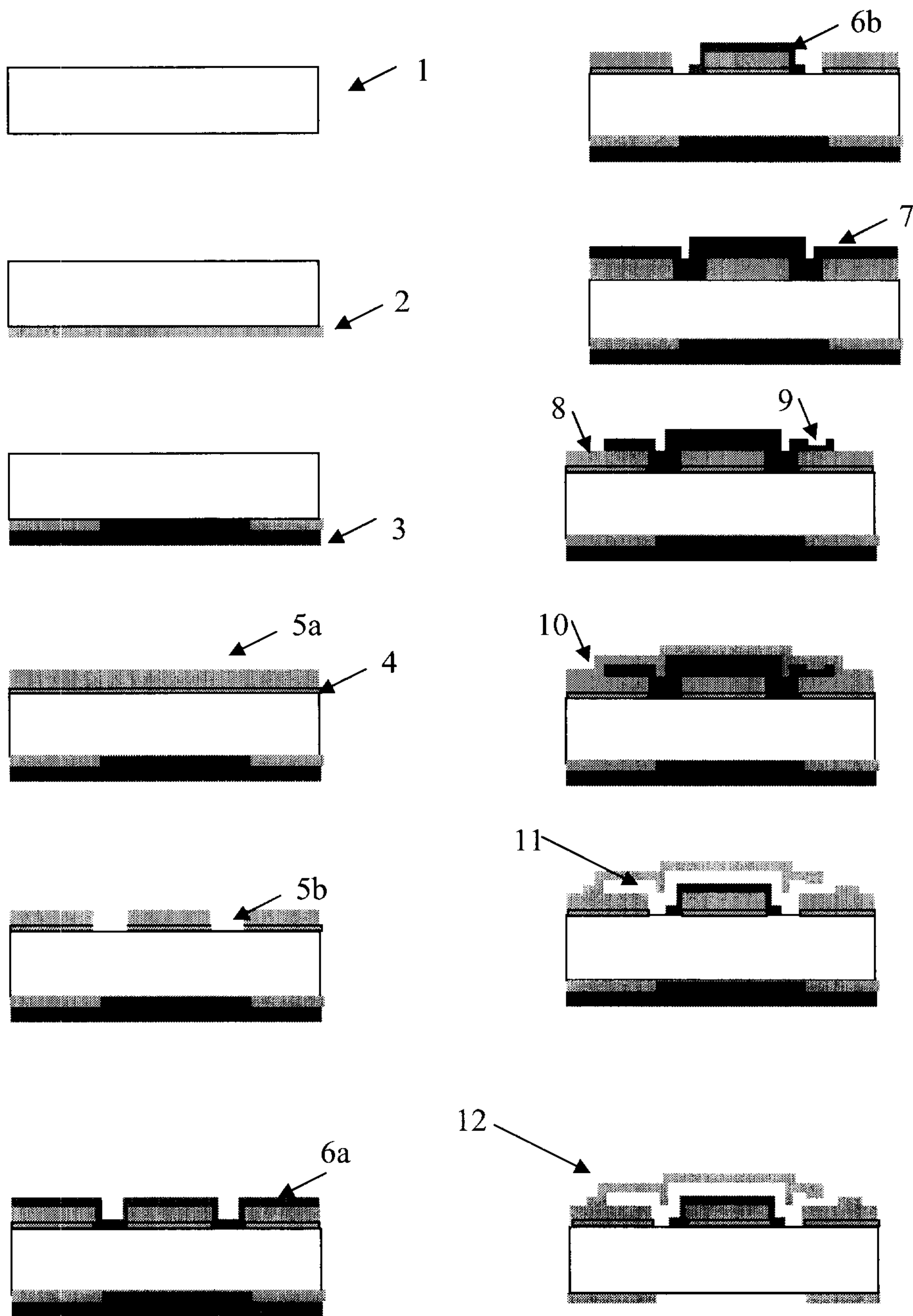
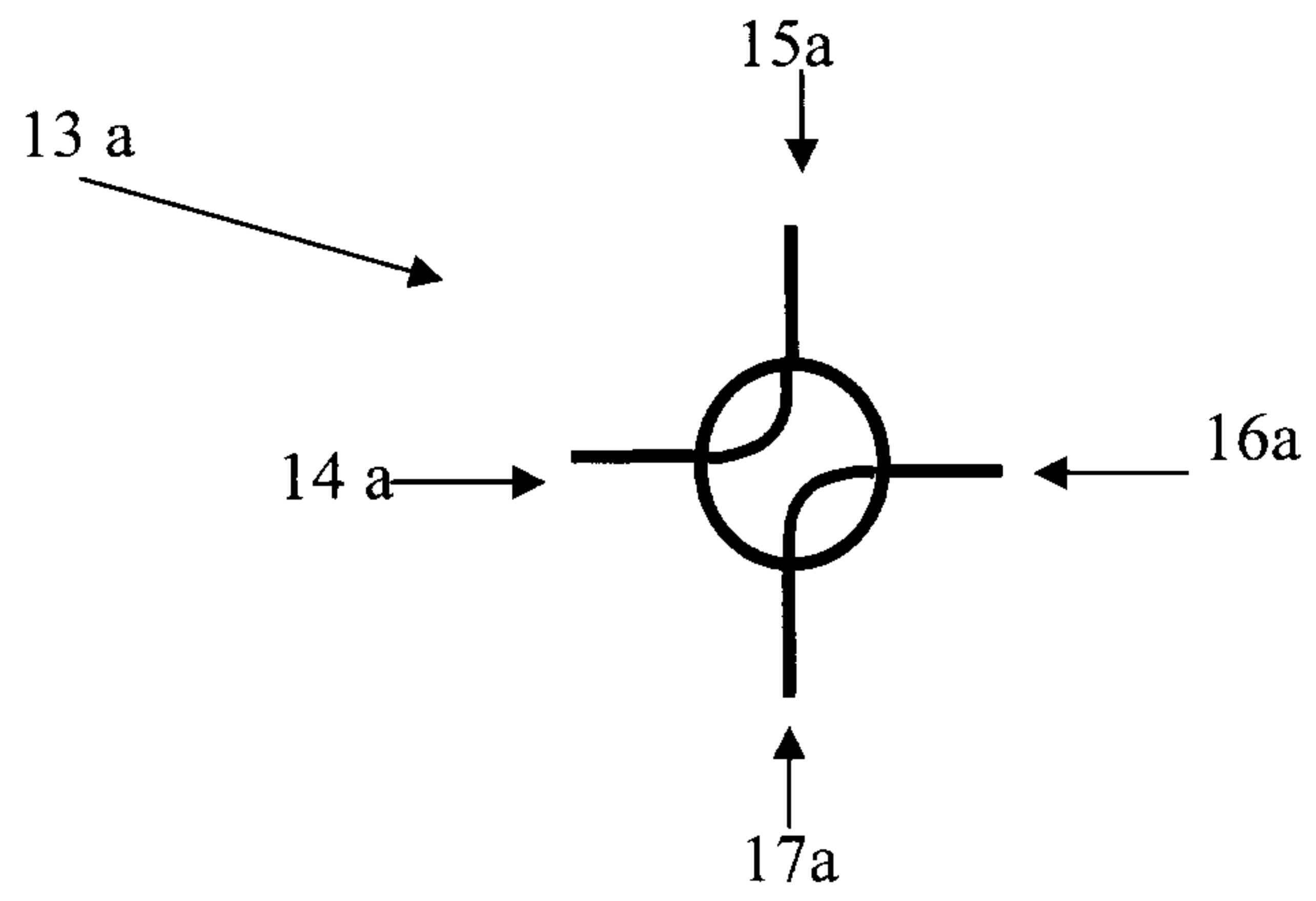
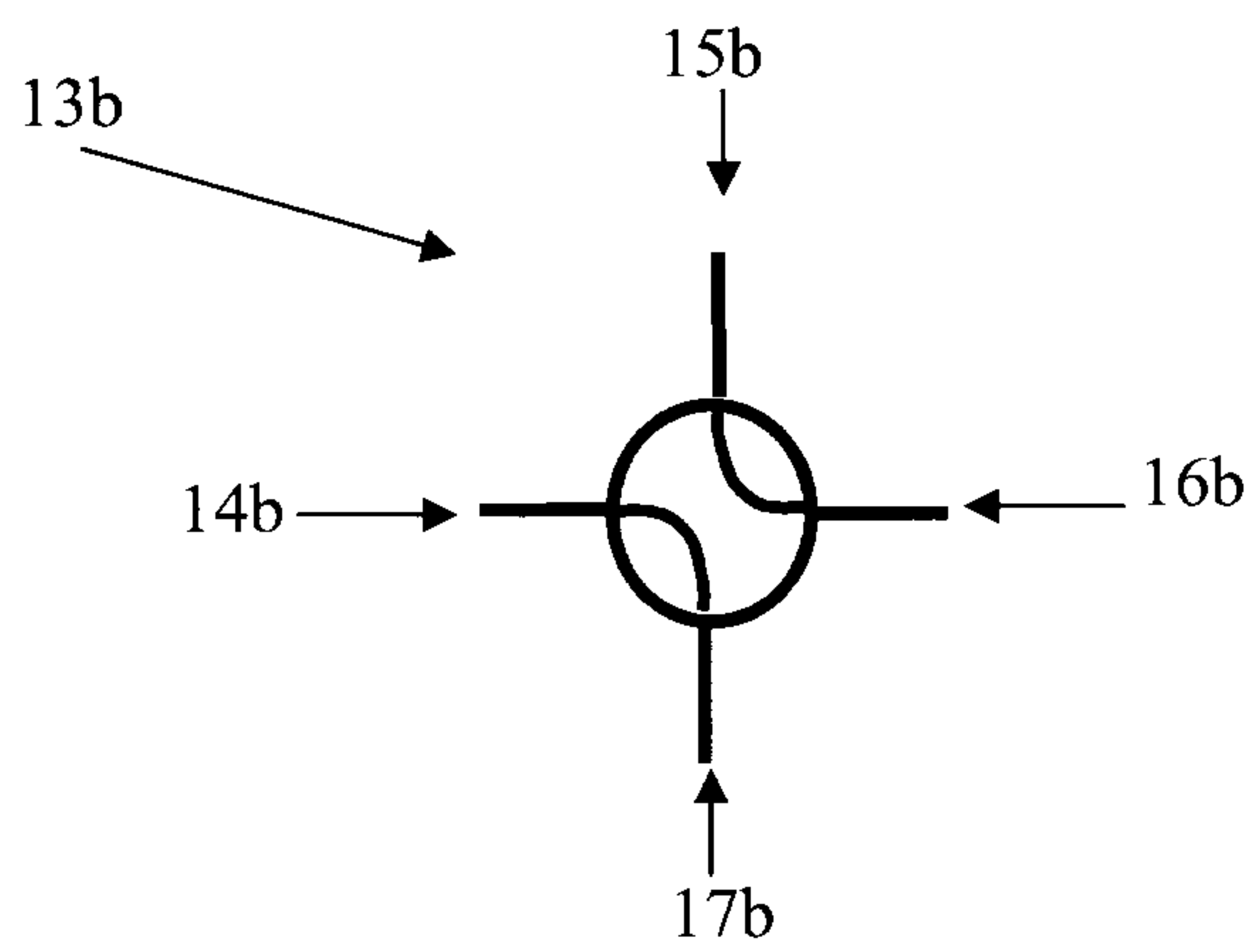


Figure 1



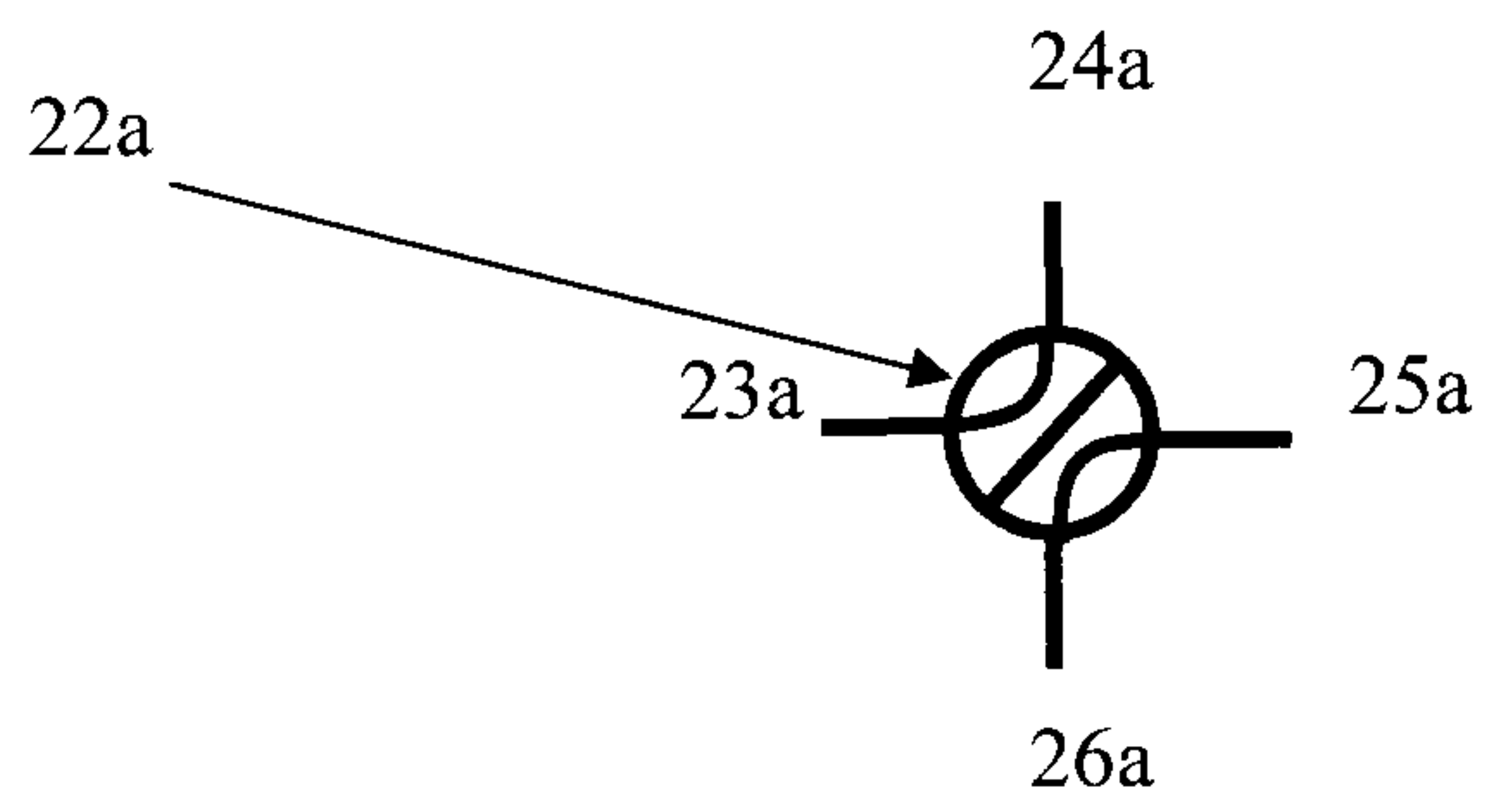


(a)

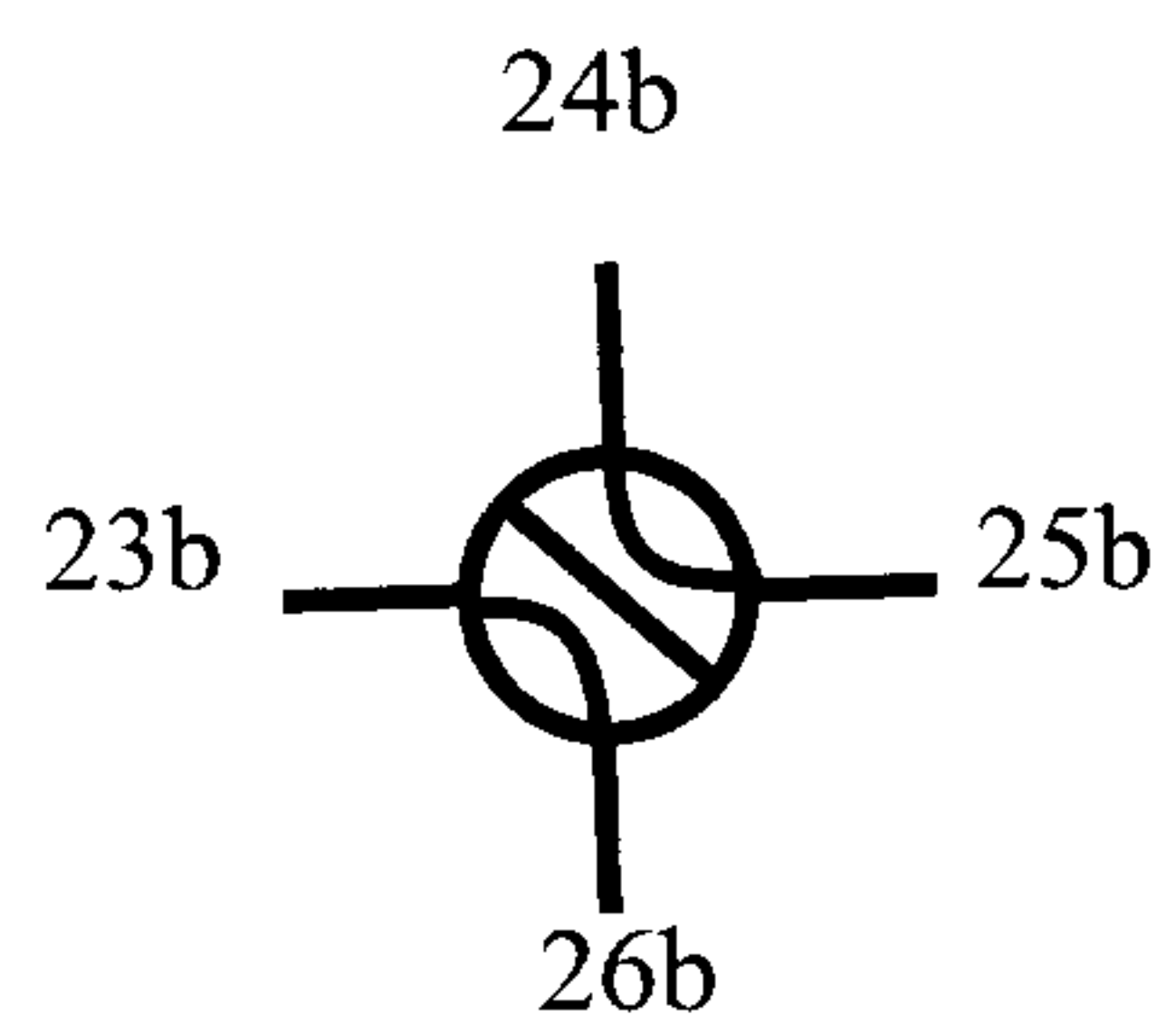


(b)

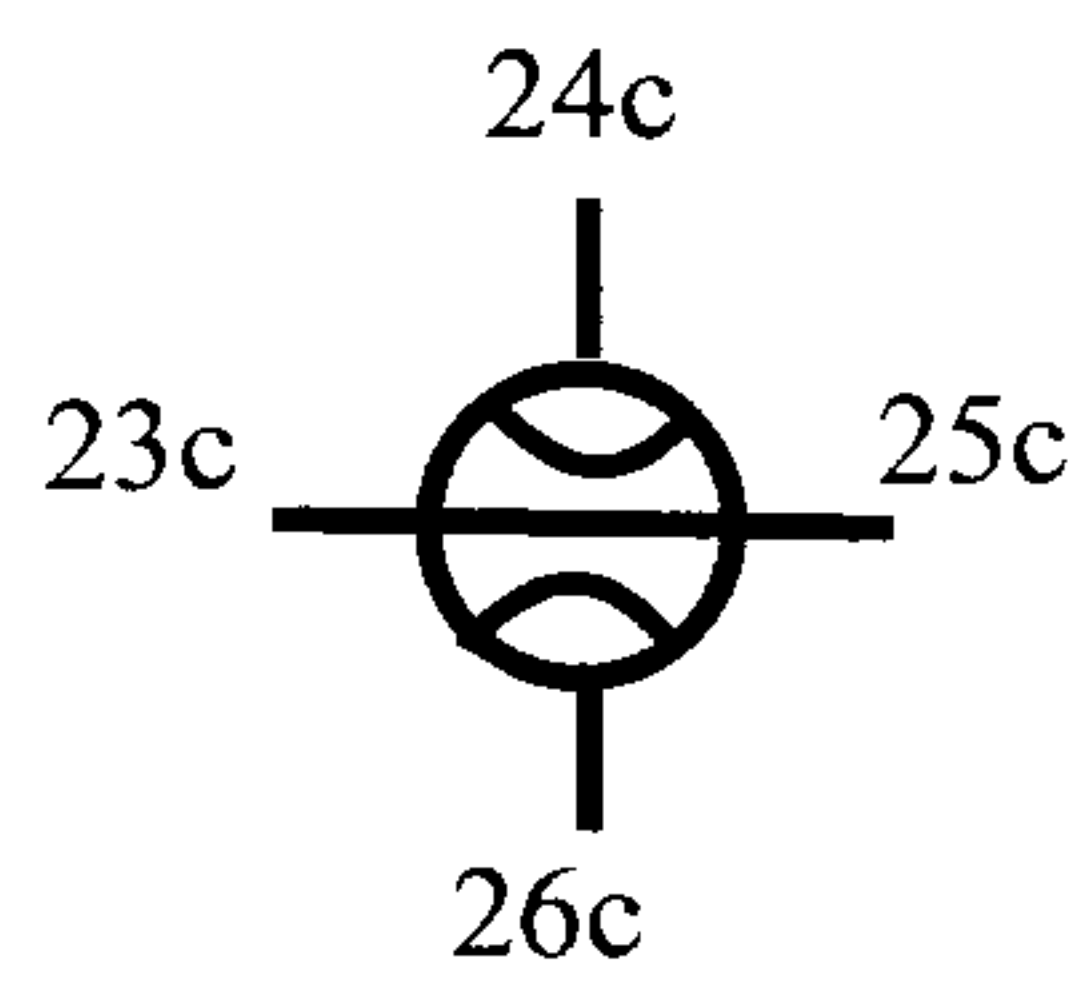
**Figure 2**



(a)



(b)



(c)

**Figure 4**

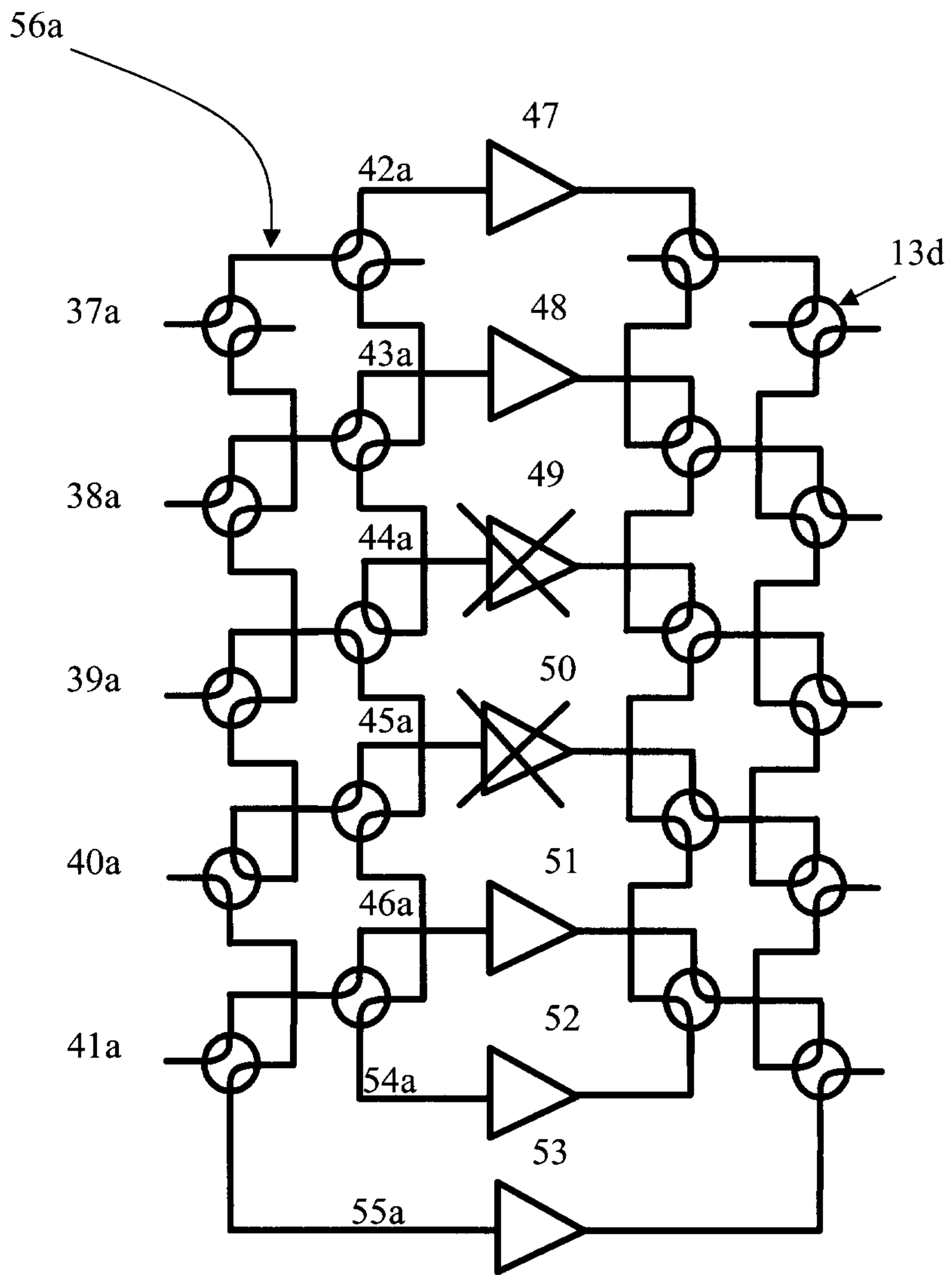


Figure 6

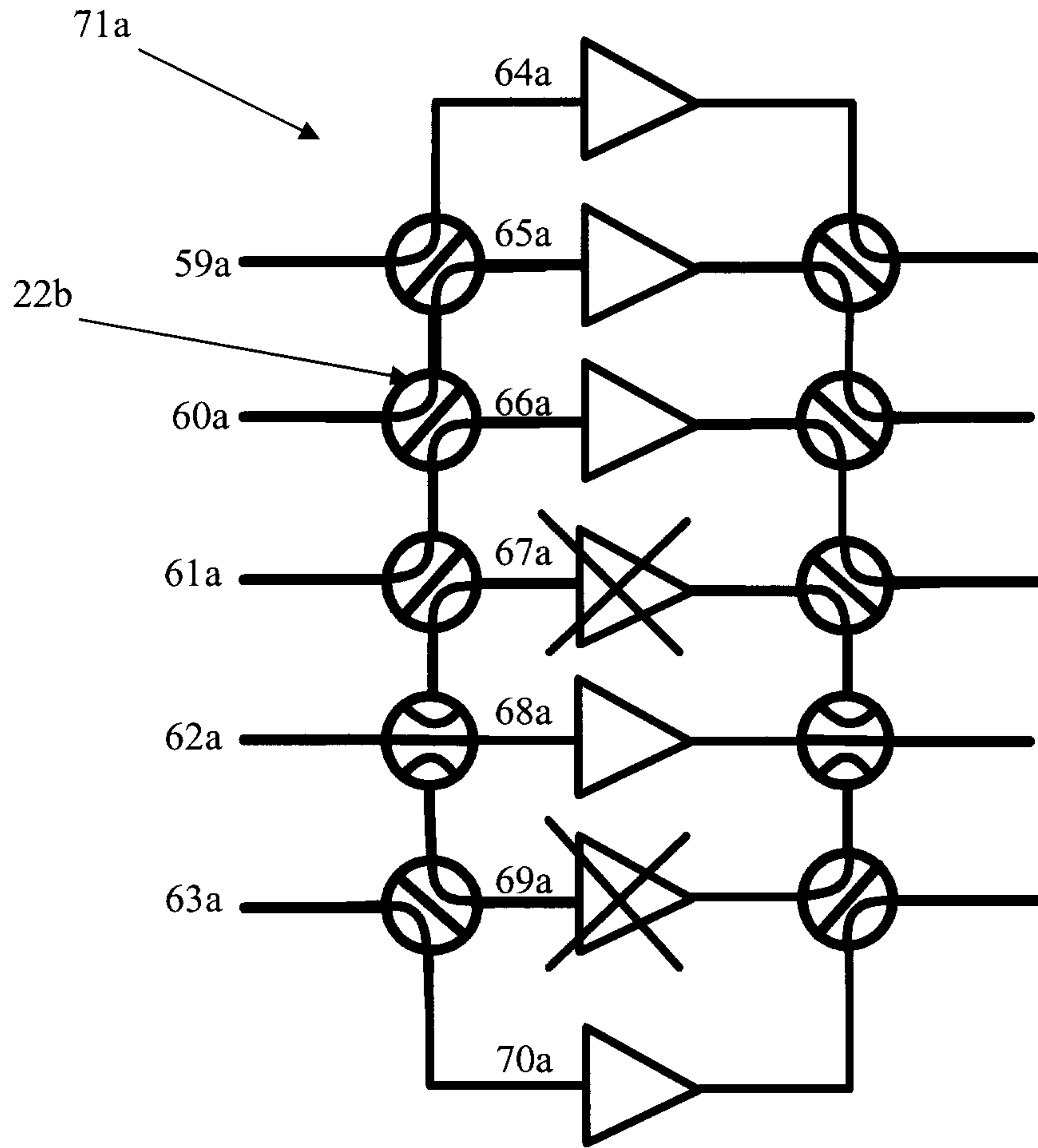


Figure 8

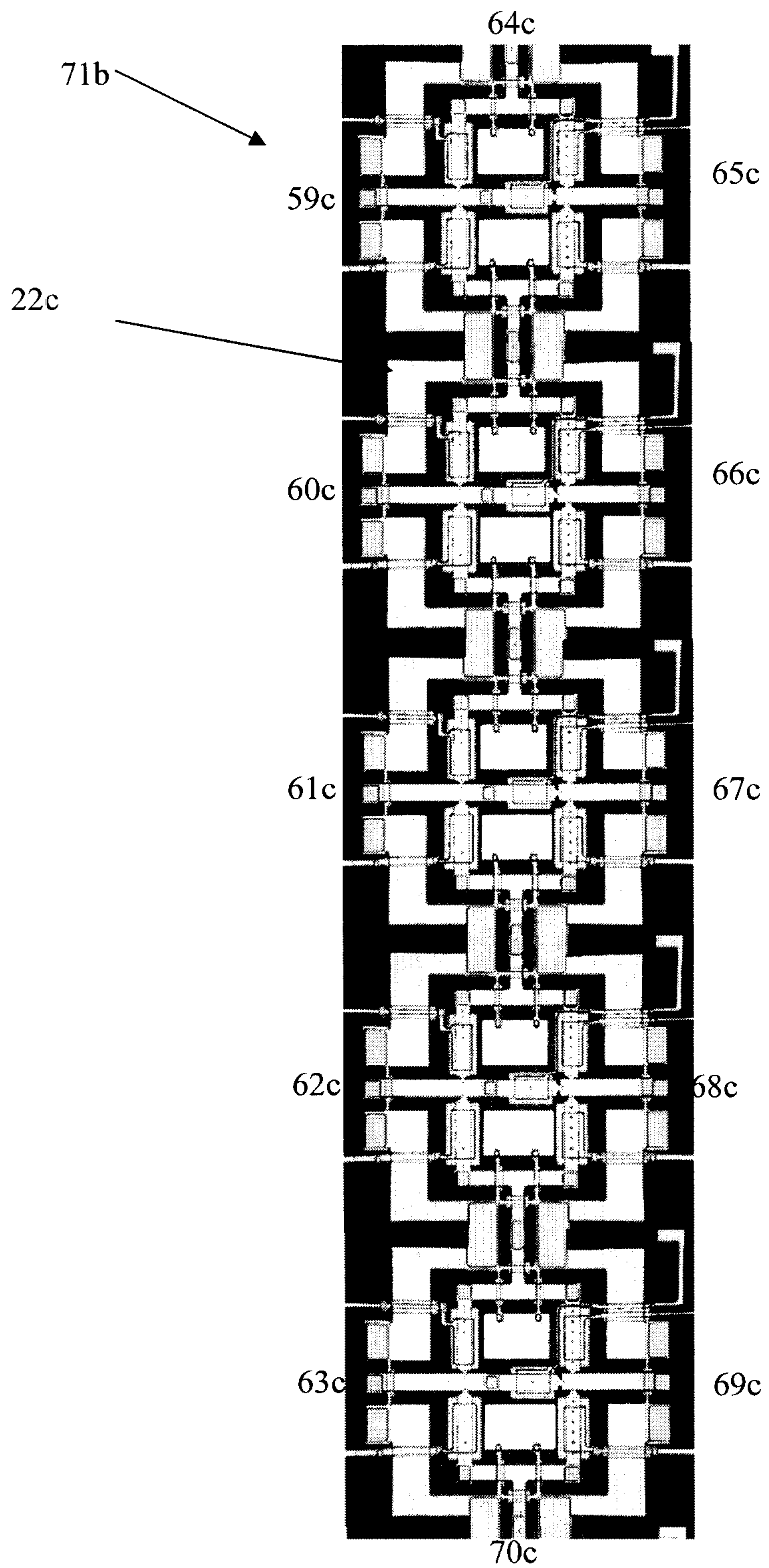


Figure 9

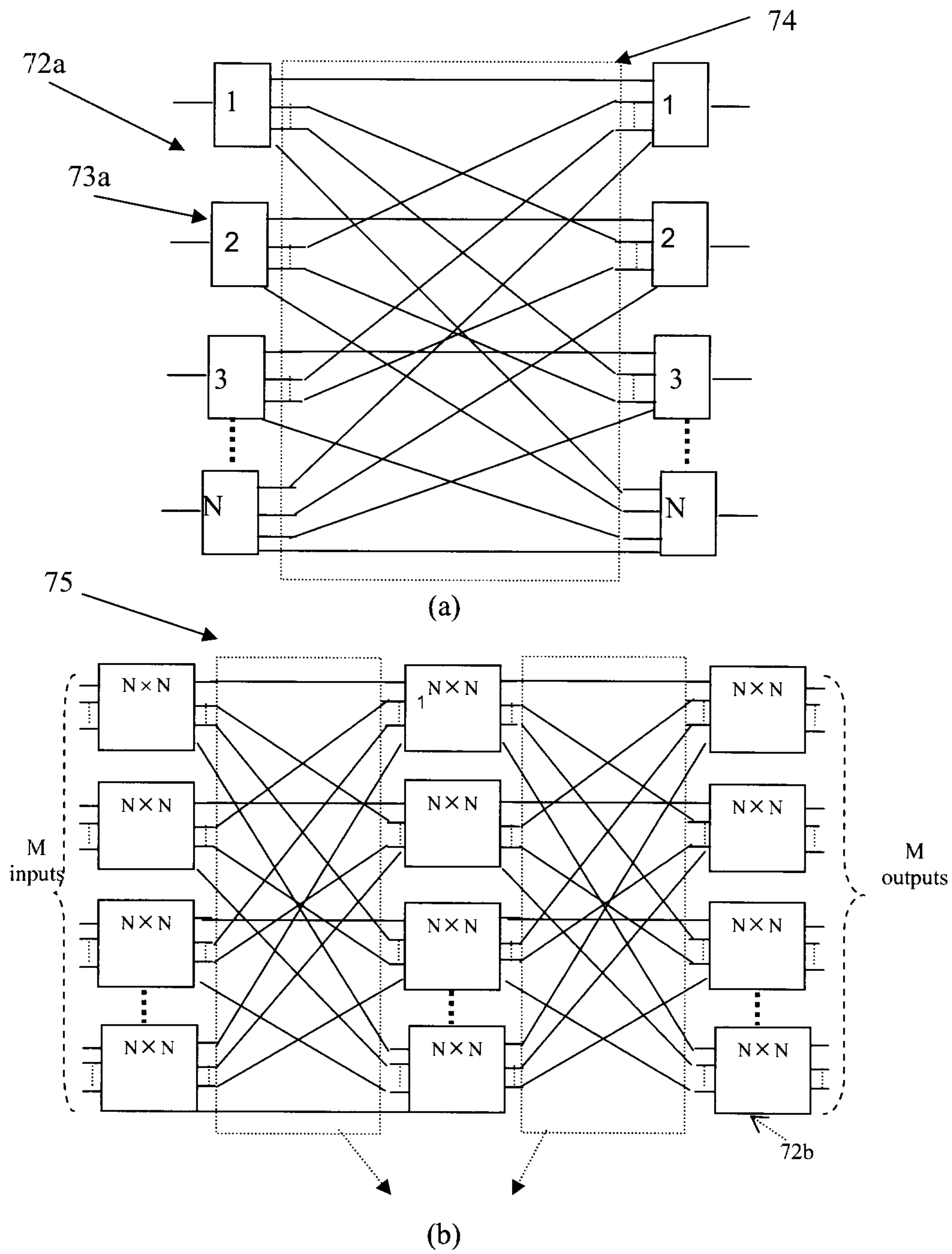


Figure 10

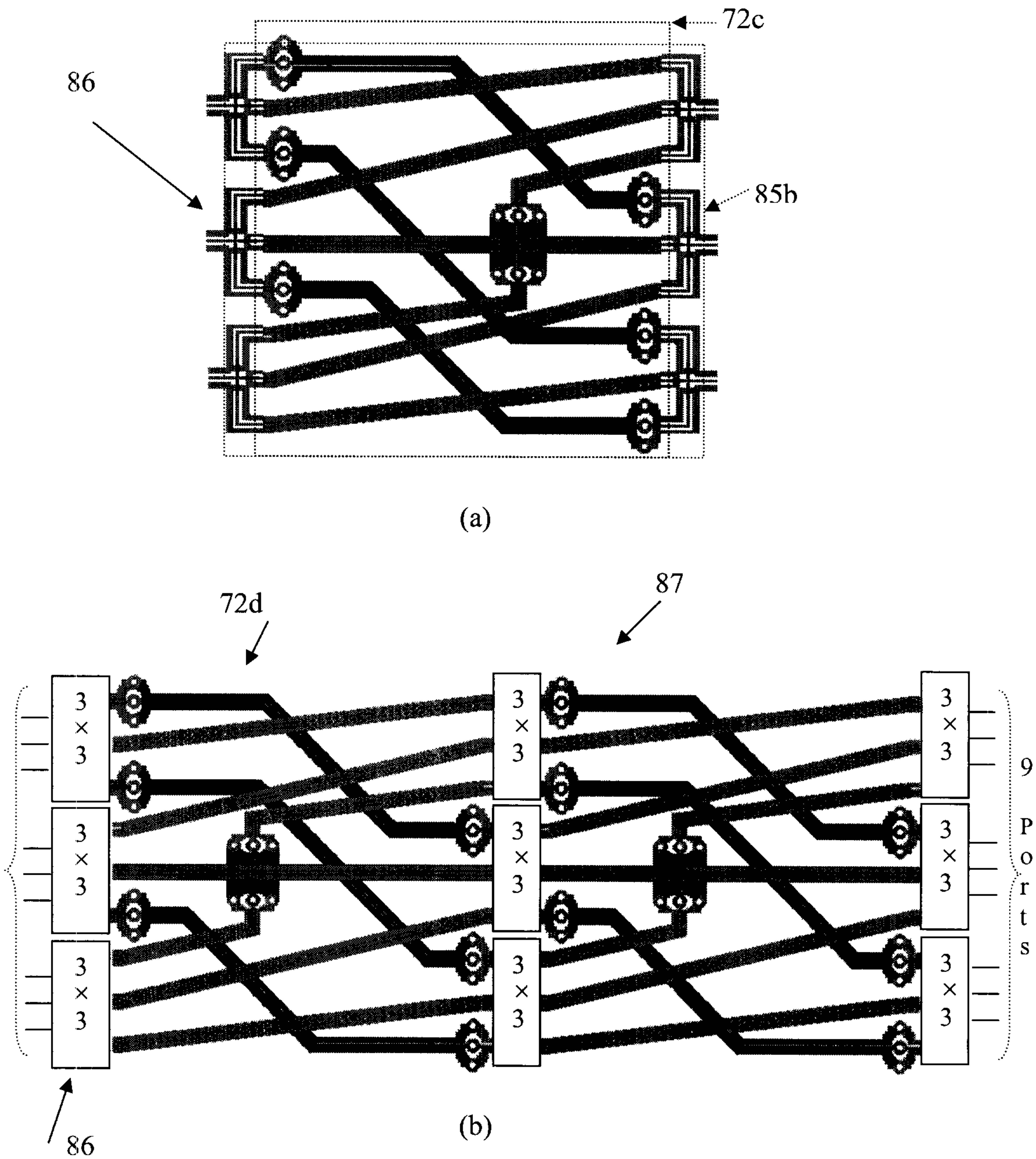


Figure 13

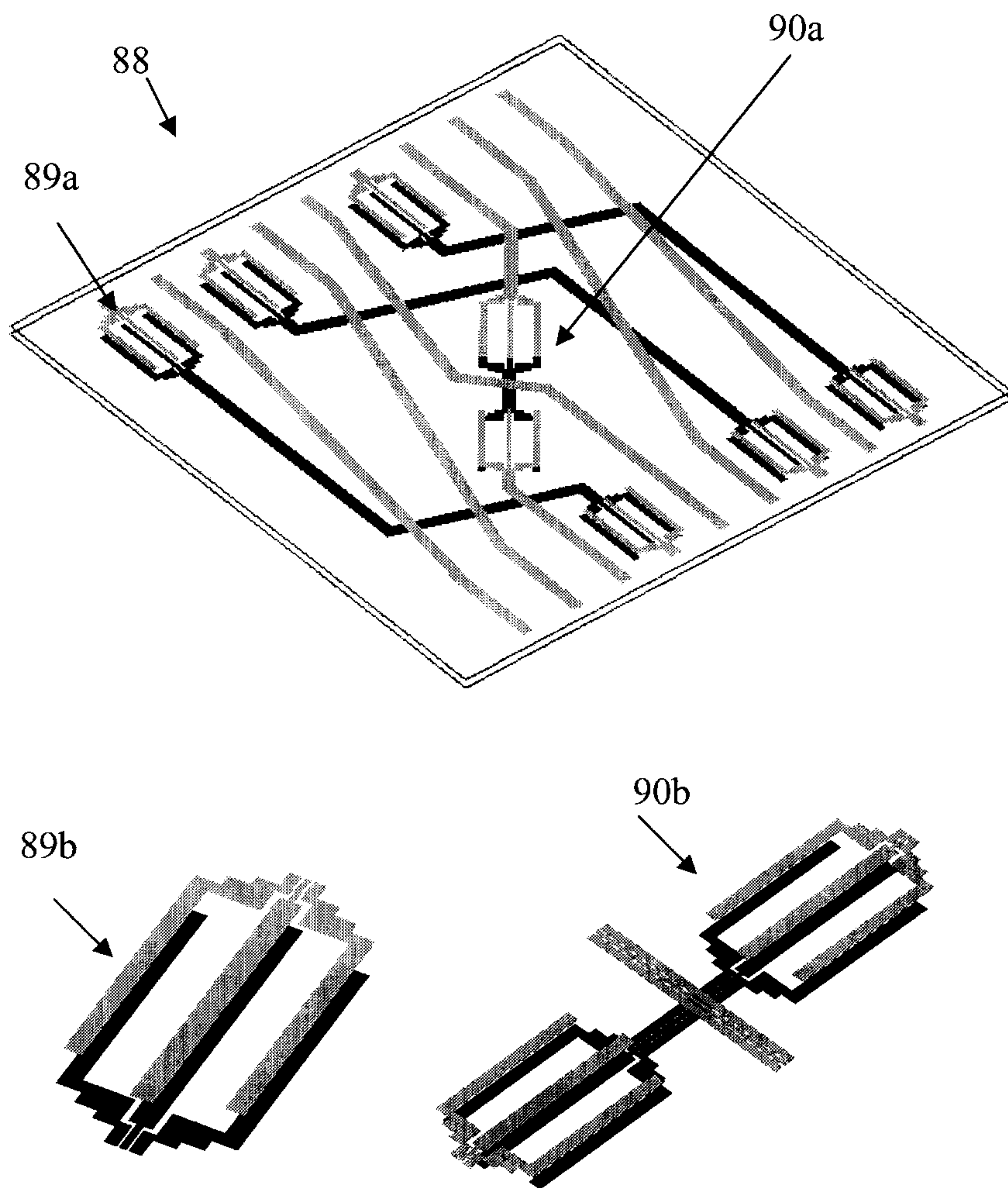
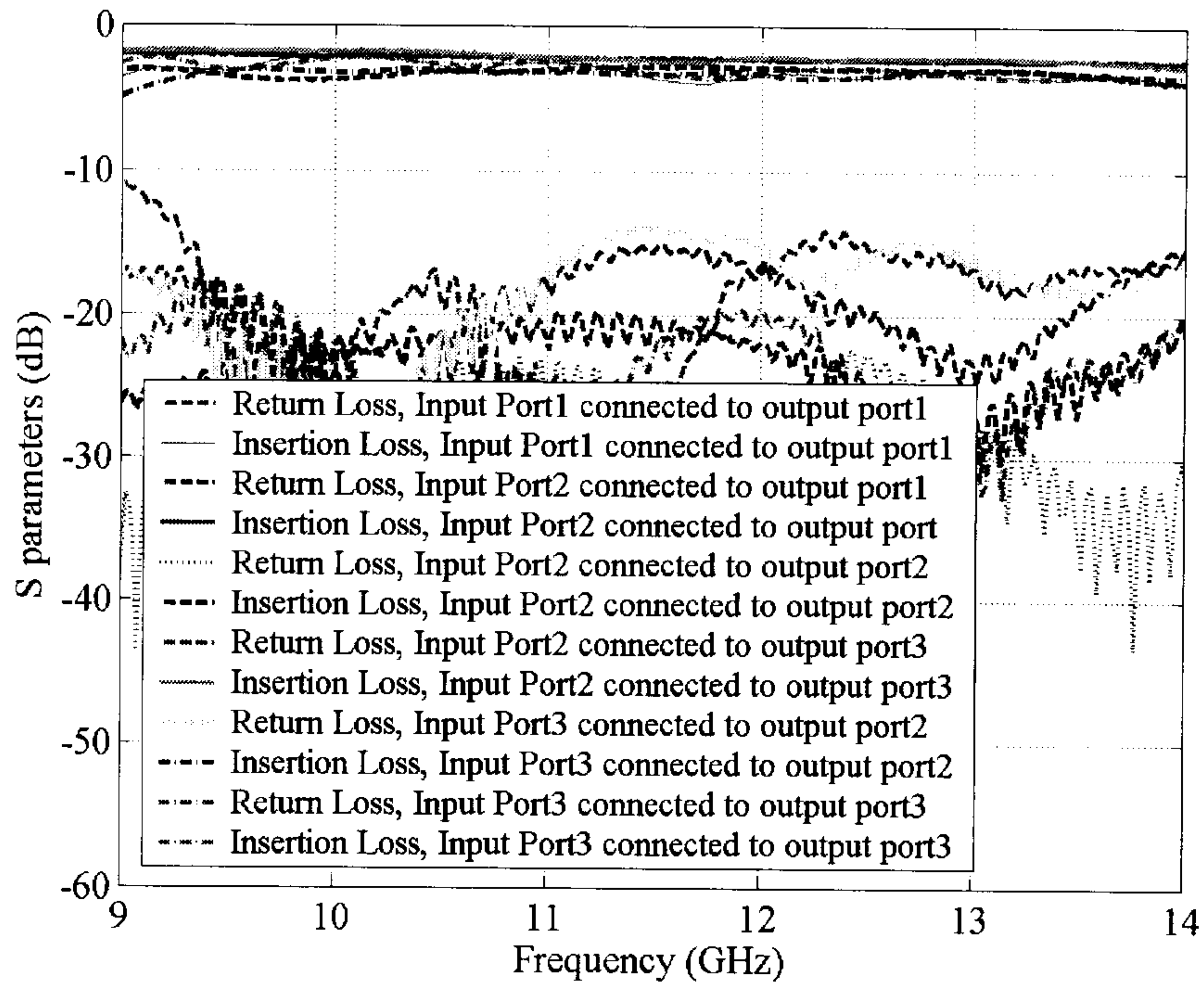
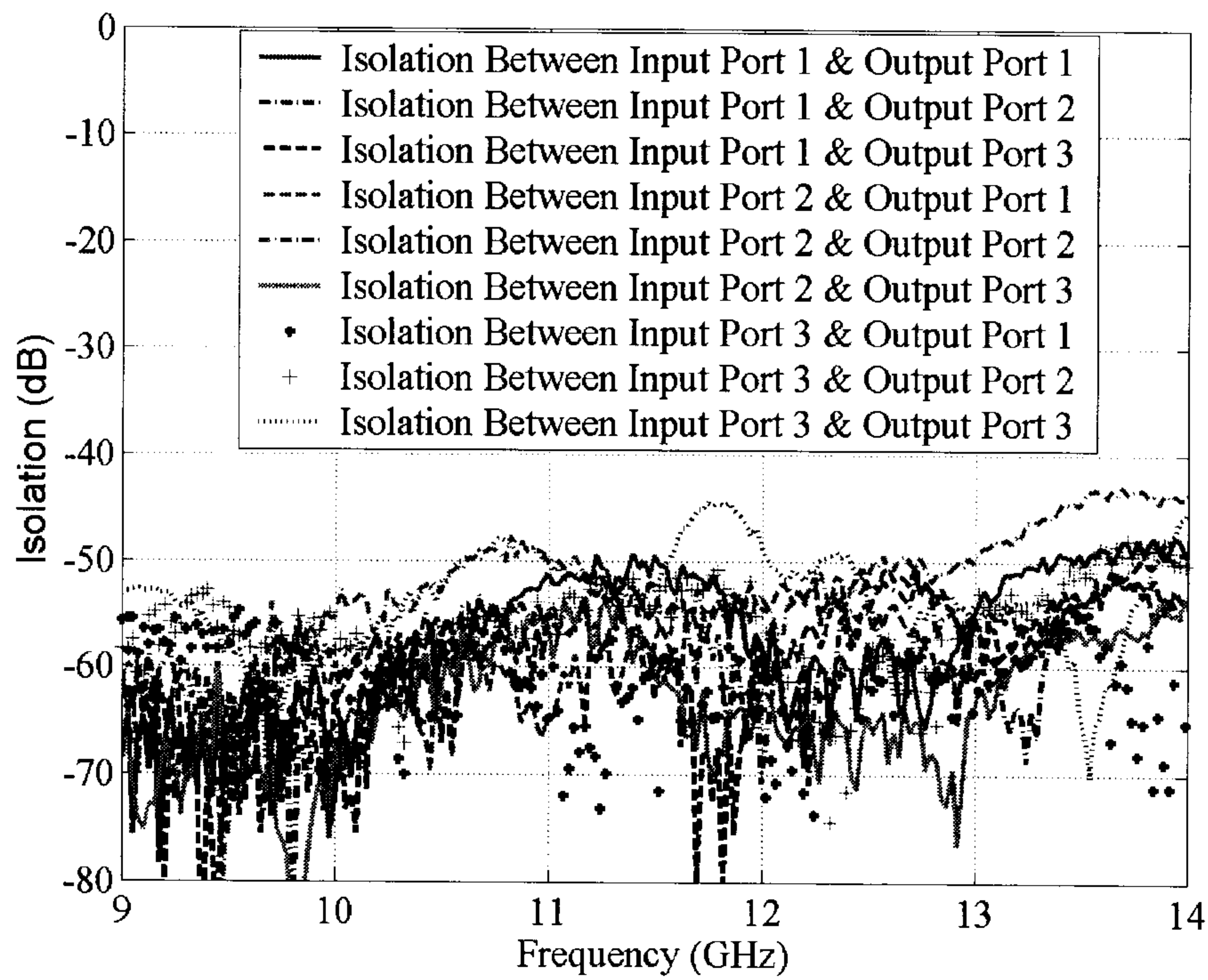


Figure 14





(a)



(b)

Figure 16.

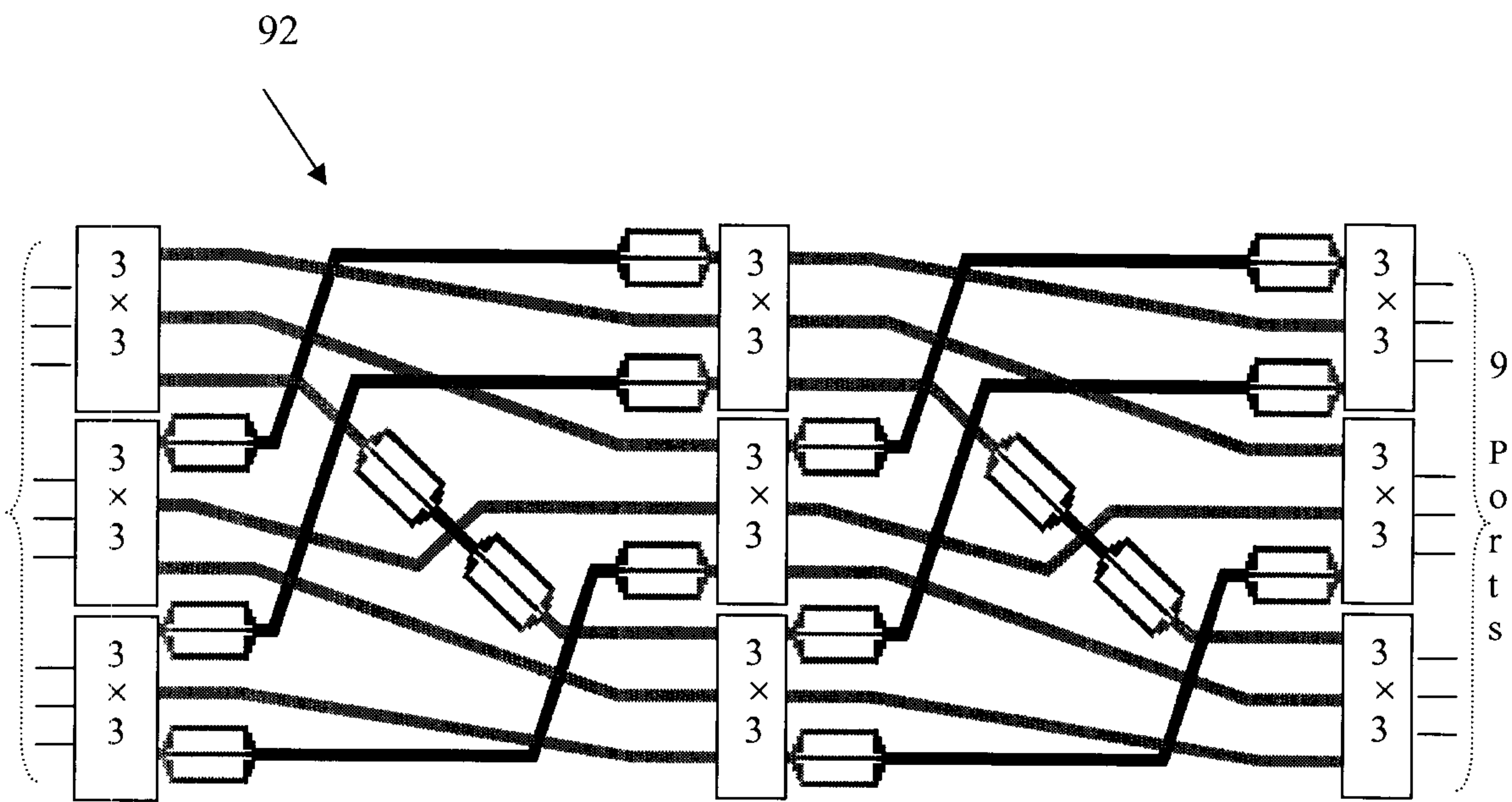
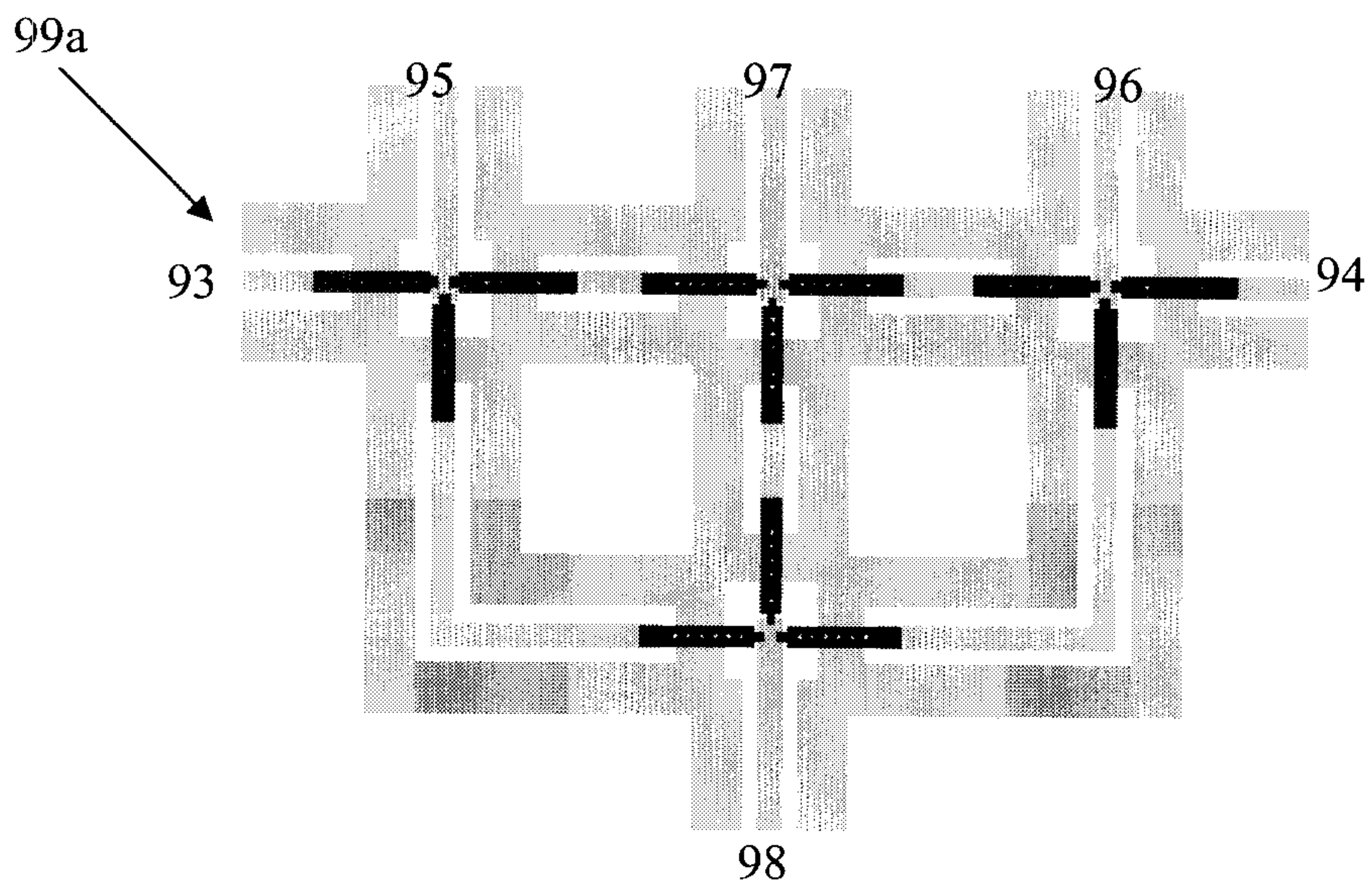
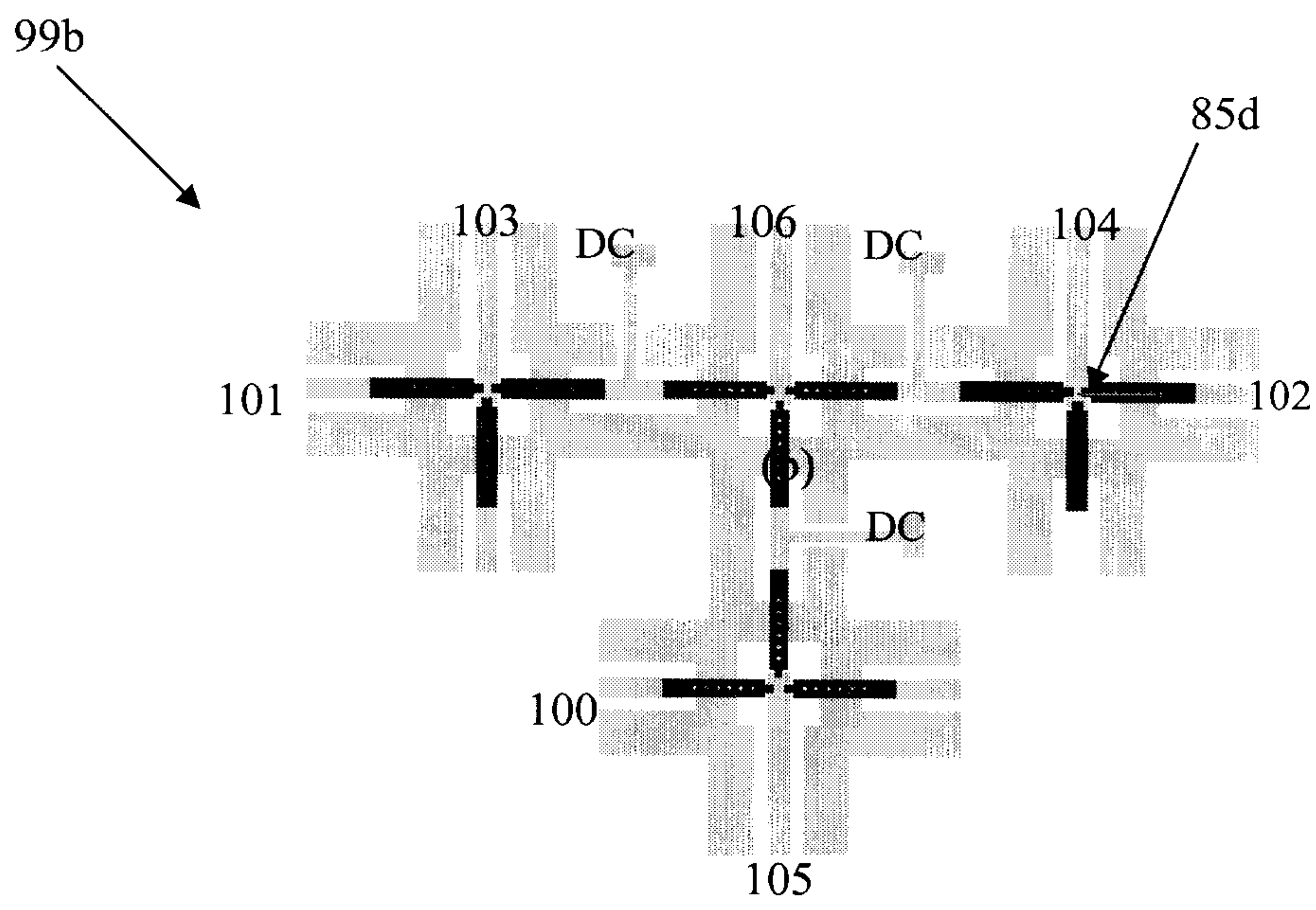


Figure 17



(a)



(b)

Figure 18

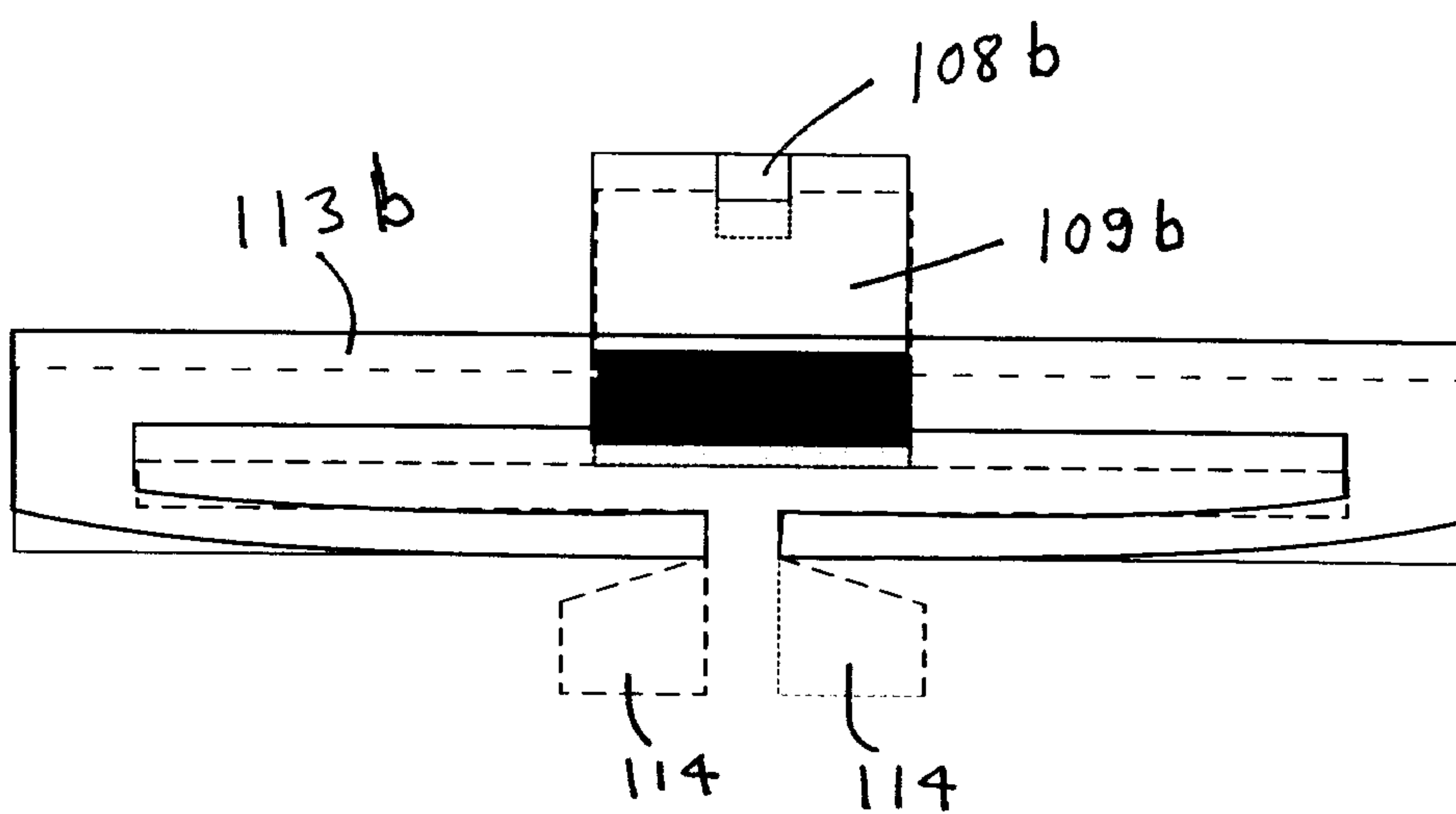


FIGURE 19(C)

