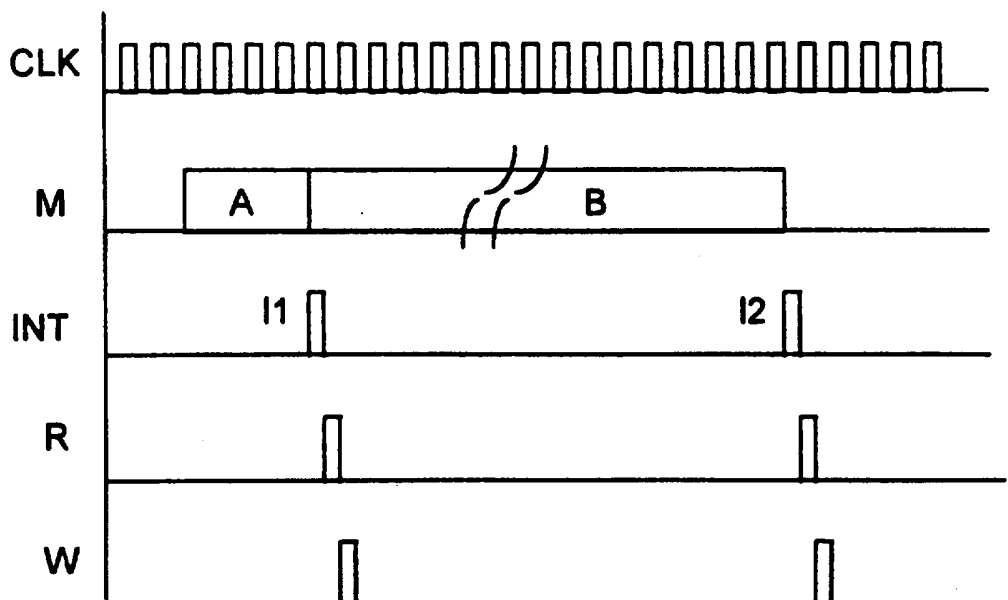




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(54) Title: COMMUNICATIONS PROTOCOL



(57) Abstract
Communications protocol of the bidirectional synchronous type based on interruptions, applicable to digital systems for controlling the transmission of messages between a peripheral terminal unit and a set of subscriber terminal units. This protocol makes use of a single type of interruption, in which the types of message employed comprises a fixed length field (A) in which is indicated, at least, the subscriber terminal unit sending the message and its length and in which, during the complete reception of each message, only two interruption signals (I1, I2) are generated regardless of the number of bits that constitute the message (M). The first interruption signal (I1) is generated when the fixed length field (A) of the message is received, and the second interruption signal (I2) on reception of the rest (B) of the complete message, the length of which has been previously indicated in the fixed length field (A) of the message (M).

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COMMUNICATIONS PROTOCOL

OBJECT OF THE INVENTION

This invention refers to a communications protocol of the bidirectional synchronous type based on interruptions that makes use of a single type of interruption signal, and it is of particular application in digital systems for controlling the transmission of messages between a central control unit of peripheral terminal units and a set of subscriber terminal units connected to these, the working rate of the central control unit of the peripheral terminal unit being greater than that of the subscriber terminal units.

BACKGROUND OF THE INVENTION

In communications systems, message transmission control is carried out by interface devices that relieve the microprocessor of this workload. To do this, use is made of different types of interface devices such as, for example, those known as USARTs (Universal Synchronous Asynchronous Receiver Transmitter) that perform functions of transmitting and receiving messages between the microprocessor and peripheral units; to do this, they admit parallel asynchronous data from the microprocessor and convert them into serial format for continuous synchronous transmission, and vice versa.

The devices of the type mentioned, can be programmed according to the characteristics of the system in question and perform, among others, the functions of series-to-parallel and parallel-to-series conversion, insertion/suppression of start, stop and parity bits, error detection, selection of suitable bit rate, synchronous-to-asynchronous conversion and vice versa, etc.

One such device, the 8251A, is described on pages 2-1 to 2-25 of the book "Microcommunications" by Intel, published by Intel Corporation in 1991, together with how it works.

By generating an interruption this device informs the microprocessor of the messages coming from the transmission medium each time it receives a character formed by a set of between 5 and 8 bits, or informs the microprocessor each time that sending of a character coming from the microprocessor for transmitting over the transmission medium has been concluded. Thus, for the case of messages formed by a large number of bits,

the time employed and the number of times that the microprocessor is interrupted because of the message transmission process are very high, meaning that the efficiency of the microprocessor in carrying out other functions is impaired.

5 As a consequence of all the foregoing, the technical problem to be overcome lies in establishing an effective protocol for controlling the transmission of messages between the peripheral terminal unit and the set of subscriber terminal units, by limiting the number of interruptions that the microprocessor of the central control unit of the peripheral terminal unit
10 receives, reducing to the greatest extent possible the time employed in this process since the working rate of the microprocessor is greater than that of the subscriber terminal units.

CHARACTERISATION OF THE INVENTION

15 This invention concerns a protocol based on interruptions for communications between a peripheral terminal unit, which comprises a central control unit which, in turn, has a microprocessor and an interface module, and a set of subscriber terminal units, this protocol being applicable in digital systems for controlling the transmission of messages originating in these subscriber terminal units. This protocol envisages a
20 single type of interruption signal for all possible interruptions.

 To execute this protocol, the messages include a fixed length field in which is indicated the subscriber terminal unit sending the message and its length, such that the interface module generates a first interruption signal for the microprocessor, informing that the field mentioned has been
25 received. This is read and interpreted by the microprocessor which then indicates to the interface module the length of the message still to arrive, whereby the interface module can generate a second interruption signal when the complete message is received.

 The advantages of employing this protocol lie in the lower workload
30 on the microprocessor through the reduction in the number of interruptions in the message reception process from the subscriber terminal units since, regardless of their length, it will only be interrupted twice by the interface module, implying lower process-associated time and thereby permitting the microprocessor to perform other tasks during the message reception
35 process.

BRIEF FOOTNOTES TO THE FIGURES

A fuller explanation of the invention is to be found in the following description of a preferred implementation based on the figures attached, in which:

5 - figure 1 illustrates graphically the system in which the communications protocol object of this invention has been implemented,

 - figure 2 shows the structure of the peripheral terminal unit, at functional block level, which permits access of the subscribers to the system through the subscriber terminal units that act as synchronous interfaces
10 with the subscribers,

 - figure 3 shows the signal interchange between the microprocessor and the interface module of the central control unit, and of the latter with the subscriber terminal units, and

 - figure 4 shows the generation of the interruption signals, and the
15 read and write commands produced in the message reception control process.

DESCRIPTION OF AN IMPLEMENTATION OF THE INVENTION

The diagram in figure 1 illustrates the system in which the communications protocol for controlling the transmission of messages
20 object of this invention has been implemented, and which refers to a point-to-multipoint radio access system to provide subscribers with access to the fixed telephone network.

This system includes a central unit UC that permits access of the system to the fixed network, a set of peripheral nodal units UPN, and a set
25 of peripheral terminal units UPT. The peripheral nodal units UPN are connected to the central unit UC directly by radio or through other peripheral nodal units UPN, and the peripheral terminal units UPT are connected directly to the central unit UC or indirectly through one or more peripheral nodal units UPN, such that the subscribers S1,...,Sn can have
30 access to the fixed network through the system described by connecting to the peripheral nodal units UPN or to the peripheral terminal units UPT.

Communication between one of the peripheral units UPT, UPN and the central unit UC or between each of the peripheral units UPT,UPN and the subscribers S1,...,Sn can be set up on a permanent basis or on request, in
35 other words, the communication is established as a result of a

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communication request generated by a subscriber S_1, \dots, S_n or by a peripheral unit UPT, UPN.

Both the central unit UC and peripheral nodal units UPN and peripheral terminal units UPT, as can be seen for the latter case in figure 2, incorporate a central control unit RCI for controlling the transmission of messages, which has a microprocessor MC and an interface module IF that serve to control the reception of messages from a set of subscriber terminal units RPU_1, \dots, RPU_m that provide final access for subscribers S_1, \dots, S_n .

Figure 3 shows the signal interchange between the microprocessor MC and the interface module IF, and of the latter with the subscriber terminal units RPU_1, \dots, RPU_m . The microprocessor MC and the interface module IF are connected by means of an address bus AD, a data bus D, two read and write microcommand lines R and W respectively, and an interruption line INT. There is also a control interface that handles the signalling information of this central control unit RCI with the subscriber terminal units RPU_1, \dots, RPU_m which is managed by the interface module IF which has a clock signal CLK at 2 Mbit/s, a frame synchronising signal SINC at 8 kHz, and two data signals, one for the downstream direction DNS from the interface module IF of the central control unit RCI to the subscriber terminal units RPU_1, \dots, RPU_m , and the other for the upstream direction UPS from the subscriber terminal units RPU_1, \dots, RPU_m to the interface module IF of the central control unit RCI.

As is shown in figure 4, the messages M that are transmitted between a peripheral terminal unit UPT and a set of subscriber terminal units RPU_1, \dots, RPU_m comprise a first field of fixed length A, in which is to be found the information relative to the total message length as well as information on the identity of the subscriber terminal unit originating the message. A second field of variable length B contains the actual message information. In this implementation of the protocol, the fixed length field A of the messages interchanged between the central control unit RCI and the subscriber terminal units RPU_1, \dots, RPU_m is formed by the first two bytes of the message.

The central unit UC also comprises other interfaces (not shown) through which the data pass, as well as for communication with the other subsystems in the peripheral terminal unit UPT like, for example, the

transceiver and baseband subsystem RTX/SBB.

The implementation of the protocol, of the semi-duplex type, object of this invention, has been made at the control interface of the central control unit RCI, for controlling the transmission of messages between the
5 central control unit RCI and the subscriber terminal units RPU1,...,RPUm.

By means of this interface the message transmission control traffic is set up between this central control unit RCI and the subscriber terminal units RPU1,...,RPUm via the interface circuit IF incorporated in the central control unit RCI. At the control interface of the central control unit RCI with
10 the peripheral subscriber units RPU1,...,RPUm, the frames are divided into 32 channels of 64 kbit/s, the first of which is used by the communications protocol object of his invention for controlling the transmission of messages. The rest of the channels in both directions are used for establishing communications between subscribers to the same peripheral terminal unit
15 UPT.

Connected to the interface module IF are up to a maximum of ten subscriber terminal units RPU1,...,RPUm and an additional subscriber terminal unit RLT, for test purposes, is also connected through this control interface to the central control unit RCI. Each subscriber terminal unit
20 RPU1,...,RPUm can handle access for up to eight subscribers S1,...,Sn.

During idle periods, the central control unit RCI is continuously transmitting 8-bit downstream signals DNS from the interface module IF of the central control unit RCI to the subscriber terminal units RPU1,...,RPUm, to permit these units to remain synchronised. When there is no activity, no
25 subscriber terminal unit RPU1,...,RPUm accesses the bus that connects it to the central control unit RCI. When any of the subscriber terminal units RPU1,...,RPUm wishes to transmit a message M, it must send at least one upstream signal UPS to the central control unit RCI to permit its synchronisation and, thereby, correct reception of this message M. The
30 subscriber terminal units RPU1,...,RPUm only send answering messages to interrogation messages made from the central control unit RCI avoiding, in this way, the possibility of collisions in accessing it.

The protocol starts in an idle state in which no messages are being transmitted or received. When it is desired to set up the communication, the
35 microprocessor MC of the central control unit RCI writes the complete

message M to be transmitted into a memory of the interface module IF and sends a request to send to the subscriber terminal unit RPU1,...,RPUm previously selected by it, the protocol progressing to a transmit state.

5 The transmission of messages M is done byte by byte adding a parity bit to each of these at a transmission rate of 64 kbit/s, though the number of bytes transmitted can be adapted to the working rate of the subscriber terminal units RPU1,...,RPUm.

10 There are two types of transmitted messages M: those that do not provoke an answer in the peripheral subscriber units RPU1,...,RPUm, and those that do. If the message is of the type that does not provoke an answer, the protocol progresses from the transmit state to an idle state once the transmission has concluded, and the interface module IF interrupts the microprocessor MC, informing it that the message transmission has ended and, in addition, there appears information in the states register of the interface module IF that this message does not provoke an answer.

15 If it is a message that provokes an answer, the protocol progresses from the transmit state to a state of waiting for the interface module IF to receive the first byte. There is a maximum time-out set in a supervision counter present in this module; once the time set has elapsed without the first message byte having been received, an interruption signal is applied to the microprocessor MC and the protocol returns to the idle state and a message appears in the states register of the interface module IF indicating that the waiting time has expired.

20 If the first byte is received correctly within a period of time less than that set in the supervision counter of the interface module IF for the maximum time-out, the protocol progresses to a second byte waiting state; once the second byte of the message has been received correctly, the protocol progresses to a two first bytes received state, and the interface module IF generates the first interruption signal I1 of the only two signals possible due to the message reception process and transmits it to the microprocessor MC. The states register of the interface module IF contains a message indicating the reception of the two first bytes. These two first bytes, which are stored in the memory of the interface module IF and form a fixed length field A, include the information concerning the length of the complete message to be received and from where it is coming.

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The microprocessor MC of the central control unit RCI then sends a read command R of the two bytes stored in the memory of the interface module IF and, once read, interprets them and informs the interface module IF of the bytes in the rest B of the message that has still to be received before
5 reception of the message M is completed; the interface module IF continues receiving and storing in its memory the bytes coming from the selected subscriber terminal unit RPU1,...,RPUm until the message M has been fully received, in accordance with the information that has been supplied to it by the microprocessor MC.

10 When the message M has been fully received, the protocol progresses to the idle state, and the interface module IF generates the second interruption signal I2 originated by the message reception process and information confirming the complete and correct reception of the message will appear in the states register of the interface module IF of the central
15 control unit RCI. At this moment the microprocessor MC can read the rest B of the message.

In the event that the message M is only formed by two bytes, the second interruption signal I2 that is applied to the microprocessor MC originated by the message reception process is not generated, since these
20 bytes have already been read by the microprocessor MC.

In the waiting states for the second byte and for the two first bytes received, the supervision counter of the interface module IF controls the time elapsed from the reception of the last byte until the reception of the next one, so that if this time exceeds the maximum time-out associated with
25 these states, the protocol progressed to an error state, the states register of the interface module IF containing the information that reception has been interrupted. If the protocol has progressed to an error state, then the microprocessor MC inputs a value to the supervision counter of the interface module IF and, once completed, the protocol progresses to the idle
30 state, generating an interruption signal for the microprocessor MC and the states register of the interface module IF will contain a message informing that the time allocated as a safety interval has expired. Once the protocol has progressed to the idle state and the microprocessor MC has read the message received M, it is possible to continue with the transmission of a
35 new message M.

CLAIMS

1.- **COMMUNICATIONS PROTOCOL** between a peripheral terminal unit (UPT) and a set of subscriber terminal units (RPU1,...,RPUm), of application in digital systems for controlling transmission of messages (M), **characterised** in that each message (M) comprises a fixed length field (A) in which, at least, is indicated the subscriber terminal unit (RPU1,...,RPUm) sending the message and its length, in such a manner that only two interruption signals (I1,I2) are generated for each message (M), a first one (I1) when the fixed length field (A) is received, and a second one (I2) on receiving the rest (B) of the complete message previously indicated in the fixed length field (A) of message.

2.- **DEVICE** for implementing the protocol of claim 1, **characterised** in that the peripheral terminal unit (UPT) comprises a central control unit (RCI) which, in turn, incorporates a microprocessor (MC) capable of interpreting the messages (M) coming from the subscriber terminal units (RPU1,...,RPUm) and an interface module (IF) between this microprocessor (MC) and the subscriber terminal units (RPU1,...,RPUm); whereby:

- the interface module (IF) receives the messages coming from the subscriber terminal units (RPU1,...,RPUm) and generates a first interruption signal (I1) which is sent to the microprocessor (MC) when reception of the fixed length field (A) of the message has concluded,

- the microprocessor (MC) when it receives this first interruption signal (I1), reads the fixed length field (A) of the message and indicates to the interface module (IF) what is the length of the message that has still to be received (B),

- the interface module (IF) generates a second interruption signal (I2) when it has received the remaining information (B) of the message; and, finally,

- the microprocessor (MC) reads the remaining information (B) of the message stored in the interface module (IF).

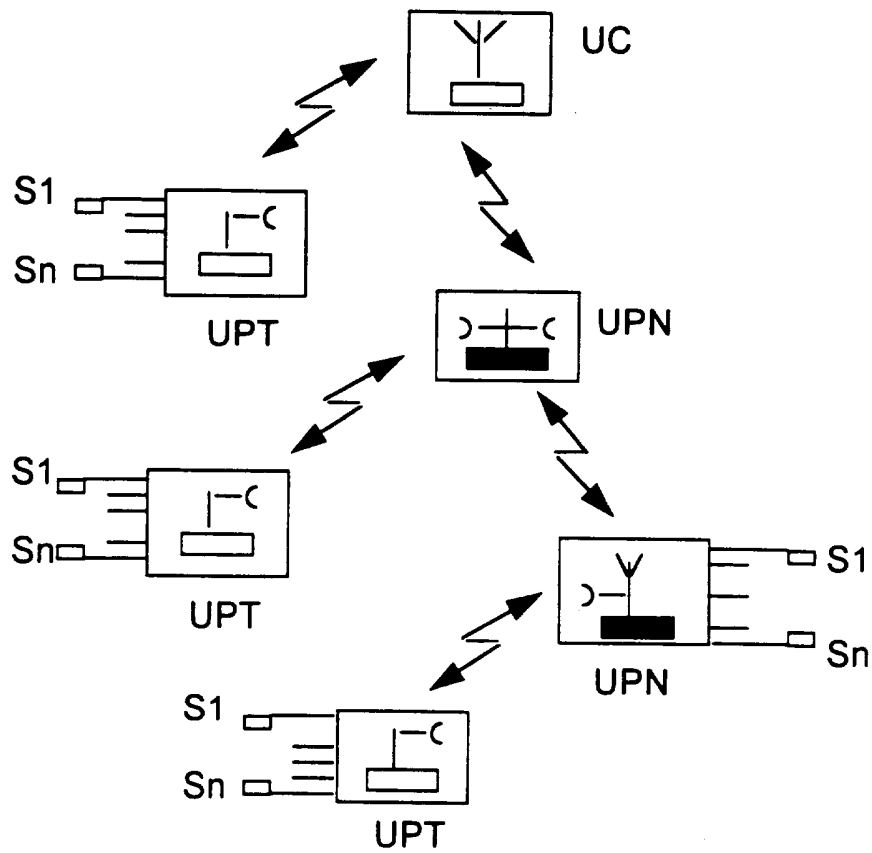


Fig. 1

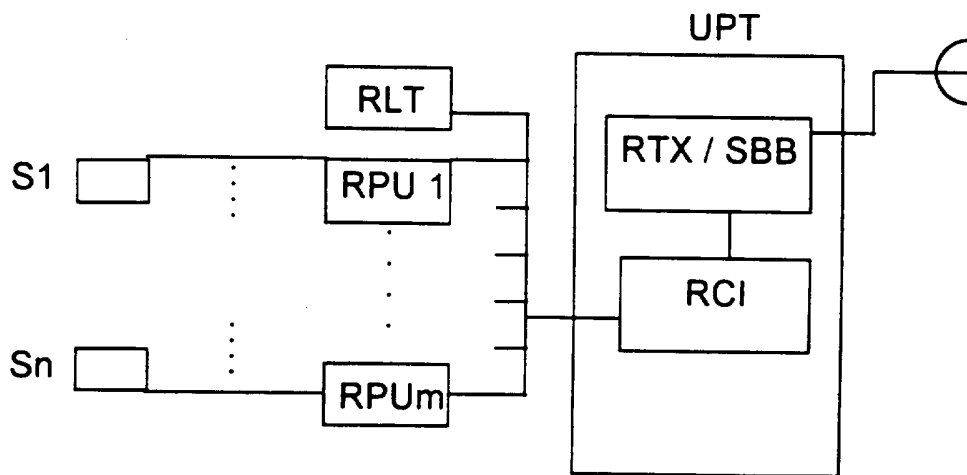


Fig. 2

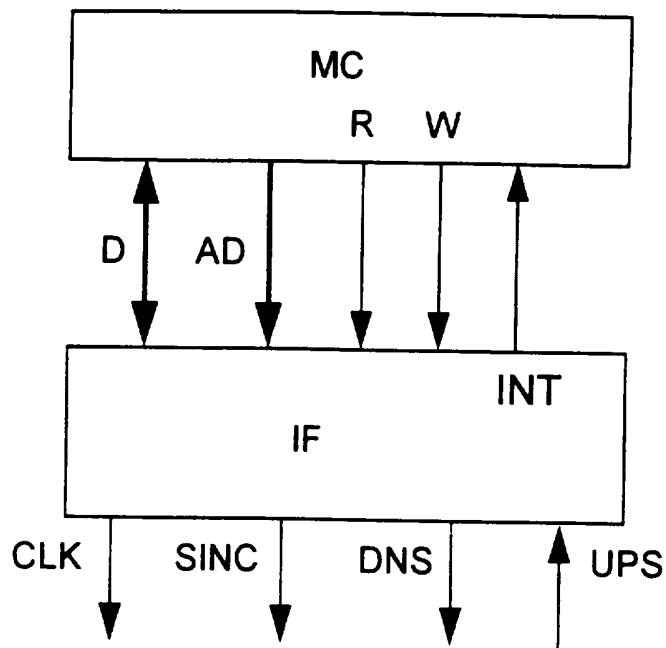


Fig. 3

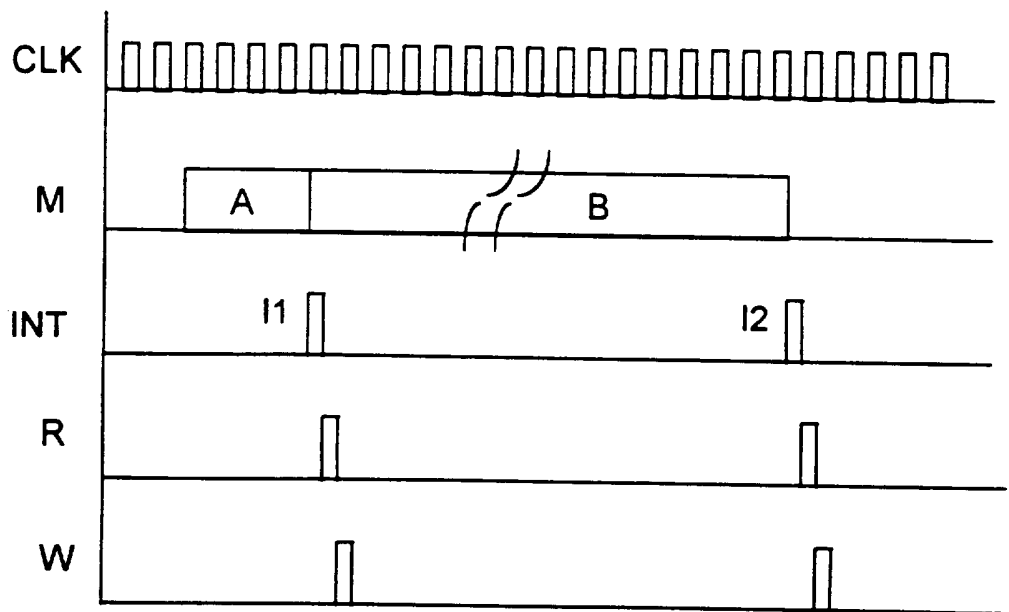


Fig. 4

INTERNATIONAL SEARCH REPORT

International Application No

PCT/EP 95/04132

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04L29/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H04L

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|------------|---|-----------------------|
| X | EP,A,0 577 115 (3COM CORP.) 5 January 1994 see column 1, line 36 - column 2, line 12 see column 3, line 35 - column 4, line 12 --- | 1,2 |
| X | WO,A,94 07201 (3COM CORP.) 31 March 1994 see page 3, line 5 - page 5, line 7 see page 49, line 5 - page 52, line 12 see figure 13 --- | 1,2 |
| A | WO,A,93 09623 (NOKIA TELECOMMUNICATIONS OY) 13 May 1993 see abstract see page 2, line 11 - page 3, line 16 ----- | 1,2 |

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Information on patent family members

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