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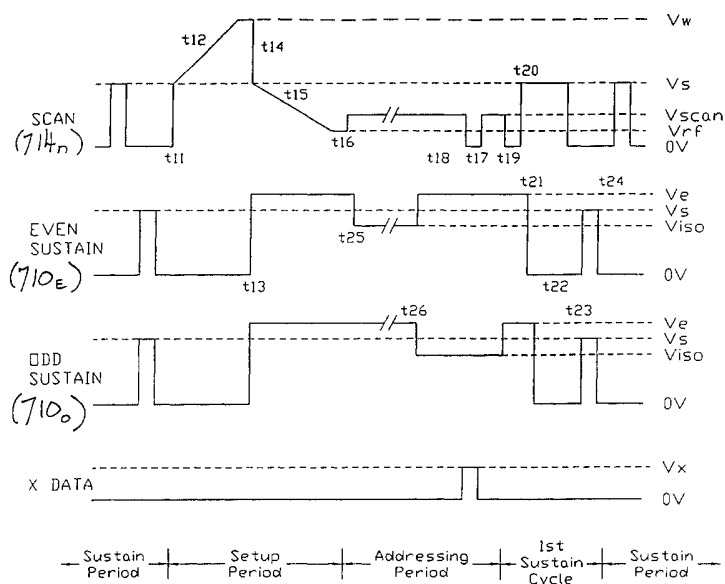
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(54) Title: SUPPRESSION OF VERTICAL CROSSTALK IN A PLASMA DISPLAY PANEL



(57) Abstract: There is provided a method for reducing the probability of the occurrence of vertical crosstalk in a plasma display panel having a paired electrode configuration wherein sustain electrodes are arranged as pairs on the display panel. Each of pair of electrodes comprises a first electrode (7100) which is odd and a second electrode (710E) which is one. The method involves enabling a first sustain electrode to produce an addressing discharge while disabling the second sustain electrode during the time in which said addressing discharge is being produced. A discharge is produced by application of a first voltage (Ve). In order to disable the second electrode during discharge, the voltage difference between the second electrode (710E) and the scan electrode (714n) is reduced by application of an isolation voltage (Viso).



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SUPPRESSION OF VERTICAL CROSSTALK IN A PLASMA DISPLAY PANEL

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BACKGROUND OF THE INVENTION

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1. Field of the Invention

The present invention relates to plasma display panels (PDPs), and more particularly, to an electronic waveform technique that minimizes vertical crosstalk
15 in a PDP.

2. Background of the Art

Color PDPs are well known. Fig. 1 illustrates a prior art embodiment of a
20 color alternating current (AC) PDP, as disclosed in US Patent No. 6,118,214 to
Marcotte (hereinafter "the Marcotte '214 patent"), which is incorporated herein by
reference. Transparent electrodes 11 are employed on a front panel. A front plate
(not shown) includes horizontal plural pairs of sustain electrodes 10 that connect
transparent electrodes 11 to a sustain bus 12. A plurality of pairs of scan
25 electrodes 14 are juxtaposed to paired sustain electrodes 10, and both electrode
sets are covered by a dielectric layer (not shown) and a magnesium oxide (MgO)
layer (not shown). A back plate (not shown) supports vertical barrier ribs 16 and
plural vertical column electrodes 18 (shown in phantom). Individual column
electrodes 18 are covered with red, green, or blue (RGB) phosphors, as the case
30 may be, to enable a full color display to be achieved. The front and rear plates are
sealed together and a space therebetween is filled with a dischargeable gas.

An electrode pair is defined as (a) a sustain electrode 10 (and its adjacent transparent electrode 11) juxtaposed with (b) a scan electrode 14 (and its adjacent transparent electrode 11). A pixel 20 is defined as an area that includes
5 intersections of (i) an electrode pair of sustain electrode 10 and scan electrode 14 on the front panel, and (ii) three column electrodes 18 for red, green, and blue, respectively, on the back panel. A subpixel corresponds to an intersection of a red, green or blue column electrode with an electrode pair of a sustain electrode and a scan electrode. For example, subpixel 19 corresponds to an intersection of a
10 red column electrode 18 with an electrode pair of sustain electrode 10 and scan electrode 14.

Operating voltage and power of the PDP are controlled by a discharge gap 13 and a width of transparent electrode 11. The operating voltage of the PDP is
15 controlled by the distance across the discharge gap 13, as the distance controls the breakdown voltage for a given gas mixture. Furthermore, sufficient voltage must be applied so that the ensuing gas discharge plasma is able to fully engulf the scan and sustain electrode pair. The power consumed by the discharge is affected by the surface capacitance of the electrode pair, which is proportional to electrode
20 area and inversely proportional to the dielectric thickness.

A width of sustain electrode 10 and a width of scan electrode 14 are chosen to produce a narrow discharge gap 13 and a wide inter-pixel gap 15. When sufficient voltage is applied across discharge gap 13, the gas will break down
25 forming a discharge plasma. For a given applied voltage, the positively charged electrode is the anode and the negatively charged electrode is the cathode. The discharge plasma has two distinct regions, the positive column and the negative glow. The positive column consists predominantly of fast moving electrons seeking the positive charge on the surface of the anode electrode. Conversely, the
30 negative glow contains slow moving ions drifting toward and across the negatively charged cathode electrode. The duration of the discharge is limited by the amount

of charge on the dielectric surfaces. Once the charge has been neutralized the discharge self-extinguishes. Within a sustain time period, this process is repeated by alternating the voltage polarity after each discharge completes. Inter-pixel gap 15 must be made sufficiently large to prevent the energetic positive column of the plasma discharge from bridging the inter-pixel gap and corrupting an ON or OFF state of an adjacent pixel. The width of the transparent electrode 11 and the thickness of a dielectric glass (not shown) over the electrode determine the pixel's discharge capacitance, which controls the discharge power and therefore brightness. For a given discharge power/brightness, a number of discharges is 10 chosen within sustain time periods to provide gray scales which sum to meet the overall brightness requirement for the panel.

Fig. 2 shows a typical prior art block diagram of a PDP system 200. An analog video signal is input into logic 230 where the signal is digitized, processed, 15 and temporarily stored. Once a frame's worth of data is stored, logic 230 begins a process of displaying data through a series of subfields, typically 8 to 12, as disclosed in US Patent No. 5,724,054 to Shinoda.

Fig. 3 is a graph showing a division of a frame time into 8 subfields (i.e., 20 SF1 - SF8). During each addressing period lines Y1 through Y480 are scanned sequentially by row drivers 210, while video input is applied through column drivers 225 to set each sub-pixel in the ON state as required by the video input. Each subsequent sustain period is weighted with sustain pulses to achieve weighted light intensities for each subfield.

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Fig. 4 shows a typical division of a subfield. Each subfield has a setup period, an addressing period, and a sustain period. The setup period turns off any ON pixels, primes the MgO layer, and sets up all the pixels for addressing. Referring to both Fig. 2 and Fig. 4, during the addressing period, a scan generator 30 205, in conjunction with row drivers 210, sequentially drives each row low for addressing. Once a given row is enabled, logic 230 loads column drivers 225 with

image data corresponding to individual RGB sub-pixels requiring illumination based upon received image data. Column drivers 225 apply voltage V_x to selected column electrodes. The coincidence of a selected row and an applied column voltage initiates a weak discharge that cascades into a discharge between the selected scan electrode and its neighboring sustain electrode. Once completed, the discharge has placed the addressed sub-pixel in the ON state. Any column not driven will remain in the OFF state. While the addressing discharge does produce visible light, it is not of sufficient brightness to represent the image properly. Consequently, a sustain period follows the addressing period after the last row has been addressed. During the sustain period, scan generator 205 and a sustain generator 220 supply alternating sustain pulses so that a momentary ac-plasma discharge occurs on an application of each pulse. Each sustain discharge produces ultra violet light the excites surrounding phosphor to produce visible light. Each subfield within a frame contains a sufficient number of sustain pulses and in-turn discharges to achieve a desired brightness for each subfield. Since each sub-pixel can be addressed independently in each subfield, a large color palate is obtainable.

Fig. 5a shows a prior art composite waveform between the scan and sustain electrodes. Due to a capacitive relationship of the scan and sustain electrodes, the composite waveform is simply an output of scan generator 205 (Fig. 4 Scan waveform), minus an output of sustain generator 220 (Fig. 4 Sustain waveform). Note that applied data pulses are not included in Fig 5a.

Figs. 5b - 5e show wall voltage waveforms for each pixel addressing sequence. A wall voltage is an AC coupled voltage present on a gas side of a dielectric layer. The wall voltage is limited, positive and negative, by a breakdown voltage of the gas, V_{br} and $-V_{br}$.

When the breakdown voltage is exceeded in either direction, two types of discharges can occur, a well-known negative resistance discharge and a more recently discovered positive resistance discharge. According to US Patent No.

5,745,086 to Weber, and referring to Fig. 4, if an applied waveform rises or falls slowly, as in rising and falling ramps of the setup period t12 and t15, the gas will discharge having a positive resistance characteristic, behaving much like a zener diode limiting the voltage across the gas to the breakdown voltage V_{br} . If the applied voltage exceeds the breakdown voltage sharply, as in the sustain periods t23, t24, a negative resistance or avalanche discharge occurs, which reduces the wall voltage to zero. Once the wall voltage reaches zero, the discharge self extinguishes.

10 The addressing discharge is also a negative resistance discharge, exhibiting the characteristics of a positive column discharge as disclosed in US Patent No. 6,184,848 to Weber (hereinafter “the Weber ‘848 patent”). The Weber ‘848 patent defines the positive column discharge as having a trigger cell and a state cell. A panel topology is similar to that of Fig. 1, but less transparent electrodes
15 11 thereby creating a large discharge gap. In the presence of a high wall voltage, due to an application of sustain pulses following an addressing operation, a weak discharge forms between a positively charged back plate electrode and a negatively charged front electrode. This intersection is said to be a trigger cell. The weak discharge, in conjunction with the high wall voltage, yields a discharge
20 where the plasma forms two clearly distinct regions, a negative glow and a positive column. The negative glow consists of slow moving positively charged ions, and the positive column consists of slow moving ions and rapidly moving electrons. The electrons move toward the positively charged anode, and the ions drift slowly toward the negatively charged cathode. As the weak discharge
25 strengthens, the negative glow expands about the trigger cell, and the positive column spreads along the back plate’s phosphor layer to the positively charged state cell. The discharge completes when the charge is neutralized between the trigger cell and the state cell.

30 For the addressing discharge, the intersection of the column electrode and the selected scan electrode forms the trigger cell, and the corresponding sustain

electrode intersecting with the same column electrode forms the state cell. At the completion of the setup period t_{16} , each pixel is setup so that wall voltage is at the discharge level $-V_{br}$. When the pixel is addressed, a weak discharge forms at the intersection of the selected scan electrode and at each of the driven back plate column electrodes. The discharge develops producing a positive column which spreads along the positively charged back plate electrode to the positively charged sustain electrode. The discharge then consumes the charge on the sustain electrode, reducing the wall voltage to zero.

10 Fig. 5b shows wall voltages for a previously OFF pixel, which is setup for addressing, not addressed, and remains OFF in a latter sustain period. Specifically, a rising ramp t_{12} in a setup period rises, bringing the wall voltage above the breakdown voltage and clamps the wall voltage at V_{br} . Voltage V_e being applied at t_{13} , as shown in Fig. 4, ensures that an address discharge will be strong enough for a first sustain discharge to occur properly. Increasing voltage V_e effectively makes the first sustain discharge stronger. A transition into the falling ramp t_{13} and t_{14} reverses the wall voltage and the falling ramp t_{15} clamps the wall voltage at $-V_{br}$. At the conclusion of the setup period, the wall voltage is at $-V_{br}$. A row select pulse at time t_{17} in Fig. 4 exceeds the breakdown voltage slightly due to a difference between V_{rf} and $0V$. Since the falling ramp during time t_{15} stops at V_{rf} above $0V$, a small negative voltage is effectively applied when the row select pulse is applied at time t_{17} to exceed the breakdown voltage $-V_{br}$. Since this effective negative voltage, caused by V_{rf} is small and the width of the row select pulse at t_{17} is narrow, no discharge activity occurs unless there is a video input dictated data pulse on a data electrode coincident with the row select pulse at time t_{17} as shown in Fig. 4. In Fig. 5b, no data pulse is applied, and so there is no discharge activity at time t_{17} . Since an address discharge did not occur, the wall voltage produced by the first sustain pulse at t_{21} is not greater the positive breakdown voltage V_{br} and no sustain discharge will occur.

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Fig. 5c shows the turn-on process for an OFF pixel. The setup period occurs as in Fig. 5b and a data pulse (not shown) is applied to the columns at time t17 triggering an address discharge which returns the wall voltage to zero. Later at time t21, after the remaining rows have been addressed, the first sustain discharge will occur on any pixel which was addressed. For the first sustain pulse, the scan electrode is driven high before lowering the sustain electrodes, unlike subsequent sustain pulses. This method of generating the first discharge prevents a premature discharge, which can form if the sustain electrode voltage of V_e , 220V is lowered before raising the scan electrode voltage to sustain voltage V_s , 180V, due to the application of voltage V_e in the setup period as shown in Fig. 4 during addressing. Having been addressed previously, the breakdown voltage V_{br} is exceeded, and a negative resistance discharge will occur, again returning the wall voltage to zero. Each subsequent sustain pulse initiates another discharge producing the light of an ON pixel.

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Following the first sustain discharge, the falling edge of the scan electrodes lowers the wall voltage towards the negative breakdown voltage $-V_{br}$. The subsequent rise of the other sustain electrodes adds more voltage across the gas and exceeds the breakdown voltage $-V_{br}$, producing the next discharge. This process continues for the duration of the sustain period with the discharges alternating back and forth.

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Fig. 5d shows a re-addressing of an ON pixel. The application of the setup pulse at time t11 causes the last negative resistance discharge of the previous subfield's sustain period. Since the wall voltage was returned to zero by the discharge, the rising ramp at t12 will not discharge since the rising wall voltage does not exceed V_{br} . The falling ramp limits the wall voltage to $-V_{br}$, as it did in Figs. 5b and 5c. At time t17, a data pulse is applied with the row select, a discharge occurs, and the pixel is returned to the ON state.

30

Fig. 5e shows an ON pixel which is erased by the falling ramp t15 as in Fig. 5d, however it is not re-addressed, and is OFF in the latter sustain period.

As disclosed in the Marcotte '214 patent, the paired front plate electrode configuration of Fig. 1 has the advantage of reduced inter-electrode capacitance, which reduces the power dissipation resulting from charging and discharging of the inter-electrode capacitance with each sustain pulse. However, there is an increased probability of vertical crosstalk. Vertical crosstalk occurs when a discharge at one discharge site spreads into a vertically adjacent discharge site. The Marcotte '214 patent utilizes a large inter-pixel gap to help increase vertical pixel-to-pixel isolation. Note that the back plate barrier ribs provide horizontal pixel isolation but no vertical isolation. The greatest probability of crosstalk occurs during the addressing discharge where the plasma discharge forms between a selected scan and data electrodes and the positive column spreads to the sustain electrode.

Fig. 6 shows the time sequenced discharge mechanics for an address discharge showing crosstalk discharge. The pictorial is a cross sectional view the PDP of Fig.1 showing front plate electrodes on top and orthogonally oriented address electrode on the bottom, which is covered by a phosphor layer. P1 refers to the red sub-pixel 19 of Fig. 1 and a vertically adjacent red sub-pixel, P2 with inter-pixel gap 15 separating P1 and P2. The time t0 for each row occurs with the application of the row select pulse at time t17 in conjunction with an applied data pulse to the address electrode. The sub-pixels were setup by the falling ramp applied to the scan electrodes while V_e was applied to the sustain electrodes. This places the negative charge on the scan electrodes and the positive charge on the sustain and back plate electrodes prior to t0. V_{rf} allows the row select pulse to slightly exceed the breakdown voltage to help speed up the address discharge. The application of voltage V_{scan} at time t16, in Fig 4, by the row drivers 210, acts as a row deselect voltage by reducing the negative charge on the non-selected rows so that the wall voltage on the scan electrodes is reduced. This prevents the

addressing of one row from affecting the other rows in the display. The full wall voltage returns at time t_{17} when the row is selected, and the breakdown voltage – V_{br} is exceeded as shown in Fig 5b. The V_{scan} voltage is a de-select voltage and must be high enough to ensure sufficient row to row isolation in the presence of applied column voltages.

If a data pulse is provided, at time t_0 in Fig. 6 a weak discharge forms between the back plate address electrode and the active scan electrode, and at time t_1 , a negative resistance plasma discharge forms. At time t_2 , the availability of positive charge on the sustain electrodes allows the positive column to rapidly engulf the sustain electrode, and at time t_3 can easily spread across the inter-pixel gap to the neighboring sustain electrode and thereby deplete the positive charge of the neighboring pixel P2. When P2's scan electrode is selected and the column electrode is driven, the weak back to front discharge may form, however, without the positive charge on the sustain electrode, the plasma will not form, the scan electrode will maintain its negative charge, and pixel P2 will remain off.

In a paper entitled "Symmetrically driven PDP, with minimized current loops to reduce EMI" by Vossen et al. (hereinafter "the Vossen et al. paper"), there is disclosed the usage of interlaced addressing to reduce crosstalk in a PDP. With interlaced addressing, the odd rows are addressed followed by the even rows. As such, any gas priming resulting from addressing the odd rows will be fully extinguished prior to addressing the even rows. The Vossen et al. paper also talks of a symmetrically sustained PDP that uses the paired electrode configuration described in the Marcotte '214 patent as helping to reduce vertical crosstalk. However, the Vossen et al. paper does not describe or correct for the form of vertical crosstalk described herein. Specifically, the Vossen et al. paper describes addressing with the electrodes configured as non-paired electrodes (i.e., scan, sustain, scan, sustain), which does not have a common potential across an inter-pixel gap during addressing. In the non-paired case, a crosstalk discharge will in

fact go in the wrong direction, discharging to an incorrect sustain electrode. The use of interlaced addressing reduces this likelihood of this artifact.

SUMMARY OF THE INVENTION

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The present invention minimizes crosstalk discharge probability between pixels in a plasma display panel while retaining benefits of a paired electrode configuration. Also, an inter-pixel gap may be reduced to enlarge the pixel size to increase brightness, and the pixel density may be increased to realize a higher resolution display.

The present invention reduces probability of address discharge crosstalk in a paired electrode configuration by reducing voltage on an inactive sustain electrode during addressing. By reducing voltage on the inactive sustain electrode, a positive column formed in an address discharge will not spread across the inter-pixel gap. The sustain electrodes are separated into odd and even row associations. Operation of the setup and sustain cycles is unchanged. During addressing, the odd rows are addressed while the voltage on the even sustain electrodes is reduced. Once addressing of the odd rows is complete, the voltage on the even sustain electrodes is returned high, the voltage on the odd sustain electrodes is reduced, and the even rows are addressed.

In some embodiments of the present invention, the voltage on the inactive sustain electrodes is reduced only during the first half of addressing. In this case, crosstalk will continue to occur during the second half of addressing. However, this is acceptable since the crosstalk results in the inactive cell always being OFF during the sustain period.

The present invention may be applied to any paired electrode configuration independent of setup or sustain waveform variations, provided that the sustain electrodes are high while the scan electrodes are low during addressing, thus

allowing for a discharge to form at the scan electrode, which then spreads to the sustain electrode, neutralizing the voltage therebetween.

The present invention a method for controlling sustain electrodes in a PDP.
5 The method includes enabling a first sustain electrode to produce an addressing discharge, and disabling a second sustain electrode when the first sustain electrode is producing the addressing discharge. The first sustain electrode is adjacent to the second sustain electrode.

10 One embodiment of the invention is a circuit for controlling sustain electrodes in a PDP. The circuit includes an output for enabling a first sustain electrode to produce an addressing discharge, and an output for disabling a second sustain electrode when the first sustain electrode is producing the addressing discharge. The first sustain electrode is adjacent to the second sustain electrode.

15 Another embodiment of the present invention is a system that has a PDP having a first sustain electrode and a second sustain electrode adjacent to the first sustain electrode, and a circuit for (a) enabling the first sustain electrode to produce an addressing discharge, and (b) disabling the second sustain electrode
20 when the first sustain electrode is producing the addressing discharge.

BRIEF DESCRIPTION OF THE DRAWINGS

25 Fig. 1 is a schematic representation of a conventional color PDP.

Fig. 2 is a block diagram of a conventional PDP system.

Fig. 3 is graph showing the division of frame time into 8 subfields.

30 Fig. 4 is a graph of conventional subfield waveforms.

Fig. 5a is a graph of a conventional composite waveform between a scan electrode and a sustain electrode, and Figs. 5b-5e are graphs of conventional wall voltage waveforms for pixel addressing sequences.

5 Fig. 6 is a schematic representation of discharge mechanics for an address discharge showing crosstalk discharge for the PDP of Fig. 1.

Fig. 7 is a schematic representation of a color PDP in accordance with the present invention.

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Fig. 8 is a block diagram of a PDP system in accordance with the present invention.

15 Fig. 9 is a graph of even and odd sustain electrode waveforms for a PDP according to the present invention.

Fig. 10a is a graph of a composite waveform, and Fig. 10b is a graph of a wall voltage waveform, for an even bank of electrodes according to the present invention.

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Fig. 11 is a schematic representation of a cross-sectional view of the odd pixel discharge mechanics according to the present invention.

25 Fig. 12 is a schematic representation of a cross-sectional view of the even pixel discharge mechanics according to the present invention.

Fig. 13 is a graph of an embodiment of the invention utilizing sequential addressing wherein sustain electrodes are enabled in conjunction with their corresponding scan electrodes.

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Fig. 14 is a graph of even and odd sustain electrode waveforms for a PDP, where the sustain electrodes are separated into odd and even sustain buses.

Fig. 15 is a graph of even and odd sustain electrode waveforms for a PDP, where an increased voltage V_f is applied to the odd or even sustain electrode buses.

DESCRIPTION OF THE INVENTION

Fig. 7 is a schematic representation of a portion of a color PDP in accordance with the present invention. The PDP is organized into rows of pixels, three of which are shown, namely, a pixel 720_n in row "n", a pixel 720_{n+1} in row "n+1", and a pixel 720_{n+2} in row "n+2". The rows are regarded as "odd" and "even" in an alternating pattern, where for example, row "n" is designated as an even row and row "n+1" is designated as an odd row.

The portion of the PDP shown in Fig. 7 includes an even sustain bus 712_E connected to a bank of even sustain electrodes 710_E , an odd sustain bus 712_O connected to a bank of odd sustain electrodes 710_O , scan electrodes 714_n , 714_{n+1} and 714_{n+2} , and column electrodes 718_R , 718_G and 718_B (for red, green, and blue, respectively). Each even sustain electrode 710_E is adjacent to an odd sustain electrode 710_O . For example, even sustain electrode 710_E in row "n" is adjacent to odd sustain electrode 710_O in row "n+1". There is also a transparent electrode 711 associated with each of sustain electrodes 710_E and 710_O , and scan electrodes 714_n , 714_{n+1} and 714_{n+2} .

An intersection of a sustain electrode, a scan electrode and a column electrode, defines a subpixel. For example, a subpixel 719_R is defined for the intersection of sustain electrode 710_E , scan electrode 714_n , and column electrode 718_R . Barrier ribs 716 separate subpixels from one another. Each pixel is defined as a region of intersection of a sustain electrode, a scan electrode, and three

column electrodes. For example, pixel 720_n is defined at the region of intersection of sustain electrode 710_E , scan electrode 714_n , and column electrodes 718_R , 718_G and 718_B . An inter-pixel gap 715 is defined for a region between adjacent pixels.

5 Each pixel includes a discharge gap where a sustain discharge forms. For example, in pixel 720_n , a discharge gap 713 is located between (a) a transparent electrode 711 associated with scan electrode 714_n and (b) a transparent electrode associated with even sustain electrode 710_E .

10 An even/odd selector 820 drives odd sustain bus 712_O via an odd sustain driver line 817_O , and drives even sustain bus 712_E via an even sustain driver line 817_E . Column driver 830 drives column electrodes 718_R , 718_G and 718_B via column driver lines 840_R , 840_G and 840_B , respectively. Row drivers 810 drive scan electrodes 714_n , 714_{n+1} , and 714_{n+2} via row driver lines 812_n , 812_{n+1} , and
15 812_{n+2} . The operation of even/odd selector 820, column driver 830 and row drivers 810 are further described in association with Fig. 8.

As mentioned earlier, Fig. 7 shows only a portion of the PDP. In practice, the PDP will include a plurality of rows and columns. Accordingly, column
20 drivers 830 will drive many more columns than are shown in Fig. 7, and row drivers 810 will drive many more rows than are shown in Fig. 7.

Fig. 8 is a block diagram of a PDP system 800 configured in accordance with the present invention. The principal components of system 800 include a
25 scan generator 805, row drivers 810, a PDP 815, even/odd selector 820, a sustain generator 825, column drivers 830 and logic 835.

Sustain generator 825 operates in the same manner as sustain generator 220 (Fig. 2), but supplies voltage V_e to even/odd selector 820 during addressing.

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Even/odd selector 820 is a circuit that employs method for controlling sustain electrodes in a PDP in accordance with the present invention. The method includes (a) enabling a first sustain electrode to produce an addressing discharge, and (b) disabling a second sustain electrode when the first sustain electrode is producing the addressing discharge, where the first sustain electrode is adjacent to the second sustain electrode.

Even/odd selector 820 controls even sustain electrodes 710_E and odd sustain electrodes 710_O . It supplies an isolation voltage (V_{iso}) to even sustain electrodes 710_E via an output to sustain driver line 817_E , and supplies V_{iso} to odd sustain electrodes 710_O via an output to sustain driver line 817_O . The purpose of V_{iso} is further explained below.

Fig. 9 is a graph of even and odd sustain electrode waveforms during an addressing of an even row at time t_{17} (odd rows are isolated at t_{17}). Assume that the waveforms are for scan electrode 714_n , even sustain electrode 710_E and odd sustain electrode 710_O . The X Data waveform represents an output of column driver 830 to one of column driver lines 840_R , 840_G and 840_B . Typical operating voltages for the PDP of Fig. 7 operated with the waveforms of Fig. 9 would be a setup voltage V_w of 400V, a sustain voltage V_s of 180V, a V_{scan} voltage of 120V, a ramp bias voltage V_{rf} of 10V, a setup/erase voltage V_e of 220V, an isolation voltage V_{iso} of 0 to 120V (V_{iso} is typically at least 60 volts below voltage V_e), and a data voltage V_x of 65V.

The voltage on even sustain electrode 710_E is referenced to a voltage on scan electrode 714_n . The voltage on odd sustain electrode 710_O is referenced to a voltage on scan electrode 714_{n+1} . These references are established during the setup period. During the setup period, even/odd selector 820 provides V_e to, and thus enables, both even sustain electrode 710_E and odd sustain electrode 710_O .

30

At t25, the addressing period begins, and even/odd selector 820 reduces the voltage supplied to even sustain electrode 710_E to V_{iso} thus reducing the difference of voltage, and therefore the magnitude, between even sustain electrode 710_E and scan electrode 714_n. This disables the even bank for the first half of the addressing period. Note that during the first half of the addressing period, odd sustain electrode 710_O is enabled. At time t26, even/odd selector 820 restates the voltage on even sustain electrode 710_E to V_e, and reduces the voltage on odd sustain electrode 710_O to V_{iso}, thus reducing the magnitude of the difference in voltage between odd sustain electrode 710_O and scan electrode 714_{n+1}. Thus, at time t26 the even and odd banks switch roles for the second half of the addressing period so that the odd bank is disabled and the even bank is enabled. At time t17, during the second half of the addressing period, even sustain electrode 710_E produces an addressing discharge to scan electrode 714_n. Crosstalk between even sustain electrode 710_E and odd sustain electrode 710_O is minimized by the lower potential (i.e., V_{iso}) on odd sustain electrode 710_O at time t17. This is because the enabling voltage V_e on even sustain electrode 710_E is referenced to the voltage on scan electrode 714_n, and the disabling voltage V_{iso} on odd sustain electrode 710_O, when referenced to the voltage on scan electrode 714_n is a lower magnitude than the enabling voltage V_e. Similarly, the row select and the respective column data are synchronized by logic block 835 to sequence through the odd rows first followed by the even rows.

In Fig. 9, a negative pulse on scan electrode 714_n during the addressing period indicates the time at which a particular pixel is addressed. Such a pulse occurs at time t17. Note that also at time t17 even sustain electrode 710_E is at V_e (and therefore enabled) while odd sustain electrode 710_O is at V_{iso} (and therefore disabled). Accordingly, the waveforms in Fig. 9 are for a case of addressing an even row in PDP 815, and more particularly, row “n”.

In the first sustain cycle, at time t20 there is a rising edge for the voltage on scan electrode 714_n, and at t21 there is a falling edge for the voltage on even

sustain electrode 710_E. The addressing discharge that was produced by even sustain electrode 710_E at time t17 allows even sustain electrode 710_E to produce a first sustain discharge during time t22.

5 Fig. 10a is a graph of a composite waveform of the scan waveform and even sustain waveform of Fig. 9, and Fig. 10b is a graph of a wall voltage waveform, for an OFF sub-pixel on the even bank of electrodes according to the present invention. Since the graph is that of an off sub-pixel, the breakdown voltage is only exceeded during the two setup ramps where the wall voltage is limited to V_{br} and -V_{br}, approximately ±200V.
10

The composite waveform is formed by subtracting the sustain electrode voltage from the scan electrode voltage. Assume for example, a case of even sustain electrode 710_E and scan electrode 714_n. Reducing voltage on even sustain
15 electrode 710_E from V_e to V_{iso} at t25 for the first half of the addressing period causes an increase in the composite voltage and thereby reduces the voltage across the gas. When the voltage on even sustain electrode 710_E is increased from V_{iso} to V_e during the second half of the addressing period, the wall voltage returns close to the breakdown voltage -V_{br}, so that the application of the row select pulse
20 at t17 slightly exceeds the breakdown voltage -V_{br}.

Figs. 11 and 12 show cross sectional views of pixel addressing discharge mechanics. More particularly, Fig. 11 shows the addressing discharge mechanics for an odd pixel P1, and Fig. 12 shows a neighboring even pixel P2. In Fig. 11,
25 P1's sustain electrode is tied to the enabled odd sustain bank, and thus has more positive charge than the disabled even sustain electrode. The P1 address discharge is initiated via an applied data pulse, however, the reduced positive charge on the even sustain electrode reduces the tendency of the positive column to spread into the P2 pixel space. The lower the V_{iso} voltage applied to the even electrode, the
30 greater the isolation achieved.

The address discharge on P1 neutralizes the voltage across the pixel site therefore, disabling the odd bank for the second half of addressing will result in a minor negative charge on the odd sustain electrode due to the drop in voltage. Since the voltage change is minor compared to the gas breakdown voltage, this effect is irrelevant. Enabling the even sustain electrodes returns them to their full positive charge so that when P2 is selected and a discharge forms, there is sufficient positive charge on P2's sustain electrode available to form a plasma to neutralize the scan electrode's negative charge.

Fig. 13 is a graph of scan and sustain electrode waveforms for a PDP in a variation of the invention where the voltage on the sustain electrodes is reduced to V_{iso} to provide cell-to-cell isolation. As each row is sequentially selected on the scan side by a negative row select pulse at t_{17} , a corresponding sustain electrode is returned to the sustain side addressing voltage V_e , thus providing a positive row select on the sustain side. Such an embodiment may be realized through the use of row drivers on the sustain side in place of even/odd selector 820 of Fig. 7.

Fig. 14 is a graph of even and odd sustain electrode waveforms for a PDP in another variation of the invention where the sustain electrodes are separated into odd and even sustain buses. Row drivers 810 provide sequential negative going row select pulses during the addressing period, while the sustain electrode voltage alternates between V_{iso} and V_e as the row select pulse is applied to each scan electrode. In Fig. 14, at time t_{17} there is a selection of an odd row, as the even sustain electrodes are driven to the isolation voltage V_{iso} , while the odd sustain electrodes are driven to the sustain side addressing voltage V_e .

Fig. 15 is a graph of even and odd sustain electrode waveforms for a PDP, where an increased forward voltage V_f of typically 10V higher than voltage V_e is applied to the odd or even sustain electrode buses. This arrangement provides additional voltage across the pixel to improve the panel's addressing margin by

increasing the charge transfer of the address discharge. Utilization of forward voltage V_f may also be applied to the waveforms of Figs. 13 and 14.

It should be understood that the foregoing description is only illustrative of
5 the invention. Various alternatives and modifications can be devised by those
skilled in the art without departing from the invention. For instance, this
invention is applicable other AC PDP and waveform configurations, where an
address discharge extends across a pixel and can spread across an inter-pixel gap,
seeking positive charge on an adjacent sustain electrode. The present invention is
10 intended to embrace all such alternatives, modifications and variances that fall
within the scope of the appended claims.

WHAT IS CLAIMED IS:

1. A method for controlling sustain electrodes in a plasma display panel (PDP), comprising:
enabling a first sustain electrode to produce an addressing discharge; and
disabling a second sustain electrode when said first sustain electrode is
producing said addressing discharge,
wherein said first sustain electrode is adjacent to said second sustain
electrode.
2. The method of claim 1, wherein said first sustain electrode is in a first
row of said PDP, and said second sustain electrode is in a second row of said PDP.
3. The method of claim 1,
wherein said enabling allows said first electrode to produce a sustain
discharge during a sustain period, and
wherein said disabling prevents said second sustain electrode from
producing a sustain discharge during said sustain period.
4. The method of claim 1,
wherein said enabling provides an enabling voltage to said first sustain
electrode, and
wherein said disabling provides a disabling voltage to said second sustain
electrode.
5. The method of claim 4,
wherein said enabling voltage is referenced to a scan electrode voltage, and
wherein said disabling voltage, when referenced to said scan electrode
voltage, is a lower magnitude than said enabling voltage.

6. The method of claim 1,
wherein said first sustain electrode is addressed during a first portion of an
addressing period, and
wherein said second sustain electrode is addressed during a second portion
of said addressing period.

7. The method of claim 6,
wherein said first portion of said addressing period is a first half of said
addressing period, and
wherein said second portion of said addressing period is a second half of
said addressing period.

8. A circuit for controlling sustain electrodes in a plasma display panel
(PDP), comprising:
an output for enabling a first sustain electrode to produce an addressing
discharge; and
an output for disabling a second sustain electrode when said first sustain
electrode is producing said addressing discharge,
wherein said first sustain electrode is adjacent to said second sustain
electrode.

9. The circuit of claim 8, wherein said first sustain electrode is in a first row
of said PDP, and said second sustain electrode is in a second row of said PDP.

10. The circuit of claim 8,
wherein said output for enabling allows said first electrode to produce a
sustain discharge during a sustain period, and
wherein said output for disabling prevents said second sustain electrode
from producing a sustain discharge during said sustain period.

11. The circuit of claim 8,
wherein said output for enabling provides an enabling voltage to said first
sustain electrode, and
wherein said output for disabling provides a disabling voltage to said second
sustain electrode.

12. The circuit of claim 11,
wherein said enabling voltage is referenced to a scan electrode voltage, and
wherein said disabling voltage, when referenced to said scan electrode
voltage, is a lower magnitude than said enabling voltage.

13. The circuit of claim 8,
wherein said first sustain electrode is addressed during a first portion of an
addressing period, and
wherein said second sustain electrode is addressed during a second portion
of said addressing period.

14. The circuit of claim 13,
wherein said first portion of said addressing period is a first half of said
addressing period, and
wherein said second portion of said addressing period is a second half of
said addressing period.

15. A system, comprising:
a plasma display panel (PDP) having a first sustain electrode and a second
sustain electrode adjacent to said first sustain electrode; and
a circuit for (a) enabling said first sustain electrode to produce an addressing
discharge, and (b) disabling said second sustain electrode when said
first sustain electrode is producing said addressing discharge.

16. The PDP system of claim 15, wherein said first sustain electrode is in a first row of said PDP, and said second sustain electrode is in a second row of said PDP.

17. The PDP system of claim 15,
wherein said enabling allows said first electrode to produce a sustain discharge during a sustain period, and
wherein said disabling prevents said second sustain electrode from producing a sustain discharge during said sustain period.

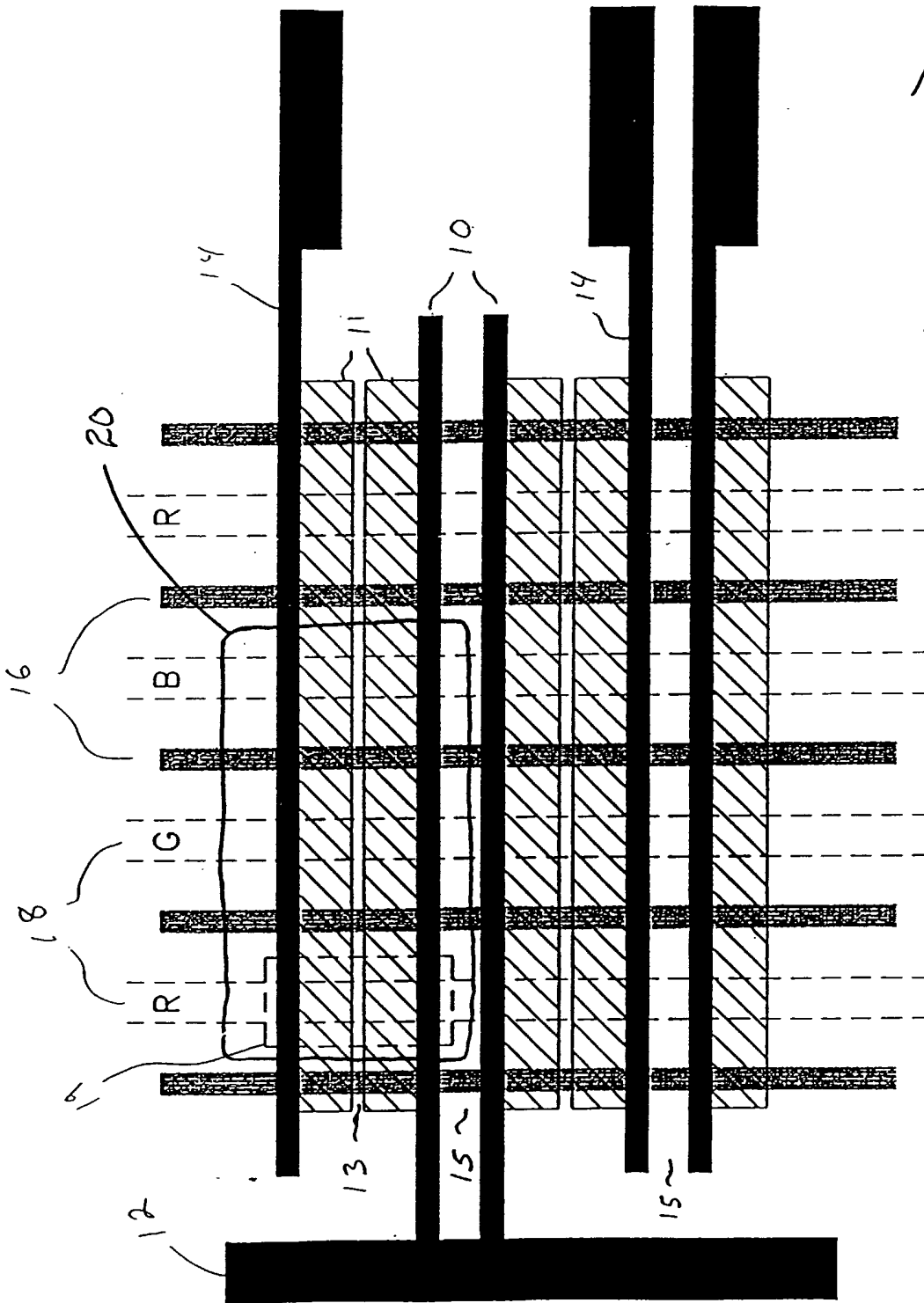
18. The PDP system of claim 15,
wherein said enabling provides an enabling voltage to said first sustain electrode, and
wherein said disabling provides a disabling voltage to said second sustain electrode.

19. The PDP system of claim 18,
wherein said enabling voltage is referenced to a scan electrode voltage, and
wherein said disabling voltage, when referenced to said scan electrode voltage, is a lower magnitude than said enabling voltage.

20. The PDP system of claim 15,
wherein said first sustain electrode is addressed during a first portion of an addressing period, and
wherein said second sustain electrode is addressed during a second portion of said addressing period.

21. The PDP system of claim 20,
wherein said first portion of said addressing period is a first half of said addressing period, and

wherein said second portion of said addressing period is a second half of
said addressing period.



(PRIOR ART)

FIG. 1

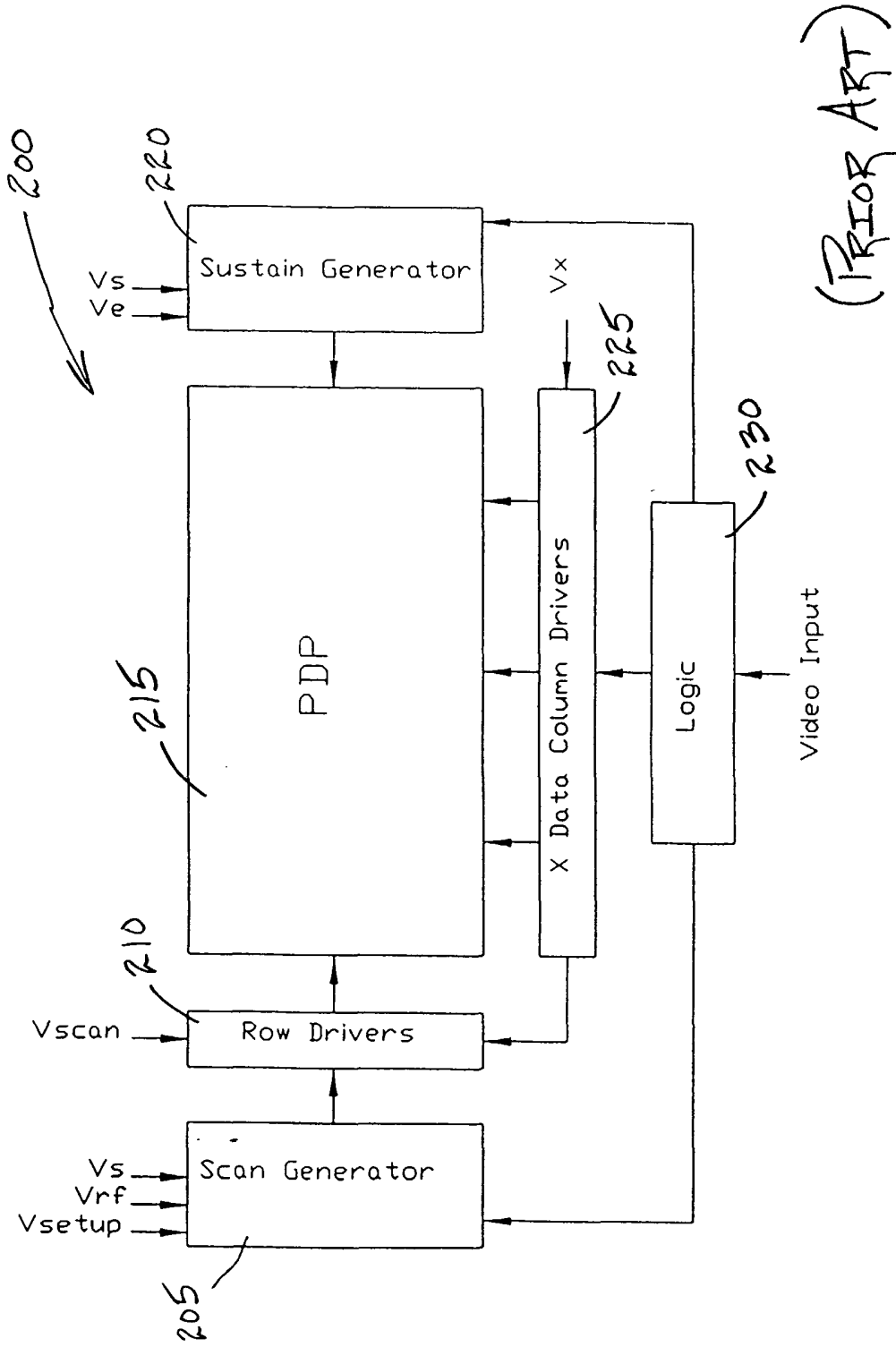
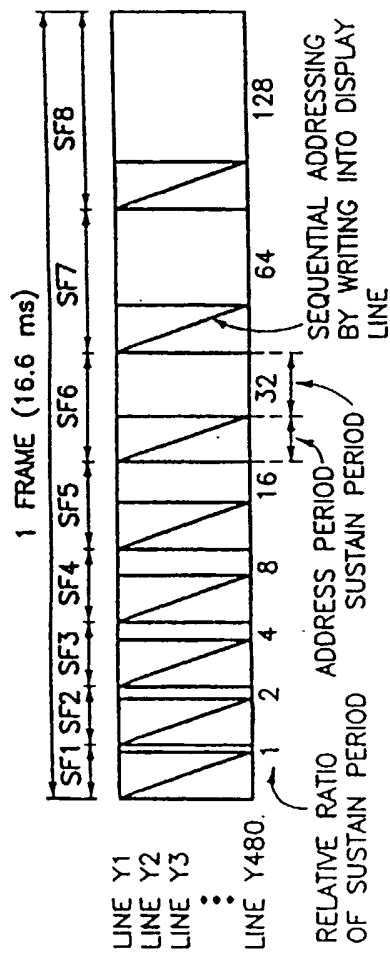


FIG. 2



(PRIOR ART)

FIG. 3

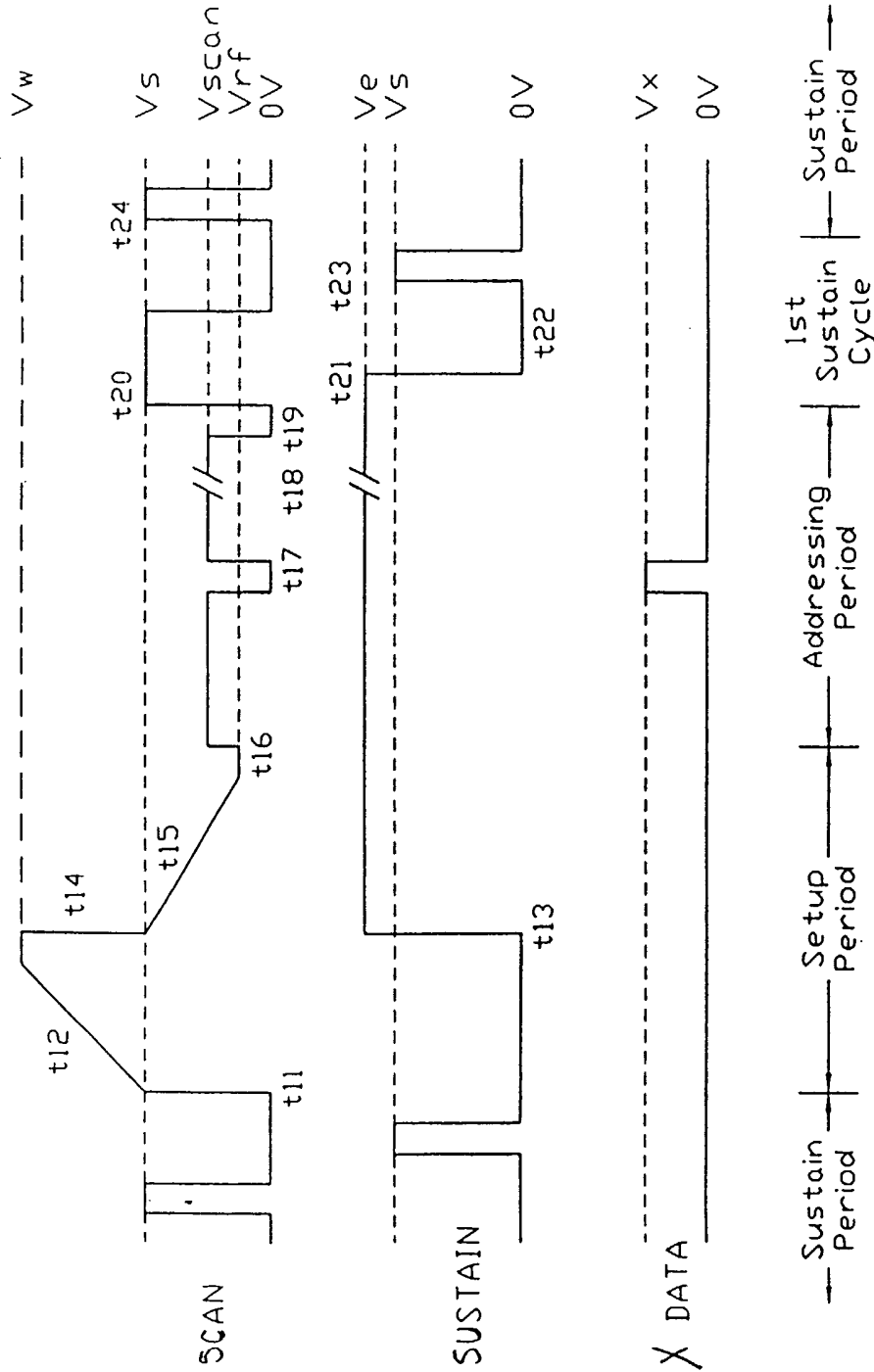


FIG. 4 (PRIOR ART)

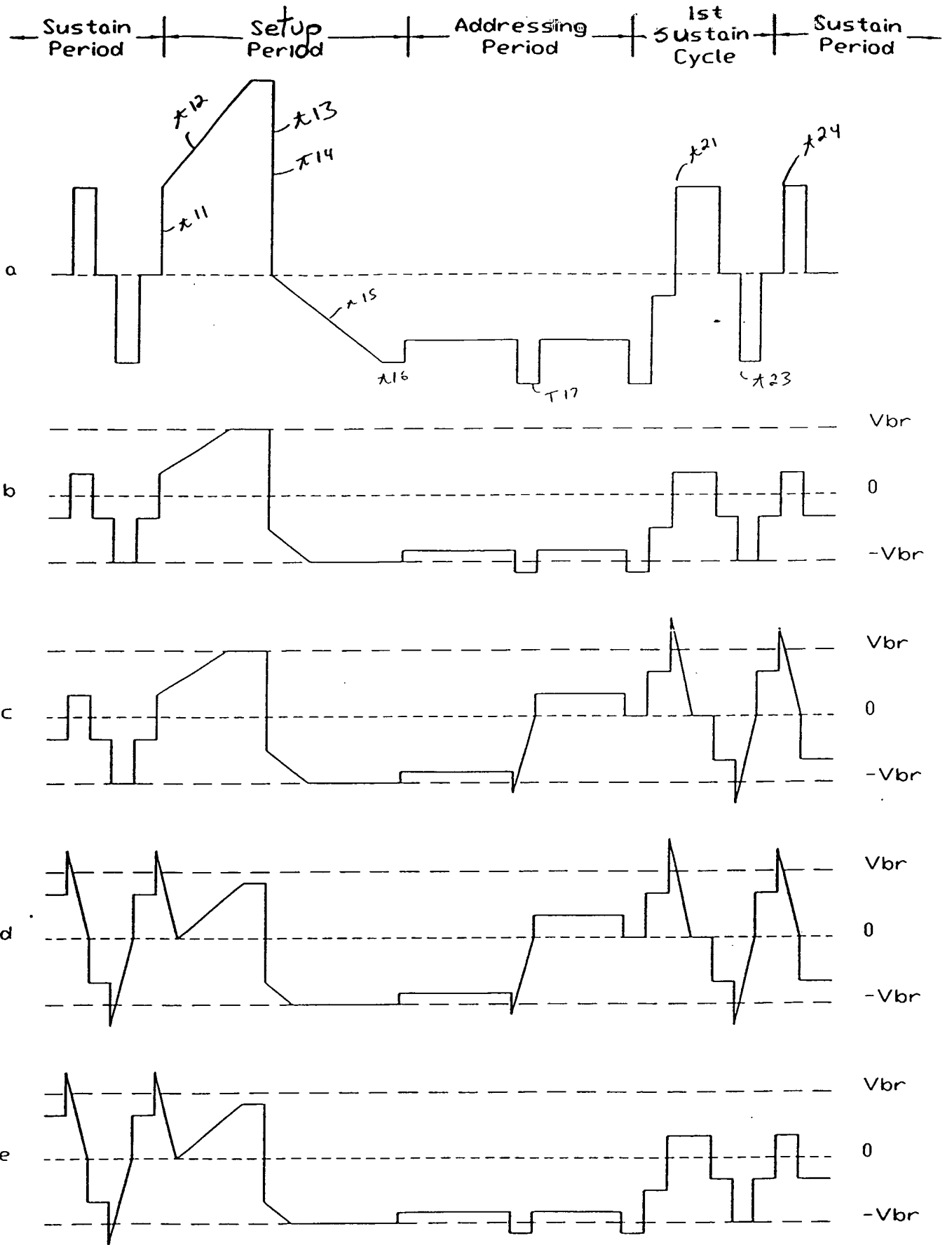


FIG. 5 (PRIOR ART)

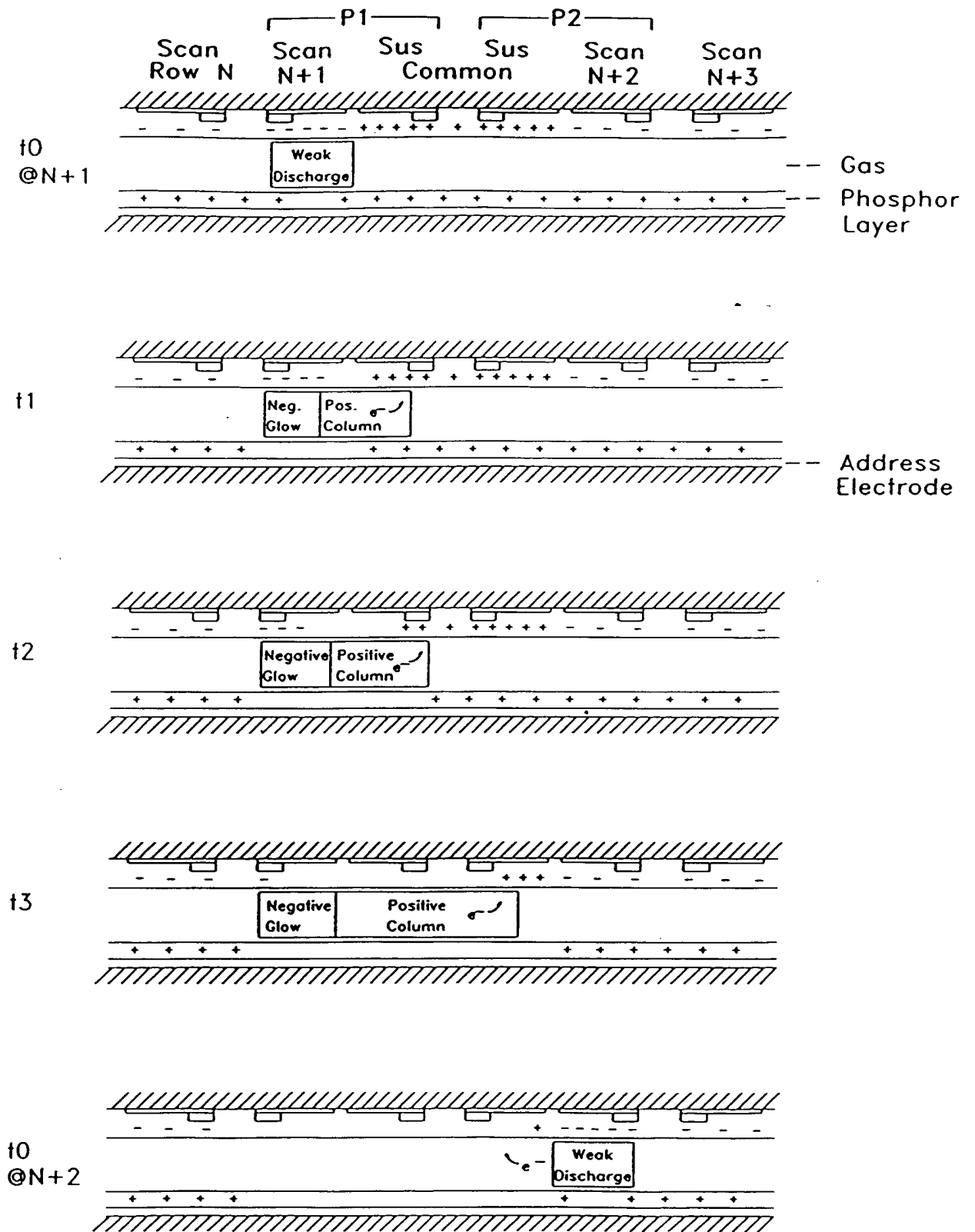


FIG. 6 (PRIOR ART)

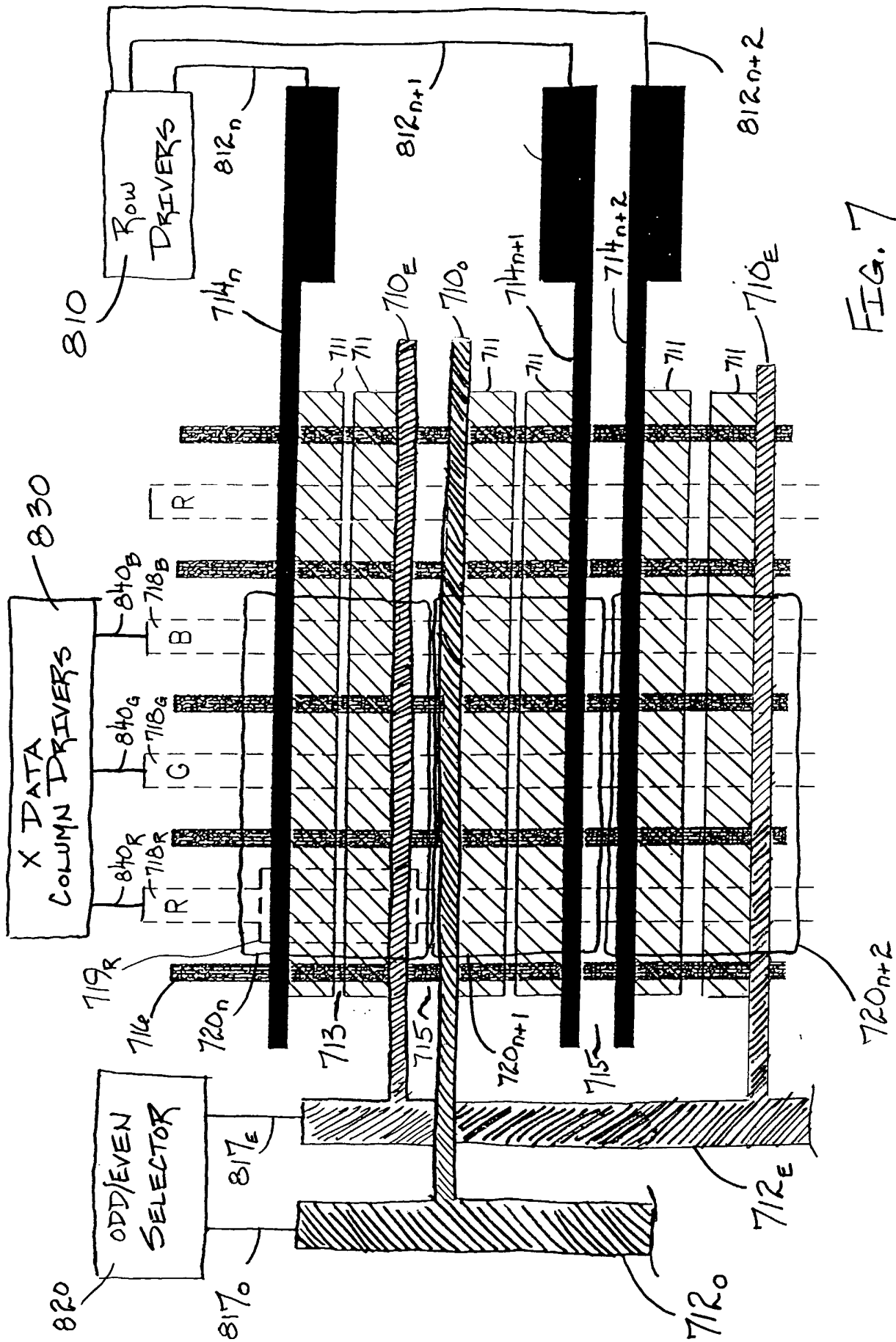


FIG. 7

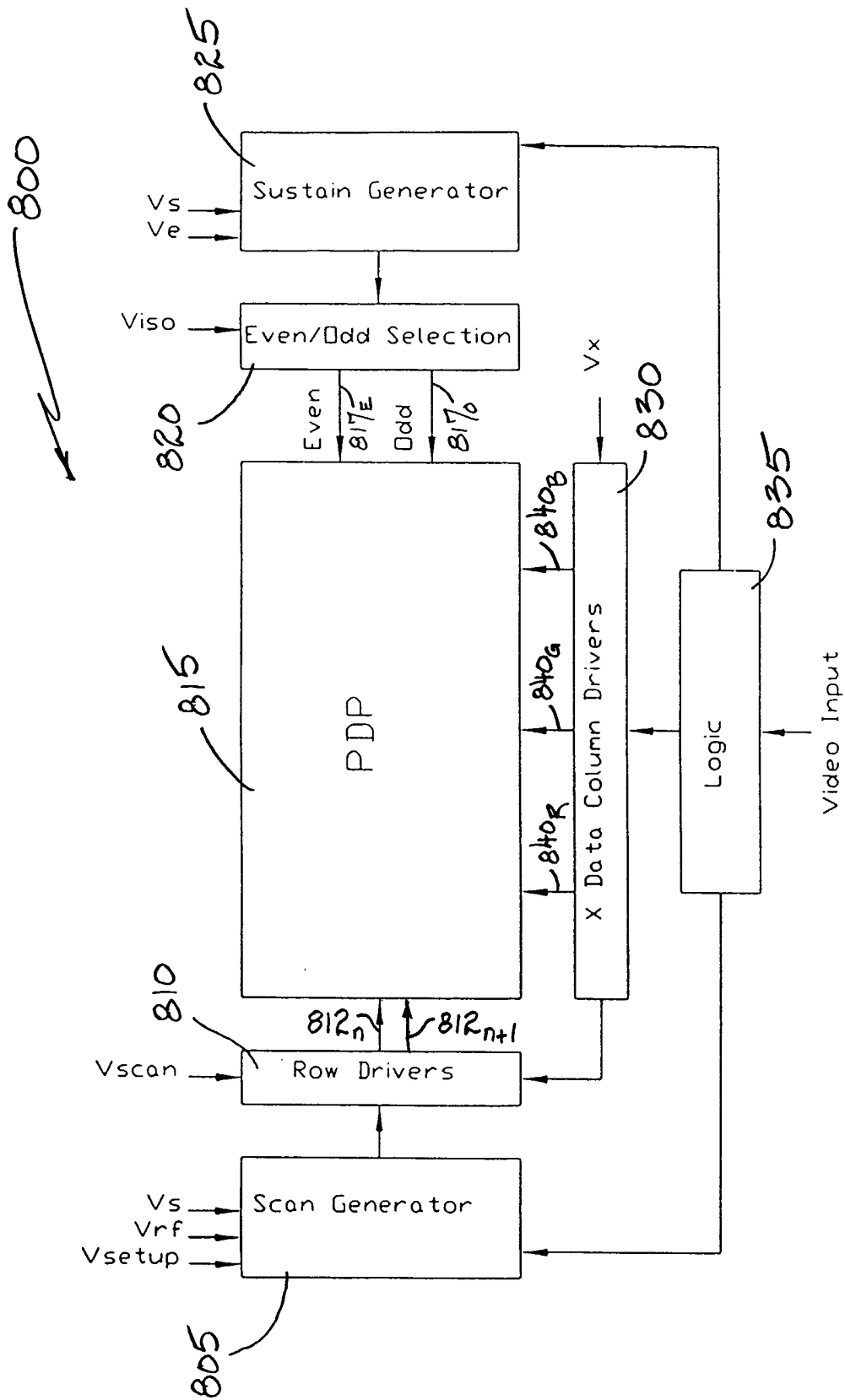


FIG. 8

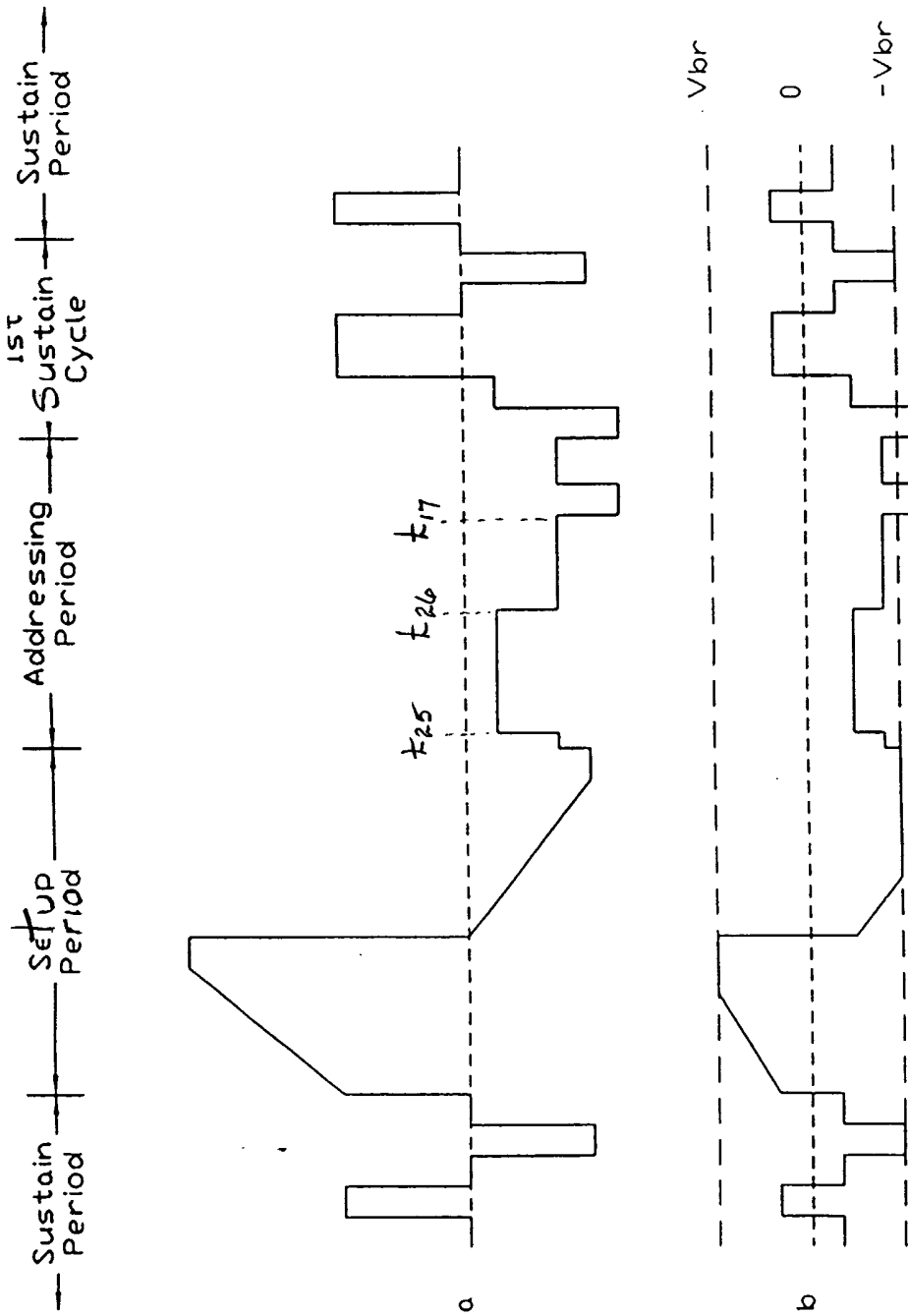


FIG. 10

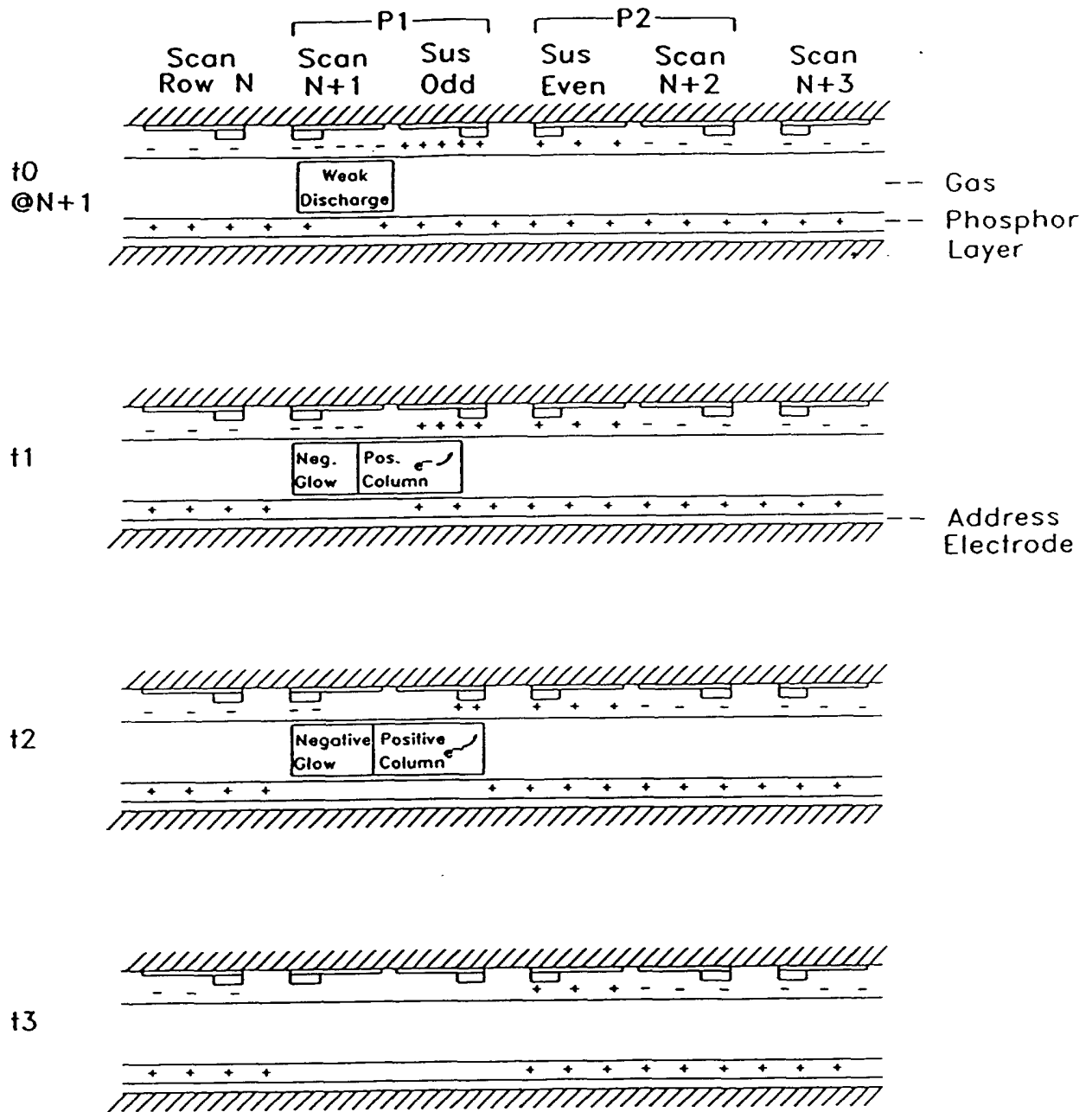


FIG. 11

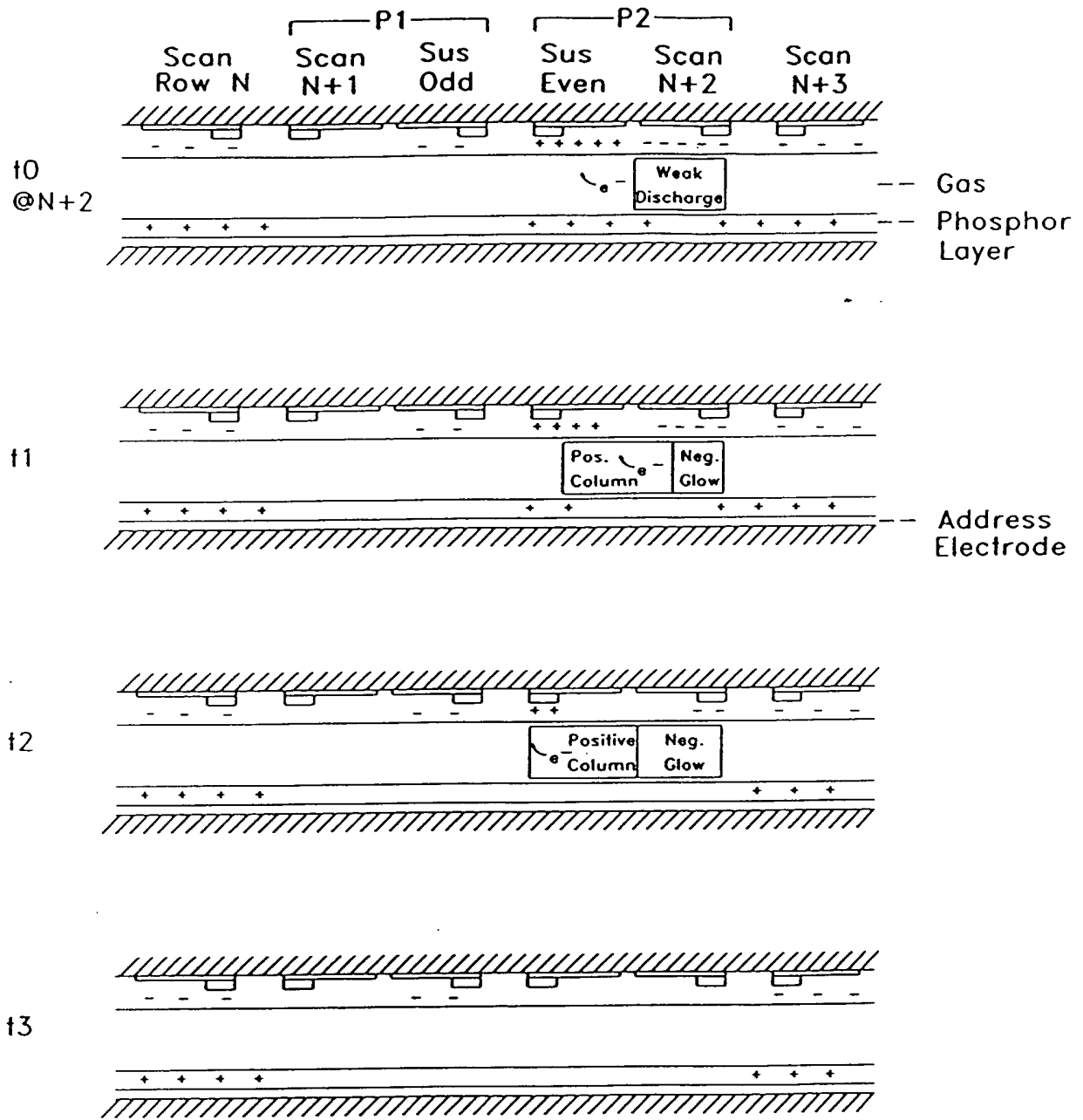


FIG. 12

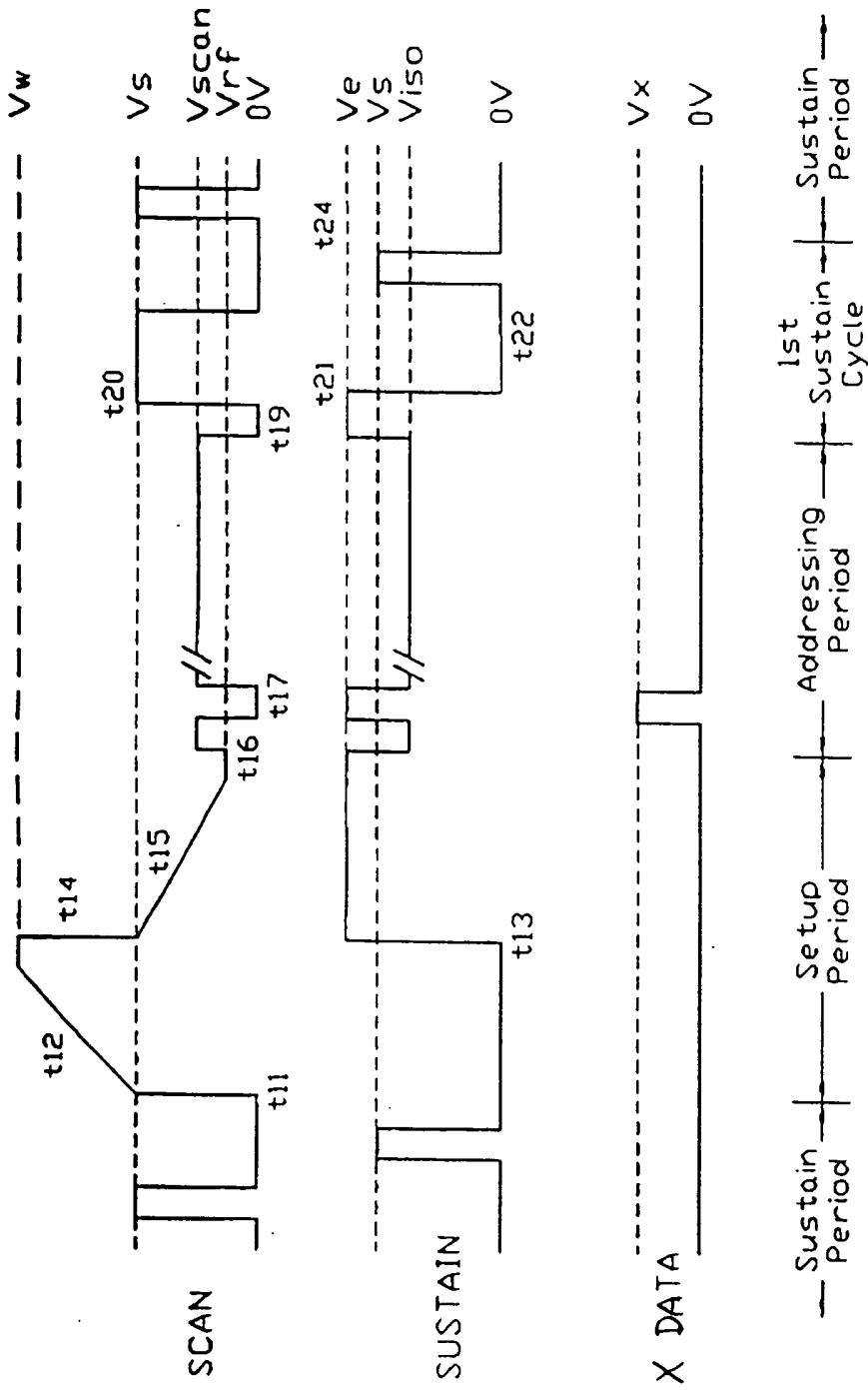


FIG. 13

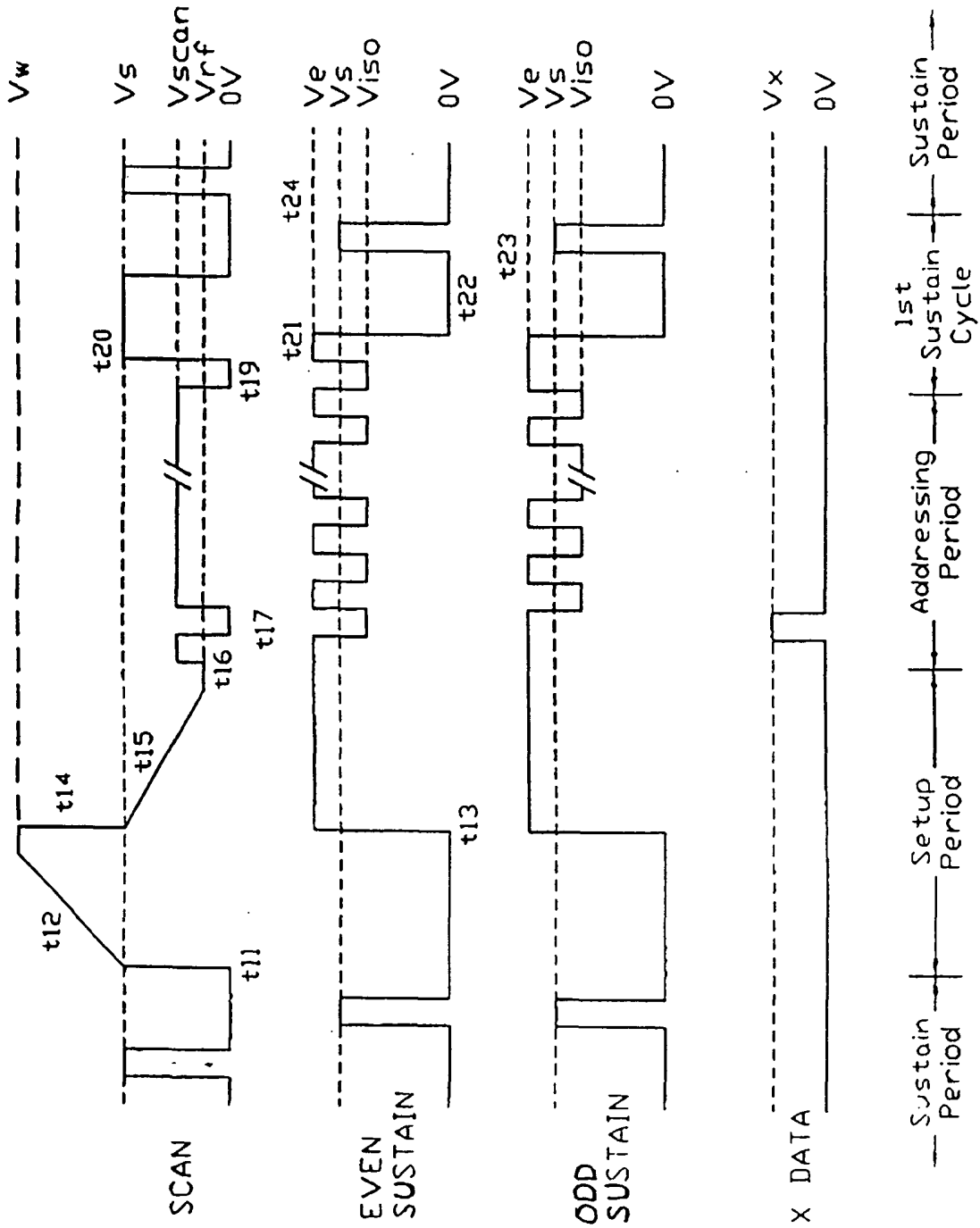


FIG. 14

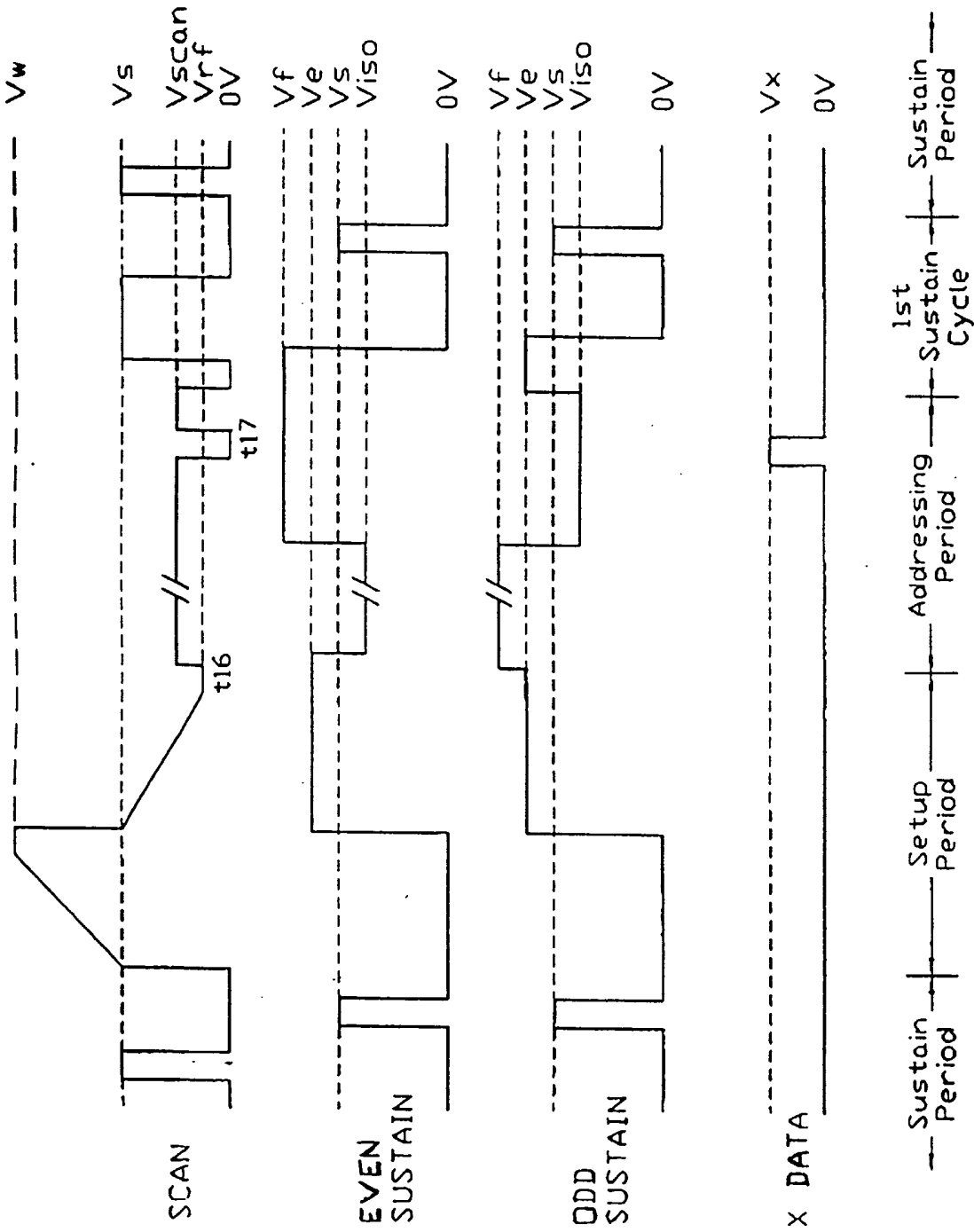


FIG. 15

INTERNATIONAL SEARCH REPORT

International Application No

PCT/IB 02/05451

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G09G3/28

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G09G H01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 762 373 A (FUJITSU LTD) 12 March 1997 (1997-03-12) column 22, line 55 -column 25, line 11; figures 18-23; example 7 ---	1-21
X	US 6 184 848 B1 (WEBER LARRY F) 6 February 2001 (2001-02-06) cited in the application ---	1-4, 6-11, 13-18, 20,21
Y	column 5, line 50 -column 4, line 17 column 25, line 31 -column 26, line 51 column 27, line 38 -column 28, line 63; figures 3, 6A, 6B, 10-14 --- -/--	5, 12, 19



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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Date of the actual completion of the international search

7 March 2003

Date of mailing of the international search report

18/03/2003

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Authorized officer

Morris, D

INTERNATIONAL SEARCH REPORT

Int. Application No

PCT/IB 02/05451

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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