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(54) METHOD AND APPARATUS FOR PROBING, TESTING, BURN-IN, REPAIRING AND PROGRAMMING OF INTEGRATED CIRCUITS IN A CLOSED ENVIRONMENT USING A SINGLE APPARATUS

(76) Inventor: **Glenn J. Leedy**, Saline, MI (US)

Correspondence Address:
MORRISON & FOERSTER LLP
755 PAGE MILL RD
PALO ALTO, CA 94304-1018 (US)

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Continuation-in-part of application No. 08/315,905, filed on Sep. 30, 1994, now Pat. No. 5,869,354, which is a division of application No. 07/865,412, filed on Apr. 8, 1992, now Pat. No. 5,354,695.
Continuation-in-part of application No. 08/217,410, filed on Mar. 24, 1994, now Pat. No. 5,453,404, which is a continuation of application No. 07/960,588, filed on Oct. 13, 1992, now Pat. No. 5,323,035.

Publication Classification

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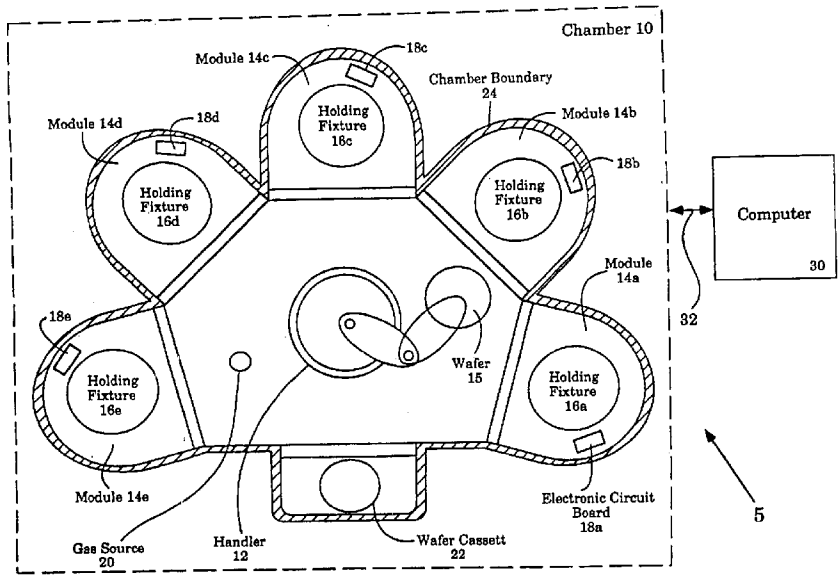
(52) **U.S. Cl.** **324/760**

(57) **ABSTRACT**

A single gas tight system which performs multi-functions including reducing the thickness of oxides on contact pads and probing, testing, burn-in, repairing, programming and binning of integrated circuits. A system according to one embodiment of the present invention includes: (a) a gas tight chamber having (**1**) a plurality of modules each having a holding fixture, a wafer, a probing device, an electronic circuit board, and a temperature control device, (**2**) a gas source for supplying non-oxidizing gases such as nitrogen and hydrogen into the chamber, (**3**) a handler for moving the wafers and the probing devices, and (b) a computer coupled to the chamber for controlling and communicating with the handler, the temperature control devices, the holding fixtures and the probing devices. A holding fixture holds a wafer having integrated circuits and aligns the wafer to a probing device. An integrated circuit has a plurality of conductive contact portions that are able to be connected to probe points of the probing device. A temperature control device is used to heat the wafer during an oxide reduction process or during burn-in of the wafer. During the oxide reduction process, hydrogen is introduced into the chamber, and the wafer is heated so that the oxides on the contact pads can combine with hydrogen to form water vapor, thus reducing the thickness of the oxides. The computer analyzes the test and/or burn-in data and provides control signals for repairing or programming the integrated circuits. The computer system also generates a database that contains the performance data of all the integrated circuits on the wafer that are tested and allows for immediate feedback of the quality of the integrated circuits.



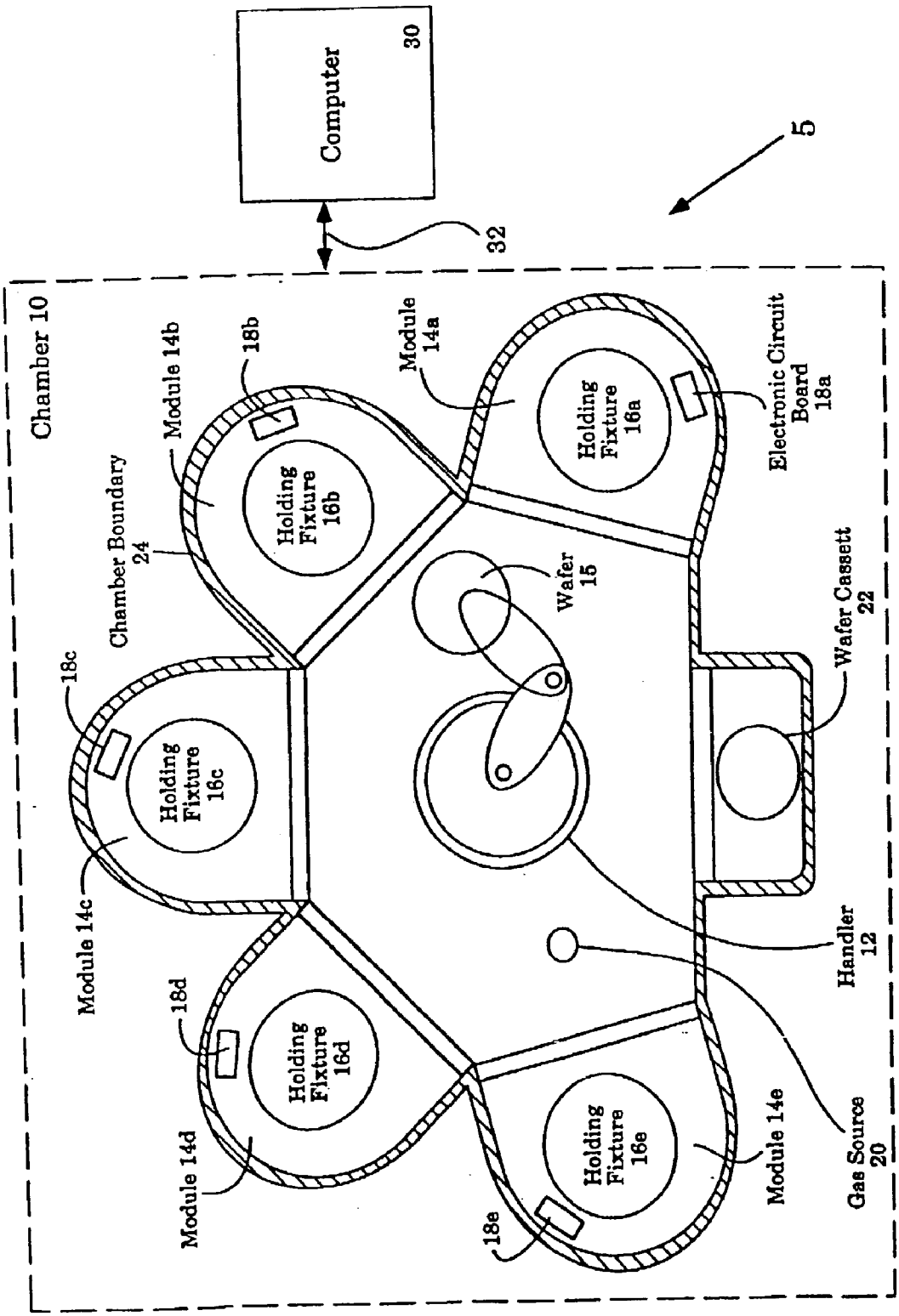

Computer
30
5
32
Chamber 10
Module 14b
18b
Module 14a
Holding Fixture 16a
Electronic Circuit Board 18a
Chamber Boundary 24
Holding Fixture 16b
Wafer 15
Wafer Cassett 22
18c
Holding Fixture 16c
Module 14c
Handler 12
18d
Holding Fixture 16d
Module 14d
Holding Fixture 16e
Module 14e
Gas Source 20
18e

Figure 1

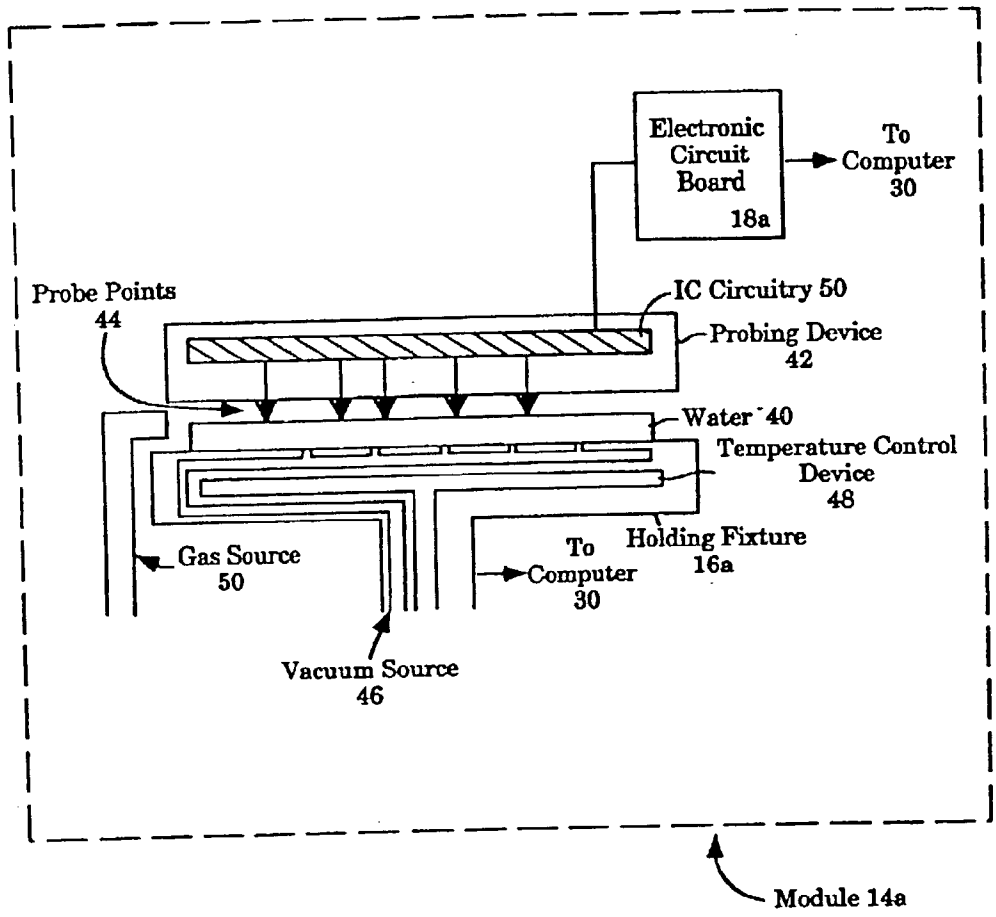

Electronic Circuit Board 18a
To Computer 30
Probe Points 44
IC Circuitry 50
Probing Device 42
Water 40
Temperature Control Device 48
Gas Source 50
To Computer 30
Holding Fixture 16a
Vacuum Source 46
Module 14a

Figure 2

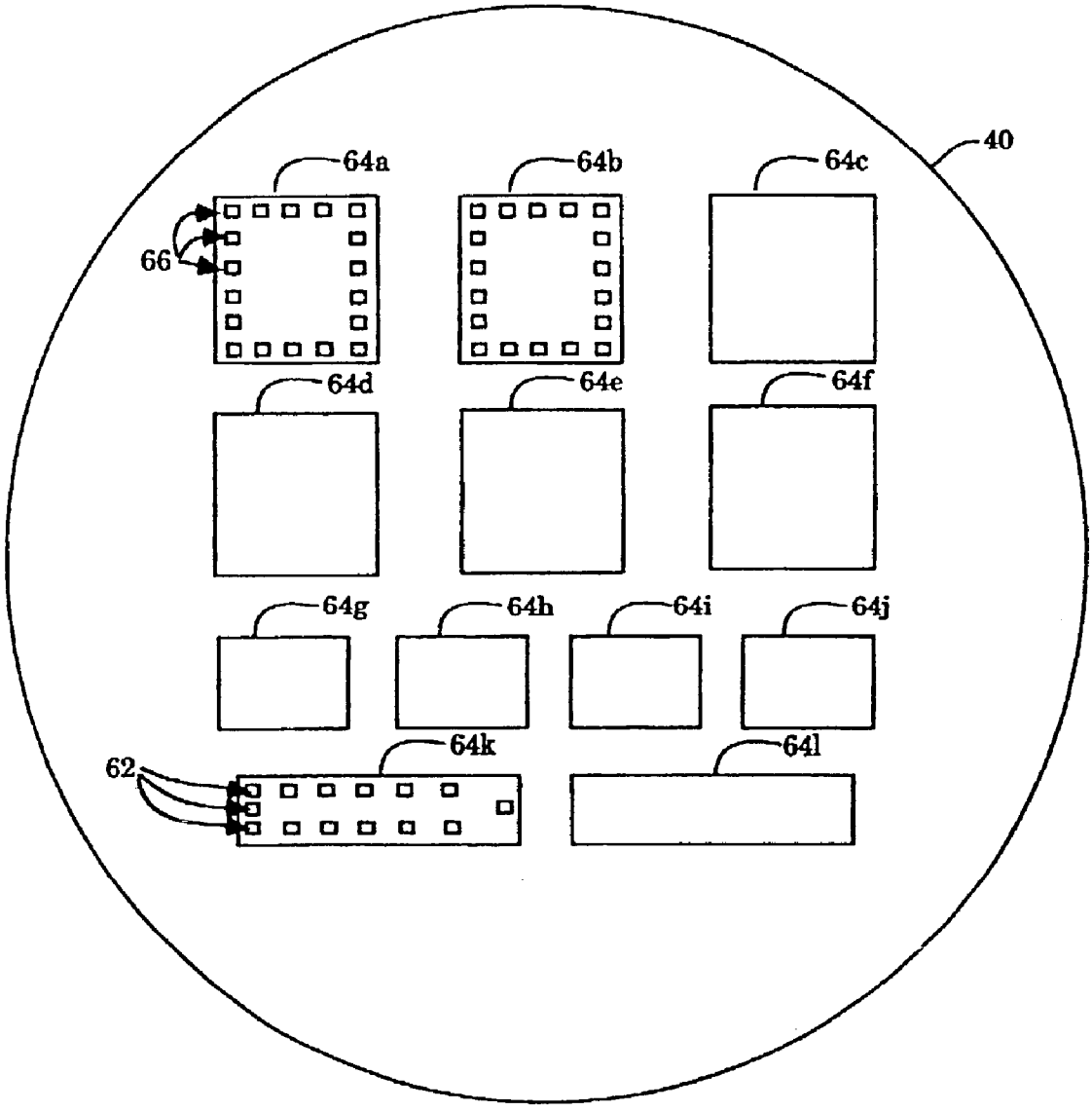


Figure 3

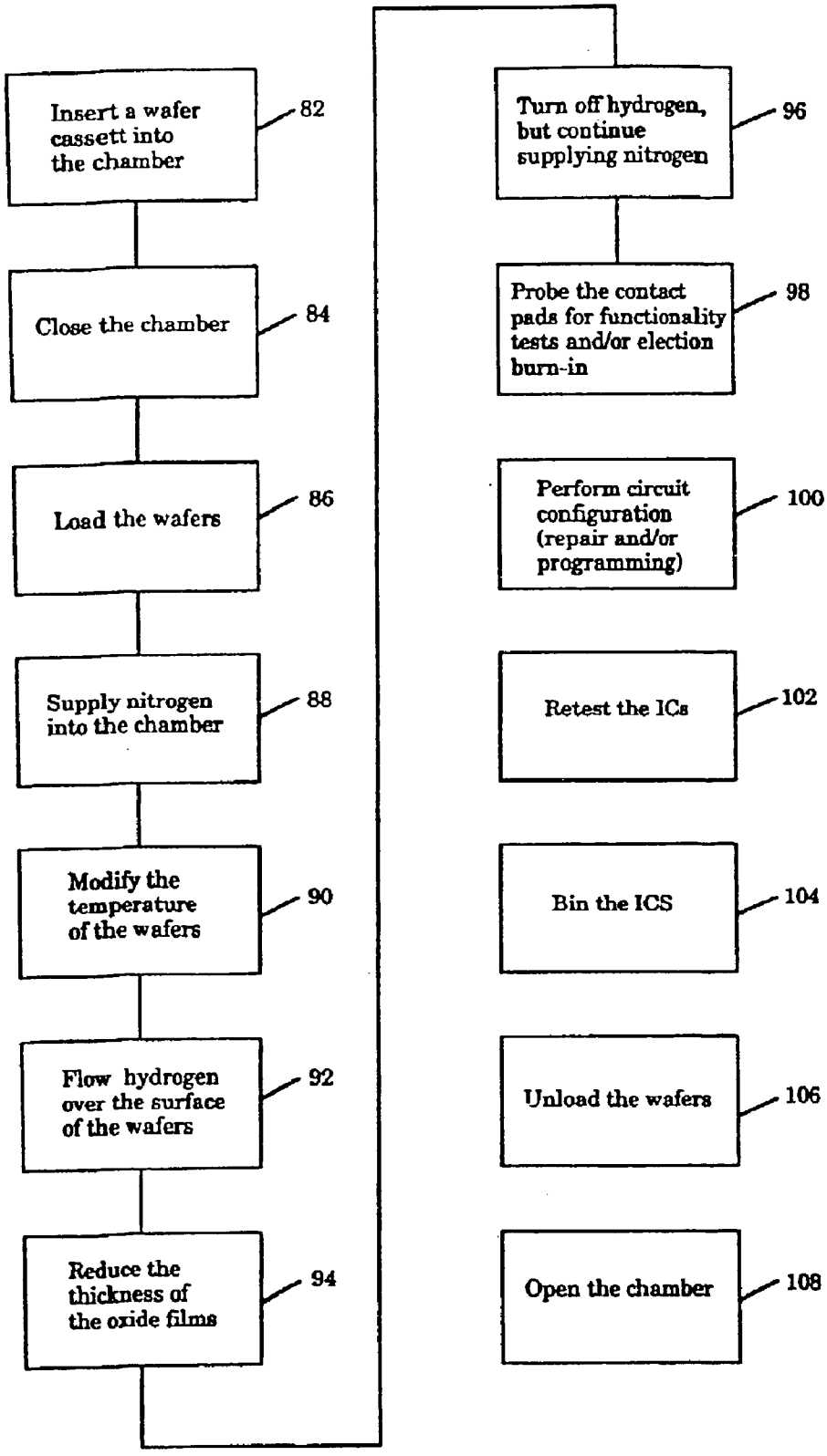

Insert a wafer cassett into the chamber
82
Close the chamber
84
Load the wafers
86
Supply nitrogen into the chamber
88
Modify the temperature of the wafers
90
Flow hydrogen over the surface of the wafers
92
Reduce the thickness of the oxide films
94
Turn off hydrogen, but continue supplying nitrogen
96
Probe the contact pads for functionality tests and/or election burn-in
98
Perform circuit configuration (repair and/or programming)
100
Retest the ICs
102
Bin the ICS
104
Unload the wafers
106
Open the chamber
108

Figure 4

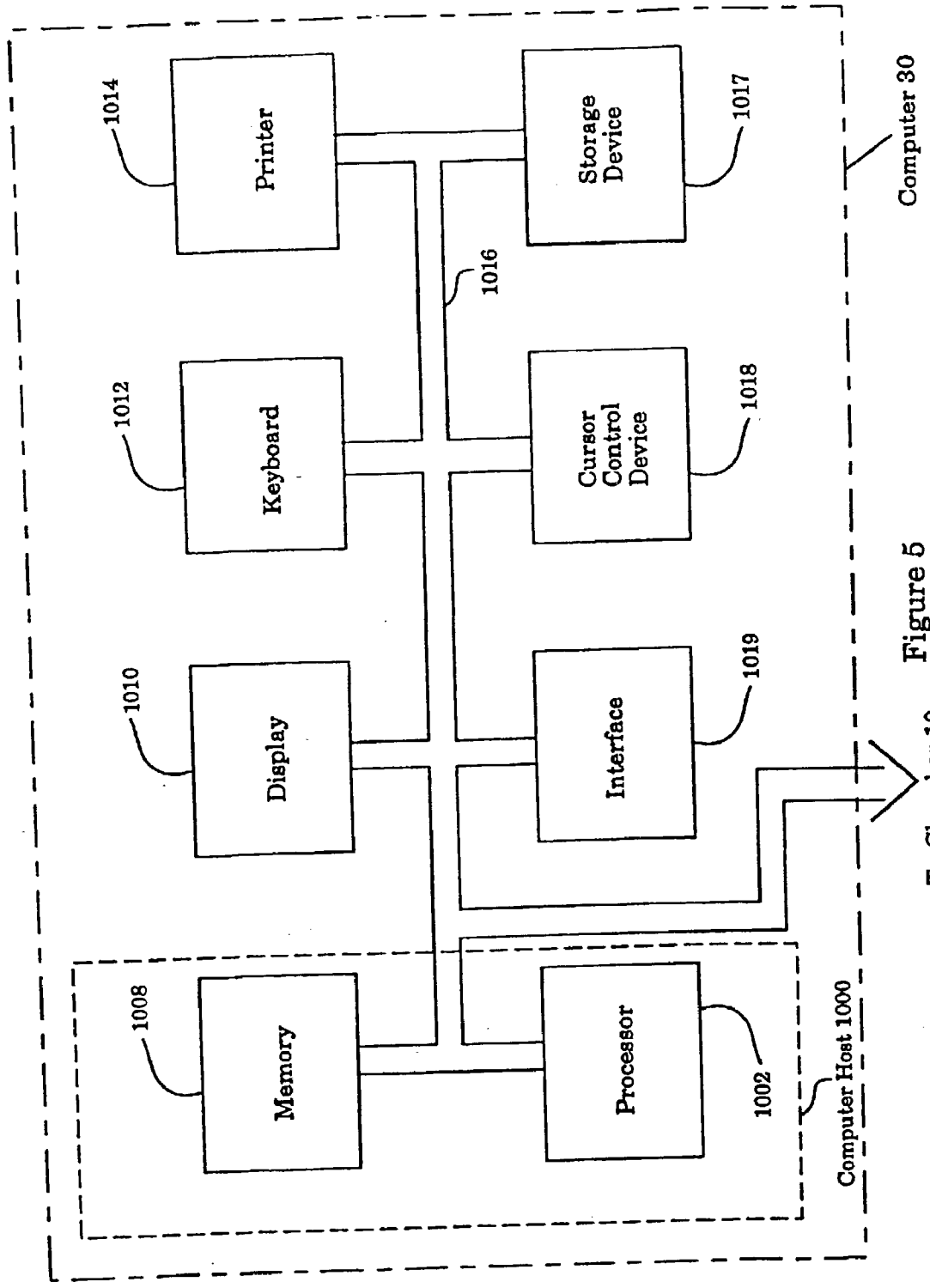

Computer 30
Printer
1014
Storage Device
1017
1016
Keyboard
1012
Cursor Control Device
1018
Display
1010
Interface
1019
To Chamber 10
Memory
1008
Processor
1002
Computer Host 1000

Figure 5

METHOD AND APPARATUS FOR PROBING, TESTING, BURN-IN, REPAIRING AND PROGRAMMING OF INTEGRATED CIRCUITS IN A CLOSED ENVIRONMENT USING A SINGLE APPARATUS

RELATED APPLICATIONS

[0001] This is a continuation of application Ser. No. 09/946,552 filed Sept. 6, 2001, which is a divisional of application Ser. No. 08/474,489 filed Jun. 7, 1995, now U.S. Pat. No. 6,288,561, which is a continuation-in-part of application Ser. No. 08/055,439 filed Apr. 30, 1993, now U.S. Pat. No. 5,451,489, which is a division of application Ser. No. 07/775,324 filed Oct. 11, 1991, now U.S. Pat. No. 5,225,771, which is a division of application Ser. No. 07/482,135 filed Feb. 16, 1990, now U.S. Pat. No. 5,103,557, which is a continuation-in-part of application Ser. No. 07/194,596 filed May 16, 1988, now U.S. Pat. No. 4,924,589; and is also a continuation-in-part of application Ser. No. 08/315,905 filed Sept. 30, 1994, now U.S. Pat. No. 5,869,354 which is a division of application Ser. No. 07/865,412 filed Apr. 8, 1992, now U.S. Pat. No. 5,354,695 and is also a continuation-in-part of application Ser. No. 08/217,410, filed Mar. 24, 1994, now U.S. Pat. No. 5,453,404, which is a continuation of application Ser. No. 07/960,588, filed Oct. 13, 1992, now U.S. Pat. No. 5,323,035.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to test equipment and more particularly to equipment for probing, testing, burn-in, repairing, programming and binning of integrated circuits.

[0004] 2. Description of the Related Art

[0005] In conventional semiconductor equipment technologies, separate pieces of equipment are required to test, burn-in, repair, program and bin integrated circuits (ICs). Integrated circuits that are in wafer form are tested or screened for packaging using a tungsten needle probe card, wafer positioning equipment called a prober and automatic test equipment (ATE) which supplies test signals to the probe card and determines the validity of any output signals. A probe card is a connector that provides a mechanical means for making a temporary contact to the contact pads on an IC for the purpose of testing the IC. The probe card may contact only a single die, but it may typically contact as many as eight or more dice if the dice consist of memory ICs.. A die typically consists of one IC; however, it may include a plurality of ICs. Conventional probe cards do not provide the capability of contacting all the dice on a wafer at once.

[0006] An IC is typically burned-in and speed-graded prior to its use or sale. Burn-in of circuit devices requires many hours of testing the devices under stressing temperature and electrical conditions. An IC is burned-in to lower the possibility that it will fail after it is inserted into an electronic assembly such as a Multi-Chip Module (MCM) or printed circuit board (PCB) of other ICs. Burn-in of an IC is performed typically after the IC is in packaged form. Burn-in fixtures for processing a die before packaging, so called bare die burn-in, are beginning to become available. Whether an IC is in packaged form or in die form, a separate piece of equipment is used to burn-in an IC. After an IC has been burned-in, it is speed-graded or binned using automatic test equipment. Binning is a process that sorts ICs according to their performance characteristics.

[0007] When an IC is in wafer form, and it contains shorts that disrupt the functionality of the IC, it may be repaired by removing portions of a deposited layer (e.g., a polysilicon layer or an aluminum metal layer). A laser cutting machine is typically used to perform the circuit repair. If an IC is a memory circuit array, yet another machine is required to program the memory circuit array by fusing or anti-fusing circuits within the memory circuit array. Subsequent to repair of an IC, the IC must be tested again.

[0008] It would be advantageous, and is therefore an object of the present invention to provide a single piece of equipment that can perform all of the functions mentioned above that are previously done by separate pieces of equipment to reduce capital equipment expense and the number of steps required for IC burn-in, testing, repairing and/or programming.

SUMMARY OF THE INVENTION

[0009] The present invention provides a single gas tight system that can perform multi-functions including reducing the thickness of oxides on contact pads and probing, testing, burn in, repairing, programming, marking and binning of integrated circuits. A system according to one embodiment of the present invention includes: (a) a gas tight chamber having (1) one or a plurality of modules each having a holding fixture, a wafer, a probing device, other processing device such as a die inking or repairing device, an electronic circuit board, and a thermal control device, (2) a gas source for supplying non-oxidizing gases such as nitrogen and hydrogen into the chamber, (3) a handler for moving the wafers and the probing or other processing devices, and (b) a computer coupled to the chamber for controlling and communicating with the handler, the temperature control devices, the holding fixtures, the probing and other processing devices.

[0010] A holding fixture holds a wafer having integrated circuits and aligns the wafer to a probing device or other processing device. An integrated circuit has a plurality of conductive contact portions, typically referred to as contact, I/O or bond pads, that are couplable to probe points of the probing device. A temperature control device is used to heat the wafer during an oxide reduction process. When hydrogen is present in the chamber and the wafer is heated, the oxides on the wafer combine with hydrogen to form water vapor, thus reducing the thickness of the oxides. The temperature control device may also be used to heat or cool the wafer during burn-in of the wafer.

[0011] A probing device can have multiple probe points or a single probe point. the probing device can be a full-wafer probing device having active switching logic circuits to allow controlled access to each of the integrated circuits on a after, and optionally, generate some or all of the test signals required for testing the die.

[0012] The computer can generate a computer database with the various status information for every circuit processed by wafer and on-wafer site location. The database can provide timely performance distribution statistics and physi-

cal distribution statistics to the circuit manufacturing engineers or process engineers to allow adjustments to be made to the manufacturing process. By using the database, processing steps that are slowly going out of specification and affecting product quality can be corrected. Thus, the capability of near-real time adjustments to the manufacturing process will allow savings by reducing the number of products that do not satisfy specifications.

[0013] The present invention allows a single semiconductor test and circuit configuration machine to perform any or all of the following: (a) reducing the thickness of oxides on contact pads of integrated circuits on a wafer by supplying a first non-oxidizing gas such as nitrogen into the chamber, heating the contact pads, and supplying a second non-oxidizing gas such as hydrogen into the chamber so that the oxides can combine with hydrogen to form water vapor, (b) probing the contact pads using a probing device, (c) testing the functionality of the integrated circuits, (d) burning-in the integrated circuits for a predetermined period of time over a predetermined range of temperature with predetermined temperature rate of change and electrical conditions, (e) generating test vector data and analyzing data collected from the integrated circuits, (f) repairing the integrated circuits, (g) programming the integrated circuits by fusing or anti-fusing specific circuits within the integrated circuits, (h) marking or printing on the wafer, (i) binning the integrated circuits according to their performance characteristics, and (j) collection of a database for immediate feedback to the manufacturing process.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The objects, features and advantage of the present invention will be apparent from the following detailed description in which:

[0015] **FIG. 1** is a multi-functional semiconductor test and circuit configuration system according to the present invention.

[0016] **FIG. 2** is one of the modules shown in **FIG. 1**.

[0017] **FIG. 3** is a wafer having a plurality of integrated circuits.

[0018] **FIG. 4** is a flow chart illustrating the steps of reducing the thickness of oxide films on the contact pads of the integrated circuits and the steps of testing, burning-in, configuring and binning the integrated circuits according to the present invention.

[0019] **FIG. 5** is a detailed block diagram of the computer shown in **FIG. 1** according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0020] The present invention provides methods and apparatus for performing testing, burn-in, repairing, programming, and binning of integrated circuits in a closed environment using a single piece of equipment. In the following detailed description, numerous specific details are set forth such as particular hardware configurations and a flow chart to provide a thorough understanding of the present invention. It will be appreciated, however, by one having ordinary skill in the art that the present invention may be practiced without such specific details. In other instances, well-known structures and methods are not described to avoid obscuring the present invention unnecessarily.

[0021] Now referring to **FIG. 1, a** semiconductor test and circuit configuration system **5**, which is a cluster tool, is presented according to one embodiment of the present invention. System **5** includes a chamber **10** and a computer **30**. Chamber **10** includes a plurality of modules **14***a*-**14***e* for processing wafers, a handler **12** for moving wafers and probing devices, and a wafer cassette **22** for holding a plurality of wafers.

[0022] It will be appreciated that the present invention may be used to process other substrates even though the specific details set forth the processing of a semiconductor wafer. Other substrates, circuit substrate types, or substrate assemblies that the present invention can process are Multi-Chip Module and flat panel display substrates which may be made from various materials such as AlN, SiC, quartz, glass or diamond.

[0023] Chamber **10** shown in **FIG. 1** includes a plurality of modules. Although five modules are shown in **FIG. 1**, chamber **10** may include more modules or fewer modules. Since a wafer cassette usually holds twenty-five wafers, a chamber can be made to include twenty-five modules for processing twenty-five wafers simultaneously. It should be noted that each of the modules may perform the same function (or functions). For instance, all of the modules may perform functional testing, burn-in and repairing of ICs in the same sequence and at the same time. On the other hand, the modules may perform different functions. For example, while module **14***a* performs a functional test, module **14***b* may perform programming of ICs. Moreover, the modules can also perform each function independently and in any order, such as performing a test function without burn-in processing or performing a test function both before and after other processing steps.

[0024] Chamber **10** may be a closed system or an open system. When chamber **10** is a closed system, chamber **10** is a gas tight system, not allowing gas molecules to move across the chamber boundary **24**. The pressure inside chamber **10** may be more than, at, or less than atmospheric pressure. In one embodiment, chamber **10** includes a gas source **20** wherein gas source **20** can introduce non-oxidizing gases such as nitrogen and hydrogen into chamber **10**. As will be described later, having a non-oxidizing environment is beneficial in forming good contacts between probing devices and the contact pads of integrated circuits.

[0025] It will be appreciated that in another embodiment, each module in chamber **10** can be in a separate gas-tight closed environment. In such a case, each module would have doors to close off and isolate the atmosphere and temperature of the module and each module could contain a separate gas source. For example, one module can contain nitrogen and hydrogen to reduce the thickness of metal oxide films, while another module may contain only nitrogen to perform another function such as a functionality test on an IC.

[0026] Handler **12** in **FIG. 1** can be a robotic system that moves wafers between wafer cassette **22** and the holding fixtures or between the holding fixtures and changes the probing devices when the type of wafer is changed. Handler **12** has the capability to move multiple wafers simulta-

neously. It should be noted that a module can be manually loaded with a wafer instead of using the handler **12**.

[**0027**] **FIG. 2** presents a module **14***a*.sup.**1**. Module **14***a*.sup.**1** is identical to module **14***a* of **FIG. 1** except that module **14***a*.sup.**1** contains a gas source **50**. Since modules **14***a*-**14***e* are identical, no separate description is provided for modules **14***a*-**14***e*. Module **14***a*.sup.**1** in **FIG. 2** includes a probing device **42** having probe points **44** for probing contact pads on wafer **40** and circuitry **50** which is coupled to an electronic circuit board **18***a*. A holding fixture **16***a* has a plurality of vacuum holes for pulling down wafer **40** onto holding fixture **16***a* and a thermal control device **48** for controlling the temperature of the substrate **40**. Module **14***a*.sup.**1** also includes a gas source **50** for introducing non-oxidizing gases into module **14***a*.sup.**1**.

[**0028**] Wafer **40** includes a plurality of integrated circuits (ICs) **64***a*-**64***l* as shown in **FIG. 3**. Each IC includes a plurality of conductive contact portions such as contact pads **66** (not all are shown in **FIG. 3**). Conductive contact portions are not limited to contact pads, and they may include various types of metal portions that are exposed on a wafer. Conductive contact portions are usually made of aluminum. However, they may be made from various other types of metal. ICs on wafer **40** may be of different sizes, and the contact pads may be also of different sizes. Wafer **40** in **FIG. 2** may represent a full wafer as shown in **FIG. 3** or a partial wafer. In the preferred embodiment, wafer **40** is a whole wafer. Wafer **40** may be a silicon wafer, GaAs wafer, or any other semiconductor wafer. It should be noted that wafer **40** may include only simple circuits wherein the circuits may be passive circuits, active circuits or metal lines.

[**0029**] Continuing to refer to **FIG. 2**, probing device **42** may contain a single probe point, a small number of probe points (5-40) or a large number of probe points (approximately 100,000 to 500,000 or more). In the preferred embodiment, probing device **42** is a full-wafer probing device. U.S. Pat. Nos. 5,103,557 and 5,323,035 issued to this inventor disclose how a full-wafer probing device can be fabricated. A full-wafer probing device has the capability to contact all of the contact pads on a wafer at once. The number of probe contact points that may be required in such wafer probing device can exceed 100,000 points. As shown in U.S. Pat. No. 5,103,557, a full-wafer probing device can also include a circuitry that allows each die of a wafer to be individually tested and/or isolated if it is faulty. This is shown as circuitry **50** in **FIG. 2**. Also, U.S. Pat. No. 5,354,695 discloses a fabrication process for making an intelligent probing device through the use of membrane circuits. IC circuitry **50** also provides the means to reduce the number of electronic signal connections to and from the probing device to a number that is approximately the same as the number of signals associated with each die and not the number of connections equal the number of dice on a wafer times the signals per die. When IC circuitry **50** incorporates active circuit switching logic, it provides a controlled access to each die on a wafer.

[**0030**] IC circuitry **50** of probing device **42** is connected to electronic circuit board **18***a* which is coupled to computer **30** in **FIG. 1**. Electronic circuit board **18***a* is used as a common mechanical and an electrical interface between probing device **42** and computer **30** so that probing device **42** can receive control signals from computer **30** and send data signals to computer **30**. In another embodiment, chamber **10** of **FIG. 1** can contain one electronic circuit board for all the probing devices instead of having one electronic circuit board for each probing device as shown in **FIG. 2**.

[**0031**] Probing device **42** has probe points **44** and IC circuitry **50** that are specific for a wafer being tested. A probing device can be changed with another by handler **12** in **FIG. 1** when the type of wafer is changed. Although probing device **42** can incorporate active device switching circuitry such as transistors on the electronic circuit boards, probing device **42** could also only incorporate passive circuit elements such as resistors, inductors, and capacitors. In the latter embodiment, there would be a reduction in the complexity of fabrication of probing devices but an increase in the number of I/O interconnections from probing devices to the supporting control circuitry. With the former embodiment of the probing devices, higher at-speed tests can be performed as there is no concern for degradation of signal integrity due to the constraints of path propagation and signal bandwidth. The incorporation of active device switching circuitry into probing devices would create intelligent and programmable probing devices.

[**0032**] Still continuing to refer to **FIG. 2**, holding fixture **16***a* is used to hold wafer **40** and align wafer **40** to probing device **42**. Holding fixture **16***a* includes a vacuum source **46** having a plurality of vacuum holes to hold wafer **40** firmly against holding fixture **16***a* and temperature control device **48** for heating or cooling wafer **40**. Holding fixture **16***a* is controlled by computer **30** in **FIG. 1**. When wafer **40** is placed on holding fixture **16***a*, computer **30** sends control signals to vacuum source **46** to apply vacuum to pull down wafer **40** against holding fixture **16***a*, and at the completion of testing, repairing or programming of the ICs on wafer **40**, vacuum source **46** may be turned off so that wafer **40** can be released from holding fixture **16***a*.

[**0033**] Temperature control device **48** is also controlled by computer **30**. To burning wafer **40** or to remove oxide from the contact pads of wafer **40**, computer **30** sends control signals to temperature control device **48** to control the temperature of the wafer **40**. Computer **30** controls and monitors the temperature of wafer **40** so that it is changed to predetermined temperatures for a predetermined period of time. The rate at which the temperature of wafer **40** is changed can also be controlled by computer **30** through the use of temperature control device **48**. In **FIG. 2**, temperature control device **48** is embedded in holding fixture **16***a* to control the temperature of wafer **40**. However, wafer **40** can be heated by radiation or by some type of ion beams. Focused ion beams can be used to heat only a portion of wafer **40** or only a specific contact pad on wafer **40**. Temperature control device **48** can also be used to reduce the temperature of wafer **40** for cases where the operation of all the circuits on a substrate may have a combined thermal energy generation exceeding the desired burn-in temperature or for situations where simulation of a low temperature environment is desired. For temperatures lower than 25 degree C., where moisture condensation can result on substrates, the use of a gas tight system as described above would be preferred such that most of the water content is removed. The common methods and apparatus used to control the temperature of a substrate is well-known in the art and thus is not discussed further. Computer **30** also

controls the movement of holding fixture **16***a* so that it can be aligned to probing device **42**. The detailed description of alignment of wafer **40** to probing device **42** is disclosed in U.S. Pat. Nos. 5,103,557 and 5,354,695, describing optical and electronic sensors, respectively. It should be noted that instead of moving holding fixture **16***a*, probing device **42** can be moved to align probing device **42** to wafer **40**. Although, in the preferred embodiment, computer **30** controls turning on and off vacuum source **46**, the movement of holding fixture **16***a* and the temperature of temperature control device **48**, such functions can be performed manually.

[**0034**] During functional circuit testing, computer **30** sends control signals to probe points **44** of probing device **42** through electronic circuit board **18***a* and IC circuitry **50**. ICs on wafer **40** generate data signals in response to the control signals, and the data signals are sent back to computer **30** so that computer **30** can analyze the data signals and determine the functionality of each IC on wafer **40**.

[**0035**] During burn-in, computer **30** sends control signals to heat or cool wafer **40** to specific temperatures for a predetermined period of time and electrical signals to probe points **44** of probing device **42** so that the ICs on wafer **40** can be tested while they are stressed under certain temperature and electrical conditions. The ICs on wafer **40** generate data signals which are sent to computer **30** to analyze and determine which ICs pass the burn-in test.

[**0036**] After a functional test or a burn-in test, computer **30** analyzes the data obtained from the ICs on wafer **40** and provides new control signals to probe points **44** either to repair the ICs on wafer **40** and/or to program the ICs by fusing or anti-fusing circuits within the ICs as is done with memory circuits. For example, to repair a circuit, computer **30** can provide control signals to probing device **42** so that high voltage or current can be provided between the appropriate probe points to open up a conducting path or conducting paths. This repairing scheme is used in many areas including, but not limited to, removing shorts created by manufacturing defects, disabling or enabling a portion of a circuit, isolating a portion of a circuit, and attaching a spare or redundant sub-circuit replacing a sub-circuit that has been detached from a main circuit. To program a memory circuit array, computer **30** sends control signals based on the data collected from each IC on wafer **40**. IC circuitry **50** of probing device **42** configures the probe points to enable direct programming of fuses or anti-fuses through the probe points. A Read Only memory circuit array is typically a programmable read only memory (PROM) or a programmable logic array (PLA).

[**0037**] The present invention allows a single semiconductor test and circuit configuration system to perform any or all of the following functions: (a) reducing the thickness of oxide films, (b) performing functionality tests on integrated circuits, (c) performing burn-in tests on ICs, (d) repairing the circuits, (e) programming fuses or anti-fuses, (f) binning the ICs that have been tested, and (g) collection of a database for immediate feedback to the manufacturing process.

[**0038**] First, the present invention can be used to reduce the thickness of oxide films on contact pads of ICs. A typical IC contact pad is made of aluminum, and it naturally forms a 25 .ANG. to 40 .ANG. oxide film on the surface of the contact pad soon after the contact pad is exposed to oxygen. This oxide film optionally can be penetrated by a piercing probe point as described in U.S. Pat. No. 5,323,035 in order to achieve a low resistance contact between a probing point and the contact pad. In operation, when a wafer is moved from wafer cassette **22** onto a holding fixture **16***a* in module **14***a*, a non-oxidizing gas such as nitrogen is introduced to flood chamber **10** and to purge the chamber of oxygen. Then the temperature of the wafer is changed to a specific temperature appropriate for the metal of the contact pads, and a few percent by volume of hydrogen is introduced over the surface of the wafer so that the oxide films can be converted into water vapor when they are combined with hydrogen. The oxide films may be completely removed from the contact pads, or at least the thickness of the oxide films will be reduced by this process. By maintaining a nitrogen environment in chamber **10**, no further oxide is formed on the surface of the metal contact pads, thus providing better contacts between the contact pads and the probing points. Nitrogen is a preferred non-oxidizing gas, and there may be other gases such as argon that may be used in chamber **10**.

[**0039**] Second, the present invention can be used for functional testing of integrated circuits. After the oxide films on the contact pads have been removed or reduced in thickness, or subsequently are to be pierced, the probing points of the probing device come into contact with the contact pads on the wafer. Computer **30** controls the functional testing of the ICs on the wafer. Computer **30** supplies the control signals, receives data signals back from the probing points, and analyzes the data to determine which ICs are functional on the wafer.

[**0040**] Third, the present invention can also perform burn-in of integrated circuits. During burn-in, the integrated circuits on the wafers are tested for a predetermined period of time over a range of predetermined temperature and electrical conditions to produce burn-in data which is transmitted to computer **30** for analysis.

[**0041**] Fourth, after obtaining data from the ICs, computer **30** can analyze the data and bin or speed-grade the integrated circuits according to their individually determined maximum performance.

[**0042**] Fifth, the present invention can also be used to repair the circuits. Computer **30** can supply appropriate control signals to the probe points of the probing device so that appropriate voltage or current can be applied between the probe points to electrically isolate defective portion of an IC or electrically connect spare circuit portions of an IC with the use of fuse and anti-fuse circuit devices. Under appropriate circumstance, arbitrary shorts in a circuit may be opened if probe points are positioned anticipating such short failure condition.

[**0043**] Sixth, the present invention provides a means for programming PROM, EEPROM or PLA circuits. The programming done is typically to pre-set or store binary values in non-volatile memories such as PROM or EEPROM. Small non-volatile memories in microprocessor circuits may also be programmed with serial numbers or version numbers, and configuration or operational parameters that have been generated by test/burn-in processing. Logic products with non-volatile memory may also be programmed such as PLA's or FPLA's. The present invention can also verify and test the capabilities of the circuits after it has been programmed. Thus, if the wafers in chamber **10** contain

memory circuits, computer **30** can supply control signals to the probe points so that the probe points can apply appropriate charges to the circuits within the memory circuits. The ICs can be re-tested for their functionality or burned-in after the circuits are repaired and/or programmed. Also, the binning process can be performed after a functionality test, burn-in or circuit configuration.

[**0044**] Seventh, the present invention provides a means for generating a computer database with the various status information for every circuit processed. This database can be used in subsequent processing steps by the present invention, such as in the repairing or programming steps. One important aspect of the database is that it can provide timely performance distribution statistics and physical distribution statistics to the circuit manufacturing engineers or process engineers. Presently, such information is only partially available after packaging is completed, typically several weeks later. The present invention would make the availability of this information timely enough to allow adjustments to be made to the manufacturing process so that processing steps that are slowly going out of specification and affecting product quality can be corrected. The capability of near-real time adjustments to the manufacturing process will allow savings by reducing the number of products that do not satisfy specifications.

[**0045**] **FIG. 4** presents a flow chart illustrating a typical process flow of the present invention. At step **82**, a wafer cassette having a plurality of wafers is inserted into the chamber. At step **84**, the chamber is closed. At step **86**, the wafers are loaded into the individual modules using handler **12** in **FIG. 1**. At step **88**, a non-oxidizing gas such as nitrogen is introduced into chamber **10** to flood the chamber and purge the chamber of oxygen and moisture. At step **90**, the wafers are heated. At step **92**, a few percent by volume of hydrogen is introduced over the surfaces of the wafers. At step **94**, the oxide films on the contact pads of the wafers are removed or reduced in thickness when the oxides combine with hydrogen. At step **96**, hydrogen is stopped from flowing into chamber **10**, but nitrogen continues to be supplied to chamber **10** to maintain a nitrogen environment in chamber **10**. At step **98**, the ICs are probed for a functionality test and/or electrical burn-in. At step **100**, circuit configuration can be performed to either repair the circuits and/or to program the circuits if the circuits are non-volatile memory circuits. At step **102**, the ICs on the wafers can be re-tested for their functionality. At step **104**, computer **30** in **FIG. 1** can analyze the data obtained from the ICs and bin the ICs according to their performance characteristics. At step **106**, the wafers are unloaded from the holding fixtures and placed into the wafer cassette. At step **108**, the chamber is opened to take the wafer cassette out from the chamber.

[**0046**] **FIG. 5** shows a computer system that may be utilized as computer **30** in **FIG. 1** in accordance with the present invention. A computer host **1000** includes a memory **1008** and a central processor **1002**. Memory **1008** and central processor **1002** are those typically found in most general purpose computers and almost all special purpose computers. In fact, these devices contained within computer host **1000** are intended to be representative of the broad category of data processors and memory. Many commercially available computers having different capabilities may be utilized in the present invention. It will be appreciated that although computer **30** may include various other components described below, it may only need computer host **1000** to control the elements in chamber **10**.

[**0047**] A system bus **1016** is provided for communicating information to and from computer host **1000** and the electronics in chamber **10** to allow control and the transfer of data. System bus **1016** can also be used to connect computer host **1000** to other components. For example, a display device **1010** utilized with the computer system of the present invention may be a liquid crystal device, cathode ray tube or other display device suitable for creating graphic images and/or alphanumeric characters recognizable to a user. The computer system may also include an alphanumeric input device **1012** including alphanumeric and function keys coupled to bus **1016** for communicating information and command selections to central processor **1002**, and a cursor control device **1018** coupled to bus **1016** for communicating user input information and command selections to central processor **1002** based on a user's hand movement. Cursor control device **1018** allows the user to dynamically signal the two-dimensional movement of the visual symbol (or cursor) on a display screen of display device **1010**. Many implementations of cursor control device **1018** are known in the art, including a track ball, mouse, pen, joystick or special keys on the alphanumeric input device **1012**, all capable of signaling movement in a given direction or manner of displacement.

[**0048**] The computer system of **FIG. 5** also includes an interface device **1019** coupled to bus **1016** for communicating information to and from the computer system. Interface device **1019** may be coupled to a microphone, a speaker, a network system, other memory devices, other computers, etc. Also available for interface with the computer system of the present invention is a data storage device **1017** such as a magnetic disk or optical disk drive, which may be communicatively coupled with bus **1016**, for storing data and instructions. The computer system of **FIG. 5** may also include a printer for outputting data.

[**0049**] Although functional testing is the typical testing capability of the preferred environment, parametric testing can also be done for circuit characterization. The software that controls the mechanics of the present invention, the data preparation for testing, test processing, and test result analyzing complements the circuitry contained in the probing devices contained in the modules.

[**0050**] While the present invention has been particularly described with reference to the various figures, it should be understood that the figures are for illustration only and should not be taken as limiting the scope of the invention. Many changes and modifications may be made to the invention, by one having ordinary skill in the art, without departing from the spirit and scope of the invention.

What is claimed is:

1. A system for processing a plurality of integrated circuits formed on a substrate, each of said integrated circuits having a plurality of conductive contact portions, said system comprising:

a first module having:

a probing device having a plurality of probe points for simultaneously contacting substantially all said integrated circuits, said probing device having a support on which said probe points are formed and having cir-

cuitry thereon which generate test signals for performing at least one of functional testing, at-speed functional testing and burn-in processing of said integrated circuits; and

a fixture which holds said substrate, wherein a maximum travel, in a plane parallel to a principal surface of said substrate, between said fixture and said probing device, is a distance across a limited central portion of said substrate, and said fixture holds said substrate;

wherein said first module electrically couples said plurality of probe points of said probing device to said plurality of conductive contact portions of said substrate; and

a programmed computer is coupled to said circuitry of said probing device, and utilizes substantially fewer signal lines than a total number of said plurality of probe points of said probing device.

2. The system of claim 1, further comprising:

a second module having:

a second probing device having a plurality of probe points for simultaneously contacting substantially all of a plurality of integrated circuits formed on a second substrate, said second probing device having a support having circuitry thereon which generate test signals for performing at least one of functional testing, at-speed functional testing and burn-in processing of said integrated circuits; and

a second fixture which holds said second substrate, wherein a maximum travel, in a plane parallel to a principal surface of said second substrate, between said second fixture and said second probing device, is a distance across a limited central portion of said second substrate, and said second fixture holds said second substrate;

wherein said second module couples said plurality of probe points of said second probing device to said plurality of conductive contact portions of said second substrate; and

said programmed computer is coupled to said circuitry of said second probing device.

3. The system according to claim 2, wherein at least one of said first and second modules further comprises a temperature control device which modifies a temperature of at least one of said substrates.

4. The system according to claim 3 further comprising a gas source coupled to said at least one module.

5. The system according to claim 2 further comprising a handler to move said substrates.

6. The system according to claim 6 further comprising:

a chamber enclosing said first and second modules, said handler and said temperature control device, wherein said programmed computer is coupled to said handler, said temperature control device, and said first and second modules.

7. The system according to claim 2 wherein at least one of said first and second modules further comprises a circuit board coupled to said programmed computer.

8. The system according to claim 2 further comprising a chamber enclosing said substrates.

9. The system according to claim 2 wherein at least one of said first and second modules is gas tight.

10. The system according to claim 2 wherein at least one of said substrates is an entire semiconductor wafer.

11. The system according to claim 1 wherein said circuitry of said probing device performs functional circuit testing, electrical burn-in, repair, and programming.

12. The system of claim 1 wherein said circuitry of said probing device performs at least two different functions selected from the group consisting of functional testing, at speed functional testing, burn-in processing, programming, and repair processing.

13. The system of claim 2, wherein said circuitry of said probing device performs functional testing and burn-in testing of said integrated circuits.

14. The system of claim 13, wherein said probing device is configured to probe an entire semiconductor wafer.

15. The system of claim 1 wherein said circuitry is configured to test each of said integrated circuits individually.

16. The system according to claim 15 further comprising:

a gas source coupled to said system said gas source providing a first gas; and

a temperature control device which modifies a temperature of portions of said integrated circuits adjacent said conductive contact portions.

17. The system according to claim 16 wherein said gas source provides a second gas that is non-oxidizing, and said first gas is hydrogen.

18. The system according to claim 16 wherein said first module is gas tight.

19. The system according to claim 15 wherein said circuitry comprises integrated circuitry.

20. The system according to claim 19 wherein said integrated circuitry comprises active switching circuits.

21. The system according to claim 15 wherein a number of said plurality of probe points exceeds 10,000.

22. The system according to claim 15 wherein said probing device further comprises a membrane supporting said plurality of probe points.

23. The system according to claim 22 wherein said circuitry comprises active switching circuitry.

24. The system according to claim 22 wherein a number of said plurality of probe points exceeds 10,000.

25. The system according to claim 22 further comprising:

a gas source for supplying at least a first gas into said system; and

a temperature control device for modifying a temperature in a predetermined area of each of said integrated circuit.

26. The system according to claim 25 wherein said gas source provides a second gas that is non-oxidizing, and said first gas is hydrogen.

27. The system according to claim 25 wherein said first module is gas tight.

28. The system of claim 1 wherein said circuitry is passive only.

29. The system of claim 1 wherein said circuitry has active switching circuitry.

30. The system of claim 29 wherein said active switching circuitry causes a given signal line to be coupled to a first of

said plurality of probe points at a first time and a second different probe point at a later time.

31. The system of claim 30 wherein said first and second probe points each correspond to an output pad of one of said integrated circuits.

32. The system of claim 1 wherein said fixture holds said substrate in a fixed position from a time at which a first of said integrated circuits is processed to a time at which a last of said integrated circuits is processed.

33. The system of claim 1 wherein said circuitry of said probing device performs both functional testing and burn-in testing of said integrated circuits.

34. The system according to claim 2, further comprising a temperature control device which modifies a temperature of one of said substrates, and a gas source.

35. The system according to claim 34 wherein at least one of said first and second modules further comprises a gas source for supplying at least a non-oxidizing gas.

36. The system according to claim 34 wherein at least one of said first and second modules further comprises a circuit board coupled to said computer.

37. The system according to claim 34 wherein at least one of said first and second modules is gas tight.

38. The system according to claim 1 wherein said computer stores a database of performance data corresponding to each of said integrated circuits.

39. A system for processing one or more substrates, each of said substrates having a plurality of integrated circuits formed thereon, each of said integrated circuits having a plurality of conductive contact portions, said system comprising:

one or more modules, each of said modules including:

a probing device including a plurality of probe points for simultaneously contacting substantially all said integrated circuits formed on an associated one of said substrates, said probing device having a support having circuitry thereon which generates test signals to perform at least one of functional testing, at-speed functional testing and burn-in testing of said integrated circuits of said associated substrate, wherein said plurality of probe points electrically contact substantially all of said plurality of conductive contact portions of each of said integrated circuits of said associated substrate, and wherein said circuitry is configured to test each of said integrated circuits of said associated substrate individually; and

a fixture which holds said associated substrate, wherein a maximum travel, in a plane parallel to a principal surface of said associated substrate, between said fixture and said probing device, is a distance across a limited central portion of said associated substrate; and

a programmed computer coupled to said circuitry of said probing device of each of said modules, and utilizing substantially fewer signal lines than a total number of said plurality of probe points of said probing device of said modules.

40. The system according to claim 39 further comprising:

a handler which moves said substrates and moves said probing devices;

wherein each of said modules further includes a circuit board for coupling said programmed computer with said circuitry of said probing device; and

wherein said computer sends signals to and receives signals from said handler, said circuit boards, and said fixtures.

41. A system for processing a plurality of integrated circuits on a work piece, each of said integrated circuits having a plurality of conductive contact portions, said system comprising:

a probing device including:

a semiconductor substrate,

a plurality of probe points on said semiconductor substrate, each of said probe points being associated with one of said plurality of conductive contact portions, and

a plurality of transistors and interconnects therebetween on said semiconductor substrate, wherein said plurality of transistors and interconnects generates signals for processing at least one of functional testing, at-speed functional testing, and burn-in testing of said plurality of integrated circuits on said work piece substrate; and

a fixture which holds said work piece for coupling said plurality said conductive contact portions to said associated probe points while substantially all of said plurality of integrated circuits are subject to said processing.

42. A method for processing integrated circuits formed on a substrate, each of said integrated circuits having a plurality of conductive contact portions, said method comprising the acts of:

loading said substrate in a test system and;

performing at least three of (a) to (g) while said substrate is in said test system:

(a) reducing an oxide thickness on at least some of said plurality of conductive contact portions;

(b) testing a functionality of at least one of said integrated circuits;

(c) burning-in said substrate;

(d) repairing at least one of said integrated circuits;

(e) programming at least one of said integrated circuits;

(f) marking a symbol on said substrate; and

(g) collecting data corresponding to performance data of at least one of said integrated circuits.

43. The method of claim 42 wherein the act of testing a functionality comprises the acts of:

transmitting first electrical signals from a computer to a circuit board;

transmitting second electrical signals from said circuit board to processing circuitry of a probing device;

applying third electrical signals from said processing circuitry electronics to said plurality of conductive contact portions of said integrated circuits through a plurality of probe points of said probing device; and

transmitting fourth electrical signals to said computer, said fourth electrical signals produced in response to said third electrical signals.

44. The method of claim 42 wherein the act of burning in said substrate comprises the act of testing for a predetermined time period over a range of predetermined temperatures and electrical conditions each of said integrated circuits of said first substrate.

45. The method of claim 42 wherein the act of repairing comprises the acts of:

transmitting electrical signals from a computer to a probing device having a plurality of probe points; and

applying an electrical stimulus via selected ones of said plurality of probe points thereby causing at least one of a fuse circuit device and an anti-fuse circuit device of said substrate to change state.

46. The method of claim 42 wherein the act of programming comprises the acts of:

transmitting electrical signals from a computer to a probing device having a plurality of probe points; and

applying electrical stimuli via selected ones of said plurality of probe points thereby causing binary values to be stored non-volatilely in said integrated circuits.

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