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(71) Applicant(s):
mqSemi AG
Delta Consultants AG, Baarerstrasse 23, Zug 6300, Switzerland

(72) Inventor(s):
Munaf Rahimo
Iulian Nistor

(74) Agent and/or Address for Service:
mqEng Ltd
101 Rose Street South Lane, Edinburgh, Scotland, EH2 3JG, United Kingdom

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Other: **WPI, EPODOC**

(54) Title of the Invention: **Semiconductor device**
Abstract Title: **Thyristor having increased maximum turn-off current with a narrowed cathode base region in the first base layer**

(57) A power semiconductor device with a five-layer structure comprises: a first base layer 8 with a high dopant concentration adjacent to a cathode region 7 and the gate electrodes 10. A second base layer 9 arranged between the first base layer 8 and a drift layer 4 has the same dopant type as the first base layer 8 and lower dopant concentration. The first base layer 8 comprises a cathode base region 8a and a gate base region 8b arranged adjacent to each other, such that the cathode base region 8a is contacting the cathode region 7. The cathode base region 8a has a lower dopant concentration than the gate base region 8b and/or the gate base region 8b has a greater depth than the cathode base region 8a to achieve an optimized distribution of the field in blocking state, and to increase the maximum turn-off current capability when operating in dynamic avalanche conditions.

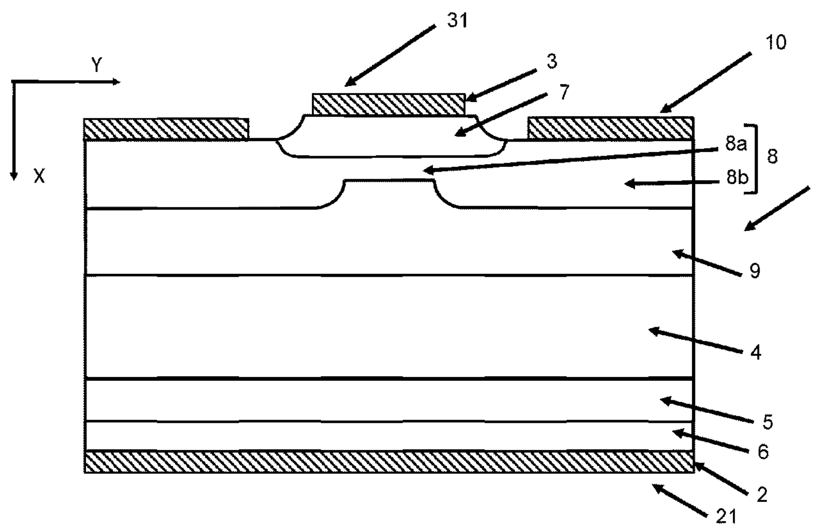

FIG. 4

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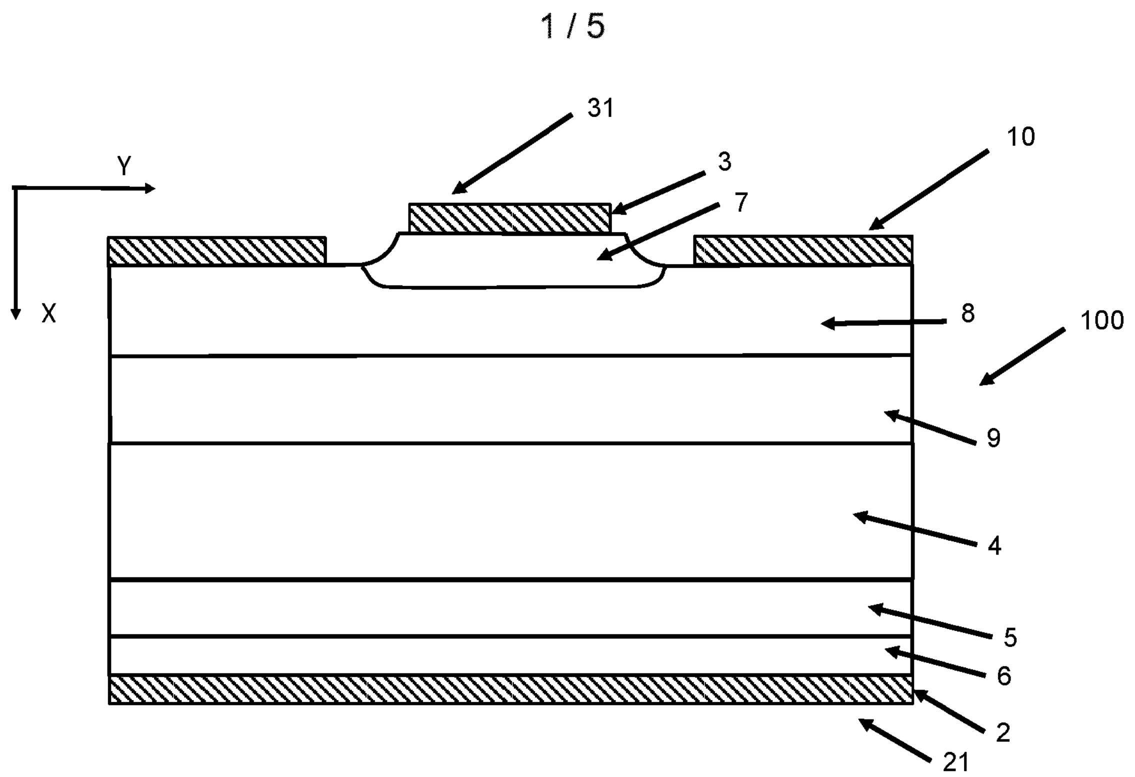

FIG. 1

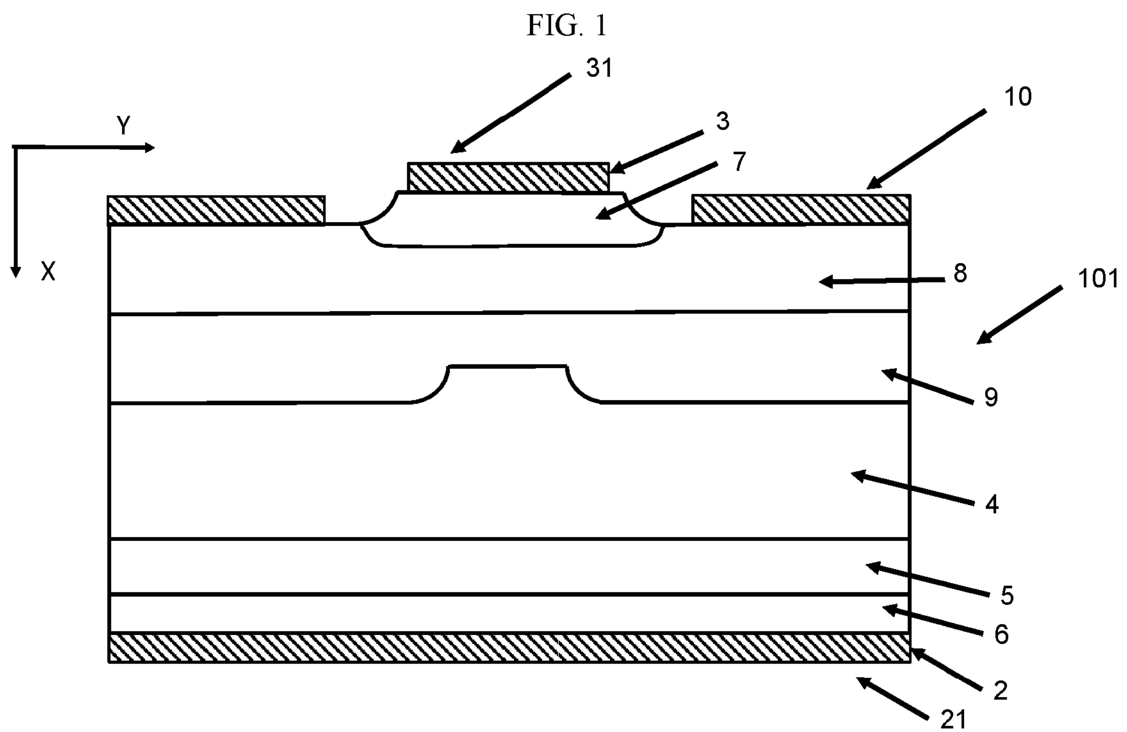

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FIG. 2

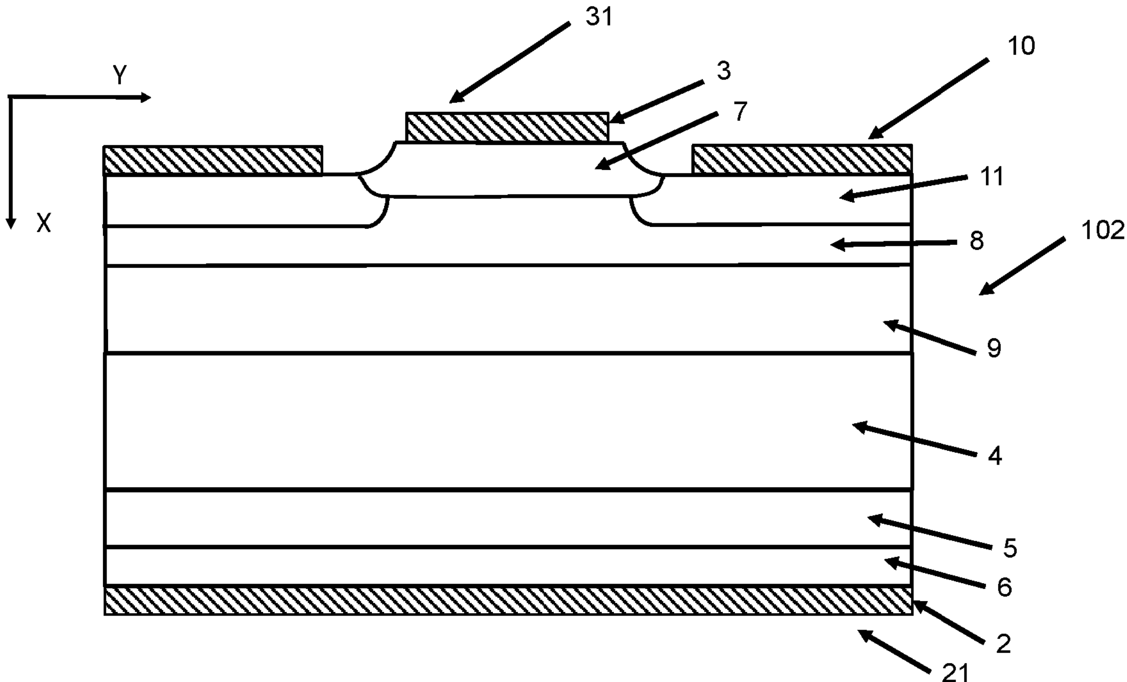

FIG. 3

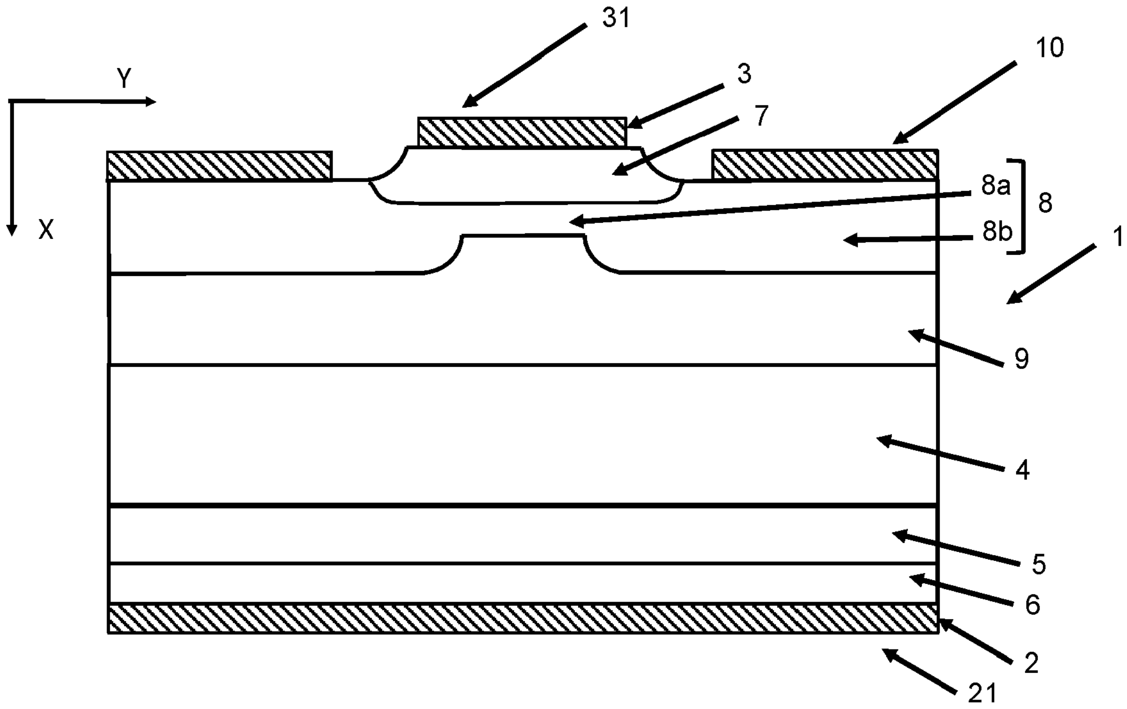

FIG. 4

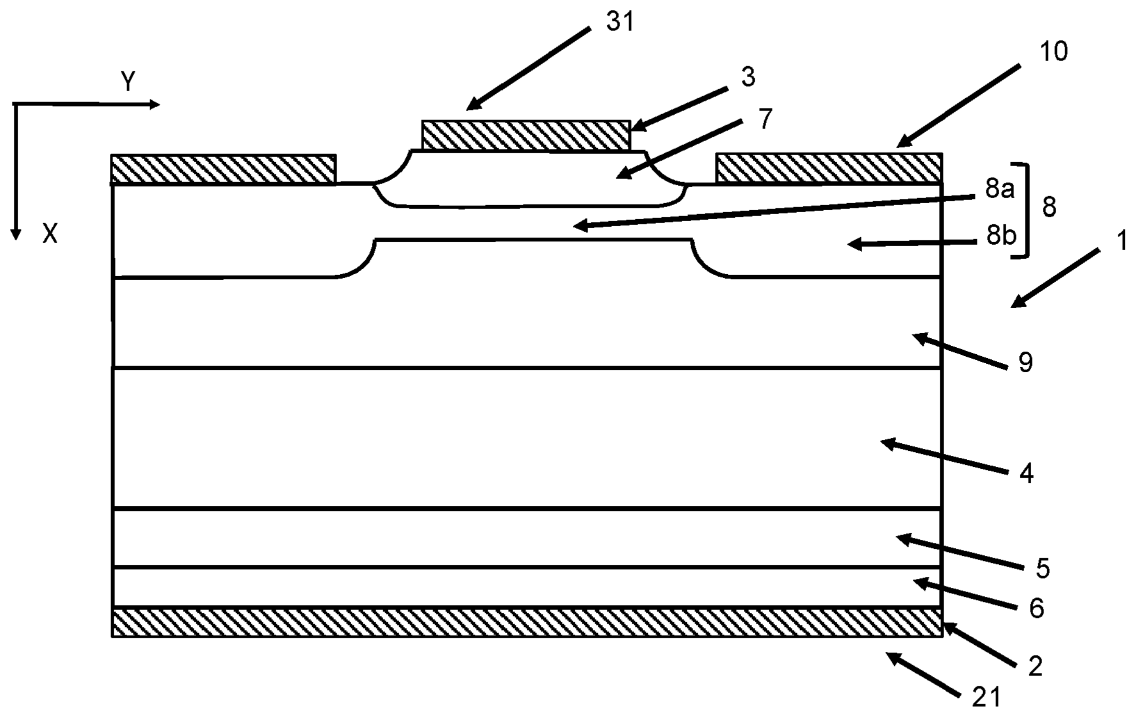

FIG. 5

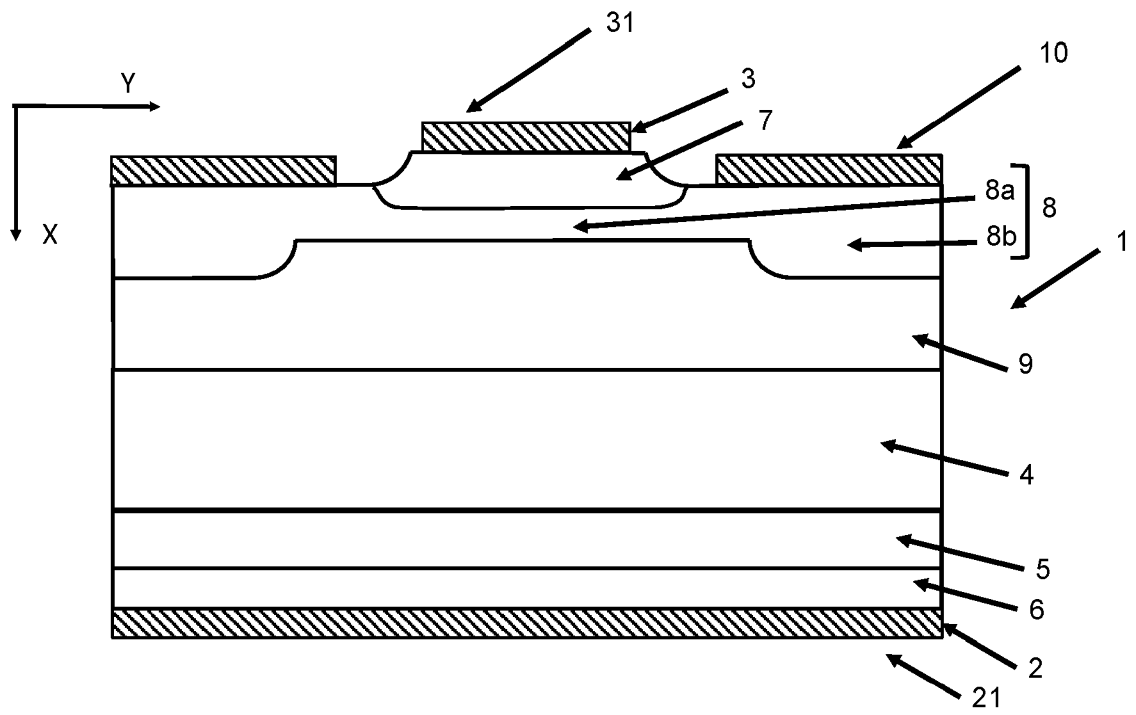

FIG. 6

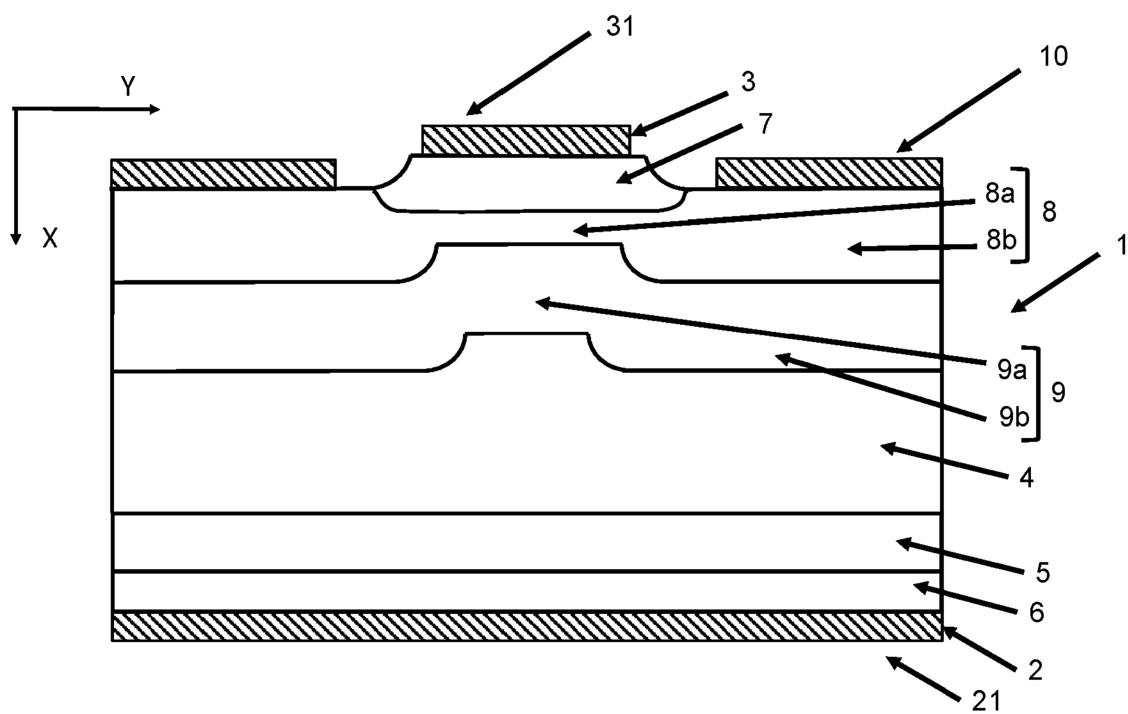

FIG. 7

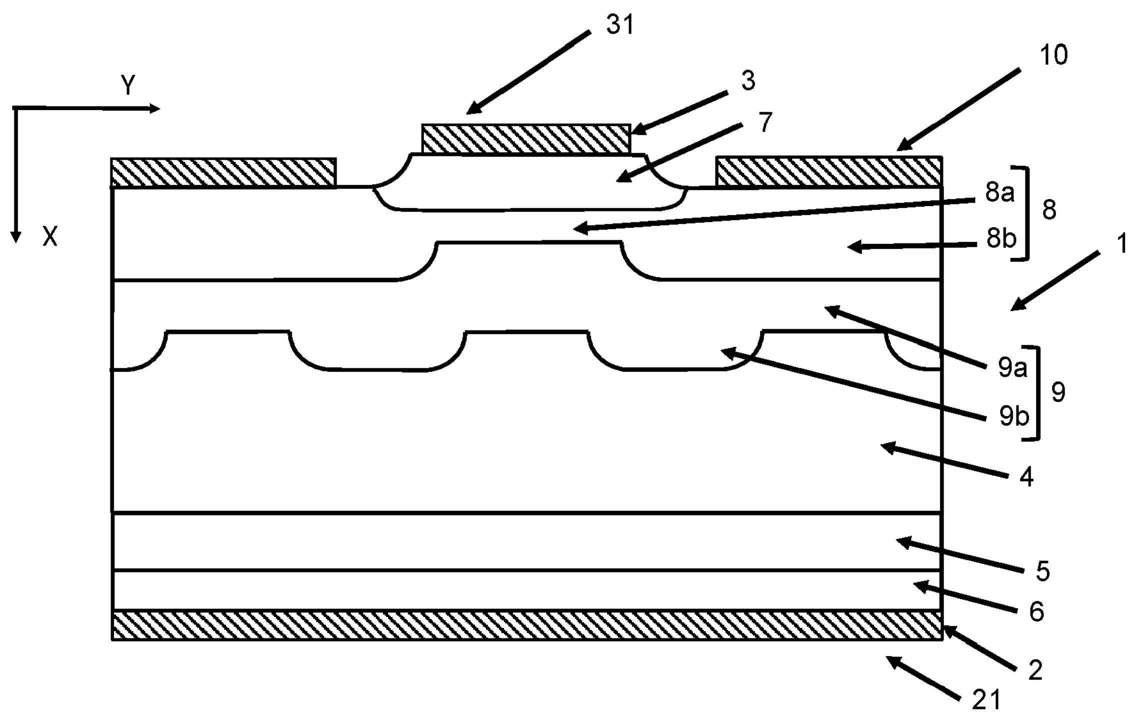

FIG. 8

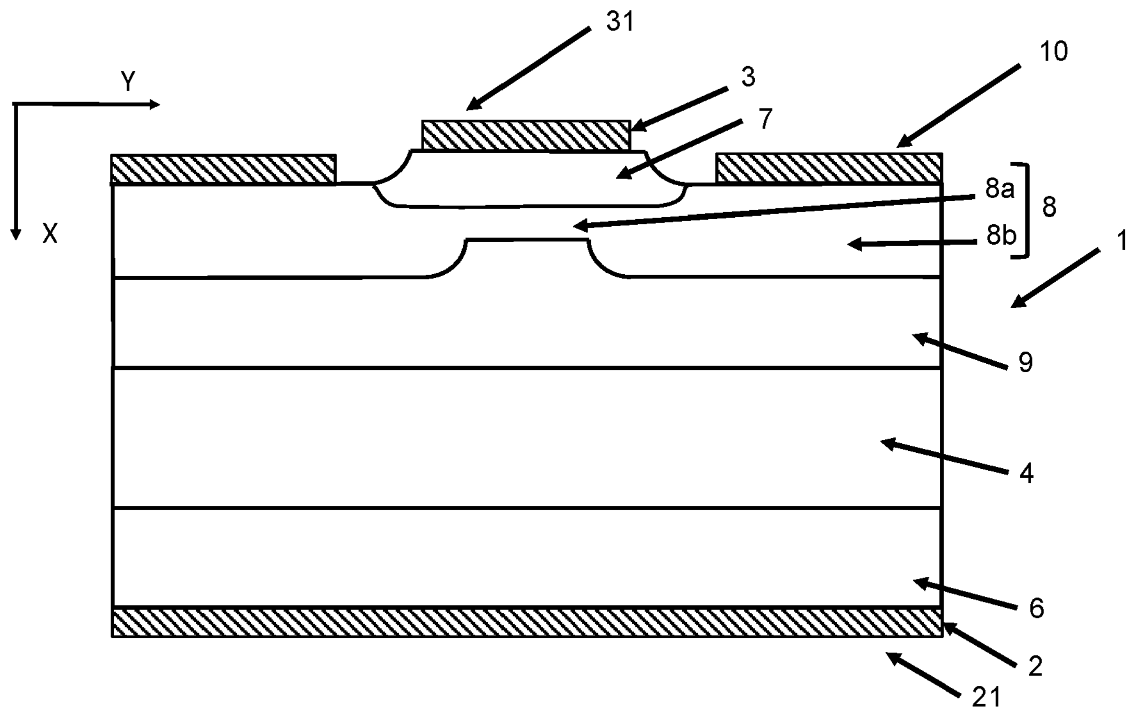

FIG. 9

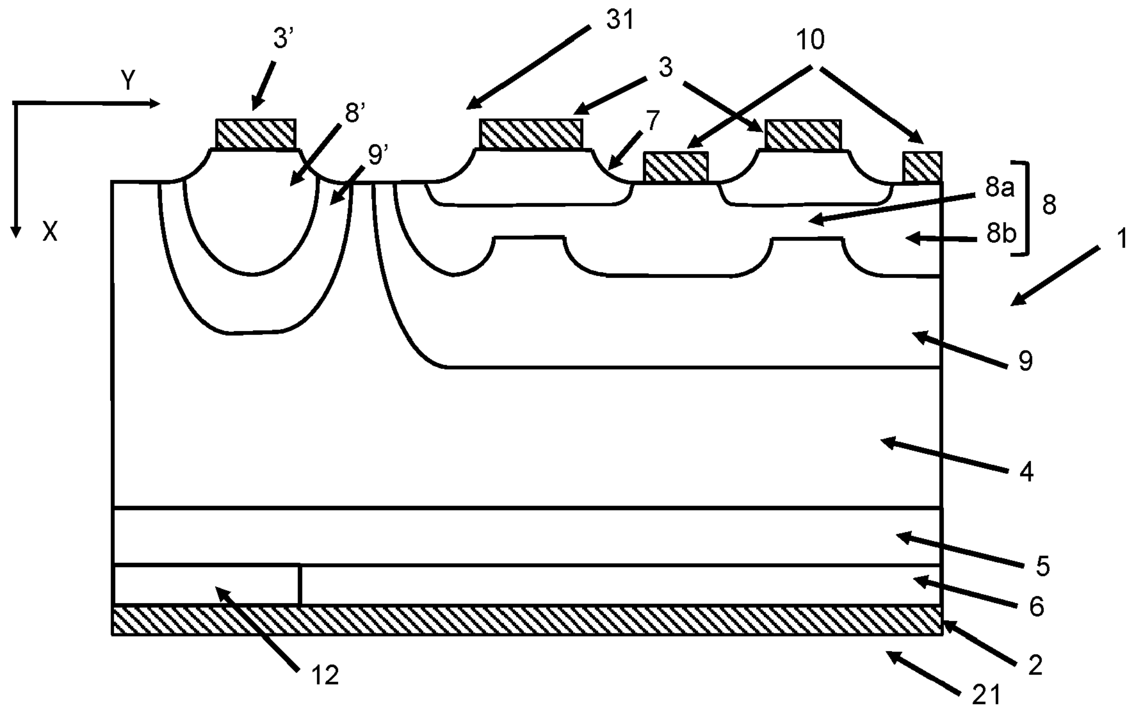

FIG. 10

SEMICONDUCTOR DEVICE

FIELD OF THE INVENTION

The invention relates to the field of power semiconductor devices. More particularly it relates to a power semiconductor device having multiple layers of different conductivity types.

TECHNICAL BACKGROUND

Integrated gate commutated thyristors (IGCT) comprise a four-layer pnpn structure comprising an (n+) doped cathode layer, on which a cathode metallization is arranged, adjacent to a (p) doped base layer, which is contacted by a gate electrode, followed by an (n−) doped drift layer and a (p+) doped anode layer. The anode layer is covered by an anode metallization. When such an IGCT is switched from the conduction state in the blocking state, in so called “turn-off phase”, holes are flowing efficiently laterally within the (p−) base layer to the gate electrode. The holes that still reach the (n+) cathode layer may retrigger the thyristor preventing the semiconductor to switch-off.

Most IGCT applications do not use snubbers (i.e. resistor-capacitors connected in parallel to the semiconductor device) to limit the voltage rise during the turn-off phase. Therefore, the device can enter the dynamic avalanche operation mode, where new carrier pairs are generated during turn-off. If an IGCT is driven into this mode, holes generated at turn-off may also reach the (n+) cathode layer, retriggering the device and thereby limiting the maximum turn-off current (referred to as SOA or “Safe Operating Area” of the semiconductor device).

The basic IGCT device concept is shown in FIG. 1 for a punch through structure (i.e. using an additional (n) doped buffer layer). The (p) base layer usually consists of two regions

- a shallow ($<80\mu m$) and highly doped first base region (maximum dopant concentration $>1e^{17}/cm^3$)

- a deep (>80μm) and lightly doped second base layer (maximum dopant concentration $<1e^{16}/cm^{3}$)

The first base layer is required to ensure good ohmic contact to the gate electrodes, and to provide a low resistance path to the flow of holes during the turn-off phase. The second base layer is required to ensure the proper voltage blocking capability of the device. The first base layer and the second base layer form a uniform (P+)/(P-) semiconductor junction extending parallel with the main sides of the semiconductor device. Similarly, the second base layer and the drift-layer form a uniform (P-)/N semiconductor junction extending parallel with the main sides of the semiconductor device.

For such a standard IGCT semiconductor device, during turn-off under extreme dynamic avalanche conditions, the peak electric field is uniform across the main PN junction between the second base layer and the drift layer. This configuration of the electric field allows extra holes to flow back towards the gate, but moving laterally close to a secondary PN junction between the (n+) cathode layer and the first base layer. At high currents, this lateral flow of holes can develop into a voltage drop that lowers the secondary PN junction potential barrier and results in electrons flowing and the thyristor latching up. Under such conditions the device will fail and its maximum turn-off current capability will be significantly reduced.

The SOA of the semiconductor device can be improved (a) by controlling the peak electric field position at the main PN junction, and (b) by further protecting the (n+) cathode layer. The U.S. Pat. No. 7,816,706 provides an alternative design to increase the maximum turn-off current capability by controlling the position of the peak electric field at the main PN junction. This is achieved by forming the second base layer with a cathode base region and a gate base region, having different depths in the first dimension leading to a “corrugated” second base layer as shown in FIG. 2. A further improvement depicted in FIG. 3 is protecting the side edges of the (n+) cathode layer by introducing additional (p++) doped regions as described in U.S. Pat. No. 8,823,052. However, both methods can only provide one of the two improvements (a) or (b) mentioned above.

It is thus further desirable to identify the optimal means to simultaneously achieve both improvements (a) and (b) mentioned above, by using a method that is easily manufactured, and does not generate other effects impairing the semiconductor device performance.

SUMMARY

A five-layer power semiconductor device with an increased maximum turn-off current which is easily manufactured is disclosed.

A power semiconductor device is disclosed with a semiconductor substrate and a cathode metallization being formed on a cathode side and an anode metallization being formed on an anode side opposite the cathode side. Such an exemplary semiconductor substrate comprises a five-layer structure with layers of different conductivity types, said five-layer structure defining an inner structure of a thyristor, which can be turned-off via a gate electrode. The five-layer structure comprises a cathode layer of a first conductivity type contacting the cathode metallization,

a first base layer of the second conductivity type contacting the cathode layer on a side opposite the cathode metallization,

a second base layer of the second conductivity type contacting the first base layer on a side opposite the cathode metallization,

a fourth or drift layer of the first conductivity type contacting the second base layer on a side opposite the cathode metallization, and

a fifth or anode layer of second conductivity type contacting the anode metallization,

said gate electrode being arranged on the cathode side and electrically contacting said first base layer.

The first base layer comprises a cathode base region and at least one gate base region, said cathode base region being arranged adjacent to the cathode layer on the side opposite the cathode metallization and contacting at least a central area of the cathode layer, said at least one gate base region being disposed adjacent to the second base layer and bordering on the cathode base region. In a first dimension being defined as a perpendicular distance from the side of the cathode layer, which is opposite the cathode metallization, the said at least one gate base region electrically contacts the gate electrode, and has at least one of the following features:

a higher doping density than the cathode base region in at least one depth, or

a greater depth than the cathode base region.

A method for manufacturing a semiconductor device is disclosed with a semiconductor substrate and a cathode metallization being formed on a cathode side and an anode metallization being formed on an anode side opposite the cathode side, the method comprising the following steps:

on a substrate of first conductivity type a structured layer is produced with a first dopant of the second conductivity type on the cathode side by implantation through a patterned oxide or photoresist layer, a continuous layer is produced on the cathode side with a second dopant of the second conductivity type, and a further continuous layer is produced on the cathode side with a third dopant of the second conductivity type, wherein the first dopant is a slow diffuser and the third dopant is a fast diffuser and the second dopant may be the same as the first dopant,

the dopants are simultaneously diffused into the substrate forming the final layers, whereby the region in which the first and the second dopants were thermally diffused forms at least the one gate base region part of the first base layer, the region in which only the second dopant was diffused forms at least one cathode base region part of the first base layer, and the region in which the third dopant was diffused forms a second base layer extending at a larger depth in the drift layer than the first base layer,

to produce the cathode, the segmented structure on the cathode side, the gate electrodes, the cathode metallization, the anode layer and the anode metallization are formed by standard processes.

It is an object of the invention to provide a power semiconductor device with improved turn-off current capability.

It may also be an object of the present invention to provide an Integrated Gate Turn-off Thyristor with improved electrical characteristics.

The power semiconductor may be a reverse conducting type device with a fifth layer formed of adjacent p and n doped regions. The power semiconductor may also be a reverse blocking type device, where the drift layer and the fifth layer are formed with characteristics required to block the voltage applied between the cathode and the anode electrodes in both polarities.

The new design can be applied to thyristors based on silicon or wide bandgap materials such as Silicon Carbide SiC, Gallium Nitride, or even with drift layers comprising “superjunctions” or “charge compensated regions.”

5 It will be understood that the first dimension corresponds to the direction of the separation of the cathode and anode electrodes, while the second dimension is perpendicular to the first direction in the cross section of the semiconductor device. It will be further understood that the device may extend in a third dimension orthogonal to the first and second dimensions. The first, second and third dimensions generally align with the X, Y and Z dimensions
10 respectively as shown in figures.

These objects may be met by the subject matter of the independent claims. Embodiments of the invention are described with respect to the dependent claims.

15 BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of the invention will be explained in more detail in the following text with reference to the attached drawings, in which:

20 FIG. 1: shows the cross section of an IGCT (prior art).

FIG. 2: shows the cross section of an IGCT with corrugated second base layer (prior art).

FIG. 3: shows the cross section of an IGCT with protected cathode layer (prior art).

FIG. 4: shows the cross section of an IGCT of a first exemplary embodiment according to the invention.

25 FIG. 5: shows the cross section of an IGCT of a second exemplary embodiment according to the invention.

FIG. 6: shows the cross section of an IGCT of a third exemplary embodiment according to the invention.

FIG. 7: shows the cross section of an IGCT of a fourth exemplary embodiment according to
30 the invention.

FIG. 8: shows the cross section of an IGCT of a fifth exemplary embodiment according to the invention.

FIG. 9: shows the cross section of an IGCT of a sixth exemplary embodiment according to the invention.

5 FIG. 10: shows the cross section of an IGCT of a seventh exemplary embodiment according to the invention.

The reference symbols used in the figures and their meaning are summarized in the list of reference symbols. The drawings are only schematically and not to scale. Generally, alike or
10 alike-functioning parts are given the same reference symbols. The described embodiments are meant as examples and shall not confine the invention.

MODES FOR CARRYING OUT THE INVENTION

15 FIG. 4 shows a cross section of the first exemplary embodiment of a semiconductor device 1 in form of a punch through Integrated Gate Commutated Thyristor (IGCT) comprising at least five doped semiconductor layers. The layers are arranged between a cathode electrode 3 on a cathode side 31 and an anode electrode 2 on an anode side 21, which is arranged opposite of the cathode side 31 in a first dimension X. The IGCT semiconductor device 1
20 comprises an n-type doped drift layer 4, an n-type doped cathode layer 7, which is arranged at the cathode side 31 and contacts the cathode electrode 3 and has a higher dopant concentration than the drift layer 4. The semiconductor device 1 further comprises a p-type doped first base layer 8, contacting the cathode layer 3 on a side opposite the cathode electrode 3, and a p-type doped second base layer 9 contacting the first base layer (8) on a
25 side opposite the cathode electrode 3.

Furthermore, a plurality of gate electrodes 10 are formed on the cathode side 31 contacting the first base layer 8. The first gate electrodes 10 can extend longitudinally in a third dimension, when observed in a top plane view.

30

Embedded into the first base layer 8, there is a cathode base region 8a and at least one gate base region 8b. The cathode base region 8a is arranged adjacent to the cathode layer 7 on the

side opposite the cathode electrode 3 and contacting at least a central area of the cathode layer 7. The at least one gate base region 8b electrically contacts the gate electrode 10, and borders said cathode base region 8a. The depth at which the gate base region 8b extends in the second base layer 9 is greater than the depth at which the cathode base region 8a extends
5 in the second base layer 9, when referenced to the main side with the cathode electrode 3.

The cathode layer 7, the first base layer 8, the second base layer 9, the drift layer 4, and the electrodes 2, 3 and 10 may extend in a top plane view in a third dimension (not shown).

10 Additional insulation layers may be arranged on the cathode side 31, protecting the surface of the first base layer 8 and of the cathode layer 7 from external influences (not shown).

The power semiconductor device according to the first exemplary embodiment further comprises a p-type doped anode layer 6 arranged between a buffer layer 5 and the anode
15 electrode 2, which anode layer 6 is in direct electrical contact to the anode electrode 2. An n-type doped buffer layer 5 is arranged between the anode layer 6 and the drift layer 4. The buffer layer 5 has a higher dopant concentration than the drift layer 4 and is used in order to stop the progression of the electric field towards the anode layer 6, when the thyristor is blocking voltage in the off-state. The n-type doped buffer layer 5 has a doping density in the
20 range of $10^{15}/cm^3$ up to $5*10^{17}/cm^3$, and/or a depth in the range of 10 µm up to 100 µm. The p-type doped anode layer 6 can have a doping density of $10^{16}/cm^3$ up to $10^{19}/cm^3$, and/or a depth in the range of 1 µm up to 150 µm, a small depth belonging to a transparent anode suitable for punch-through type thyristors, and a large depth to a diffused anode suitable for non-punch-through type thyristors.

25

To better understand the functionality of a semiconductor device according to the first exemplary embodiment of the invention, when a trigger current is applied on the gate electrodes 10, hole charge carriers are injected from the gate electrodes 10 into the first base layer 8 through the gate base region 8b. This turns-on the npn transistor formed between the
30 cathode layer 7, first base layer 8 and second base layer 9, and the drift layer 4. The electron charge carriers are now entering the drift layer 4 and turn-on the pnp transistor formed between the first base layer 8 and second base layer 9, the drift layer 4, and the anode layer 6. The thyristor structure is thus latched up, the semiconductor device is in conduction state,

and a plasma of hole charge carriers is established in the drift layer 4 that modulate its conductivity and allows for minimum losses in conduction state.

During the turn-off state, a negative voltage is applied on the gate electrodes 10 such that over a short period, in the microseconds range, a large current of hole charge carriers is established from the conduction plasma in the drift layer 4, towards the gate electrodes 10 through the gate base region 8b. Differently from a prior art semiconductor designs, the area in which the dynamic avalanche sets in is shifted towards the gate electrodes 10, further away from the centre of the cathode layer 7. The hole charge carriers generated by the dynamic avalanche conditions can reach the gate electrodes 10 more easily, without the risk of retriggering the cathode layer 7. The main PN junction between the deep second base layer 9 and the drift layer 4 is parallel with the main surfaces 21 and 31 of the semiconductor device, unlike prior art where the main PN junction depth was modulated due to the presence of different base regions of different depths and dopant concentrations. Still, the inventors observed in simulations a local modulation effect of the electric field strength at the main PN junction due to the different depths of the cathode base region 8a and the gate base region 8b forming the shallower first base layer 8, while keeping a constant depth of the deeper second base layer 9.

In the first exemplary embodiment, the length of the cathode base region 8a in the Y direction is smaller than the length of the cathode layer 7 in the Y direction. In a second exemplary embodiment as shown in FIG. 5, the length of the cathode base region 8a is substantially same as the length of the cathode layer 7 in the Y direction. Furthermore, in a third exemplary embodiment shown in FIG. 6, the length of the cathode base region 8a is substantially larger than the length of the cathode layer 7 in the Y direction.

In a fourth exemplary embodiment shown in FIG. 7, the first base layer 8 comprises a cathode base region 8a and its corresponding gate base region 8b, while the second base layer 9 comprises a shallow base region 9a and at least one deep base region 9b. The shallow base region 9a is substantially centered in the Y direction with the cathode base region 8a of the first base layer 8. Furthermore, the said deep base region 9b has at least one of the following features:

a higher doping density than the shallow base region 9a in at least one depth, or

a greater depth than the shallow base region 9a.

A fifth exemplary embodiment shown in FIG. 8 and comprises a plurality of shallow base regions 9a and deep base regions 9b, such that in the Y direction some shallow base regions 9a are substantially centered with the gate electrodes 10.

The buffer layer 5 can also be completely omitted if the semiconductor is not of punch-through type, for example a reverse blocking type thyristor as depicted as a sixth exemplary embodiment in FIG. 9. In this case, the extent of the drift layer 4 in the X direction and the dopant concentration of the drift layer 4 must be selected to ensure that the electric field does not reach the anode layer 6 even under highest blocking voltage at breakdown. Similarly, the extent of the anode layer 6 in the X direction and the dopant concentration of the anode layer 6 must be selected to ensure that the electric field does not reach the anode electrode 2 under reverse blocking voltage conditions.

A fully functional semiconductor device consists of multiple thyristor cell structures 1, arranged adjacent to each other on the surface of a semiconductor wafer. A seventh exemplary embodiment, a reverse-conducting type thyristor is shown in FIG. 10 wherein, some regions of the semiconductor wafer are structured with thyristor cell structures, while other regions of the same functional semiconductor wafer are structured as diodes in freewheeling mode. In such devices, a diode cell structure will comprise a diode anode electrode 3' that uses the same metal layer as the cathode electrode 3, and a diode anode region comprising the p-type doped regions 8' and 9' (which may be substantially identical to the first base layer 8 and the second base layer 9 of the thyristor structure, respectively). Furthermore, the anode layer 6 is electrically shorted using an n-type doped layer 12 positioned in the anode layer 6, substantially centered with the corresponding diode anode electrode 3'. The layer 12 must be highly doped to overcompensate the dopant concentration of the anode layer 6. The layer 12 provides a path for electron charge carriers to flow from the anode electrode 2 (which acts as a cathode metallization of the diode part) through the drift layer 4 and the buffer layer 5. Furthermore, the layers 8' and 9' can be made substantially different than the corresponding first base layer 8 and second base layer 9, wherein for example the depth or dopant concentration of the layers 8' and 9' will be optimized taking into account the performance requirements of the diode part (i.e.

conduction and reverse-recovery losses). For example, to reduce the reverse-recovery losses of the diode part, the layer 9' can have a depth substantially smaller than the depth of the corresponding second base layer 9.

5 In the following, a manufacturing method of the inventive semiconductor device is explained. The manufacturing method starts on a wafer of semiconductor material with a first conductivity type representing the drift layer 4 and comprising a cathode side 31 and an anode side 21 opposite the cathode side 21. A first dopant of second conductivity type, which is a slow diffuser, is implanted using a patterned layer of oxide or photoresist deposited on
10 the cathode side 31. In the regions where the patterned layer is present, no first dopants are implanted. The patterned layer is subsequently removed from the cathode side, and a second dopant of second conductivity type, which is also a slow diffuser is implanted on the cathode side 31. Subsequently, a third dopant of second conductivity type, which is a fast diffuser, is implanted on the cathode side 31. Thermal diffusion of all dopants is performed at high
15 temperatures. Subsequently, a cathode base region 8a is formed in the regions where the second dopant was diffused, and at least one gate base region 8b is formed in the regions where the first and second dopants were diffused. A first base layer 8 is thus formed comprising the cathode base region 8a and the at least one gate base region 8b. Because the dopant concentration at the surface of the cathode side 31 is larger in the regions where both
20 the first and second dopants were implanted, the depth of the at least one gate base region 8b is larger than the depth of the cathode base region 8a, when referencing the direction from the cathode side 31 towards the anode side 21. Because the third dopant is a fast diffuser, a second base layer 9 is formed in the regions where the third dopant was diffused, having a depth larger than the depth of the cathode base layer 8a and the gate base layer 8b.

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The steps following the manufacturing of the first base layer 8, and the second base layer 9 are state of the art, comprising forming the cathode layer 7, the anode layer 6, the anode metal electrodes 2, cathode metal electrodes 3 and gate electrodes 10.

30 An inventive semiconductor device produced by such a method comprises a first base layer 8 and a second base layer 9 made from a double or multiple dopant profile with the part of the profile with the smallest depth being formed in a way described above, where the depth is defined with respect to the cathode main side 31. The dopant concentration of the p-doped

regions below the cathode layer 7 is reduced, while keeping a high dopant concentration in the regions below the gate electrodes 10.

Other manufacturing methods for the manufacturing of an inventive semiconductor device are possible. For example, a third dopant of second conductivity type, which is a fast diffuser, is uniformly implanted on the cathode side 31. Thermal diffusion of the third dopant is performed at high temperatures. Subsequently, a first dopant of second conductivity type, which is a slow diffuser is implanted through a patterned layer of oxide or photoresist formed on the cathode side 31. In the regions where the patterned layer is present, no first dopants are implanted. The patterned layer is removed and a second dopant of second conductivity type is implanted on the cathode side 31, and thermal diffusion of all three dopants is performed at high temperatures. Subsequently, a cathode base region 8a is formed in the regions where the second dopant was diffused, and at least one gate base region 8b is formed in the regions where the first and second dopants were diffused. A first base layer 8 is thus formed comprising the cathode base region 8a and the at least one gate base region 8b. The depth of the at least one gate base region 8b is larger than the depth of the cathode base region 8a, when referencing the direction from the cathode side 31 towards the anode side 21. Because the third dopant is a fast diffuser, a second base layer 9 is formed in the regions where the third dopant was diffused, having a depth larger than the depth of the cathode base layer 8a and the gate base layer 8b.

In other embodiments, the material of the drift layer 4 may be different than Silicon, for example it may be made of Silicon Carbide, Gallium Nitride, Gallium Oxide, Zinc Oxide or the like. In this case, the same embodiments as described above can be applied, however the specific dimensions and dopant profiles have to be adjusted accordingly by means known to those experts in the field.

Furthermore, in other embodiments, the drift layer 4 can be formed of plurality of alternating regions shaped as pillars extending in the first dimension, each region comprising a pillar doped with first conductivity type for example p-type doped, and an adjacent pillar doped with second conductivity type, which is opposite of the first conductivity type, for example n-type. The respective dopant concentrations and width of the pillars must be carefully selected to ensure perfect charge compensation when integrating the value of the dopants

over the spatial extent of each pillar. Such structures are mostly known as superjunction or charge compensated semiconductors.

Furthermore, in other embodiments it may be possible that the power semiconductor is made of a multitude of different thyristor cells, but not all cells may be of the same design. For example, the power semiconductor device may be formed with some thyristor cells having the first exemplary embodiment, and with some other thyristor cells having a different design covered in the previous embodiments, or in the prior art.

It is also possible to apply the invention to power semiconductor devices, in which the conductivity type of all layers is reversed, i.e. with a lightly p-type doped drift layer etc.

Reference list

1 : inventive semiconductor device
3 : cathode metallization of the thyristor cell (electrode)
5 3’ : anode metallization of the integrated diode part (electrode)
31 : cathode side
2 : anode metallization of the thyristor cell (electrode)
21 : anode side
4 : (n-) drift layer, substrate
10 5 : (n) buffer layer
6 : (p+) anode layer
7 : (n+) cathode layer
8 : (p) first base layer
8a: (p) cathode base region of the first base layer
15 8b: (p) gate base region of the first base layer
8’ : (p+) anode layer of the integrated diode part
9 : (p-) second base layer
9a: (p) cathode base region of the second base layer
9b: (p) gate base region of the second base layer
20 9’ : (p-) anode layer of the integrated diode part
10 : gate electrodes
11 : additional (p++) doped regions
12 : (n+) shorts in the anode layer (6)
100 : standard IGCT (prior art)
25 101: IGCT with corrugated second base layer (prior art)
102: IGCT with protected cathode layer corners (prior art)

CLAIMS

1. A semiconductor device with a semiconductor substrate and a cathode metallization being formed on a cathode side and an anode metallization being formed on an anode side opposite the cathode side in a first dimension,

said semiconductor substrate comprising a five-layer structure with layers of different conductivity types,

said five-layer structure defining an inner structure of a thyristor, which can be turned-off via a gate electrode, and

said five-layer structure comprising

an outer cathode layer of a first conductivity type contacting the cathode metallization,

a first base layer of the second conductivity type contacting the cathode layer on a side opposite the cathode metallization,

a second base layer of the second conductivity type contacting the first base layer on a side opposite the outer cathode layer,

a drift layer of the first conductivity type contacting the second base layer on a side opposite the outer cathode layer, and

an outer anode layer of second conductivity type contacting the drift layer and the anode metallization,

said gate electrode being arranged on the cathode side and electrically contacting said first base layer,

the first base layer comprising a cathode base region and at least one gate base region,

said cathode base region being arranged adjacent to the cathode layer on the side opposite the cathode metallization and contacting at least a central area of the cathode layer,

said at least one gate base region being disposed adjacent to the cathode base region and the second base layer,

said at least one gate base region electrically contacting the gate electrode, and said at least one gate base region having at least one of the following features:

a higher doping density than the cathode base region in at least one depth, and

a greater depth than the cathode base region.

2. The semiconductor device according to claim 1, wherein the cathode base region of the first base layer has an extent more than the extent of the cathode layer, in a second dimension perpendicular to the first dimension.

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3. The semiconductor device according to claim 1, wherein the cathode base region of the first base layer has a substantially same extent as the extent of the cathode layer, in the second dimension.

10 4. The semiconductor device according to claim 1, wherein the second base layer comprises at least one shallow base region and at least one deep base region,

said at least one deep base region having at least one of the following features:

a higher doping density than the shallow base region in at least one depth, and

a greater depth than the shallow base region.

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5. The semiconductor device according to claim 4, wherein the second base layer comprises at least two shallow base regions and at least one shallow base region is substantially centered in the second dimension with the gate electrode 10.

20 6. The semiconductor device according to any preceding claim, further comprising at least one of:

a buffer layer of the first conductivity type arranged between the drift layer and the anode metallization on the anode side, wherein the doping concentration of the buffer layer is greater than a doping concentration of the drift layer; and

25 an anode layer of the second conductivity type arranged between and directly contacting the buffer layer and the anode metallization on the anode side.

7. The semiconductor device comprising a plurality of thyristor cells according to any preceding claims, wherein the anode layer comprises alternating regions of opposite first and

30 second conductivity types, characterized in that, some of the plurality of thyristor cells have

at least one of the first base layer or the second base layer in direct contact with the cathode metallization.

8. The semiconductor device according to any preceding claim, wherein at least the drift layer is formed of a wide bandgap material.

9. The semiconductor device according to any preceding claim, wherein the drift layer is formed of alternating regions of opposite first and second conductivity types.

10. The semiconductor device comprising a plurality of thyristor cells, with at least one cell according to any preceding claims.

11. A method of manufacturing a semiconductor device according to claim 1, comprising the following steps:

starting with a wafer of semiconductor material with a first conductivity type having a cathode side an opposite anode side,

implanting on the cathode side a first dopant of second conductivity type, through a patterned layer of oxide or photoresist,

removing the patterned layer from the cathode side,

implanting on the cathode side a second dopant of second conductivity type,

implanting on the cathode side a third dopant of second conductivity type,

performing thermal diffusion of all dopants at high temperature,

wherein subsequently,

a cathode base region is formed in the regions where the second dopant was diffused,

at least one gate base region is formed in the regions where the first and second dopants were diffused

a second base layer is formed in the regions where the third dopant was diffused.

12. A method of manufacturing according to claim 11, comprising using first dopants of different ionic species than the second dopants.

13. A method of manufacturing according to claim 11, comprising using third dopants with a higher rate of diffusion than the first and the second dopants.

Intellectual Property Office

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Claims searched:	1-13	**Date of search:**	7 December 2021

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
A	-	JP S58194366 A (MURAKAMI) See abstract.
A	-	JP S57138175 A (MURAKAMI) See abstract.

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
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Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC^{X} :

Worldwide search of patent documents classified in the following areas of the IPC

H01L

The following online and other databases have been used in the preparation of this search report

WPI, EPODOC

International Classification:

Subclass	Subgroup	Valid From
H01L	0029/10	01/01/2006
H01L	0029/08	01/01/2006
H01L	0029/744	01/01/2006