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H01L 21/471

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U1S 2121 H1K

(56) Documents cited
None

(58) Field of search
H1K

(54) **Process of fabricating semiconductor integrated circuit device**

(57) A semiconductor integrated circuit device has a word line (WL) of a memory array formed by a polycrystalline silicon layer 9A and a layer 9B containing a refractory metal of high melting point (e.g. a molybdenum silicide layer). A phosphosilicate glass film 12 insulates the word line from a conductive layer 14 forming a bit line of the memory array. The formation of the phosphosilicate glass film 12 tends to cause the layer 9B containing refractory metal to peel away from the polycrystalline layer 9A. To prevent this, a layer 11 of insulating material is formed between the phosphosilicate glass film 12 and the layer 9B containing refractory metal. This layer 11 eliminates or reduces peeling and so improves the device. The layer 11 may be formed by deposition, its thickness depending on the material from which it is formed.

FIG. 1B

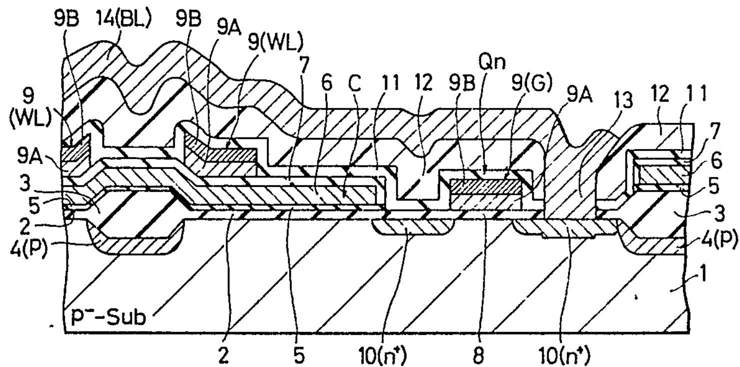

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FIG. 1A

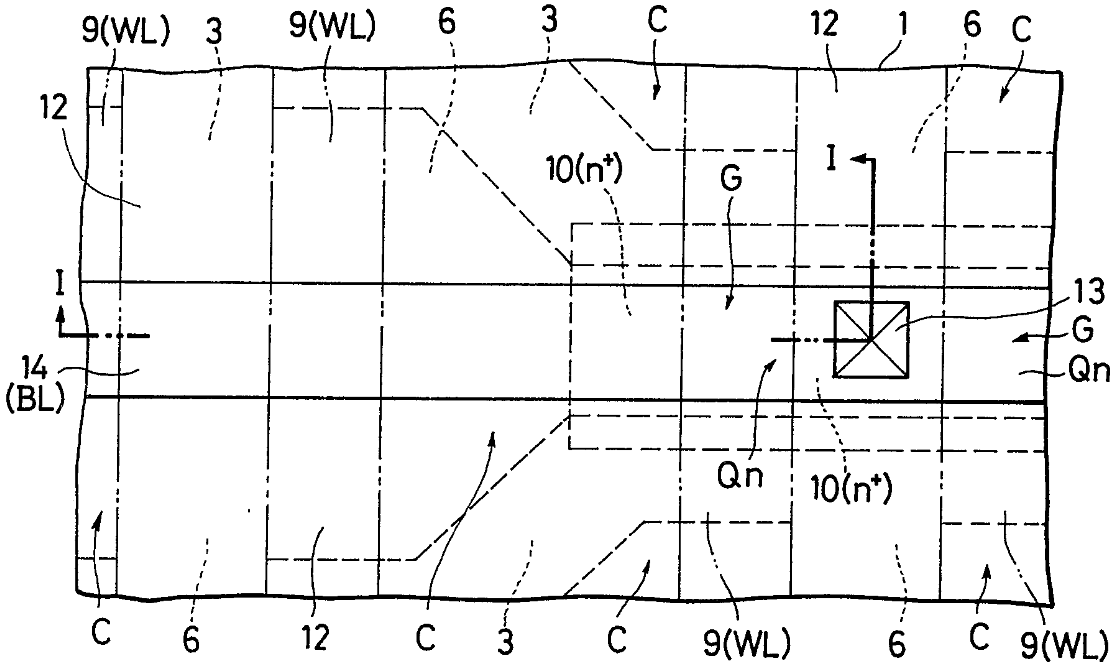

FIG. 1B

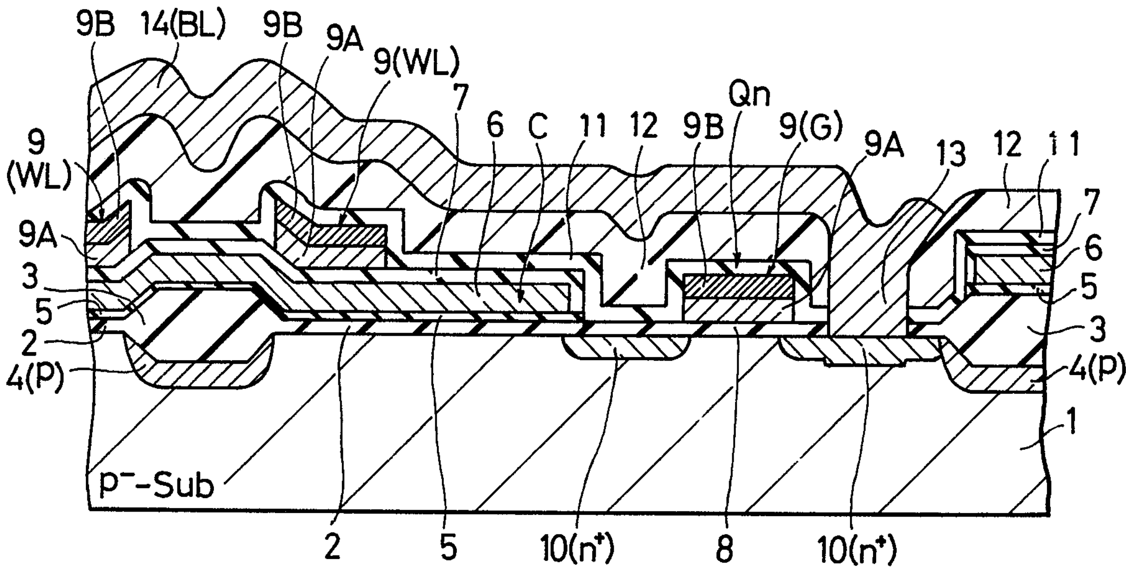

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FIG. 2A

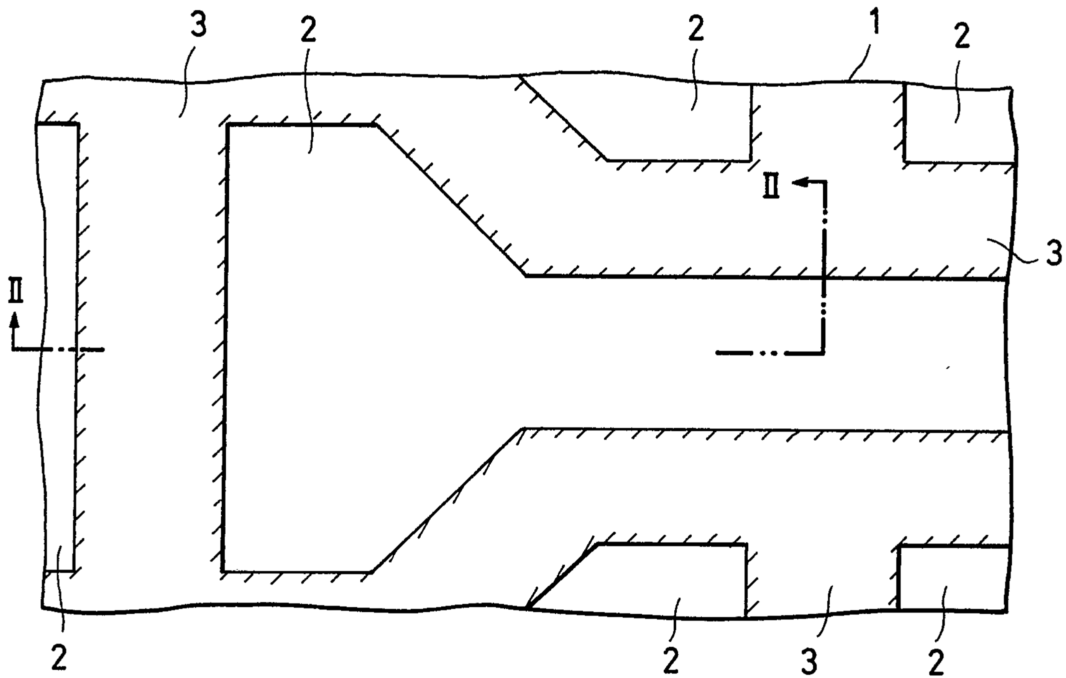

FIG. 2B

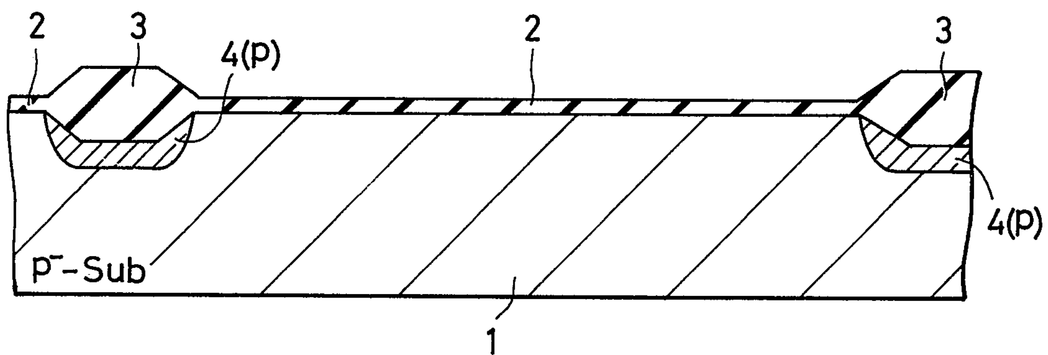

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FIG. 3A

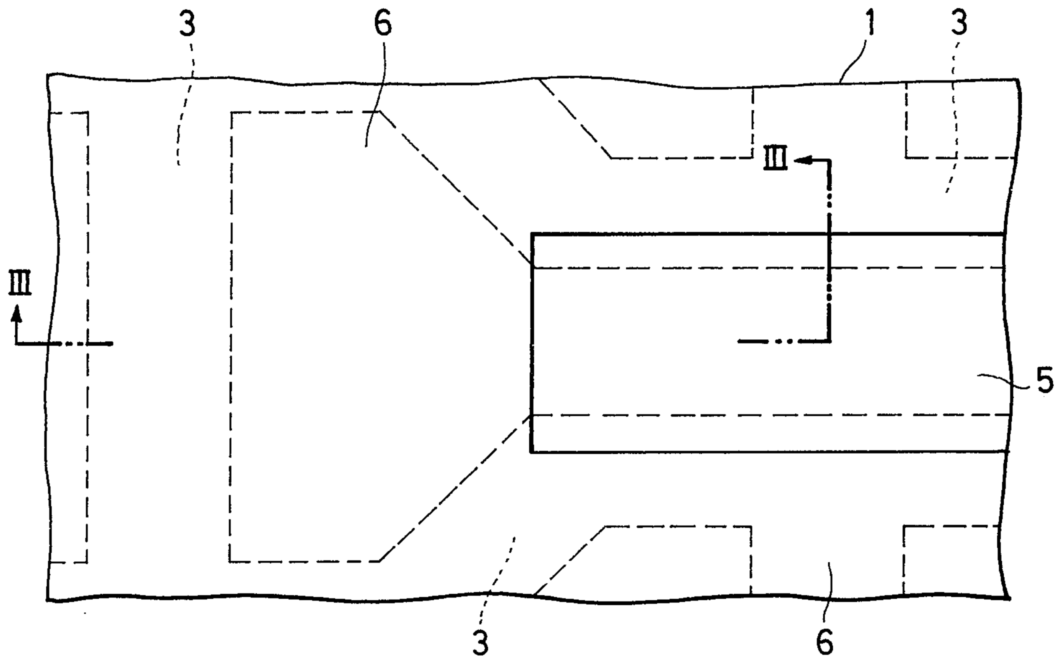

FIG. 3B

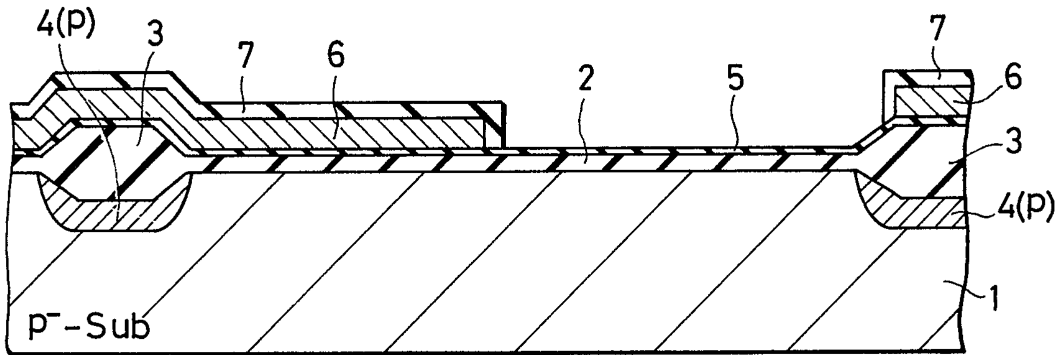

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FIG. 4A

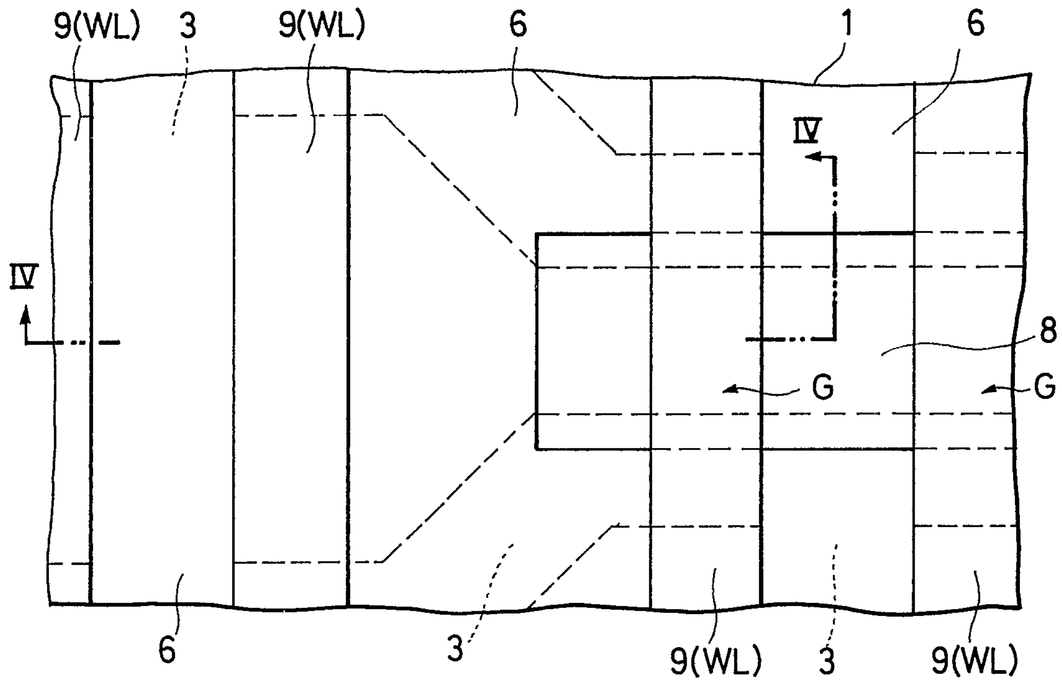

FIG. 4B

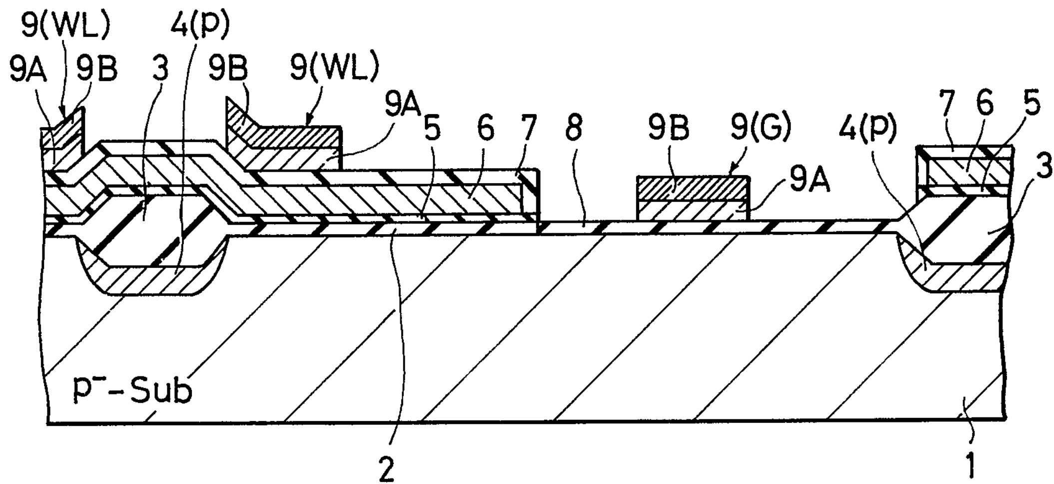

FIG. 5

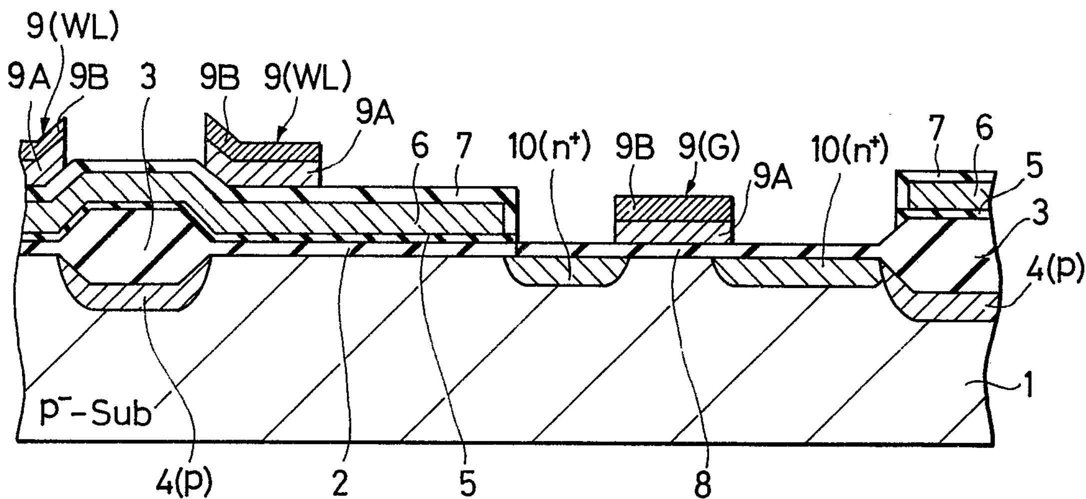

FIG. 6

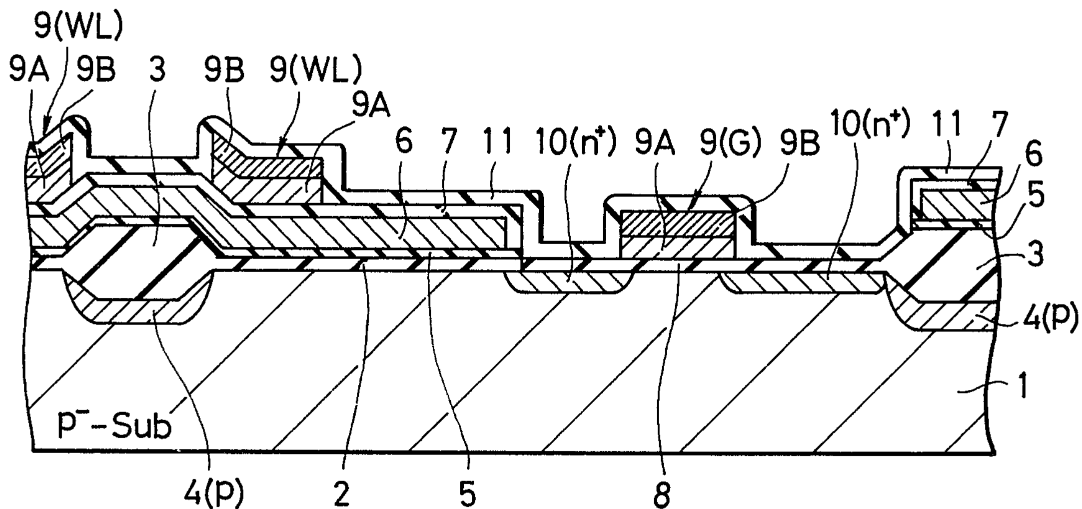

FIG. 7A

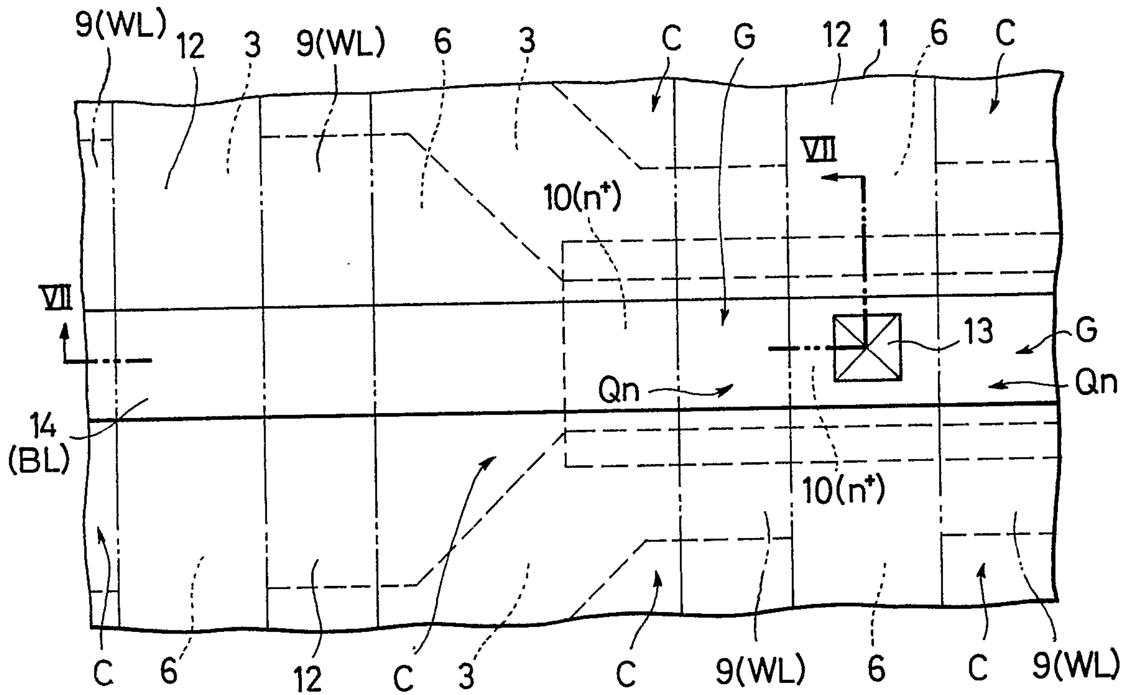

FIG. 7B

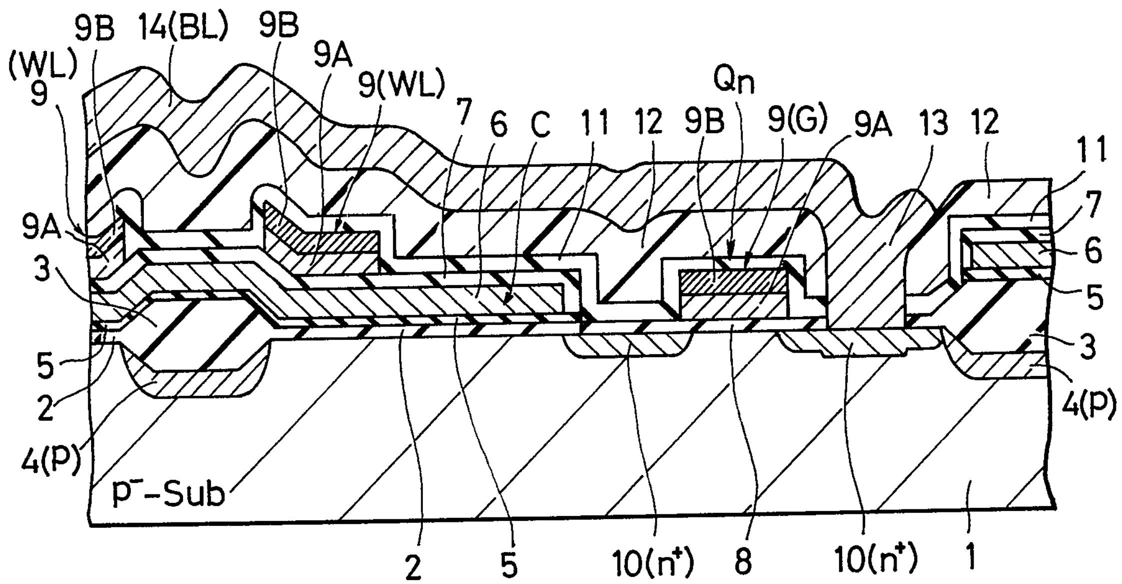

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FIG. 8

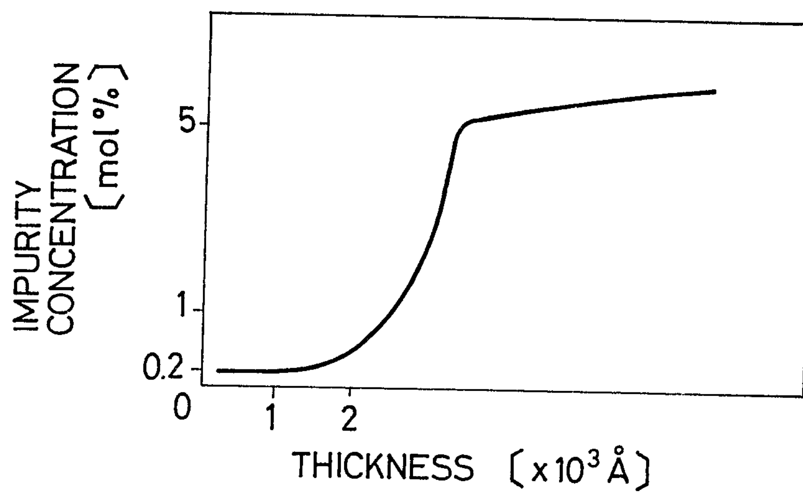


FIG. 10

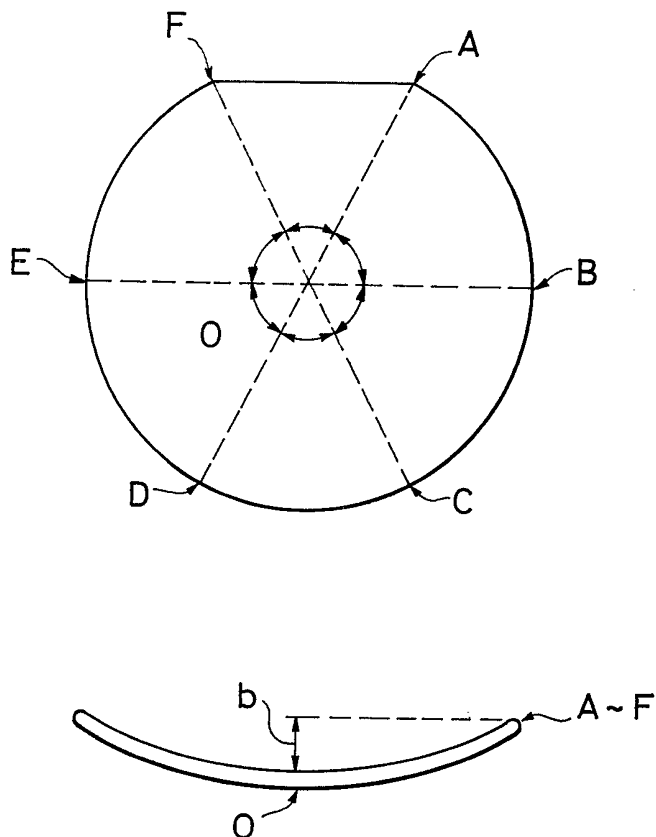
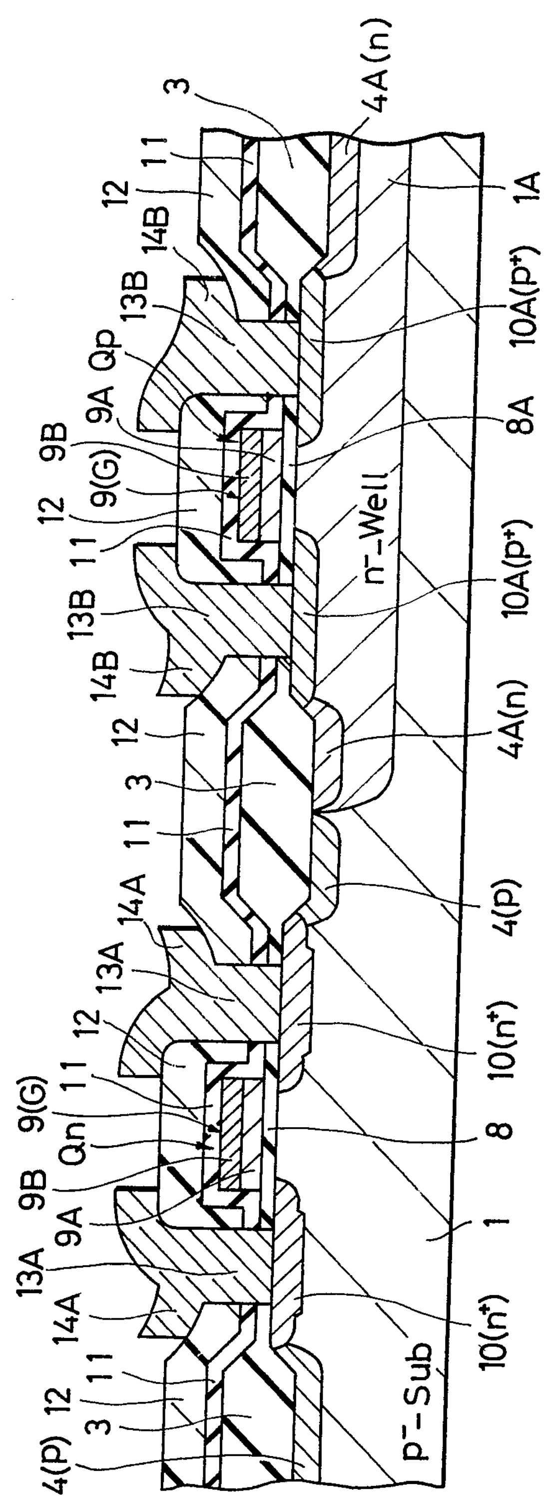


FIG. 9



SPECIFICATION

Process of fabricating a semiconductor integrated circuit device

5 The present invention relates to a process of fabricating a semiconductor integrated circuit device. 5
One well known semiconductor integrated circuit device is a Dynamic Random Access Memory (hereinafter referred to as a DRAM). In order to achieve high-speed operation in a DRAM, it is important that the resistance of a word line is reduced. It is, therefore, possible to use a conductive layer as the word line which is prepared by covering a polycrystalline silicon layer with a layer containing a refractory metal and
10 possibly silicon. The layer containing the refractory metal has a lower resistance than the polycrystalline 10 silicon layer and is remarkably stable under the atmospheres present during the various treatment steps of the fabricating process, as in the polycrystalline silicon layer. The use of such a polycrystalline silicon layer is of advantage in the semiconductor device and has such a high reliability that the refractory metal may be prevented from affecting the electrical characteristics of the semiconductor integrated circuit device.
15 In DRAM, a MISFET acting as a switching element of a memory cell frequently has its gate electrode 15 integrated with the word line in the same fabrication step. Japanese Patent Publication No. 57-194567 shows an arrangement in which the polycrystalline silicon layer is formed beneath the layer containing the refractory metal so that the threshold voltage of the MISFET does not fluctuate.
It has now been discovered that the following problems arise when a phosphosilicate glass film is used as
20 an inter-layer insulating film between a word line, which is composed of a polycrystalline silicon layer and a 20 layer containing a refractory metal of high melting point, e.g. a molybdenum silicide ($MoSi_2$) layer, and a bit line, which is formed above the word line and which is made of aluminium, and when the phosphor concentration is increased to about 10 mol% to promote "glass flow" (refer to U.S. patent No. 3,825,442) so as to promote flattening of the glass film.
25 It has been found that the molybdenum silicide layer will tend to peel from the polycrystalline silicon layer 25 at the peripheral (or end) portions of the boundary with the polycrystalline silicon layer. This phenomon occurs not only in the word line but also in the peripheral circuit portion of the DRAM which is formed with a conductive layer consisting of the polycrystalline silicon layer and the molybdenum silicide layer. It has also been found that the molybdenum silicide layer may peel partially from the polycrystalline silicon layer but
30 sometimes may be completely separated from it. 30
It is thought that the reason for this is that the phosphosilicate glass film has a larger coefficient of thermal expansion than those of the polycrystalline silicon layer and the molybdenum silicide layer. Moreover, the adhesiveness between the molybdenum silicide layer and the phosphosilicate glass film is stronger than that between the polycrystalline silicon layer and the molybdenum silicide layer. After the phosphosilicate
35 glass is subjected to glass flow at e.g. about 1,000°C for about 30 min., unnecessary stress, resulting in 35 peeling of the molybdenum silicide layer, is generated as a result of elongation or contraction in the peripheral portion of the conductive layer.
The present invention seeks to reduce or eliminate peeling of the layer containing a refractory metal of high melting point from the underlying polycrystalline silicon layer. It achieves this by providing an
40 insulating film on the layer containing the refractory metal which has a thickness such as to reduce forces 40 which cause peeling. Then when the phosphosilicate glass film is formed on the insulating film, and is heated so that if flows, it is found that peeling is reduced. In this way it becomes possible to manufacture a more reliable device.
Preferably the refractory metal is molybdenum.
45 The insulating film may be a silicon dioxide film, in which case its thickness is preferably equal to or 45 greater than 1000 Å, or may be a silicon nitride film in which case its thickness is preferably equal to or greater than 600 Å.
Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:
50 *Figure 1A* is a top plan view showing parts of a DRAM for explaining one embodiment of the present 50 invention;
Figure 1B is a sectional view along the line I – I of Figure 1A;
Figure 2A, Figure 3A, Figure 4A, Figure 5, Figure 6, and *Figure 7A* are top plan views and sectional views showing the parts of the DRAM at individual fabrication steps for explaining one embodiment of the present
55 invention; 55
Figure 2B is a sectional view along the line II – II of Figure 2A;
Figure 3B is a sectional view along the line III – III of Figure 3A;
Figure 4B is a sectional view along the line IV – IV of Figure 4A;
Figure 7B is a sectional view along the line VII – VII of Figure 7A;
60 *Figure 8* is a graph showing the distribution of phosphor impurity concentration in an insulating film made 60 of phosphosilicate glass for explaining one embodiment of the present invention;
Figure 9 is a sectional view showing part of the peripheral circuit of a DRAM for explaining a second embodiment of the present invention;
Figure 10 is a diagram showing a method for measuring the warpage of a semiconductor wafer.

In these figures, corresponding parts are indicated by the same reference numerals and will not be repeatedly described.

Referring first to Figures 1A and 1B, a memory cell of a DRAM has an insulating film 2, formed on a p^--type semiconductor substrate (p^--Sub) 1 made of a single crystal of silicon. This insulating film 2 extends over 5 that part of the substrate 1 on which is formed a capacitor of the memory cell. The main surface of the semiconductor substrate 1 other than the region to be formed with the capacitor and a MISFET which acts as a switching element is occupied by a field insulating film 3 and a p-type channel stopper 4 underlying the field insulating film 3. These isolate the semiconductor elements electrically. An insulating film 5 is formed above the insulating film 2 and the field insulating film 3 in the region to be formed with a capacitor electrode 10 (conducting plate), as will be described subsequently. The insulating film 5 forms part of the capacitor. The insulating film 2 and the field insulating film 3 may be silicon dioxide films, for example, and the insulating film 5 may be a film having a higher dielectric constant than the insulating film 2, e.g., a silicon nitride film.

A conducting plate 6 of polycrystalline silicon is formed on part of the insulating film 5 other than the region to be formed with a MISFET acting as a switching element. The capacitor C of the memory cell is 15 formed by the semiconductor substrate 1, the insulating films 2 and 5 and the conducting plate 6. This conducting plate 6 is electrically isolated from a word line of the memory device by an insulating film 7 which covers the conducting plate 6. An insulating film 8 is formed on the region of the main surface of the semiconductor substrate 1 which is to have the MISFET and forms part of the gate insulating film of the MISFET.

20 A conductive layer 9 extends in the column direction (i.e. vertically in Figure 1A) on the insulating films 7 and 8 and forms a gate electrode at the region which will have the MISFET and elsewhere forms a word line. The conductive layer 9 should have a low resistance so that the turn-on and turn-off operation times of the MISFET may be improved, to speed-up the DRAM. A polycrystalline silicon layer 9A is formed on the insulating films 8 and 7. A layer 9B covers the polycrystalline silicon layer 9A and may be made of a 25 composition of a refractory metal such as molybdenum and silicon, e.g. molybdenum silicide ($MoSi_2$). The polycrystalline silicon layer 9A traps impurities contained in trace amounts in the molybdenum silicide layer 9B, and which are not desirable if the MISFET is to have satisfactory electrical characteristics. The molybdenum silicide layer 9B has a lower resistance than the polycrystalline silicon layer 9A and both it and the polycrystalline silicon layer 9A are highly stable in the atmospheres present during the various treatment 30 steps in the fabrication process.

The layer 9B may alternatively be made of a compound of a refratory metal and silicon such as tantalum silicide ($TaSi_2$), tungsten silicide (WSi_2) or titanium silicide ($TiSi_2$), or may be a refractory metal layer having a lower resistance, such as molybdenum, tungsten, tantalum or titanium. What is important is that the layer 9B should be a layer containing a refractory metal. This refractory metal can cope with the heat treatment of the 35 DRAM fabrication process.

An n^+-type semiconductor region 10, is formed in the main surface of the semiconductor substrate 1 on both the sides of the conductive layer 9 which will contain the gate electrode (G), of the MISFET. This semiconductor region 10 forms the source region 2 and drain region of the MISFET acting as the switching element of the memory cell. The semiconductor region 10 is similarly doped with impurity at the part to 40 which the bit line is connected, the impurity being introduced into phosphosilicate glass so that its junction depth (x_j) from the surface of the semiconductor substrate 1 is slightly greater than that of the rest of the region 10. This prevents the pn-junction between the semiconductor region 10 and the semiconductor substrate 1 from breaking down when a voltage is applied to the semiconductor region 10.

The MISFET Q_n acting as the switching element of the memory cell is formed primarily by the gate 45 electrode (G) of the conductive layer 9, the insulating film 8, and the two semiconductor regions 10 formed on both sides of the gate electrode (G) in the main surface of the semiconductor substrate 1.

An insulating film 11 is formed on the entire exposed surface to cover the conductive layer 9. The insulating film 11 reduces unnecessary stress which is generated as a result of glass flow of the phosphosilicate glass, and which may cause peeling of the molybdenum silicide layer 9B. The film 11 50 therefore prevents the separation of the molybdenum silicide layer 9B from the polycrystalline silicon layer 9A. The insulating film 11 may be a silicon dioxide (SiO_2) film prepared by Chemical Vapour Deposition (CVD), for example, or a silicon nitride film formed by CVD, a silicon dioxide film or a silicon nitride film formed by plasma CVD, or a phosphosilicate glass film which has a low phosphor impurity concentration (e.g., 4 mol% or lower) so that it causes no glass flow.

55 An inter-layer insulating film 12 of a phosphosilicate glass (PSG) film is formed to cover the entire surface of the conductive layer 9. This electrically isolates the conductive layer 9 from a bit line (which will be described later). The insulating film 12 is subjected to glass flow by setting the phosphor concentration at about 10 mol% so as to flatten the undulations resulting from the multi-layered construction and so to improve the coverage of the upper conductive layer. Thus the PSG film is first deposited with a generally 60 uniform thickness all over the substrate. Then the PSG film is heated to about 1,000°C so that it flows. This causes the steps in the surface of the PSG film to be flattened and the corners of the film to have a gentle gradient. The insulating film 12 elongates and contracts when the glass is heated and cooled respectively. Unnecessary stress, tending to cause peeling of the molybdenum silicide layer 9B, is generated when the insulating film 12 contracts. According to the present embodiment, however, the stess can be reduced so 65 that peeling of the molybdenum silicide layer 9B may be prevented because the insulating film 11 covers the

conductive layer 9.

A contact hole 13 is formed by selectively removing the insulating films 8, 11 and 12 lying over the semiconductor region 10 where the bit line is to be connected. A bit line (BL) 14 is formed which is electrically connected to the semiconductor region 10 through the contact hole 13. The bit line 14 extends in the row direction (i.e. horizontally in Figure 1A) over the insulating film 12. The bit line 14 may be e.g. an aluminium film.

In order to prevent peeling it is desirable that the insulating film 11 is a film which is formed not by thermal oxidization but by deposition.

Moreover, the insulating film 11 should desirably have a thickness equal to or greater than a predetermined value. To show this, experimental results will now be described.

TABLE 1

Films	*Thickness*			
	0 Å	*1,000 Å*	*1,500 Å*	*3,500 Å*
CVD High Temp. Low Press.	x	○	○	○
CVD Normal	x	Δ	○	○

Table 1 tabulates the presence or absence of peel of the polycrystalline silicon layer 9A and the molybdenum silicide layer 9B when the thickness (Å) of the insulating film 11 is varied. It should be noted that the thicknesses appearing in the Table are those in the state of Figure 6, i.e., immediately after the insulating film is formed. The reason for this will be discussed later. The insulating films 11 used were respectively an SiO_2 film which was formed by CVD at a high temperature (e.g., 700 to 800°C) and at a low pressure (e.g., 0.1 to 10 Torr), and an SiO_2 film which was formed by normal CVD (at a temperature around 400°C and under a pressure of 760 Torr).

In the Table, symbols x indicate that the molybdenum silicide layer often peeled from the polycrystalline layer and symbol ○ indicates no peeling. In fact, the chip in which peeling occurred for one wafer was zero or one and the peeling was limited to the periphery of the wafer. Symbol Δ indicates that peeling occurred in some, but not all, the cases. The number of chips in which peel had taken place was about 2/17 of the total.

As is apparent from the above description, peel occurs to a considerable extent when the insulating film 11 has a thickness of 0 Å, i.e., when the film 11 is not present. The peeling phenomenon may be substantially completely prevented when the insulating film 11 has a thickness equal to or larger than 1,500 Å.

TABLE 2

Steps	*Thickness*	
	0 Å	*3,500 Å*
Formation of PSG Film	42 to 49 μm	50 to 52 μm
Glass Flow	16 μm	28 to 30 μm

The strength of the stress causing peeling is tabulated in Table 2. This Table 2 indicates the stress which is generated in the wafer after the tabulated fabrication step, in terms of wafer warpage b (μm). The insulating film 11 was a SiO_2 film formed by CVD at a high temperature and a low pressure.

In the absence of the insulating film 11, the reduction (or change) in the wafer warpage as a result of the glass flow is high (from 42 to 49 μm to 16 μm). In the presence of the insulating film 11 having a thickness of 3,500 Å, the reduction (or change) in the wafer warpage as a result of the glass flow is low (from 50 to 52 μm to 28 to 30 μm).

It has now been found that peel is dependent not upon the wafer warpage itself but upon the change in the wafer warpage during each step of the manufacturing process. Peeling is not caused by a small change but by a large change. The insulating film 11 softens the change in the warpage due to glass flow. In other words, the insulating film 11 reduces the change in stress. Thanks to the presence of the insulating film 11, moreover, the force when the stress changes due to glass flow is not applied to the interface between the polycrystalline silicon layer 9A and the silicide 9B.

Incidentally, the wafer warpage used is an average of the warpages at points A to F by the method shown in Figure 10. It has also been confirmed that the wafer warpage changes at each step after the formation of the gate electrode 9 and before the formation of the insulating film 11. It is also possible that the changes of

the wafer warpage during the individual steps are related to peeling. However, it has also been found that peeling actually occurs only during glass flow and may be prevented or at least ameliorated by the present invention.

According to the Table 1, the number of times peel occurs differs in dependence upon the method of forming the film when the insulating film 11 has a thickness of 1,000 Å. In this respect, the following facts have been revealed.

When a SiO_2 film is used as the insulating film 11, phosphor diffuses into the film from the PSG film 12. The diffusion rate of the phosphor is different for a SiO_2 film formed by a CVD method at a high temperature and a low pressure and for a SiO_2 film formed by a normal CVD method; the diffusion rate being lower for the former method. This is because the films have different densities. A SiO_2 film into which phosphor diffuses has the same property as that of a PSG film. Since the insulating film 11 has a thickness which may be as small as 1,000 Å, a pure SiO_2 film containing no phosphor is not substantially present, and the phosphor concentration thereabove (i.e., at the side of the PSG film 12) is considerably higher near the PSG film 12. Moreover, it has been found that the upper portion of the insulating film having a predetermined or higher phosphor concentration diffused reflows simultaneously with the glass flow. The concentration of the phosphor diffused is dependent upon the phosphor concentration of the PSG film 12 and upon the temperature and duration of the glass flow. A fluidity is obtained when the phosphor concentration reaches 4 mol% or higher.

Furthermore, it has now been found that no peel takes place if the part of the insulating film 11 which does not reflow simultaneously with the glass flow has at least a predetermined thickness. This thickness may be about 600 Å. In order to ensure that there is a thickness of about 600 Å at the part of the film 11 which does not reflow, it is necessary that a SiO_2 film produced by CVD at a high temperature and a low pressure is 1,000 Å thick and that a SiO_2 film produced by the normal CVD method is rather thicker.

As a result, when the insulating film 11 is made of e.g. silicon nitride film which is hard to dope with phosphor for effecting glass flow of the phosphosilicate glass film, unnecessary stress causing peeling of the silicide layer 9B can be reduced sufficiently if the insulating film 11 has a thickness of about 600 Å or more while it is being formed. When the insulating film 11 is made of e.g. a silicon dioxide film which is easy to dope with impurity for effecting glass flow, the part for reducing the unnecessary stress has to have a thickness of about 600 Å while considering the part which is to be highly doped with the phosphor until it reflows.

For this purpose, the thickness of the insulating film 11 has to be controlled during the step of the fabrication process in which it is formed. When the insulating film 11 is a silicon nitride film, its thickness may be about 600 Å. This value varies in dependence upon the method of forming the film, as can be deduced from the Table 1. The foregoing description describes the use of a silicon dioxide film. When a PSG film has a phosphor concentration of about 1 mol%, the film thickness has to be made larger than for a silicon dioxide film. Thus, peel may be prevented. In other words, the change in the stress having been described with reference to the Table 2 may be reduced.

The total thickness of the insulating films 11 and 12, i.e., the thickness of the inter-layer insulating film, has a preferred value. In order that unnecessary impurity may be introduced into the insulating film 8 of the MISFET to affect its electrical characteristics, it is desirable that the thickness is larger in order to ensure that the phosphate film provides sufficient electric isolation between the conductive layers. However, considering the formation of the contact hole for connecting the bit line, the total thickness is desirably small. When the insulating film 11 is an SiO_2 film, the difference in the etching rate from that of a PSG film has to be taken into consideration. In order to flatten a PSG film by glass flow, moreover, a PSG film should have at least a predetermined thickness. From the points described above, the thickness of the insulating film 11 is preferably 4,000 Å or less. This value is preferred particularly when a SiO_2 film is used.

By taking the dispersion of the fabricating conditions, incidentally, the thickness of the insulating film 11 while being formed may be determined. For the SiO_2 film, it is most desirable that the film thickness during formation be 1,500 to 3,500 Å.

A specific fabrication process will now be explained.

Figure 2A, Figure 3A, Figure 4A, Figure 5, Figure 6 and Figure 7 are top plan views and sections of parts of a DRAM showing one memory cell during the individual fabrication steps, for explaining the embodiment of the present invention. Figure 2B is a section taken along line II – II of Figure 2A. Figure 3B is a section taken along line III – III of Figure 3A. Figure 4B is a section taken along line IV – IV of Figure 4A. Figure 7B is a section taken along line VII – VII of Figure 7a.

First of all, a p^--type semiconductor susbtrate 1 of a single crystal of silicon is prepared. As shown in Figures 2A and 2B, moreover, a field insulating film 3 is formed on the main surface of the semiconductor substrate 1 between the regions to have the semiconductor element, and a p-type channel stopper region 4 is formed simultaneously therewith on the main surface of the semiconductor substrate 1 below the field insulating film 3. An insulating film 2 is formed on the surface of the substrate 1 other than the region formed with the field insulating film 3, the insulating film 2 being prepared by thermal oxidization of the surface, for example, to produce an SiO_2 film having a thickness of 300 to 500 Å. The field insulating film 3 may be a silicon dioxide film formed by selective thermal oxidization of the substrate 1, for example, so that it has a thickness of about 1 μm.

After the step shown in Figures 2A and 2B, the insulating film 2 and the field insulating film 3 are covered over their entire surface with an insulating film 5. This insulating film 5 may be a silicon nitride film made by CVD, for example, having a thickness of 100 to 200 Å. A silicon dioxide film (not shown) is formed on the insulating film 5 made of silicon nitride, the silicon dioxide film having a thickness of about 30 to 50 Å, for example, so as to reduce the stress which is caused by the difference in the coefficients of thermal expansion between the insulating film 5 and a conducting plate to be formed at a later step. After this, a conducting plate 6 is selectively formed on the insulating film 5 other than the region which is to have a MISFET acting as the switching element of the memory cell. The conducting plate 6 may be made of a polycrystalline silicon film which is prepared by CVD, for example, having a thickness of about 3,000 to 5,000 Å and having its resistance lowered by introducing phosphor. Moreover, the exposed insulating film 5 is used as a mask to oxidize thermally the polycrystalline silicon layer or the conducting plate 6 thereby selectively to form an insulating film (i.e., SiO_2) film 7 covering the conducting plate 6, as shown in Figures 3A and 3B. The insulating film to be formed between the individual conductive layers, i.e., the insulating film 7, is omitted from Figure 3A and Figure 4A so as to clarify the pattern of the conducting plate 6 and to facilitate its illustration.

After the step shown in Figures 3A and 3B, the insulating films 5 and 2 in the regions to have the MISFET are selectively removed to expose the semiconductor substrate 1. Then, an insulating film 8 is formed on the exposed main surface of the semiconductor substrate 1. The insulating film 8 may be a silicon dioxide film produced by thermal oxidation of the substrate surface and may have a thickness of 500 to 600 Å so that the gate insulating film of the MISFET may be constructed. In order to form a word line and the gate electrode of the MISFET, moreover, the insulating film 7 and the insulating film 8 are covered over their entire surface with a polycrystalline silicon layer 9A, which is covered over its entire surface with a molybdenum silicide layer 9B. The polycrystalline silicon layer 9A may be prepared by CVD, for example, having its resistance reduced by introducing phosphor and having a thickness of about 2,000 to 3,000 Å. The molybdenum silicide layer 9B may be a molybdenum silicide film produced by sputtering, with a thickness of about 2,500 to 3,500 Å. Subsequently the molybdenum silicide layer 9B and the polycrystalline silicon layer 9A are selectively patterned to form the conductive layer 9 for providing a word line (WL) and a gate electrode (G) of the MISFET, as shown in Figures 4A and 4B, and are then subjected to a heat treatment at about 1,000°C in an atmosphere of an inert gas such as argon. This heat treatment may alternatively be conducted before the patterning step for forming the conductive layer 9.

After the step shown in Figures 4A and 4B, as shown in Figure 5, an n^+-type semiconductor region 10 is formed in the main surface of the semiconductor substrate 1 through the insulating film 8 on both the sides of the conductive layer 9 (G) in the region to have the MISFET, as shown in Figure 5. The semiconductor region 10 is formed using a mask for doping the conductive layer 9 (G) and the insulating film 7 with an impurity and may be formed in self-alignment by ion implantation, for example. In this case, energy of about 70 to 90 KeV is used to introduce an impurity of arsenic (As) ions in a concentration of about 1.0×10^{15} to 1.0×10^{17} atms/cm^2.

After the step shown in Figure 5, an insulating film 11 covering the conductive layer 9 is formed, as shown in Figure 6, so as to reduce unnecessary stress which causes peeling of the molybdenum silicide layer 9B by glass flow of the phosphosilicate glass film formed in a subsequent step. That insulating film 11 may be made of a silicon dioxide film which is prepared by CVD at a high temperature of about 700 to 800°C and at a pressure lower by 0.1 to 10 Torr than atmospheric pressure.

As discussed above, however, it is preferable that the insulating film 11 has a thickness equal to or larger than 1,000 Å. In the present embodiment, the thickness of the insulating film 11 is suitably about 1,000 to 4,000 Å and may preferably be 1,500 to 3,500 Å.

After the step shown in Figure 6, an insulating film 12 of phosphosilicate glass is formed. This insulating film 12 may have a phosphor impurity concentration of about 10 mol%, for example, and a thickness of about 6,000 to 9,000 Å so as to ensure glass flow. Moreover, the insulating films 8, 11 and 12 above the predetermined semiconductor region 10, which are to be connected to the bit line to be formed during a subsequent step, are selectively removed to form a contact hole 13. After that, in order to improve the coverage of the conductive layer formed on the insulating film 12, a glass flow of 30 min. at a temperature of about 1,000°C is effected to flatten the undulations of the upper surface of the insulating film 12. As shown in Figures 7A and 7B, a bit line 14 is selectively formed such that it is electrically connected to the semiconductor region 10 through the contact hole 13 and that it extends in the row direction on the insulating film 12. The bit line 14 may be made of e.g. an aluminium film and have a thickness of about 0.8 to 1.0 μm. It should be noted that the semiconductor region 10 diffuses during introduction of the impurity and during the various subsequent heat treatment steps so that it has a predetermined depth (x_j). Moreover, the semiconductor region 10 connected to the bit line 14 is doped during glass flow with a phosphor impurity via the contact hole 13 so that one part of it is deeper than other parts.

During the subsequent heat treatment steps, the impurity for glass flow of the insulating film 12 is introduced into the upper part of the insulating film 11. Since it is believed that glass flow is liable to take place at the doped part, the result is that there is a part which prevents peeling of the molybdenum silicide layer 9B. Upon completion of the DRAM, the insulating film 11 for reducing the unnecessary stress which causes peeling of the molybdenum silicide layer 9B as a result of glass flow of the insulating film 12 may have a thickness of about 600 Å or larger. After this, a protecting film is formed all over the entire surface.

In the present embodiment, unnecessary stress of the insulating film 12, which causes peeling of the molybdenum silicide layer 9B by glass flow, is reduced by the insulating film 11. Despite this, an insulating film 12A made of phosphosilicate glass may be given both the function of glass flow and also to reduce the unnecessary stress.

5 Figure 8 is a graph showing the distribution of the phosphor impurity concentration of the insulating film 12A made of phosphosilicate glass for explaining the embodiment of the present invention. 5

In Figure 8, the abscissa indicates the thickness ($\times 10^3$ Å) of the insulating film (PSG) 12 from the boundary between the conductive layer 9 and the insulating film 12A, whereas the ordinate indicates the concentration mol% of the phosphor impurity. In this case, the thickness of the insulating film 12A may be, for example, 10 about 8,000 to 12,000 Å. 10

As is apparent from the same Figure, the part of the insulating film 12A covering and adjoining the conductive layer 9, i.e., the part having a thickness equal to or smaller than 1,000 to 2,000 Å has a remarkably low phosphor impurity concentration. The phosphor impurity concentration necessary for the insulating film 12A to effect glass flow is equal to or higher than 4 mol%. Therefore, the phosphor impurity concentration of 15 the insulating film 12A covering and adjoining the conductive layer 9 may be lower than those of the other 15 portions, e.g. lower than about 4 mol%. As a result, unnecessary stressing of the insulating film 12A, which is caused by glass flow and results in peeling of the molybdenum silicide layer 9B, may be reduced by the insulating film 12A in the vicinity of the conductive layer 9.

According to the method of formation described above, the insulating film 12A is formed from a 20 phosphosilicate glass film produced by CVD to cover the conductive layer 9 and by introducing a phosphor 20 impurity into the phosphosilicate glass film from the surface to a predetermined depth so as to effect glass flow. This does not lead to a significant increase in the number of the steps of the fabricating process because it can be conducted in one furnace.

The above description is directed mainly to a memory cell which forms an element of a memory cell array 25 of a DRAM. A Complementary MISFET (hereinafter referred to as a CMIS) forming a peripheral circuit of the 25 DRAM will now be described.

Figure 9 is a sectional view showing the parts of the peripheral circuit of the DRAM for explaining a construction of another embodiment of the present invention.

In Figure 9, an n^--type well region (N^--well) 1A is formed in a predetermined main surface of a 30 semiconductor substrate 1 to form a p-channel MISFET. An n-type channel stopper region 4A is formed 30 under a field insulating film 3 in the well region 1A. An insulating film 8A is formed on the main surface of the well region 1A in the region to be formed with a semiconductor element, such as the p-channel MISFET, and is used to form the gate insulating film of the p-channel MISFET. A p^+-type semiconductor region 10A is formed in the main surface of the well region 1A through the insulating film 8A on both sides of the 35 conductive layer 9 in the region to be formed with the p-channel MISFET and which is used in the formation 35 of the p-channel MISFET. This p-channel MISFET Q_p has a gate electrode (G) formed by the conductive layer 9, the insulating film 8A, and a pair of the semiconductor regions 10A are formed on both sides of the gate electrode (G) in the main surface of the well region 1A. The insulating film 11 is formed, as in the first embodiment, to cover the conductive layer 9 and to reduce unnecessary stress of the insulating film 12 of 40 phosphosilicate glass which would cause peeling of the molybdenum silicide layer 9B by glass flow. 40 Moreover, the insulating film 11 covers the semiconductor regions 10 and 10A simultaneously with the conductive layer 9. The insulating film acts to prevent the phosphor impurity, which is introduced into the insulating film 12 to effect glass flow, from being introduced unnecessarily into the semiconductor regions 10 and 10A through the insulating films 8 and 8A. There is a risk of this because the insulating films 8 and 8A 45 of the MISFETS Q_n Q_p are very thin, for example, about 500 to 600 Å. In other words, the insulating film 11 45 prevents the silicide layer 9B from peeling and prevents unnecessary phosphor impurity from being introduced at that time thereby to leave the electrical characteristics of the MISFETs Q_n and Q_p unaffected. The insulating film 11 is remarkably effective, particularly in a CMIS, because the part of the MISFET Q_p in the vicinity of the surface of the semiconductor region 10A has a low impurity concentration and so has an 50 increased resistance. This causes a reduction in the operating time. A contact hole 13A is formed by 50 selectively removing the insulating films 8, 11 and 12 from above the predetermined semiconductor region 10 of the MISFET Q_n. The contact hole 13A is used to connect electrically the semiconductor region 10 and a wire (which will be described later). A contact hole 13B is formed by selectively removing the insulating films 8A, 11 and 12 from above the predetermined semiconductor region 10A of the MISFET Q_p. The contact hole 55 13B is used to connect electrically the semiconductor region 10A and a wire (which will be mentioned later). 55 Wire 14A is formed on the insulating film 12 so that it is electrically connected to the semiconductor region 10 through the contact hole 13A, whilst wire 14B is on the insulating film 12 so that it is electrically connected to the semiconductor region 10A through the contact hole 13B.

The second insulating film is formed between the conductive layer and the first insulating film which cover 60 at least the conductive layer. Unnecessary stress (or change in the stress) of the first insulating film due to 60 glass flow, which flow causes peeling of the silicide layer, is reduced by the second insulating film. The phosphor impurity concentration of the second insulating film is preferably such that no glass flow occurs in the vicinity of the insulating film, and hence any unnecessary stress generated does not affect the conductive layer. As a result, it is possible to provide a highly reliable semiconductor integrated circuit device in which 65 there is little or no peeling of the molybdenum silicide layer. 65

The conductive layer of e.g. the word line may be a polycrystalline silicon layer and either a refractory metal layer having a lower resistance or a silicide layer. As a result, the wiring resistance of the conductive layer, which cannot be made of aluminium or an aluminium alloy, may be reduced so that the resultant semiconductor integrated circuit device may have an improved operating time.

The second insulating film is formed between the gate electrode (i.e., the conductive layer) and the semiconductor region e.g., the source or drain region and the first insulating film. Unnecessary stress which causes peel of the molybdenum silicide layer of the first insulating film by glass flow is reduced by the second insulating film so that the glass flow does not affect the gate electrode and so that the phosphor impurity introduced into the first insulating film is not unnecessarily introduced into the semiconductor region. As a result, it is possible to provide a highly reliable semiconductor integrated circuit device in which peel of the silicide layer may be prevented or at least ameliorated and in which the electrical characteristics of the MISFETs may be stabilised.

The present invention is not limited to the embodiments described above but may be modified in various ways. For example, the embodiments described above show the appliation of the present invention to a DRAM, for example. However, the present invention may also be applied to a semiconductor integrated circuit device such as a SRAM or a mask ROM, which is constructed of a conductive layer having a polycrystalline silicon layer and either a refractory metal layer or a silicide layer of the refractory metal, and an insulating film overlying the conductive layer, which film is made of phosphosilicate glass for flattening the undulations.

The description thus far made is directed mainly to the case in which our invention is applied to the semiconductor integrated circuit device belonging to the field of application backing the invention, but the present invention should not be limited thereto.

CLAIMS

1. A process of fabricating a semiconductor integrated circuit device, comprising:
(a) forming a conductive layer over a semiconductor substrate, the conductive layer having a polycrystalline silicon layer and a layer on the polycrystalline silicon layer which contains a refractory metal of high melting point;
(b) forming a first insulating film covering the conductive layer and having a thickness such as to reduce forces tending to peel the layer containing refractory metal from the polycrystalline layer; and
(c) forming a second insulating film of phosphosilicate glass on the first insulating film, the phosphosilicate glass film being heated after it has been deposited so that it flows.

2. A process according to claim 1, wherein the first insulating film has a thickness equal to or greater than 600 Å.

3. A process according to claim 1 or claim 2, wherein the first insulating film has a thickness between 600 Å and 4,000 Å.

4. A process according to claim 3, wherein the first insulating film has a thickness between 1,500 Å and 3,500 Å.

5. A process according to any one of claims 1 to 4, wherein the refractory metal is molybdenum.

6. A process according to any one of the preceding claims, wherein the first insulating film is a silicon dioxide film having a thickness equal to or greater than 1,000 Å.

7. A process according to any one of claims 1 to 5, wherein the first insulating film is a silicon nitride film having a thickness equal to or greater than 600 Å.

8. A process according to any one of claims 1 to 5, wherein the first insulating film is a phosphosilicate glass film having a thickness between 1,000 Å and 2,000 Å and having a phosphor concentration equal to or less than 4 mol%.

9. A process according to any one of the preceding claims, wherein the layer containing refractory metal is a silicide layer of a compound of the refractory metal with silicon, and wherein the first insulating film is formed by deposition.

10. A process according to claim 9, wherein the deposition of the first insulating film is by chemical vapour deposition at a high temperature and under a low pressure.

11. A process of fabricating a semiconductor integrated circuit device, comprising:
(a) forming a conductive layer over a semiconductor substrate, the conductive layer having a polycrystalline silicon layer and a layer on the polycrystalline silicon layer which contains a refractory metal of high melting point; and
(b) forming an insulating film made of phosphosilicate glass on the conductive layer, the phosphosilicate glass being heated after it has been deposited so that it flows, the insulating film having a first film with a high phosphor concentration so that it flows during the heating of the phosphosilicate glass film, and a second film with a low phosphor concentration so that it does not flow, the first film lying on the second film.

12. A process according to claim 13, wherein the second film has a phosphor concentration equal to or less than 4 mol% and a thickness between 1,000 Å and 2,000 Å.

13. A process of fabricating a semiconductor integrated circuit device having a MISFET, comprising:
(a) forming a gate electrode over a semiconductor substrate of a first conductivity type, the gate electrode having a polycrystalline silicon layer and a layer on the polycrystalline silicon layer which contains a

refractory metal of high melting point;

(b) forming semiconductor regions of a second conductivity type for providing source and/or drain regions in the semiconductor substrate on both sides of the gate electrode;

(c) forming a first insulating film covering the gate electrode and the semiconductor regions, the first insulating film having a thickness such as to reduce forces tending to peel the layer containing the refractory metal from the polycrystalline layer; and

(d) forming a second insulating film made of phosphosilicate glass on the first insulating film, the phosphosilicate glass being heated after it has been deposited, so that it flows, the first insulating film having a thickness such as substantially to prevent the phosphor in the phosphosilicate glass from being diffused into the semiconductor regions during the heating of the phosphosilicate glass.

14. A process of fabricating a semiconductor integrated circuit device substantially as any one herein described with reference to the accompanying drawings.

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