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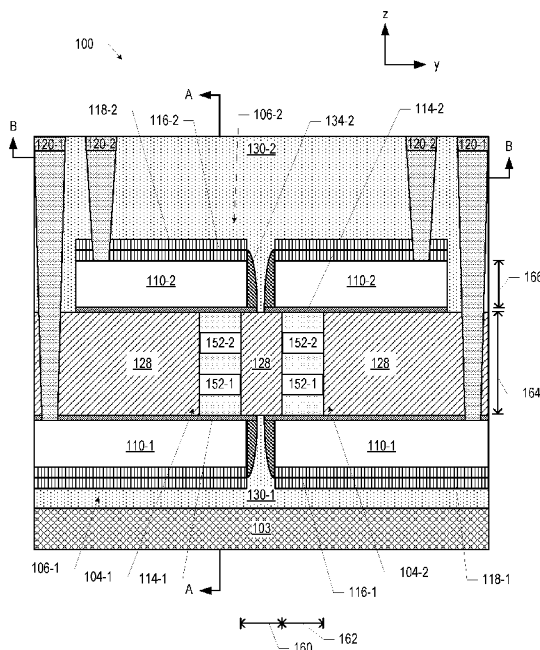

FIG. 1

(57) Abstract: Disclosed herein are quantum dot devices, as well as related computing devices and methods. For example, in some embodiments, a quantum dot device may include: a quantum well stack structure including a base, a first strained layer, and a second strained layer, wherein the first strained layer is disposed between the base and the second strained layer, and the first and second strained layers are oppositely strained; and a plurality of gates disposed on the quantum well stack structure.

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QUANTUM WELL STACK STRUCTURES FOR QUANTUM DOT DEVICES

Background

[0001] Quantum computing refers to the field of research related to computation systems that use quantum mechanical phenomena to manipulate data. These quantum mechanical phenomena, such as superposition (in which a quantum variable can simultaneously exist in multiple different states) and entanglement (in which multiple quantum variables have related states irrespective of the distance between them in space or time), do not have analogs in the world of classical computing, and thus cannot be implemented with classical computing devices.

Brief Description of the Drawings

[0002] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0003] FIGS. 1-3 are cross-sectional views of a quantum dot device, in accordance with various embodiments.

[0004] FIGS. 4-31 illustrate various example stages in the manufacture of a quantum dot device, in accordance with various embodiments.

[0005] FIGS. 32-34 are cross-sectional views of another example quantum dot device, in accordance with various embodiments.

[0006] FIG. 35 is a cross-sectional view of an example quantum well stack structure that may be used in a quantum dot device, in accordance with various embodiments.

[0007] FIGS. 36-39 illustrate various example stages in the manufacture of a quantum well stack structure for a quantum dot device, in accordance with various embodiments.

[0008] FIG. 40 is a perspective view of a substrate that may be formed in accordance with the operations discussed with reference to FIGS. 36 and 37, in accordance with various embodiments.

[0009] FIG. 41 is a cross-sectional view of a quantum dot device that may include the substrate of FIG. 40 or the substrate of FIG. 45, in accordance with various embodiments.

[0010] FIGS. 42-44 illustrate various example stages in the manufacture of an alternative quantum well stack structure for a quantum dot device, in accordance with various embodiments.

[0011] FIG. 45 is a perspective view of a substrate that may be formed in accordance with the operations discussed with reference to FIG. 42, in accordance with various embodiments.

[0012] FIGS. 46-48 illustrate various alternative example stages in the manufacture of the quantum well stack structure illustrated in FIG. 39, in accordance with various embodiments.

[0013] FIGS. 49-50 illustrate various example stages in the manufacture of another alternative quantum well stack structure, in accordance with various embodiments.

[0014] FIG. 51 is a perspective view of a substrate that may be formed in accordance with the operations discussed with reference to FIGS. 49-50, in accordance with various embodiments.

[0015] FIG. 52 is a cross-sectional view of a quantum dot device that may include the substrate of FIG. 51, in accordance with various embodiments.

[0016] FIG. 53 illustrates an embodiment of a quantum dot device having multiple groups of gates on a single fin, in accordance with various embodiments.

[0017] FIGS. 54-58 illustrate various alternative stages in the manufacture of a quantum dot device, in accordance with various embodiments.

[0018] FIGS. 59-60 illustrate detail views of various embodiments of a doped region in a quantum dot device.

[0019] FIG. 61 is a flow diagram of an illustrative method of manufacturing a quantum dot device, in accordance with various embodiments.

[0020] FIGS. 62-63 are flow diagrams of illustrative methods of operating a quantum dot device, in accordance with various embodiments.

[0021] FIG. 64 is a block diagram of an example quantum computing device that may include any of the quantum dot devices disclosed herein, in accordance with various embodiments.

Detailed Description

[0022] Disclosed herein are quantum dot devices, as well as related computing devices and methods. For example, in some embodiments, a quantum dot device may include: a quantum well stack structure including a base, a first strained layer, and a second strained layer, wherein the first strained layer is disposed between the base and the second strained layer, and the first and second strained layers are oppositely strained; and a plurality of gates disposed on the quantum well stack structure.

[0023] The quantum dot devices disclosed herein may enable the formation of quantum dots to serve as quantum bits ("qubits") in a quantum computing device, as well as the control of these quantum dots to perform quantum logic operations. Unlike previous approaches to quantum dot formation and manipulation, various embodiments of the quantum dot devices disclosed herein provide strong spatial localization of the quantum dots (and therefore good control over quantum dot interactions and manipulation), good scalability in the number of quantum dots included in the device, and/or design flexibility in making electrical connections to the quantum dot devices to integrate the quantum dot devices in larger computing devices.

[0024] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0025] Various operations may be described as multiple discrete actions or operations in turn in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0026] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges. As used herein, the notation "A/B/C" means (A), (B), and/or (C).

[0027] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. The accompanying drawings are not necessarily drawn to scale. As used herein, a "high-k dielectric" refers to a material having a higher dielectric constant than silicon oxide. As used herein, two strained materials are "oppositely strained" when one of the strained materials is compressively strained and the other is tensilely strained. Oppositely strained materials may or may not be under strain of the same magnitude.

[0028] FIGS. 1-3 are cross-sectional views of a quantum dot device 100, in accordance with various embodiments. In particular, FIG. 2 illustrates the quantum dot device 100 taken along the section A-A of FIG. 1 (while FIG. 1 illustrates the quantum dot device 100 taken along the section C-C of FIG. 2), and FIG. 3 illustrates the quantum dot device 100 taken along the section B-B of FIG. 1 with a number of components not shown to more readily illustrate how the gates 106/108 may be patterned (while FIG. 1 illustrates a quantum dot device 100 taken along the section D-D of FIG. 3). Although FIG. 1 indicates that the cross section illustrated in FIG. 2 is taken through the fin 104-1, an

analogous cross section taken through the fin 104-2 may be identical, and thus the discussion of FIG. 2 refers generally to the "fin 104."

[0029] The quantum dot device 100 may include multiple fins 104 spaced apart by insulating material 128. The fins 104 may include a quantum well stack structure 146, which may include a quantum well layer 152-1 and a quantum well layer 152-2. Examples of quantum well stack structures 146 are discussed in detail below with reference to FIGS. 5 and 35-52. In particular, the quantum well layers 152-1 and 152-2 may be strained layers that are part of a strain compensation region, as discussed below. The quantum dot device 100 may, in some embodiments, include a support 103 to provide mechanical support for the quantum dot device 100 (e.g., in the form of a carrier or other support). In some embodiments, the quantum dot device 100 may not include a support 103.

[0030] Although only two fins, 104-1 and 104-2, are shown in FIGS. 1-3, this is simply for ease of illustration, and more than two fins 104 may be included in the quantum dot device 100. In some embodiments, the total number of fins 104 included in the quantum dot device 100 is an even number, with the fins 104 organized into pairs including one active fin 104 and one read fin 104, as discussed in detail below. When the quantum dot device 100 includes more than two fins 104, the fins 104 may be arranged in pairs in a line (e.g., 2N fins total may be arranged in a 1x2N line, or a 2xN line) or in pairs in a larger array (e.g., 2N fins total may be arranged as a 4xN/2 array, a 6xN/3 array, etc.). The discussion herein will largely focus on a single pair of fins 104 for ease of illustration, but all the teachings of the present disclosure apply to quantum dot devices 100 with more fins 104.

[0031] As noted above, each of the fins 104 may include two quantum well layers 152. The quantum well layers 152 included in the fins 104 may be arranged normal to the z-direction, and may provide layers in which a two-dimensional electron gas (2DEG) may form to enable the generation of a quantum dot during operation of the quantum dot device 100, as discussed in further detail below. The quantum well layers 152 themselves may provide a geometric constraint on the z-location of quantum dots in the fins 104, and the limited extent of the fins 104 (and therefore the quantum well layers 152) in the y-direction may provide a geometric constraint on the y-location of quantum dots in the fins 104. To control the x-location of quantum dots in the fins 104, voltages may be applied to gates disposed on the fins 104 to adjust the energy profile along the fins 104 in the x-direction and thereby constrain the x-location of quantum dots within quantum wells (discussed in detail below with reference to the gates 106/108). The dimensions of the fins 104 may take any suitable values. For example, in some embodiments, the fins 104 may each have a width 162 between 10 and 30 nanometers. In some embodiments, the fins 104 may each have a height

164 between 200 and 400 nanometers (e.g., between 250 and 350 nanometers, or equal to 300 nanometers).

[0032] The fins 104 may be arranged in parallel, as illustrated in FIGS. 1 and 3, and may be spaced apart by an insulating material 128, which may be disposed on opposite faces of the fins 104. The insulating material 128 may be a dielectric material, such as silicon oxide. For example, in some embodiments, the fins 104 may be spaced apart by a distance 160 between 100 and 250 microns.

[0033] Multiple gates may be disposed on each of the fins 104. In particular, a first set of gates 105-1 may be disposed proximate to the "bottom" of each fin 104, and a second set of gates 105-2 may be disposed proximate to the "top" of each fin 104. In the embodiment illustrated in FIG. 2, the first set of gates 105-1 includes three gates 106-1 and two gates 108-1, and the second set of gates 105-2 includes three gates 106-2 and two gates 108-2. This particular number of gates is simply illustrative, and any suitable number of gates may be used. Additionally, as discussed below with reference to FIG. 34, multiple sets of the gates 105-1 and 105-2 may be disposed on the fin 104.

[0034] As shown in FIG. 2, the gate 108-11 may be disposed between the gates 106-11 and 106-12, and the gate 108-12 may be disposed between the gates 106-12 and 106-13. The gates 106-21, 108-21, 106-22, 108-22, and 106-23 (of the set of gates 105-2) are distributed along the fin 104 analogously to the distribution of the gates 106-11, 108-11, 106-12, 108-12, and 106-13 (of the set of gates 105-1). References to a "gate 106" herein may refer to any of the gates 106, while reference to a "gate 108" herein may refer to any of the gates 108. Reference to the "gates 106-1" herein may refer to any of the gates 106 of the first set of gates 105-1 (and analogously for the "gates 106-2") and reference to the "gates 108-1" herein may refer to any of the gates 108 of the first set of gates 105-1 (and analogously for the "gates 108-2").

[0035] Each of the gates 106/108 may include a gate dielectric 114 (e.g., the gate dielectric 114-1 for the gates 106-1/108-1, and the gate dielectric 114-2 for the gates 106-2/108-2). In the embodiment illustrated in FIG. 2, the gate dielectric 114 for all of the gates 106/108 in a particular set of gates 105 is provided by a common layer of gate dielectric material. In other embodiments, the gate dielectric 114 for each of the gates 106/108 in a particular set of gates 105 may be provided by separate portions of gate dielectric 114 (e.g., as discussed below with reference to FIGS. 38-42). In some embodiments, the gate dielectric 114 may be a multilayer gate dielectric (e.g., with multiple materials used to improve the interface between the fin 104 and the corresponding gate metal). The gate dielectric 114 may be, for example, silicon oxide, aluminum oxide, or a high-k dielectric, such as hafnium oxide. More generally, the gate dielectric 114 may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of materials that may be used in the gate

dielectric 114 may include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, tantalum oxide, tantalum silicon oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric 114 to improve the quality of the gate dielectric 114. The gate dielectric 114-1 may be a same material as the gate dielectric 114-2, or a different material.

[0036] Each of the gates 106-1 may include a gate metal 110-1. The gate dielectric 114-1 may be disposed between the gate metal 110-1 and the quantum well stack structure 146. In some embodiments, the gate metal 110-1 may be a superconductor, such as aluminum, titanium nitride (e.g., deposited via atomic layer deposition), or niobium titanium nitride. The sides of the gate metal 110-1 may be substantially parallel, as shown in FIG. 2, and insulating spacers 134-1 may be disposed on the sides of the gate metal 110-1. As illustrated in FIG. 2, the spacers 134-1 may be thinner farther from the fin 104 and thicker closer to the fin 104. In some embodiments, the spacers 134-1 may have a convex shape. The spacers 134-1 may be formed of any suitable material, such as a carbon-doped oxide, silicon nitride, silicon oxide, or other carbides or nitrides (e.g., silicon carbide, silicon nitride doped with carbon, and silicon oxynitride).

[0037] Each of the gates 108-1 may include a gate metal 112-1. The gate dielectric 114-1 may be disposed between the gate metal 112-1 and the quantum well stack structure 146. In some embodiments, the gate metal 112-1 may be a different metal from the gate metal 110-1; in other embodiments, the gate metal 112-1 and the gate metal 110-1 may have the same material composition. In some embodiments, the gate metal 112-1 may be a superconductor, such as aluminum, titanium nitride (e.g., deposited via atomic layer deposition), or niobium titanium nitride.

[0038] Each of the gates 106-2 may include a gate metal 110-2 and a hardmask 116-2. The hardmask 116-2 may be formed of silicon nitride, silicon carbide, or another suitable material. The gate metal 110-2 may be disposed between the hardmask 116-2 and the gate dielectric 114-2, and the gate dielectric 114-2 may be disposed between the gate metal 110-2 and the fin 104. Only one portion of the hardmask 116-2 is labeled in FIG. 2 for ease of illustration. In some embodiments, the gate metal 110-2 may be a superconductor, such as aluminum, titanium nitride (e.g., deposited via atomic layer deposition), or niobium titanium nitride. In some embodiments, the hardmask 116-2 may not be present in the quantum dot device 100 (e.g., a hardmask like the hardmask 116-2 may be removed during processing, as discussed below). The sides of the gate metal 110-2 may be substantially parallel, as shown in FIG. 2, and insulating spacers 134-2 may be disposed on the sides of the gate metal 110-2 and the hardmask 116-2. As illustrated in FIG. 2, the spacers 134-2 may be

thicker closer to the fin 104 and thinner farther away from the fin 104. In some embodiments, the spacers 134-2 may have a convex shape. The spacers 134-2 may be formed of any suitable material, such as a carbon-doped oxide, silicon nitride, silicon oxide, or other carbides or nitrides (e.g., silicon carbide, silicon nitride doped with carbon, and silicon oxynitride). In some embodiments, the gate metal 110-2 may be a different metal from the gate metal 110-1; in other embodiments, the gate metal 110-2 and the gate metal 110-1 may have the same material composition.

[0039] Each of the gates 108-2 may include a gate metal 112-2 and a hardmask 118-2. The hardmask 118-2 may be formed of any of the materials discussed above with reference to the hardmask 116-2. The gate metal 112-2 may be disposed between the hardmask 118-2 and the gate dielectric 114-2, and the gate dielectric 114-2 may be disposed between the gate metal 112-2 and the fin 104. In the embodiment illustrated in FIG. 2, the hardmask 118-2 may extend over the hardmask 116-2 (and over the gate metal 110-2 of the gates 106-2), while in other embodiments, the hardmask 118-2 may not extend over the gate metal 110-2 (e.g., as discussed below with reference to FIG. 43). In some embodiments, the gate metal 112-2 may be a different metal from the gate metal 110-2; in other embodiments, the gate metal 112-2 and the gate metal 110-2 may have the same material composition. In some embodiments, the gate metal 112-2 may be a different metal from the gate metal 112-1; in other embodiments, the gate metal 112-2 and the gate metal 112-1 may have the same material composition. In some embodiments, the gate metal 112-2 may be a superconductor, such as aluminum, titanium nitride (e.g., deposited via atomic layer deposition), or niobium titanium nitride. In some embodiments, the hardmask 118-2 may not be present in the quantum dot device 100 (e.g., a hardmask like the hardmask 118-2 may be removed during processing, as discussed below).

[0040] The gate 108-11 may extend between the proximate spacers 134-1 on the sides of the gate 106-11 and the gate 106-12, as shown in FIG. 2. In some embodiments, the gate metal 112-1 of the gate 108-11 may extend between the spacers 134-1 on the sides of the gate 106-11 and the gate 106-12. Thus, the gate metal 112-1 of the gate 108-11 may have a shape that is substantially complementary to the shape of the spacers 134-1, as shown. Similarly, the gate 108-12 may extend between the proximate spacers 134-1 on the sides of the gate 106-12 and the gate 106-13. The gates 106-2/108-2 and the dielectric material 114-2 of the second set of gates 105-2 may take the form of any of these embodiments of the gates 106-1/108-1 and the dielectric material 114-1. As illustrated in FIGS. 1 and 2, in some embodiments, the gates 106-1/108-1 may be mirror images of the gates 106-2/108-2 around the quantum well stack structure 146. In some embodiments in which the gate dielectric 114 is not a layer shared commonly between the associated gates 106 and 108, but instead is separately deposited on the fin 104 between the associated spacers 134 (e.g., as

discussed below with reference to FIGS. 38-42), the gate dielectric 114 may extend at least partially up the sides of the associated spacers 134, and the gate metal 112 may extend between the portions of the associated gate dielectric 114 on the associated spacers 134.

[0041] The dimensions of the gates 106/108 may take any suitable values. For example, in some embodiments, the z-height 166 of the gate metal 110 may be between 40 and 75 nanometers (e.g., approximately 50 nanometers); the z-height of the gate metal 112 may be in the same range. In embodiments like the ones illustrated in FIGS. 2, 37, and 43, the z-height of the gate metal 112 may be greater than the z-height of the gate metal 110. In some embodiments, the length 168 of the gate metal 110 (i.e., in the x-direction) may be between 20 and 40 nanometers (e.g., 30 nanometers). In some embodiments, the distance 170 between adjacent ones of the gates 106 (e.g., as measured from the gate metal 110 of one gate 106 to the gate metal 110 of an adjacent gate 106 in the x-direction, as illustrated in FIG. 2) may be between 40 and 60 nanometers (e.g., 50 nanometers). In some embodiments, the thickness 172 of the spacers 134 may be between 1 and 10 nanometers (e.g., between 3 and 5 nanometers, between 4 and 6 nanometers, or between 4 and 7 nanometers). The length of the gate metal 112 (i.e., in the x-direction) may depend on the dimensions of the gates 106 and the spacers 134, as illustrated in FIG. 2. As indicated in FIG. 1, the gates 106/108 on one fin 104 may extend over the insulating material 128 beyond their respective fins 104 and towards the other fin 104, but may be isolated from their counterpart gates by the intervening insulating material 130 and spacers 134.

[0042] As shown in FIG. 2, the gates 106 and 108 of each set 105 may be alternatingly arranged along the fin 104 in the x-direction. During operation of the quantum dot device 100, voltages may be applied to the gates 106-1/108-1 to adjust the potential energy in the quantum well layer 152-1 in the fin 104 to create quantum wells of varying depths in which quantum dots 142-1 may form. Similarly, voltages may be applied to the gates 106-2/108-2 to adjust the potential energy in the quantum well layer 152-2 in the fin 104 to create quantum wells of varying depths in which quantum dots 142-2 may form. Only one quantum dot 142-1 and one quantum dot 142-2 are labeled with a reference numeral in FIG. 2 for ease of illustration, but five are indicated as dotted circles in each fin 104. The spacers 134 may themselves provide "passive" barriers between quantum wells under the gates 106/108 in the associated quantum well layer 152, and the voltages applied to different ones of the gates 106/108 may adjust the potential energy under the gates 106/108 in the quantum well layer; decreasing the potential energy may form quantum wells, while increasing the potential energy may form quantum barriers. The discussion below may generally refer to gates 106/108, quantum dots 142, and quantum well layers 152. This discussion may apply to the gates 106-1/108-

1, quantum dots 142-1, and quantum well layer 152-1, respectively; to the gates 106-2/108-2, quantum dots 142-2, and quantum well layer 152-2, respectively; or to both.

[0043] The fins 104 may include doped regions 140 that may serve as a reservoir of charge carriers for the quantum dot device 100. In particular, the doped regions 140-1 may be in conductive contact with the quantum well layer 152-1, and the doped regions 140-2 may be in conductive contact with the quantum well layer 152-2. For example, an n-type doped region 140 may supply electrons for electron-type quantum dots 142, and a p-type doped region 140 may supply holes for hole-type quantum dots 142. In some embodiments, an interface material 141 may be disposed at a surface of a doped region 140, as shown by the interface material 141-1 at the surface of the doped regions 140-1 and the interface material 141-2 at the surface of the doped regions 140-2. The interface material 141 may facilitate electrical coupling between a conductive contact (e.g., a conductive via 136, as discussed below) and the doped region 140. The interface material 141 may be any suitable metal-semiconductor ohmic contact material; for example, in embodiments in which the doped region 140 includes silicon, the interface material 141 may include nickel silicide, aluminum silicide, titanium silicide, molybdenum silicide, cobalt silicide, tungsten silicide, or platinum silicide (e.g., as discussed below with reference to FIGS. 28-29). In some embodiments, the interface material 141 may be a non-silicide compound, such as titanium nitride. In some embodiments, the interface material 141 may be a metal (e.g., aluminum, tungsten, or indium).

[0044] The quantum dot devices 100 disclosed herein may be used to form electron-type or hole-type quantum dots 142. Note that the polarity of the voltages applied to the gates 106/108 to form quantum wells/barriers depend on the charge carriers used in the quantum dot device 100. In embodiments in which the charge carriers are electrons (and thus the quantum dots 142 are electron-type quantum dots), amply negative voltages applied to a gate 106/108 may increase the potential barrier under the gate 106/108, and amply positive voltages applied to a gate 106/108 may decrease the potential barrier under the gate 106/108 (thereby forming a potential well in the associated quantum well layer 152 in which an electron-type quantum dot 142 may form). In embodiments in which the charge carriers are holes (and thus the quantum dots 142 are hole-type quantum dots), amply positive voltages applied to a gate 106/108 may increase the potential barrier under the gate 106/108, and amply negative voltages applied to a gate 106 and 108 may decrease the potential barrier under the gate 106/108 (thereby forming a potential well in the associated quantum well layer 152 in which a hole-type quantum dot 142 may form). The quantum dot devices 100 disclosed herein may be used to form electron-type or hole-type quantum dots.

[0045] Voltages may be applied to each of the gates 106 and 108 separately to adjust the potential energy in the quantum well layer under the gates 106 and 108, and thereby control the formation of

quantum dots 142 under each of the gates 106 and 108. Additionally, the relative potential energy profiles under different ones of the gates 106 and 108 allow the quantum dot device 100 to tune the potential interaction between quantum dots 142 under adjacent gates. For example, if two adjacent quantum dots 142 (e.g., one quantum dot 142-1 under a gate 106-1 and another quantum dot 142-1 under a gate 108-1) are separated by only a short potential barrier, the two quantum dots 142 may interact more strongly than if they were separated by a taller potential barrier. Since the depth of the potential wells/height of the potential barriers under each gate 106/108 may be adjusted by adjusting the voltages on the respective gates 106/108, the differences in potential between adjacent gates 106/108 may be adjusted, and thus the interaction tuned.

[0046] In some applications, the gates 108 may be used as plunger gates to enable the formation of quantum dots 142 under the gates 108, while the gates 106 may be used as barrier gates to adjust the potential barrier between quantum dots 142 formed under adjacent gates 108. In other applications, the gates 108 may be used as barrier gates, while the gates 106 are used as plunger gates. In other applications, quantum dots 142 may be formed under all of the gates 106 and 108, or under any desired subset of the gates 106 and 108.

[0047] Conductive vias and lines may make contact with the gates 106/108, and with the doped regions 140, to enable electrical connection to the gates 106/108 and the doped regions 140 to be made in desired locations. As shown in FIGS. 1-3, the gates 106-1 may extend away from the fins 104, and conductive vias 120-1 may extend through the insulating material 130-2 to contact the gate metal 110-1 of the gates 106-1. The gates 108-1 may extend away from the fins 104, and conductive vias 122-1 may extend through the insulating material 130-2 to contact the gate metal 112-1 of the gates 108-1. The gates 106-2 may extend away from the fins 104, and conductive vias 120-2 may contact the gates 106-2 (and are drawn in dashed lines in FIG. 2 to indicate their location behind the plane of the drawing). The conductive vias 120-2 may extend through the hardmask 116-2 and the hardmask 118-2 to contact the gate metal 110-2 of the gates 106-2. The gates 108-2 may extend away from the fins 104, and conductive vias 122-2 may contact the gates 108-2 (also drawn in dashed lines in FIG. 2 to indicate their location behind the plane of the drawing). The conductive vias 122-2 may extend through the hardmask 118-2 to contact the gate metal 112-2 of the gates 108-2. Conductive vias 136 may contact the interface material 141 and may thereby make electrical contact with the doped regions 140. In particular, the conductive vias 136-1 may extend through the insulating material 130 and make contact with the doped regions 140-1, and the conductive vias 136-2 may extend through the insulating material 130 and make contact with the doped regions 140-2. The quantum dot device 100 may include further conductive vias and/or lines (not shown) to make electrical contact to the gates 106/108 and/or the doped regions 140, as desired. The

conductive vias and lines included in a quantum dot device 100 may include any suitable materials, such as copper, tungsten (deposited, e.g., by CVD), or a superconductor (e.g., aluminum, tin, titanium nitride, niobium titanium nitride, tantalum, niobium, or other niobium compounds such as niobium tin and niobium germanium).

[0048] As illustrated in FIG. 2, in some embodiments, the fins 104 may include recesses 107 that extend down to the interface material 141-1 to make conductive contact with the doped regions 140-1 (and thereby the quantum well layer 152-1). The recesses 107 may be filled with the insulating material 130, and the bottoms of the recesses 107 may be doped to provide the doped regions 140-1.

[0049] During operation, a bias voltage may be applied to the doped regions 140 (e.g., via the conductive vias 136 and the interface material 141) to cause current to flow through the doped regions 140. When the doped regions 140 are doped with an n-type material, this voltage may be positive; when the doped regions 140 are doped with a p-type material, this voltage may be negative. The magnitude of this bias voltage may take any suitable value (e.g., between 0.25 volts and 2 volts).

[0050] The conductive vias 120, 122, and 136 may be electrically isolated from each other by an insulating material 130. The insulating material 130 may be any suitable material, such as an interlayer dielectric (ILD). Examples of the insulating material 130 may include silicon oxide, silicon nitride, aluminum oxide, carbon-doped oxide, and/or silicon oxynitride. As known in the art of integrated circuit manufacturing, conductive vias and lines may be formed in an iterative process in which layers of structures are formed on top of each other. In some embodiments, the conductive vias 120/122/136 may have a width that is 20 nanometers or greater at their widest point (e.g., 30 nanometers), and a pitch of 80 nanometers or greater (e.g., 100 nanometers). In some embodiments, conductive lines (not shown) included in the quantum dot device 100 may have a width that is 100 nanometers or greater, and a pitch of 100 nanometers or greater. The particular arrangement of conductive vias shown in FIGS. 1-3 is simply illustrative, and any electrical routing arrangement may be implemented.

[0051] As discussed above, the structure of the fin 104-1 may be the same as the structure of the fin 104-2; similarly, the construction of gates 106/108 on the fin 104-1 may be the same as the construction of gates 106/108 on the fin 104-2. The gates 106/108 on the fin 104-1 may be mirrored by corresponding gates 106/108 on the parallel fin 104-2. The insulating material 130-1 and the spacers 134-1 may separate the sets of gates 105-1 on the different fins 104-1 and 104-2, and the insulating material 130-2 and the spacers 134-2 may separate the sets of gates 105-2 on the different fins 104-1 and 104-2.

[0052] In some embodiments, the quantum dots 142-2 in a fin 104 may be used as "active" quantum dots in the sense that these quantum dots 142-2 act as qubits and are controlled (e.g., by voltages applied to the gates 106-2/108-2 of the fin 104-1) to perform quantum computations. The quantum dots 142-1 in a fin 104 may be used as "read" quantum dots in the sense that these quantum dots 142-2 may sense the quantum state of the quantum dots 142-2 in the same fin 104 by detecting the electric field generated by the charge in the quantum dots 142-1, and may convert the quantum state of the quantum dots 142-2 into electrical signals that may be detected by the gates 106-1/108-1. Each quantum dot 142-2 in a fin 104 may be read by its corresponding quantum dot 142-1 in the fin 104. Thus, the quantum dot device 100 enables both quantum computation and the ability to read the results of a quantum computation within a single fin, if desired.

[0053] In some embodiments, the quantum dots 142 in the fin 104-1 may be used as "active" quantum dots in the sense that these quantum dots 142 act as qubits and are controlled (e.g., by voltages applied to the gates 106/108 of the fin 104-1) to perform quantum computations. The quantum dots 142 in the fin 104-2 may be used as "read" quantum dots in the sense that these quantum dots 142 may sense the quantum state of the quantum dots 142 in the fin 104-1 by detecting the electric field generated by the charge in the quantum dots 142 in the fin 104-1, and may convert the quantum state of the quantum dots 142 in the fin 104-1 into electrical signals that may be detected by the gates 106/108 on the fin 104-2. Each quantum dot 142 in the fin 104-1 may be read by its corresponding quantum dot 142 in the fin 104-2. Thus, the quantum dot device 100 enables both quantum computation and the ability to read the results of a quantum computation across two fins 104.

[0054] The quantum dot devices 100 disclosed herein may be manufactured using any suitable techniques. FIGS. 4-31 illustrate various example stages in the manufacture of the quantum dot device 100 of FIGS. 1-3, in accordance with various embodiments. Although the particular manufacturing operations discussed below with reference to FIGS. 4-31 are illustrated as manufacturing a particular embodiment of the quantum dot device 100, these operations may be applied to manufacture many different embodiments of the quantum dot device 100, as discussed herein. Any of the elements discussed below with reference to FIGS. 4-31 may take the form of any of the embodiments of those elements discussed above (or otherwise disclosed herein). For ease of illustration, not all elements in each of FIGS. 4-31 are expressly labeled with reference numerals, but reference numerals for each element are included among the drawings of FIGS. 4-31.

[0055] FIG. 4 illustrates a cross-sectional view of an assembly 200 including a base 144. The base 144 may include any suitable semiconductor material or materials. In some embodiments, the base 144 may include a semiconductor material. For example, the base 144 may include silicon (e.g., may

be formed from a silicon wafer). In some embodiments, the base 144 may include a substrate and a buffer material, as discussed below with reference to FIG. 35 and FIGS. 36-52.

[0056] FIG. 5 illustrates a cross-sectional view of an assembly 202 subsequent to providing a additional layers 159 on the base 144 of the assembly 200 (FIG. 4). The assembly 202 may be regarded as a quantum well stack structure 146. The additional layers 159 may include one or more quantum well layers 152 as part of a strain compensated region, as discussed in detail below. In particular, in the embodiment discussed in FIGS. 1-3 and 4-31, the additional layers 159 may include a quantum well layer 152-1 and a quantum well layer 152-2 (spaced apart by, e.g., a barrier layer, as discussed below). As discussed above, a 2DEG may form in the quantum well layer 152-1 and/or the quantum well layer 152-2 during operation of the quantum dot device 100. Various embodiments of the quantum well stack structure 146 are discussed below with reference to FIG. 35 and FIGS. 36-52. As illustrated in FIG. 4, in some embodiments, the base 144 may be substantially planar, and the additional layers 159 may be "blanket deposited" on the base 144; in other embodiments, the base 144 or one of its components (e.g., the substrate 312 of the embodiments discussed below with reference to FIGS. 36-52) may have trenches or other features, and the additional layers 159 may be grown on such a base 144.

[0057] FIG. 6 illustrates a cross-sectional view of an assembly 204 subsequent to forming fins 104 in the assembly 202 (FIG. 5). The fins 104 may be formed in the assembly 202 by patterning and then etching the assembly 202, as known in the art; the portion of the structure from which the fins 104 extend may provide a support 102. For example, a combination of dry and wet etch chemistry may be used to form the fins 104, and the appropriate chemistry may depend on the materials included in the assembly 202, as known in the art. At least some of the base 144 may be included in the support 102, and at least some of the quantum well stack structure 146 may be included in the fins 104. In particular, the quantum well layers 152-1 and 152-2 of the quantum well stack structure 146 may be included in the fins 104.

[0058] FIG. 7 illustrates a cross-sectional view of an assembly 206 subsequent to providing an insulating material 128 to the assembly 204 (FIG. 6). Any suitable material may be used as the insulating material 128 to electrically insulate the fins 104 from each other. As noted above, in some embodiments, the insulating material 128 may be a dielectric material, such as silicon oxide.

[0059] FIG. 8 illustrates a cross-sectional view of an assembly 208 subsequent to planarizing the assembly 206 (FIG. 7) to remove the insulating material 128 above the fins 104. In some embodiments, the assembly 206 may be planarized using a chemical mechanical polishing (CMP) technique.

[0060] FIG. 9 is a perspective view of at least a portion of the assembly 208, showing the fins 104 extending from the support 102 and separated by the insulating material 128. The cross-sectional views of FIGS. 4-8 are taken parallel to the plane of the page of the perspective view of FIG. 9. FIG. 10 is another cross-sectional view of the assembly 208, taken along the dashed line along the fin 104-1 in FIG. 9. The cross-sectional views illustrated in FIGS. 11-31 are taken along the same cross section as FIG. 10.

[0061] FIG. 11 is a cross-sectional view of an assembly 210 subsequent to forming a gate stack 174 on the fins 104 of the assembly 208 (FIGS. 8-10). The gate stack 174 may include the gate dielectric 114-1, the gate metal 110-1, and a hardmask 116-1. The hardmask 116-1 may be formed of an electrically insulating material, such as silicon nitride or carbon-doped nitride.

[0062] FIG. 12 is a cross-sectional view of an assembly 212 subsequent to patterning the hardmask 116-1 of the assembly 210 (FIG. 11). The pattern applied to the hardmask 116-1 may correspond to the locations for the gates 106-1, as discussed below. The hardmask 116-1 may be patterned by applying a resist, patterning the resist using lithography, and then etching the hardmask (using dry etching or any appropriate technique).

[0063] FIG. 13 is a cross-sectional view of an assembly 214 subsequent to etching the assembly 212 (FIG. 12) to remove the gate metal 110-1 that is not protected by the patterned hardmask 116-1 to form the gates 106-1. In some embodiments, as illustrated in FIG. 13, the gate dielectric 114-1 may remain after the etched gate metal 110-1 is etched away; in other embodiments, the gate dielectric 114-1 may also be etched during the etching of the gate metal 110-1. Examples of such embodiments are discussed below with reference to FIGS. 38-42.

[0064] FIG. 14 is a cross-sectional view of an assembly 216 subsequent to providing spacer material 132 on the assembly 214 (FIG. 13). The spacer material 132 may include any of the materials discussed above with reference to the spacers 134-1, for example, and may be deposited using any suitable technique. For example, the spacer material 132 may be a nitride material (e.g., silicon nitride) deposited by sputtering.

[0065] FIG. 15 is a cross-sectional view of an assembly 218 subsequent to etching the spacer material 132 of the assembly 216 (FIG. 14), leaving spacers 134-1 formed of the spacer material 132 on the sides of the gates 106-1 (e.g., on the sides of the hardmask 116-1 and the gate metal 110-1). The etching of the spacer material 132 may be an anisotropic etch, etching the spacer material 132 "downward" to remove the spacer material 132 on top of the gates 106-1 and in some of the area between the gates 106-1, while leaving the spacers 134-1 on the sides of the gates 106. In some embodiments, the anisotropic etch may be a dry etch.

[0066] FIG. 16 is a cross-sectional view of an assembly 220 subsequent to providing the gate metal 112-1 on the assembly 218 (FIG. 15). The gate metal 112-1 may fill the areas between adjacent ones of the gates 106-1, and may extend over the tops of the gates 106-1.

[0067] FIG. 17 is a cross-sectional view of an assembly 222 subsequent to planarizing the assembly 220 (FIG. 16) to remove the gate metal 112-1 above the gates 106-1. In some embodiments, the assembly 220 may be planarized using a CMP technique. Some of the remaining gate metal 112-1 may fill the areas between adjacent ones of the gates 106-1, while other portions 150 of the remaining gate metal 112-1 may be located "outside" of the gates 106-1.

[0068] FIG. 18 is a cross-sectional view of an assembly 224 subsequent to providing a hardmask 118-1 on the planarized surface of the assembly 222 (FIG. 17). The hardmask 118-1 may be formed of any of the materials discussed above with reference to the hardmask 116-1, for example.

[0069] FIG. 19 is a cross-sectional view of an assembly 226 subsequent to patterning the hardmask 118-1 of the assembly 224 (FIG. 18). The pattern applied to the hardmask 118-1 may extend over the hardmask 116-1 (and over the gate metal 110-1 of the gates 106-1, as well as over the locations for the gates 108-1 (as illustrated in FIG. 2). The hardmask 118-1 may be non-coplanar with the hardmask 116-1, as illustrated in FIG. 19. The hardmask 118-1 illustrated in FIG. 19 may thus be a common, continuous portion of hardmask 118-1 that extends over all of the hardmask 116-1. Examples of embodiments in which the hardmask 118-1 is not disposed over the entirety of the hardmask 116-1 are discussed below with reference to FIGS. 35-37 and 43. The hardmask 118-1 may be patterned using any of the techniques discussed above with reference to the patterning of the hardmask 116-1, for example.

[0070] FIG. 20 is a cross-sectional view of an assembly 228 subsequent to etching the assembly 226 (FIG. 19) to remove the portions 150 that are not protected by the patterned hardmask 118-1 to form the gates 108-1. Portions of the hardmask 118-1 may remain on top of the hardmask 116-1, as shown. The operations performed on the assembly 226 may include removing any gate dielectric 114-1 that is "exposed" on the fin 104, as shown. The excess gate dielectric 114-1 may be removed using any suitable technique, such as chemical etching or silicon bombardment.

[0071] FIG. 21 is a cross-sectional view of an assembly 230 subsequent to providing an insulating material 130-1 on the assembly 228 (FIG. 20). The insulating material 130-1 may take any of the forms discussed above. For example, the insulating material 130-1 may be a dielectric material, such as silicon oxide. The insulating material 130-1 may be provided on the assembly 228 using any suitable technique, such as spin coating, chemical vapor deposition (CVD), or plasma-enhanced CVD (PECVD). In some embodiments, the insulating material 130-1 may be polished back after deposition, and before further processing. In some embodiments, the assembly 230 may be

planarized to remove the hardmasks 116-1 and 118-1, then additional insulating material 130-1 may optionally be provided on the planarized surface; in such an embodiment, the hardmasks 116-1 and 118-1 would not be present in the quantum dot device 100.

[0072] FIG. 22 is a cross-sectional view of an assembly 232 subsequent to attaching a support 103 to the insulating material 130-1. The support 103 may take any suitable form for providing mechanical support for the operations discussed below. For example, in some embodiments, the support 103 may be a carrier wafer and may be secured to the insulating material 130-1 using an adhesive. In some embodiments, the support 103 may be a mechanical fixture that may be temporarily secured to the insulating material 130-1, and removed when no longer needed.

[0073] FIG. 23 is a cross-sectional view of an assembly 234 subsequent to removing the support 102 from the assembly 232 (FIG. 22). The fin 104 may remain secured to the gates 106-1/108-1 and the insulating material 130-1 (which may be mechanically supported by the support 103). Any suitable technique may be used to separate the support 102 from the rest of the assembly 232. For example, in some embodiments, an ion implantation and wafer bonding technique may be used in which the support 103 is adhered to the assembly 230 (as discussed above with reference to FIG. 22) and then the support 102 is polished or etched away. In some embodiments, the support 102 may be mechanically separated from the rest of the assembly 232, and then the "broken" surface of the assembly 234 may be polished or etched.

[0074] FIG. 24 is a cross-sectional view of an assembly 236 subsequent to turning the assembly 234 (FIG. 23) "upside down" so that further processing may be performed on the exposed fin 104. In some embodiments, the assembly 234 need not be physically reoriented (as illustrated in FIG. 24) in order for subsequent processing operations to be performed.

[0075] FIG. 25 is a cross-sectional view of an assembly 238 subsequent to forming gates 106-2/108-2 with a gate dielectric 114-2 on the fin 104 proximate to the quantum well layer 152-2. The gates 106-2/108-2 may be formed using any of the techniques discussed above with reference to the formation of the gates 106-1/108-1 (e.g., discussed above with reference to FIGS. 11-20), or any of the techniques discussed below (e.g., with reference to FIGS. 36-44). For example, as shown in FIG. 25, hardmasks 116-2 and 118-2 may be part of the gates 106-2/108-2, analogously to the hardmasks 116-1 and 118-1 of the gates 106-1/108-1.

[0076] FIG. 26 is a cross-sectional view of an assembly 240 subsequent to forming recesses 107 in the quantum well stack structure 146 of the assembly 238 (FIG. 25). The recesses 107 may be formed using any of the fin patterning techniques discussed above with reference to FIG. 6, and as discussed above, may extend down to the quantum well layer 152-1.

[0077] FIG. 27 is a cross-sectional view of an assembly 242 subsequent to doping the quantum well stack structure 146 of the assembly 240 (FIG. 26) to form doped regions 140-1 at the bottoms of the recesses 107 in the quantum well stack structure 146, and doped regions 140-2 adjacent to the gates 106-2/108-2. The doped regions 140-1 may be in conductive contact with the quantum well layer 152-1, and the doped regions 140-2 may be in conductive contact with the quantum well layer 152-2. The type of dopant used to form the doped regions 140 may depend on the type of quantum dot desired, as discussed above. In some embodiments, the doping may be performed by ion implantation. For example, when a quantum dot 142 is to be an electron-type quantum dot 142, the doped regions 140 may be formed by ion implantation of phosphorous, arsenic, or another n-type material. When a quantum dot 142 is to be a hole-type quantum dot 142, the doped regions 140 may be formed by ion implantation of boron or another p-type material. An annealing process that activates the dopants and causes them to diffuse farther into the fins 104 may follow the ion implantation process. The depth of the doped regions 140 may take any suitable value; for example, in some embodiments, the doped regions 140 may each have a depth 115 between 500 and 1000 Angstroms.

[0078] The outer spacers 134-2 on the outer gates 106-2 may provide a doping boundary, limiting diffusion of the dopant from the doped regions 140-2 into the area under the gates 106-2/108-2. As shown, the doped regions 140-2 may extend under the adjacent outer spacers 134-2. In some embodiments, the doped regions 140-2 may extend past the outer spacers 134-2 and under the gate metal 110-2 of the outer gates 106-2, may extend only to the boundary between the outer spacers 134-2 and the adjacent gate metal 110-2, or may terminate under the outer spacers 134-2 and not reach the boundary between the outer spacers 134-2 and the adjacent gate metal 110-2. Examples of such embodiments are discussed below with reference to FIGS. 44 and 45. The doping concentration of the doped regions 140 may, in some embodiments, be between $10^{17}/cm^3$ and $10^{20}/cm^3$.

[0079] FIG. 28 is a cross-sectional side view of an assembly 244 subsequent to providing a layer of nickel or other material 143 over the assembly 242 (FIG. 27). The nickel or other material 143 may be deposited on the assembly 242 using any suitable technique (e.g., a plating technique, chemical vapor deposition, or atomic layer deposition).

[0080] FIG. 29 is a cross-sectional side view of an assembly 246 subsequent to annealing the assembly 244 (FIG. 28) to cause the material 143 to interact with the doped regions 140 to form the interface material 141, then removing the unreacted material 143. When the doped regions 140 include silicon and the material 143 includes nickel, for example, the interface material 141 may be nickel silicide. Materials other than nickel may be deposited in the operations discussed above with

reference to FIG. 28 in order to form other interface materials 141, including titanium, aluminum, molybdenum, cobalt, tungsten, or platinum, for example. More generally, the interface material 141 of the assembly 246 may include any of the materials discussed herein with reference to the interface material 141.

[0081] FIG. 30 is a cross-sectional view of an assembly 248 subsequent to providing an insulating material 130-2 on the assembly 246 (FIG. 29). The insulating material 130-2 may take any of the forms discussed above. For example, the insulating material 130-2 may be a dielectric material, such as silicon oxide. The insulating material 130-2 may be provided on the assembly 246 using any suitable technique, such as spin coating, chemical vapor deposition (CVD), or plasma-enhanced CVD (PECVD). In some embodiments, the insulating material 130-2 may be polished back after deposition, and before further processing.

[0082] FIG. 31 is a cross-sectional view of an assembly 250 subsequent to forming, in the assembly 248 (FIG. 30), conductive vias 120 through the insulating material 130-2 (and the hardmasks 116 and 118) to contact the gate metal 110 of the gates 106 (only the conductive vias 120-2 are illustrated in FIG. 31, but the conductive vias 120-1 are illustrated in FIG. 3), conductive vias 122 through the insulating material 130 (and the hardmask 118) to contact the gate metal 112 of the gates 108 (only the conductive vias 122-2 are illustrated in FIG. 31, but the conductive vias 122-1 are illustrated in FIG. 3), and conductive vias 136 through the insulating material 130 to contact the interface material 141 of the doped regions 140. Further conductive vias and/or lines may be formed on the assembly 248 using conventional interconnect techniques, if desired. The resulting assembly 250 may take the form of the quantum dot device 100 discussed above with reference to FIGS. 1-3. In some embodiments, the assembly 250 may be planarized to remove the hardmasks 116-2 and 118-2, then additional insulating material 130-2 may be provided on the planarized surface before forming the conductive vias 120, 122, and 136; in such an embodiment, the hardmasks 116-2 and 118-2 would not be present in the quantum dot device 100.

[0083] As discussed above, FIGS. 1-4 depict a quantum dot device 100 with two sets of gates 105 disposed on opposite faces of a quantum well stack structure 146. In some embodiments, a quantum dot device 100 may include a set of gates 105 disposed on only one face of a quantum well stack structure 146. For example, FIGS. 32-34 are views of such a quantum dot device 100 (analogous to the views presented in FIGS. 1-3), which may include only a single quantum well layer 152. The components of the quantum dot device 100 of FIG. 1-3 may take the form of any of the analogous components of the quantum dot device 100, and may be manufactured in accordance with the techniques discussed above with reference to FIGS. 4-31. For example, the operations discussed above with reference to FIGS. 4-20 may be used to form the quantum well stack structure

146 and the set of gates 105 of the quantum dot device 100 of FIGS. 32-34 (although the quantum well stack structure 146 may include only a single quantum well layer 152), and instead of removing the support 102 and forming another set of gates 105 (as discussed above with reference to FIGS. 21-25), the manufacturing process may proceed to the operations discussed above with reference to FIGS. 26-31 (e.g., forming recesses in the quantum well stack structure 146). Any suitable ones of the embodiments of the quantum dot device 100 discussed above with reference to FIGS. 1-3 may provide embodiments of the quantum dot device 100 of FIGS. 32-34. For example, the quantum dot device 100 may include fins 104 arranged in an array, pairs of fins 104 may include an "active" fin and a "read" fin, gates 106/108 in a set of gates may be formed in any desired manner, etc.

[0084] As noted above, a quantum well stack structure 146 included in the quantum dot devices 100 disclosed herein may include a strain compensation region. Strain in the quantum well layer(s) 152 may improve the mobility of the carriers that flow therein, which may improve performance. In particular, tensile strain may improve electron mobility (and thus may be useful for quantum dot devices 100 in which electrons are the carriers of interest, as discussed above) and compressive strain may improve hole mobility (and thus may be useful for quantum dot devices 100 in which holes are the carriers of interest, as discussed above). In the embodiments disclosed herein, strain may be imparted to layers in the quantum well stack structure 146 (including the quantum well layer(s) 152) via lattice mismatch between the layers and the base 144, as discussed in detail below. Additionally, the total strain of the quantum well stack structure 146 may be mitigated by including a strain compensation region that includes layers having tensile strain and layers having compressive strain to reduce the overall strain energy of the quantum well stack structure 146 and thereby reducing the likelihood of strain-induced defects. The resulting quantum well stack structures 146 may exhibit increased strain and barrier offset confinement relative to a quantum well stack structure grown without strain compensation. Additionally, quantum well stack structures including strain compensation regions may readily provide multiple strained quantum well layers 152.

[0085] FIG. 35 is a cross-sectional view of a quantum well stack structure 146 including a base 144 and additional layers 159 disposed on the base 144. The additional layers 159 may include a strain compensation region 156 including alternating layers 153 and layers 155, as shown. The surface of the base 144 on which the additional layers 159 are disposed may be formed of a material having a base lattice constant, and the layer 153 may have a first lattice constant different from the base lattice constant such that the layer 153 is under tensile strain (when the base lattice constant is greater than the first lattice constant) or compressive strain (when the base lattice constant is less than the first lattice constant). The layer 155 (disposed on the layer 153) may also have a second lattice constant that is different from the base lattice constant such that the layer 155 is oppositely

strained relative to the layer 153. That is, when the layer 153 is under tensile strain, the layer 155 may be under compressive strain (e.g., by having a second lattice constant that is greater than the base lattice constant), and when the layer 153 is under compressive strain, the layer 155 may be under tensile strain (e.g., by having a second lattice constant that is less than the base lattice constant). Thus, the oppositely strained layers 153 and 155 may be compressively or tensilely strained relative to a material at the surface of the base 144. One or more of the layers 153 and 155 may provide the quantum well layer(s) 152 of a quantum dot device 100, and the other layers 153/155 may provide potential barriers between multiple quantum well layers 152 and/or between the quantum well layers 152 and other components of the quantum dot device 100 (e.g., the gates 106/108).

[0086] The layers 153 and 155 may be grown sequentially via epitaxy, and the strain may be created through crystal lattice mismatches between adjacent materials. In particular, the first layer 153 may be grown in an epitaxial deposition process on the base 144. The first layer 153 may be grown so that compressive (tensile) strain is preserved in the first layer 153 (i.e., the lattice of the first layer 153 does not have the opportunity to substantially "relax"). The second layer 155 with a smaller (larger) lattice constant with respect to the base 144 may be grown in an epitaxial deposition process on top of the first layer 153. The second layer 155 may also be grown below its critical layer thickness so that tensile (compressive) strain is preserved in the second layer 155. Additional successive layers 153 and 155 having a pattern of alternating compressive and tensile strain may be grown as desired. Although a particular number of layers 153 and 155 is illustrated in FIG. 35, any number of layers 153 (greater than or equal to 1) and any number of layers 155 (greater than or equal to 1) may be included as appropriate.

[0087] In FIG. 35, the base 144 includes a substrate 312 and a buffer layer 154, with the buffer layer 154 disposed between the substrate 312 and the first layer 153 so that the buffer layer 154 provides the surface on which the first layer 153 is disposed. The buffer layer 154 may trap defects that form in the quantum well stack structure as it is grown on the substrate 312. In such an embodiment, the base lattice constant is the lattice constant of the buffer layer 154. In other embodiments, the buffer layer 154 may not be included, and the lattice constant 154 of the substrate 312 may provide the base lattice constant. In other embodiments, the substrate 312 may not be included.

[0088] The quantum well stack structure 146 of FIG. 35 may also include a barrier layer 157 arranged on the strain compensation region 156 such that the strain compensation region 156 is disposed between the base 144 and the barrier layer 157. In a quantum dot device 100, the gates 106/108 may be disposed on the barrier layer 157. For example, in the quantum dot device 100 of FIGS. 1-3, the quantum well stack structure 146 may be disposed on the gate dielectric 114-1 such

that the buffer layer 154 is disposed between the quantum well layer 152-1 and the gate dielectric 114-1. The barrier layer 157 may be disposed between the quantum well layer 152-2 and the gate dielectric 114-2. In the quantum dot device 100 of FIGS. 32-34, the barrier layer 157 may be disposed between the buffer layer 154 and the gate dielectric 114.

[0089] In some embodiments, the buffer layer 154 and the barrier layer 157 may be formed of the same material, but the buffer layer 154 may be grown under different conditions (e.g., deposition temperature or growth rate) from the barrier layer 157. In particular, the barrier layer 157 may be grown under conditions that achieve fewer defects than the buffer layer 154. When the support 102 is separated from the rest of the assembly 232 during manufacturing of the quantum dot device 100 of FIGS. 1-3 (e.g., as discussed above with reference to FIG. 23), the quantum well stack structure 146 may be "broken" in the buffer layer 154. In some embodiments, the barrier layer 157 may be omitted; in some such embodiments, the topmost layer 155 may provide a barrier function.

[0090] Any suitable materials may be used in the quantum well stack structure 146. In some embodiments, the surface of the base 144 (e.g., the buffer layer 154) may be provided by a material including elements from group III, IV, and/or V of the periodic table, or any combination thereof. The layers 153 and 155 may be formed of pure elements and/or mixtures of elements, such as silicon, germanium, and III-V semiconductor materials (i.e., materials including elements found in groups III and V of the periodic table), for example.

[0091] In some embodiments, the surface of the base 144 may be Si_xGe_{1-x}, the layers 153 (layers 155) may be Si_yGe_{1-y} where $y>x$, and the layers 155 (layers 153) may be Si_zGe_{1-z}, where $z<x$ and x, y, and z are between 0 and 1. For example, in some embodiments, the buffer layer 154 may be Si_xGe_{1-x} (with a substrate 312 formed of, e.g., silicon), the layers 153 (layers 155) may be Si_yGe_{1-y} where $y>x$, and the layers 155 (layers 153) may be germanium. A particular example of such an arrangement may include a $Si_{0.5}Ge_{0.5}$ buffer layer 154, a $Si_{0.7}Ge_{0.3}$ layer 153 (layer 155), and a germanium layer 155 (layer 153). In such embodiments, the Si_yGe_{1-y} layer may be tensilely strained and the germanium layer may be compressively strained. As noted above, such embodiments may be particularly useful when one or more of the germanium layers act as a quantum well layer 152 for hole-type quantum dot devices 100.

[0092] In some embodiments, the surface of the base 144 may be Si_xGe_{1-x}, the layers 153 (layers 155) may be Si_yGe_{1-y} where $x>y$, and the layers 155 (layers 153) may be Si_zGe_{1-z}, where $z>x$ and x, y, and z are between 0 and 1. For example, in some embodiments, the buffer layer 154 may be Si_xGe_{1-x} (with a substrate 312 formed of, e.g., silicon), the layers 153 (layers 155) may be Si_yGe_{1-y} where $y<x$, and the layers 155 (layers 153) may be silicon. A particular example of such an arrangement may include a $Si_{0.7}Ge_{0.3}$ buffer layer, a $Si_{0.5}Ge_{0.5}$ layer 153 (layer 155), and a silicon layer 155 (layer 153). In

such embodiments, the Si_yGe_{1-y} layer may be compressively strained and the silicon layer may be tensilely strained. As noted above, such embodiments may be particularly useful when one or more of the silicon layers act as a quantum well layer 152 for electron-type quantum dot devices 100.

[0093] In some embodiments, the surface of the base 144 may be InP, the layers 153 (the layers 155) may be $In_xGa_{1-x}As$ where x is between 0.53 and 1, and the layers 155 (the layers 153) may be $In_yGa_{1-y}As$, where y is between 0 and 0.53. In such embodiments, the layers 153 (the layers 155) may be compressively strained, and the layers 155 (the layers 153) may be tensilely strained. In some embodiments, the surface of the base 144 may be GaSb, the layers 153 (the layers 155) may be AlSb, and the layers 155 (the layers 153) may be InAs. In such embodiments, the layers 153 (the layers 155) may be tensilely strained, and the layers 155 (the layers 153) may be compressively strained. In some embodiments, the surface of the base may be germanium, the layers 153 (the layers 155) may be Si_xGe_{1-x} where x is between 0 and 1, and the layers 155 (the layers 153) may be $In_yGa_{1-y}As$ where y is between 0 and 1. In such embodiments, the layers 153 (the layers 155) may be tensilely strained, and the layers 155 (the layers 153) may be compressively strained. In some embodiments, the surface of the base 144 may be GaAs, the layers 153 (the layers 155) may be $GaAs_xP_{1-x}$ where x is between 0 and 1, and the layers 155 (the layers 153) may be $In_yGa_{1-y}P$ where y is between 0.51 and 1. In such embodiments, the layers 153 (the layers 155) may be tensilely strained, and the layers 155 (the layers 153) may be compressively strained.

[0094] The thicknesses (i.e., z-heights) of the layers in the quantum well stack structure 146 of FIG. 35 may take any suitable values (e.g., respecting critical thickness limits). In some embodiments, the thickness of the buffer layer 154 (e.g., silicon germanium) may be between 0 and 400 nanometers. In some embodiments, the thickness of the barrier layer 157 (e.g., silicon germanium) may be between 25 and 75 nanometers (e.g., 32 nanometers). In some embodiments, the thickness of the layers 153/155 that provide the quantum well layers 152 (e.g., silicon or germanium) may be between 5 and 30 nanometers.

[0095] Although FIGS. 4 and 5 illustrate an embodiment in which the additional layers 159 of the quantum well stack structure 146 are grown on a planar surface of the base 144, this need not be the case. In some embodiments, the base 144 or one of its components may have a contoured surface, and the quantum well stack structure 146 may be formed on this contoured surface. For example, FIGS. 36-52 illustrate various embodiments in which the base 144 includes one or more trenches 261 in the substrate 312 in which the buffer layer 154 (and, in some cases, the additional layers 159) is at least partially disposed. Any of the arrangements of the base 144 and additional layers 159 discussed below with reference to FIGS. 36-52 may be used with any of the other

embodiments disclosed herein. Embodiments of the quantum well stack structure 146 discussed below include the buffer layer 154, but in some embodiments, the buffer layer 154 may be omitted.

[0096] FIGS. 36-39 illustrate various example stages in the manufacture of a quantum well stack structure 146 for a quantum dot device 100, in accordance with various embodiments. FIG. 36 is a cross-sectional view of an assembly 260 in which a second substrate material 304 is disposed on a first substrate material 302. The first substrate material 302 may be a material on which the buffer layer 154 and the additional layers 159 may be grown, and thus the choice of an appropriate material for the first substrate material 302 may depend on the material composition of the buffer layer 154 and the additional layers 159. In some embodiments (e.g., when the additional layers 159 include a silicon compound, such as silicon germanium), the first substrate material 302 may be silicon (e.g., a portion of a silicon wafer). In some embodiments, the second substrate material 304 may have a different material composition from the first substrate material 302, and as discussed below with reference to FIG. 38, may serve to trap defects in the buffer layer 154 and/or the additional layers 159 as they are grown on the first substrate material 302. The second substrate material 304 may be, for example, an oxide of the first substrate material 302. For example, the first substrate material 302 may be silicon, and the second substrate material 304 may be silicon oxide. In some embodiments, the second substrate material 304 may be provided on the first substrate material 302 using any suitable technique.

[0097] FIG. 37 is a cross-sectional view of an assembly 262 subsequent to patterning the second substrate material 304 of the assembly 260 (FIG. 36) to form one or more trenches 261 in the second substrate material 304. The substrate 312 may be provided by the first substrate material 302 and the patterned second substrate material 304. The trenches 261 may extend through the second substrate material 304 such that the bottoms of the trenches 261 are provided by the first substrate material 302. The depth 263 of the trenches 261 may be dictated by the thickness of the second substrate material 304, and the width 265 of the trenches 261 may be dictated by the pattern applied to the second substrate material 304. The depth 263 and the width 265 of the trenches 261 may be selected so that the ratio of the depth 263 to the width 265 is sufficiently large to ensure that defects generated during growth of the buffer layer 154 and/or the additional layers 159 on the first substrate material 302 in the trenches 261 are terminated in the second substrate material 304 at the sides of the trenches 261.

[0098] In particular, materials that may be included in the buffer layer 154 and/or the additional layers 159 may, when grown on the first substrate material 302, include defects that may arise because of epitaxial errors or lattice mismatches between the material of the buffer layer 154 and/or the additional layers 159 and the first substrate material 302. In the quantum dot devices

100 disclosed herein, such defects may compromise performance by acting as undesirable recombination centers or scattering sites. These defects may originate close to the first substrate material 302, and may propagate in the buffer layer 154 and/or the additional layers 159 at an angle relative to the surface of the first substrate material 302. If the depth 263 of the trenches 261 is great enough relative to the width 265 of the trenches 261, these defects may terminate at the walls of the trenches 261, and the material of the buffer layer 154 and/or the additional layers 159 grown above these termination points may exhibit a substantially lower proportion of defects than if the buffer layer 154 and/or the additional layers 159 were grown on the first substrate material 302 without the presence of the trenches 261. The use of the trenches 261 may thus result in a lower defect density in the quantum well stack structure 146 (e.g., in the strain compensation region 156, as discussed below).

[0099] As discussed above, buffer layers in quantum well stack structures 146 may be used to mitigate defects by presenting a thick region of material over which the effective defects may be attenuated; in some embodiments, the use of the trenches 261 may enable the use of a thinner quantum well stack structure 146 (e.g., a thinner buffer layer 154, as discussed below) than achievable without the trenches 261, because defects may be eliminated more "quickly" during growth. In some embodiments, the ratio between the depth 263 and the width 265 may be greater than or equal to 1 (e.g., greater than 1.5, greater than 2.5, or greater than 10). In some embodiments, the depth 263 may be between 50 and 100 nanometers (e.g., between 50 and 60 nanometers). In some applications, a depth 263 between 50 and 60 nanometers, and a ratio of depth 263 to width 265 that is greater than or equal to 1, may be adequate to trap defects arising from 1% lattice mismatch between the first substrate material 302 and the adjacent material of the quantum well stack structure 146 (e.g., the buffer layer 154, as discussed below).

[0100] FIG. 38 is a cross-sectional view of an assembly 264 subsequent to growing the buffer layer 154 (e.g., via epitaxy) in the trenches 261 on the first substrate material 302. In the embodiment illustrated in FIG. 38, the growth of the buffer layer 154 may stop before the trenches 261 are filled with the material of the buffer layer 154. The thickness 269 of the buffer layer 154 may be selected so that defects formed at the interface between the buffer layer 154 and the first substrate material 302 have been substantially terminated at the walls of the trenches 261 and do not extend to the top surface 271 of the buffer layer 154. In some embodiments, the first substrate material 302 may be silicon, the second substrate material 304 may be silicon oxide, and the buffer layer 154 may be silicon germanium.

[0101] FIG. 39 is a cross-sectional view of an assembly 266 subsequent to providing additional layers 159 on the top surface 271 of the buffer layer 154 in the trenches 261 of the assembly 264

(FIG. 38). Strain compensation regions 156 may be provided in each of the trenches 261 as a result. In some embodiments, the first substrate material 302 may be silicon, the second substrate material 304 may be silicon oxide, the buffer layer 154 may be silicon germanium, and the quantum well layer(s) 152 (included as one or more of the layers 153/155 of the additional layers 159) may be silicon.

[0102] In some embodiments, the material provided in different ones of the trenches 261 may provide the fins 104 of a quantum dot device 100. In particular, the first substrate material 302 may provide the support 102, and the remaining portion of the quantum well stack structures 146 formed in the trenches 261 may provide the fins 104 (extending from the support 102). The second substrate material 304 may provide the insulating material 128 (e.g., discussed above with reference to FIGS. 1 and 32). Thus, in various embodiments, suitable dimensions of the trenches 261 (and the spacing between the trenches 261) may take the form of any of the embodiments of the fins 104 disclosed herein.

[0103] FIG. 40 is a perspective view of a substrate 312 in which two trenches 261-1 and 261-2 are dimensioned so that the buffer layer 154 and the additional layers 159 (not shown) that fill the trenches 261-1 and 261-2 may take the form of some of the fins 104-1 and 104-2 discussed above (e.g., with reference to FIG. 9). The cross section illustrated in FIG. 37 may be the cross section of the perspective view of FIG. 40 taken along the dashed-dotted line. The footprints 273 of two example fins 104 are shown in FIG. 40 by shaded areas. In the substrate 312 illustrated in FIG. 40, if the length 267 of the trenches 261 is greater than the width 265 of the trenches 261, the ratio that controls the ability of the trenches 261 to absorb defects in the quantum well stack structures 146 may be the ratio of the depth 263 to the length 267 (and thus the length 267 may serve as the relevant "width" discussed above with reference to FIG. 37 for ratio purposes).

[0104] FIG. 41 is a cross-sectional view of a quantum dot device 100 taking the form discussed above with reference to FIG. 33 that may be formed on the embodiment of the substrate 312 illustrated in FIG. 40 (with the cross section taken along the dashed line of FIG. 40). In particular, the fin 104 may be provided by the buffer layer 154 and the additional layers 159 (and may be bordered by the patterned second substrate material 304), and the support 102 may be provided by the first substrate material 302. Although the quantum dot device 100 of FIG. 33 is illustrated in FIG. 41, any of the quantum dot devices 100 may be built on a substrate 312 as discussed above with reference to FIGS. 36-40.

[0105] Some of the embodiments discussed above with reference to FIGS. 36-40 included different fins 104 provided by portions of quantum well stack structures 146 provided in different trenches 261 of a substrate 312. In other embodiments, multiple fins 104 may be formed from a buffer layer

154 and additional layers 159 formed in a single trench 261 of a substrate 312. FIGS. 42-44 illustrate various operations in the manufacture of such a quantum well stack structure 146. In particular, FIG. 42 is a cross-sectional view of an assembly 268 subsequent to patterning the second substrate material 304 of the assembly 260 (FIG. 36) to form a substrate 312 with a trench 261 large enough so that the buffer layer 154 and the additional layers 159 formed in the trench 261 may be patterned into multiple fins 104 of a desired size. The ratio between the depth 263 and the width 265 of the trench 261 may take any of the forms discussed above with reference to FIG. 37 (e.g., the trench 261 may be sufficiently deep to adequately trap defects).

[0106] FIG. 43 is a cross-sectional view of an assembly 270 subsequent to growing the buffer layer 154 on the first substrate material 302 in the trench 261 of the assembly 268 (FIG. 42). The growth of the buffer layer 154 may take the form of any of the embodiments discussed above with reference to FIG. 38.

[0107] FIG. 44 is a cross-sectional view of an assembly 272 subsequent to providing additional layers 159 on the buffer layer 154 of the assembly 270 (FIG. 43). The provision of the additional layers 159 may take the form of any of the embodiments discussed above with reference to FIG. 39.

[0108] FIG. 45 is a perspective view of a substrate 312 in which a trench 261 is dimensioned so that the buffer layer 154 and the additional layers 159 (not shown) that fill the trench 261 may be patterned to take the form of some of the fins 104-1 and 104-2 discussed above (e.g., with reference to FIG. 9). The cross section illustrated in FIG. 42 may be the cross section of the perspective view of FIG. 45 taken along the dashed-dotted line. The footprints 273 of two example fins 104 are shown in FIG. 45 by shaded areas. In the substrate 312 illustrated in FIG. 45, if the length 267 of the trench 261 is greater than the width 265 of the trench 261, the ratio that controls the ability of the trenches 261 to absorb defects in the quantum well stack structures 146 may be the ratio of the depth 263 to the length 267 (and thus the length 267 may serve as the relevant "width" discussed above with reference to FIG. 37 for ratio purposes). Fins 104 may be patterned in the buffer layer 154 and additional layers 159 formed in the trench 261 of the substrate 312 of FIG. 45 using any suitable technique (e.g., any of the techniques discussed above with reference to FIG. 6). The cross-sectional view of a quantum dot device 100 illustrated in FIG. 41 may also be a cross-sectional view of a quantum dot device 100 having the substrate 312 illustrated in FIG. 45 (with the cross section taken along the dashed line of FIG. 45). The trench 261 of FIG. 45 may have a square footprint. A cross-sectional view of an example quantum dot device 100 formed on the embodiment of the substrate 312 of FIG. 45 may also take the form illustrated in FIG. 41.

[0109] FIGS. 46-48 illustrate alternative stages in the manufacture of the assembly 266 of FIG. 39. Although FIGS. 46-48 illustrate stages in the manufacture of the assembly 266 of FIG. 39, analogous operations may be used to manufacture the assembly 272 of FIG. 44.

[0110] FIG. 46 is a cross-sectional view of an assembly 274 subsequent to growing the buffer layer 154 on the first substrate material 302 in the trenches 261 of the assembly 262 (FIG. 37). Any of the techniques discussed above with reference to FIG. 38 may be used to grow the buffer layer 154; however, unlike the assembly 264 of FIG. 38, the buffer layer 154 of the assembly 274 of FIG. 46 may grow until the trenches 261 are filled and the buffer layer 154 extends over the top of the second substrate material 304 (e.g., as part of a lateral epitaxial overgrowth process). Lateral epitaxial overgrowth may be controlled to allow for largely defect-free films to grow and glide over the second substrate material 304, achieving a high-quality crystal structure in the buffer layer 154.

[0111] FIG. 47 is a cross-sectional view of an assembly 276 subsequent to planarizing the assembly 274 (FIG. 46) to remove the portion of the buffer layer 154 that extends over the second substrate material 304. In some embodiments, some of the second substrate material 304 may also be removed during planarization.

[0112] FIG. 48 is a cross-sectional view of an assembly 278 subsequent to recessing the buffer layer 154 of the assembly 276 (FIG. 47) back into the trenches 261 so that the buffer layer 154 no longer fills the trenches 261. The assembly 278 may then undergo further processing to complete formation of the quantum well stack structures 146, as discussed above with reference to FIG. 39. Any suitable technique may be used to recess the buffer layer 154 (e.g., a wet or dry recess). Recessing the buffer layer 154 may help ensure that the subsequent processing operations occur at a known distance from the top of the trenches 261, achieving more uniform material growth.

[0113] In some embodiments, the buffer layer 154 and/or the additional layers 159 of a quantum well stack structure 146 may be only partially disposed in a trench 261 of a substrate 312. FIGS. 49-50 illustrate various example stages in the manufacture of such a quantum well stack structure 146.

[0114] FIG. 49 is a cross-sectional view of an assembly 280 subsequent to growing the buffer layer 154 on the first substrate material 302 in the trenches 261 of the assembly 262 (FIG. 37). The growth process, and the resulting buffer layer 154, may take the form of any of the embodiments discussed above with reference to the assembly 274 of FIG. 46. The buffer layer 154 of the assembly 280 may have a top surface 271 that is spaced away from the trenches 261, and in particular, the second substrate material 304 may be disposed between the top surface 271 and the first substrate material 302.

[0115] FIG. 50 is a cross-sectional view of an assembly 282 subsequent to providing additional layers 159 on the top surface 271 of the buffer layer 154 of the assembly 280 (FIG. 49). In the

embodiment illustrated in FIG. 50, the buffer layer 154 of the quantum well stack structure 146 extends above the trenches 261.

[0116] FIG. 51 is a perspective view of a substrate 312 including multiple trenches 261 in which a buffer layer 154 and/or additional layers 159 of a quantum well stack structure 146 may be partially disposed, as discussed above with reference to FIGS. 49-50. The buffer layer 154 and the additional layers 159 (not shown) that fill the trenches 261 (and extend above the trenches 261) may be patterned to take the form of some of the fins 104-1 and 104-2 discussed above (e.g., with reference to FIG. 9). The footprints 273 of two example fins 104 are shown in FIG. 51 by shaded areas, and the considerations discussed above with reference to the dimensions of the trenches 261 of FIGS. 40 and 45 may apply to the trenches 261 of FIG. 51. Fins 104 may be patterned in a buffer layer 154 and additional layers 159 formed in and on the trenches 261 of the substrate 312 of FIG. 51 using any suitable technique (e.g., any of the techniques discussed above with reference to FIG. 6).

[0117] FIG. 52 is a cross-sectional view of a quantum dot device 100 (taking the form discussed above with reference to FIG. 33) that may be formed on the embodiment of the substrate 312 illustrated in FIG. 51. In particular, the fin 104 may be at least partially provided by the additional layers 159, and the trenches 261 (and the second substrate material 304) may be disposed between the gate metals 110/112 and the first substrate material 302. Although the quantum dot device 100 of FIG. 33 is illustrated in FIG. 52, any of the quantum dot devices 100 may be built on a substrate 312 as illustrated in FIG. 41.

[0118] Although the fins 104 have been illustrated in many of the preceding figures as substantially rectangular with parallel sidewalls, this is simply for ease of illustration, and the fins 104 may have any suitable shape (e.g., a shape appropriate to the manufacturing processes used to form the fins 104). For example, in some embodiments, the fins 104 may be tapered, narrowing as they extend away from the support 102 (FIG. 6). In some embodiments, the fins 104 may taper by 3-10 nanometers in x-width for every 100 nanometers in z-height (e.g., 5 nanometers in x-width for every 100 nanometers in z-height). In some embodiments, the patterning may extend into the substrate 312, while in other embodiments, the patterning may not extend into the substrate 312.

[0119] As noted above, a single fin 104 may include multiple sets of gates 105, spaced apart along the fin 104. FIG. 53 is a cross-sectional view of an example of such a quantum dot device 100 having multiple groups of sets of gates 180 on a single fin 104, in accordance with various embodiments. Each of the groups 180 may include a set of gates 105-1 and a set of gates 105-2 (not labeled in FIG. 53 for ease of illustration) that may take the form of any of the embodiments of the sets of gates 105-1 and 105-2 discussed herein. A doped region 140-1 (and its interface material 141-1) may be disposed between the sets of gates 105-1 of two adjacent groups 180 (labeled in FIG. 53 as groups

180-1 and 180-2), and may provide a common reservoir for the sets of gates 105-1 of both groups 180. In some embodiments, this "common" doped region 140-1 may be electrically contacted by a single conductive via 136-1. The particular number of gates 106/108 illustrated in FIG. 53, and the particular number of groups 180, is simply illustrative, and a fin 104 may include any suitable number of gates 106/108 arranged in any suitable number of groups 180. Similar embodiments having multiple sets of gates 105 may be realized for the "single-sided" embodiment of the quantum dot device 100 illustrated in FIGS. 32-34.

[0120] As discussed above with reference to FIGS. 1-3, in some embodiments in which the gate dielectric 114 is not a layer shared commonly between the gates 108 and 106, but instead is separately deposited on the fin 104 between the spacers 134, the gate dielectric 114 may extend at least partially up the sides of the spacers 134, and the gate metal 112 may extend between the portions of gate dielectric 114 on the spacers 134. FIGS. 54-58 illustrate various alternative stages in the manufacture of such an embodiment of a quantum dot device 100, in accordance with various embodiments. In particular, the operations illustrated in FIGS. 54-58 may take the place of the operations illustrated in FIGS. 13-15 with reference to the formation of the gates 106-1/108-1, but the same stages may be used to form the gates 106-1/108-1 instead of or in addition to the gates 106-1/108-1. Similar operations may be used to form variants of the "single-sided" quantum dot device 100 illustrated in FIGS. 32-34.

[0121] FIG. 54 is a cross-sectional view of an assembly 284 subsequent to etching the assembly 212 (FIG. 12) to remove the gate metal 110-1, and the gate dielectric 114-1 that is not protected by the patterned hardmask 116-1, to form the gates 106-1.

[0122] FIG. 55 is a cross-sectional view of an assembly 286 subsequent to providing spacer material 132 on the assembly 284 (FIG. 54). The deposition of the spacer material 132 may take any of the forms discussed above with reference to FIG. 14, for example.

[0123] FIG. 56 is a cross-sectional view of an assembly 288 subsequent to etching the spacer material 132 of the assembly 286 (FIG. 55), leaving spacers 134-1 formed of the spacer material 132 on the sides of the gates 106-1 (e.g., on the sides of the hardmask 116-1, the gate metal 110-1, and the gate dielectric 114-1). The etching of the spacer material 132 may take any of the forms discussed above with reference to FIG. 15, for example.

[0124] FIG. 57 is a cross-sectional view of an assembly 290 subsequent to providing a gate dielectric 114-1 on the fin 104 between the gates 106-1 of the assembly 288 (FIG. 56). In some embodiments, the gate dielectric 114-1 provided between the gates 106-1 of the assembly 288 may be formed by atomic layer deposition (ALD) and, as illustrated in FIG. 57, may cover the exposed fin 104 between the gates 106-1, and may extend onto the adjacent spacers 134-1.

[0125] FIG. 58 is a cross-sectional view of an assembly 292 subsequent to providing the gate metal 112-1 on the assembly 290 (FIG. 57). The gate metal 112-1 may fill the areas between adjacent ones of the gates 106-1, and may extend over the tops of the gates 106-1, as shown. The provision of the gate metal 112-1 may take any of the forms discussed above with reference to FIG. 16, for example. The assembly 256 may be further processed as discussed above with reference to FIGS. 17-31.

[0126] As discussed above with reference to FIGS. 2 and 27, the outer spacers 134-2 on the outer gates 106-2 may provide a doping boundary, limiting diffusion of the dopant from the doped regions 140-2 into the area under the gates 106-2/108-2. In some embodiments, the doped regions 140-2 may extend past the outer spacers 134-2 and under the outer gates 106-2. For example, as illustrated in FIG. 59, the doped region 140-2 may extend past the outer spacers 134-2 and under the outer gates 106-2 by a distance 182 between 0 and 10 nanometers. In some embodiments, the doped regions 140-2 may not extend past the outer spacers 134-2 toward the outer gates 106-2, but may instead "terminate" under the outer spacers 134-2. For example, as illustrated in FIG. 60, the doped regions 140-2 may be spaced away from the interface between the outer spacers 134-2 and the outer gates 106-2 by a distance 184 between 0 and 10 nanometers. The interface material 141-2 is omitted from FIGS. 59 and 60 for ease of illustration.

[0127] As noted above, any suitable techniques may be used to manufacture the quantum dot devices 100 disclosed herein. FIG. 61 is a flow diagram of an illustrative method 1000 of manufacturing a quantum dot device, in accordance with various embodiments. Although the operations discussed below with reference to the method 1000 are illustrated in a particular order and depicted once each, these operations may be repeated or performed in a different order (e.g., in parallel), as suitable. Additionally, various operations may be omitted, as suitable. Various operations of the method 1000 may be illustrated with reference to one or more of the embodiments discussed above, but the method 1000 may be used to manufacture any suitable quantum dot device (including any suitable ones of the embodiments disclosed herein).

[0128] At 1002, a quantum well stack structure may be formed. The quantum well stack structure may be formed at 1002 by providing a base having a surface including a material having a base lattice constant, providing a first layer on the base, wherein the first layer has a first lattice constant that is greater than (less than) the base lattice constant, and providing a second layer on the first layer, wherein the second layer has a second lattice constant that is less than (greater than) the base lattice constant. For example, a quantum well stack structure 146 may be formed by providing a base 144, providing a first layer 153 on the base, and providing a second layer 155 on the first layer 153 (e.g., as discussed above with reference to one or more of FIGS. 35-52).

[0129] At 1004, a plurality of gates may be formed on the quantum well stack structure. For example, gates 106-1 and 108-1 (and, in some embodiments, gates 106-2 and 108-2) may be formed proximate to the quantum well layer 152-1 (e.g., as discussed above with reference to one or more of FIGS. 11-20, 25, and 54-58).

[0130] A number of techniques are disclosed herein for operating a quantum dot device 100. FIGS. 62-63 are flow diagrams of particular illustrative methods 1020 and 1040, respectively, of operating a quantum dot device, in accordance with various embodiments. Although the operations discussed below with reference to the methods 1020 and 1040 are illustrated in a particular order and depicted once each, these operations may be repeated or performed in a different order (e.g., in parallel), as suitable. Additionally, various operations may be omitted, as suitable. Various operations of the methods 1020 and 1040 may be illustrated with reference to one or more of the embodiments discussed above, but the methods 1020 and 1040 may be used to operate any suitable quantum dot device (including any suitable ones of the embodiments disclosed herein).

[0131] Turning to the method 1020 of FIG. 62, at 1022, electrical signals may be applied to a first set of gates disposed on a quantum well stack structure to cause one or more first quantum dots to form in the quantum well stack structure, wherein the quantum well stack structure includes an alternating arrangement of one or more compressively strained layers and one or more tensilely strained layers. For example, one or more voltages may be applied to the gates 106-1/108-1 (or 106-2/108-2, in embodiments with multiple such sets of gates 105) on a quantum well stack structure 146 to cause at least one quantum dot 142-1 (or 142-2) to form in the quantum well layer 152-1 (or 152-2).

[0132] At 1024, electrical signals may be applied to a second set of gates disposed on the quantum well stack structure or a different quantum well stack structure to cause one or more second quantum dots to form in the quantum well stack structure or the different quantum well stack structure. For example, in some embodiments in which one or more voltages are applied to the gates 106-1/108-1 to cause at least one quantum dot 142-1 to form in the quantum well layer 152-1 at 1022, at 1024, one or more voltages may be applied to the gates 106-2/108-2 on the quantum well stack structure 146 to cause at least one quantum dot 142-2 to form in the quantum well layer 152-2 (or vice versa). In other embodiments in which one or more voltages are applied to the gates 106-1/108-1 to cause at least one quantum dot 142-1 to form in the quantum well layer 152-1 of a fin 104-1 at 1022, at 1024, one or more voltages may be applied to the gates 106-1/108-1 on a quantum well stack structure 146 in a different fin 104-1 to cause at least one quantum dot 142-1 to form in the quantum well layer of the different fin 104-1. In other embodiments, a fin 104-1 may include gates 106/108 and a single quantum well layer 152 in which a quantum dot 142 is formed at

1022; in some such embodiments, a quantum dot may be formed at 1024 in a different fin 104-2 (e.g., as discussed above with reference to FIGS. 32-34).

[0133] At 1026, quantum states of the first quantum dots may be sensed with the second quantum dots. For example, a quantum state of a quantum dot 142-1 in the quantum well layer 152-1 may be sensed by a quantum dot 142-2 in the quantum well layer 152-2 (or vice versa). In some embodiments, a quantum state of a quantum dot 142 in one fin 104 may be sensed by a quantum dot 142 in another fin 104.

[0134] Turning to the method 1040 of FIG. 63, at 1042, electrical signals may be provided to one or more first gates disposed on a quantum well stack structure to cause a first quantum dot to form in a first quantum well in the quantum well stack structure. The quantum well stack structure may include an alternating arrangement of one or more compressively strained layers and one or more tensilely strained layers. For example, voltages may be applied to some of the gates 106/108 to cause a first quantum dot 142 to form in a quantum well layer 152 in a strain compensation region 156.

[0135] At 1044, electrical signals may be provided to one or more second gates disposed on the quantum well stack structure to cause a second quantum dot to form in a second quantum well in the quantum well stack structure. For example, voltages may be applied to some of the gates 106/108 to cause a second quantum dot 142 to form in the strain compensation region 156.

[0136] At 1046, electrical signals may be provided to one or more third gates disposed on the quantum well stack structure to (1) cause a third quantum dot to form in the quantum well stack structure or (2) provide a potential barrier between the first quantum well and the second quantum well. For example, voltages may be applied to some of the gates 106/108 to (1) cause a third quantum dot 142 to form in the strain compensation region 156. For example, when a first quantum dot 142-1 forms under the gate 108-11 at 1042, and a second quantum dot 142-1 forms under the gate 108-12, a voltage may be applied to the gate 106-12 to (1) cause a third quantum dot 142-1 to form (e.g., when the gate 106-12 acts as a "plunger" gate) or (2) provide a potential barrier between the first quantum dot 142-1 (under the gate 108-11) and the second quantum dot 142-1 (under the gate 108-12) (e.g., when the gate 106-12 acts as a "barrier" gate).

[0137] FIG. 64 is a block diagram of an example quantum computing device 2000 that may include any of the quantum dot devices disclosed herein. A number of components are illustrated in FIG. 64 as included in the quantum computing device 2000, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the quantum computing device 2000 may be attached to one or more printed circuit boards (e.g., a motherboard). In some embodiments, various ones of these

components may be fabricated onto a single system-on-a-chip (SoC) die. Additionally, in various embodiments, the quantum computing device 2000 may not include one or more of the components illustrated in FIG. 64, but the quantum computing device 2000 may include interface circuitry for coupling to the one or more components. For example, the quantum computing device 2000 may not include a display device 2006, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 2006 may be coupled. In another set of examples, the quantum computing device 2000 may not include an audio input device 2024 or an audio output device 2008, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 2024 or audio output device 2008 may be coupled.

[0138] The quantum computing device 2000 may include a processing device 2002 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 2002 may include a quantum processing device 2026 (e.g., one or more quantum processing devices), and a non-quantum processing device 2028 (e.g., one or more non-quantum processing devices). The quantum processing device 2026 may include one or more of the quantum dot devices 100 disclosed herein, and may perform data processing by performing operations on the quantum dots that may be generated in the quantum dot devices 100, and monitoring the result of those operations. For example, as discussed above, different quantum dots may be allowed to interact, the quantum states of different quantum dots may be set or transformed, and the quantum states of quantum dots may be read (e.g., by another quantum dot). The quantum processing device 2026 may be a universal quantum processor, or specialized quantum processor configured to run one or more particular quantum algorithms. In some embodiments, the quantum processing device 2026 may execute algorithms that are particularly suitable for quantum computers, such as cryptographic algorithms that utilize prime factorization, encryption/decryption, algorithms to optimize chemical reactions, algorithms to model protein folding, etc. The quantum processing device 2026 may also include support circuitry to support the processing capability of the quantum processing device 2026, such as input/output channels, multiplexers, signal mixers, quantum amplifiers, and analog-to-digital converters.

[0139] As noted above, the processing device 2002 may include a non-quantum processing device 2028. In some embodiments, the non-quantum processing device 2028 may provide peripheral logic to support the operation of the quantum processing device 2026. For example, the non-quantum processing device 2028 may control the performance of a read operation, control the performance

of a write operation, control the clearing of quantum bits, etc. The non-quantum processing device 2028 may also perform conventional computing functions to supplement the computing functions provided by the quantum processing device 2026. For example, the non-quantum processing device 2028 may interface with one or more of the other components of the quantum computing device 2000 (e.g., the communication chip 2012 discussed below, the display device 2006 discussed below, etc.) in a conventional manner, and may serve as an interface between the quantum processing device 2026 and conventional components. The non-quantum processing device 2028 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices.

[0140] The quantum computing device 2000 may include a memory 2004, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the states of qubits in the quantum processing device 2026 may be read and stored in the memory 2004. In some embodiments, the memory 2004 may include memory that shares a die with the non-quantum processing device 2028. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random-access memory (STT-MRAM).

[0141] The quantum computing device 2000 may include a cooling apparatus 2030. The cooling apparatus 2030 may maintain the quantum processing device 2026 at a predetermined low temperature during operation to reduce the effects of scattering in the quantum processing device 2026. This predetermined low temperature may vary depending on the setting; in some embodiments, the temperature may be 5 degrees Kelvin or less. In some embodiments, the non-quantum processing device 2028 (and various other components of the quantum computing device 2000) may not be cooled by the cooling apparatus 2030, and may instead operate at room temperature. The cooling apparatus 2030 may be, for example, a dilution refrigerator, a helium-3 refrigerator, or a liquid helium refrigerator.

[0142] In some embodiments, the quantum computing device 2000 may include a communication chip 2012 (e.g., one or more communication chips). For example, the communication chip 2012 may be configured for managing wireless communications for the transfer of data to and from the quantum computing device 2000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid

medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0143] The communication chip 2012 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 1402.11 family), IEEE 1402.16 standards (e.g., IEEE 1402.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 1402.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 1402.16 standards. The communication chip 2012 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 2012 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 2012 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 2012 may operate in accordance with other wireless protocols in other embodiments. The quantum computing device 2000 may include an antenna 2022 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0144] In some embodiments, the communication chip 2012 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 2012 may include multiple communication chips. For instance, a first communication chip 2012 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 2012 may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 2012 may be dedicated to wireless communications, and a second communication chip 2012 may be dedicated to wired communications.

[0145] The quantum computing device 2000 may include battery/power circuitry 2014. The battery/power circuitry 2014 may include one or more energy storage devices (e.g., batteries or

capacitors) and/or circuitry for coupling components of the quantum computing device 2000 to an energy source separate from the quantum computing device 2000 (e.g., AC line power).

[0146] The quantum computing device 2000 may include a display device 2006 (or corresponding interface circuitry, as discussed above). The display device 2006 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0147] The quantum computing device 2000 may include an audio output device 2008 (or corresponding interface circuitry, as discussed above). The audio output device 2008 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0148] The quantum computing device 2000 may include an audio input device 2024 (or corresponding interface circuitry, as discussed above). The audio input device 2024 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0149] The quantum computing device 2000 may include a global positioning system (GPS) device 2018 (or corresponding interface circuitry, as discussed above). The GPS device 2018 may be in communication with a satellite-based system and may receive a location of the quantum computing device 2000, as known in the art.

[0150] The quantum computing device 2000 may include an other output device 2010 (or corresponding interface circuitry, as discussed above). Examples of the other output device 2010 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0151] The quantum computing device 2000 may include an other input device 2020 (or corresponding interface circuitry, as discussed above). Examples of the other input device 2020 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0152] The quantum computing device 2000, or a subset of its components, may have any appropriate form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device.

[0153] Although various ones of the embodiments illustrated in the accompanying drawings may include exactly two quantum well layers 152, this is simply for illustrative purposes, and any of the quantum dot devices 100 (or associated methods or devices) discussed herein may include three or more quantum well layers 152, in accordance with the teachings of the present disclosure. Thus, various ones of the quantum dot devices 100 disclosed herein may be regarded as stacked quantum well structures including two or more quantum well layers 152. For example, a double quantum well structure in a quantum dot device 100 may include two or more quantum well layers 152.

[0154] The following paragraphs provide examples of various ones of the embodiments disclosed herein.

[0155] Example 1 is a quantum dot device, including: a quantum well stack structure including a base, a first strained layer, and a second strained layer, wherein the first strained layer is disposed between the base and the second strained layer, and the first and second strained layers are oppositely strained; and a plurality of gates disposed on the quantum well stack structure.

[0156] Example 2 may include the subject matter of Example 1, and may further specify that the base includes a substrate and a buffer layer, and the buffer layer is disposed between the substrate and the first strained layer.

[0157] Example 3 may include the subject matter of Example 2, and may further specify that the buffer layer is an epitaxial layer.

[0158] Example 4 may include the subject matter of any of Examples 2-3, and may further specify that the buffer layer includes Si_xGe_{1-x}.

[0159] Example 5 may include the subject matter of Example 4, and may further specify that the first strained layer includes Si_yGe_{1-y}, where $x>y$.

[0160] Example 6 may include the subject matter of Example 5, and may further specify that the second strained layer includes intrinsic silicon.

[0161] Example 7 may include the subject matter of Example 4, and may further specify that the first strained layer includes Si_yGe_{1-y}, wherein $x<y$.

[0162] Example 8 may include the subject matter of Example 7, and may further specify that the second strained layer includes intrinsic germanium.

[0163] Example 9 may include the subject matter of any of Examples 2-8, and may further specify that the substrate includes a portion of a silicon wafer.

[0164] Example 10 may include the subject matter of any of Examples 1-9, and may further specify that the quantum well stack structure further includes a buffer layer arranged such that the first and second strained layers are disposed between the buffer layer and the base.

[0165] Example 11 may include the subject matter of Example 10, and may further specify that the buffer layer includes silicon germanium.

[0166] Example 12 may include the subject matter of any of Examples 10-11, and may further specify that the buffer layer is unstrained.

[0167] Example 13 may include the subject matter of any of Examples 1-12, and may further specify that the first strained layer is one of a plurality of first strained layers, the second strained layer is one of a plurality of second strained layers, the plurality of first strained layers are oppositely strained from the plurality of second strained layers, and the plurality of first strained layers are alternatingly arranged with the plurality of second strained layers in the quantum well stack structure.

[0168] Example 14 may include the subject matter of Example 13, and may further specify that at least one of the first strained layers or the second strained layers is a quantum well layer.

[0169] Example 15 may include the subject matter of Example 14, and may further specify that at least two of the first strained layers or the second strained layers is a quantum well layer.

[0170] Example 16 may include the subject matter of any of Examples 14-15, and may further include conductive vias in conductive contact with the at least one quantum well layer.

[0171] Example 17 may include the subject matter of any of Examples 1-16, and may further specify that the first strained layer and the second strained layer have thicknesses below their respective critical thicknesses.

[0172] Example 18 may include the subject matter of any of Examples 1-17, and may further specify that the first strained layer has a first lattice constant, and the second strained layer has a second lattice constant different from the first lattice constant.

[0173] Example 19 may include the subject matter of Example 18, and may further specify that the first strained layer is in contact with a surface of the base, the surface of the base includes a material having a base lattice constant, and the first lattice constant is different from the base lattice constant.

[0174] Example 20 may include the subject matter of Example 19, and may further specify that the first lattice constant is less than the base lattice constant, and the second lattice constant is greater than the base lattice constant.

[0175] Example 21 may include the subject matter of Example 19, and may further specify that the first lattice constant is greater than the base lattice constant, and the second lattice constant is less than the first lattice constant.

[0176] Example 22 may include the subject matter of any of Examples 1-21, and may further specify that at least two gates of the plurality of gates are spaced apart by spacer material.

[0177] Example 23 may include the subject matter of any of Examples 1-22, and may further specify that each gate includes a gate electrode and a gate dielectric disposed between the gate electrode and the quantum well stack structure.

[0178] Example 24 may include the subject matter of any of Examples 1-23, and may further specify that the quantum well stack structure includes at least first and second quantum well layers with a barrier layer disposed therebetween, the plurality of gates includes a first set of gates arranged such that the first quantum well layer is disposed between the first set of gates and the barrier layer, and the plurality of gates includes a second set of gates arranged such that the second quantum well layer is disposed between the second set of gates and the barrier layer.

[0179] Example 25 may include the subject matter of any of Examples 1-24, and may further specify that the first and second strained layers are included in a fin.

[0180] Example 26 may include the subject matter of Example 25, and may further include insulating material disposed on opposite faces of the fin.

[0181] Example 27 may include the subject matter of any of Examples 1-26, and may further specify that two adjacent gates of the plurality of gates are spaced apart by a distance between 40 and 60 nanometers.

[0182] Example 28 may include the subject matter of any of Examples 1-27, and may further specify that the base includes a buffer material disposed in a trench, and a bottom of the trench is provided by a first material different from the buffer material.

[0183] Example 29 may include the subject matter of Example 28, and may further specify that the first and second strained layers are disposed in the trench.

[0184] Example 30 may include the subject matter of Example 28, and may further specify that the first and second strained layers are disposed outside of the trench.

[0185] Example 31 may include the subject matter of any of Examples 1-30, and may further include doped regions in the quantum well stack structure.

[0186] Example 32 is a method of operating a quantum dot device, including: providing electrical signals to one or more first gates disposed on a quantum well stack structure to cause a first quantum dot to form in a first quantum well in the quantum well stack structure, wherein the quantum well stack structure includes an alternating arrangement of one or more compressively strained layers and one or more tensilely strained layers; providing electrical signals to one or more second gates disposed on the quantum well stack structure to cause a second quantum dot to form in a second quantum well in the quantum well stack structure; and providing electrical signals to one or more third gates disposed on the quantum well stack structure to (1) cause a third quantum dot

to form in a third quantum well in the quantum well stack structure or (2) provide a potential barrier between the first quantum well and the second quantum well.

[0187] Example 33 may include the subject matter of Example 32, and may further specify that adjacent gates on the quantum well stack structure are spaced apart by spacer material.

[0188] Example 34 may include the subject matter of any of Examples 32-33, and may further specify that the first, second, and third gates each include a gate metal and a gate dielectric disposed between the gate metal and the quantum well stack structure.

[0189] Example 35 may include the subject matter of any of Examples 32-34, and may further specify that the quantum well stack structure is a first quantum well stack structure, and the method further includes: providing electrical signals to one or more fourth gates disposed on a second quantum well stack structure to cause a fourth quantum dot to form in a fourth quantum well in the second quantum well stack structure, wherein the second quantum well stack structure includes an alternating arrangement of one or more compressively strained layers and one or more tensilely strained layers, and an insulating material is disposed between the first and second quantum well stack structures; and sensing a quantum state of the first quantum dot with the fourth quantum dot.

[0190] Example 36 may include the subject matter of Example 35, and may further specify that the first and second quantum well stack structures are spaced apart by a minimum distance between 100 and 250 nanometers.

[0191] Example 37 may include the subject matter of any of Examples 32-36, and may further specify that the one or more first gates are disposed proximate to a first face of the quantum well stack structure, and the method further includes applying voltages to one or more fourth gates disposed proximate to a second face of the quantum well stack structure to cause a fourth quantum dot to form in a fourth quantum well in the quantum well stack structure, wherein the second face is opposite to the first face.

[0192] Example 38 may include the subject matter of Example 37, and may further include sensing a quantum state of the first quantum dot with the fourth quantum dot.

[0193] Example 39 is a method of manufacturing a quantum dot device, including: forming a quantum well stack structure by: providing a base having a surface including a material having a base lattice constant, providing a first layer on the base, wherein the first layer has a first lattice constant that is different from the base lattice constant, and providing a second layer on the first layer, wherein the second layer has a second lattice constant, the second lattice constant is less than the base lattice constant when the first lattice constant is greater than the base lattice constant, and the second lattice constant is greater than the base lattice constant when the first lattice constant is

less than the base lattice constant; and forming a plurality of gates on the quantum well stack structure.

[0194] Example 40 may include the subject matter of Example 39, and may further specify that adjacent gates of the plurality of gates are spaced apart by spacer material.

[0195] Example 41 may include the subject matter of any of Examples 39-40, and may further include patterning the quantum well structure prior to forming the plurality of gates.

[0196] Example 42 may include the subject matter of any of Examples 39-42, and may further include doping one or more regions of the quantum well structure.

[0197] Example 43 may include the subject matter of any of Examples 39-42, and may further specify that providing the base includes: providing a second material on a first material;

[0198] forming a trench in the second material, wherein the trench extends down to the first material; and growing a buffer material in the trench.

[0199] Example 44 may include the subject matter of Example 43, and may further specify that the first and second layers are provided in the trench.

[0200] Example 45 may include the subject matter of any of Examples 43-44, and may further include providing additional layers on the second layer, wherein the additional layers alternate having lattice constants greater than or less than the base lattice constant.

[0201] Example 46 may include the subject matter of any of Examples 43-45, and may further specify that the first and second layers are provided by epitaxy.

[0202] Example 47 may include the subject matter of any of Examples 43-46, and may further specify that the first layer or the second layer includes silicon germanium.

[0203] Example 48 may include the subject matter of Example 47, and may further specify that the first layer or the second layer includes intrinsic silicon or intrinsic germanium.

[0204] Example 49 is a quantum computing device, including: a quantum processing device, wherein the quantum processing device includes a quantum well stack structure having a plurality of alternatingly arranged tensilely strained layers and compressively strained layers, and the quantum processing device further includes a plurality of gates disposed on the quantum well stack structure to control quantum dot formation in the quantum well stack structure; a non-quantum processing device, coupled to the quantum processing device, to control voltages applied to the plurality of gates.

[0205] Example 50 may include the subject matter of Example 49, and may further include a memory device to store data generated by quantum dots formed in the quantum well stack structure during operation of the quantum processing device.

[0206] Example 51 may include the subject matter of Example 50, and may further specify that the memory device is to store instructions for a quantum computing algorithm to be executed by the quantum processing device.

[0207] Example 52 may include the subject matter of any of Examples 49-51, and may further include a cooling apparatus to maintain a temperature of the quantum processing device below 5 degrees Kelvin.

[0208] Example 53 may include the subject matter of any of Examples 49-52, and may further specify that quantum dots are formed in at least one of the tensilely strained layers or at least one of the compressively strained layers during operation of the quantum processing device.

Claims:

1. A quantum dot device, comprising:

a quantum well stack structure including a base, a first strained layer, and a second strained layer, wherein the first strained layer is disposed between the base and the second strained layer, and the first and second strained layers are oppositely strained; and

a plurality of gates disposed on the quantum well stack structure.

2. The quantum dot device of claim 1, wherein the base includes a substrate and a buffer layer, and the buffer layer is disposed between the substrate and the first strained layer.

3. The quantum dot device of claim 2, wherein the buffer layer includes Si_xGe_{1-x}.

4. The quantum dot device of claim 2, wherein the substrate includes a portion of a silicon wafer.

5. The quantum dot device of claim 1, wherein the quantum well stack structure further includes a buffer layer arranged such that the first and second strained layers are disposed between the buffer layer and the base.

6. The quantum dot device of claim 1, wherein the first strained layer is one of a plurality of first strained layers, the second strained layer is one of a plurality of second strained layers, the plurality of first strained layers are oppositely strained from the plurality of second strained layers, and the plurality of first strained layers are alternatingly arranged with the plurality of second strained layers in the quantum well stack structure.

7. The quantum dot device of claim 6, wherein at least one of the first strained layers or the second strained layers is a quantum well layer.

8. The quantum dot device of claim 7, wherein at least two of the first strained layers or the second strained layers is a quantum well layer.

9. The quantum dot device of claim 1, wherein the first strained layer and the second strained layer have thicknesses below their respective critical thicknesses.

10. The quantum dot device of claim 1, wherein the first strained layer has a first lattice constant, and the second strained layer has a second lattice constant different from the first lattice constant.

11. The quantum dot device of any of claims 1-10, wherein the quantum well stack structure includes at least first and second quantum well layers with a barrier layer disposed therebetween, the plurality of gates includes a first set of gates arranged such that the first quantum well layer is disposed between the first set of gates and the barrier layer, and the plurality of gates includes a second set of gates arranged such that the second quantum well layer is disposed between the second set of gates and the barrier layer.

12. The quantum dot device of any of claims 1-10, wherein the first and second strained layers are included in a fin.

13. The quantum dot device of any of claims 1-10, wherein the base includes a buffer material disposed in a trench, and a bottom of the trench is provided by a first material different from the buffer material.

14. The quantum dot device of claim 13, wherein the first and second strained layers are disposed in the trench.

15. The quantum dot device of claim 13, wherein the first and second strained layers are disposed outside of the trench.

16. A method of operating a quantum dot device, comprising:

providing electrical signals to one or more first gates disposed on a quantum well stack structure to cause a first quantum dot to form in a first quantum well in the quantum well stack structure, wherein the quantum well stack structure includes an alternating arrangement of one or more compressively strained layers and one or more tensilely strained layers;

providing electrical signals to one or more second gates disposed on the quantum well stack structure to cause a second quantum dot to form in a second quantum well in the quantum well stack structure; and

providing electrical signals to one or more third gates disposed on the quantum well stack structure to (1) cause a third quantum dot to form in a third quantum well in the quantum well stack structure or (2) provide a potential barrier between the first quantum well and the second quantum well.

17. The method of claim 16, wherein adjacent gates on the quantum well stack structure are spaced apart by spacer material.

18. The method of any of claims 16-17, wherein the first, second, and third gates each include a gate metal and a gate dielectric disposed between the gate metal and the quantum well stack structure.

19. A method of manufacturing a quantum dot device, comprising:

forming a quantum well stack structure by:

providing a base having a surface including a material having a base lattice constant,

providing a first layer on the base, wherein the first layer has a first lattice constant that is different from the base lattice constant, and

providing a second layer on the first layer, wherein the second layer has a second lattice constant, the second lattice constant is less than the base lattice constant when the first lattice constant is greater than the base lattice constant, and the second lattice constant is greater than the base lattice constant when the first lattice constant is less than the base lattice constant; and

forming a plurality of gates on the quantum well stack structure.

20. The method of claim 19, wherein providing the base includes:

providing a second material on a first material;

forming a trench in the second material, wherein the trench extends down to the first material; and

growing a buffer material in the trench.

21. The method of claim 20, wherein the first and second layers are provided in the trench.

22. The method of claim 20, further comprising:

providing additional layers on the second layer, wherein the additional layers alternate having lattice constants greater than or less than the base lattice constant.

23. A quantum computing device, comprising:

a quantum processing device, wherein the quantum processing device includes a quantum well stack structure having a plurality of alternatingly arranged tensilely strained layers and compressively strained layers, and the quantum processing device further includes a plurality of gates disposed on the quantum well stack structure to control quantum dot formation in the quantum well stack structure;

a non-quantum processing device, coupled to the quantum processing device, to control voltages applied to the plurality of gates.

24. The quantum computing device of claim 23, further comprising:

a memory device to store data generated by quantum dots formed in the quantum well stack structure during operation of the quantum processing device.

25. The quantum computing device of any of claims 23-24, wherein quantum dots are formed in at least one of the tensilely strained layers or at least one of the compressively strained layers during operation of the quantum processing device.

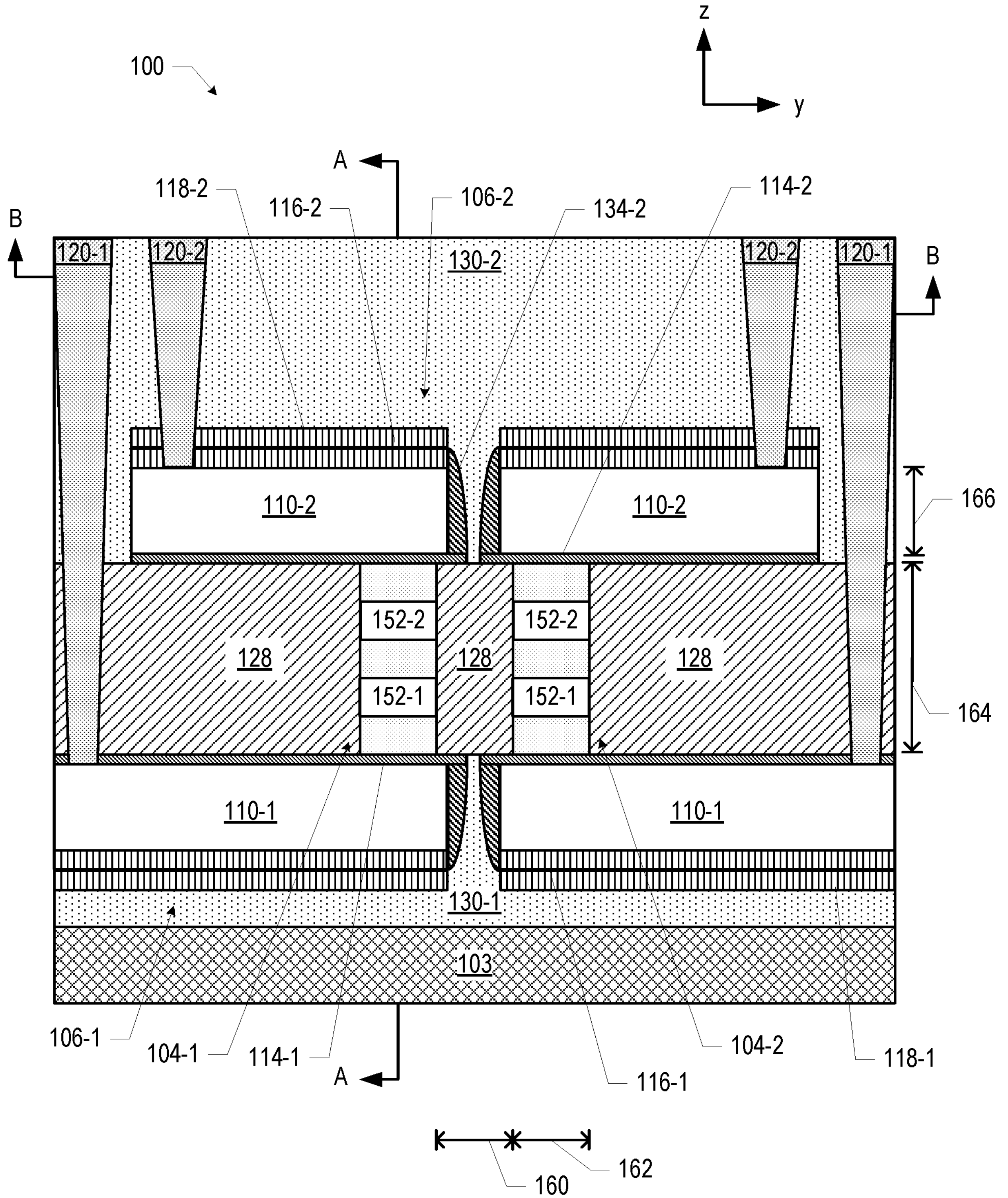

FIG. 1

100
118-2
142-2
105-2
141-2
130-2
106-21
108-21
116-2
106-22
108-22
141-1
107
134-2
114-2
106-23
107
136-1 136-2 120-2 122-2 120-2 122-2 120-2 136-2 136-1
110-2 112-2 110-2 112-2 110-2
140-2 152-2 140-2
140-1 152-1 140-1
110-1 112-1 110-1 112-1 110-1
130-1
103
104
108-11
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z
x

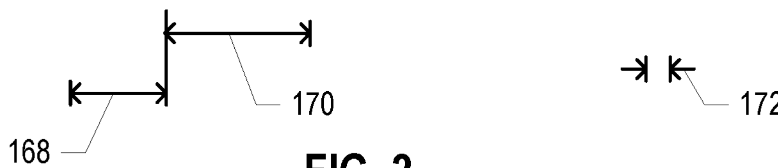


FIG. 2

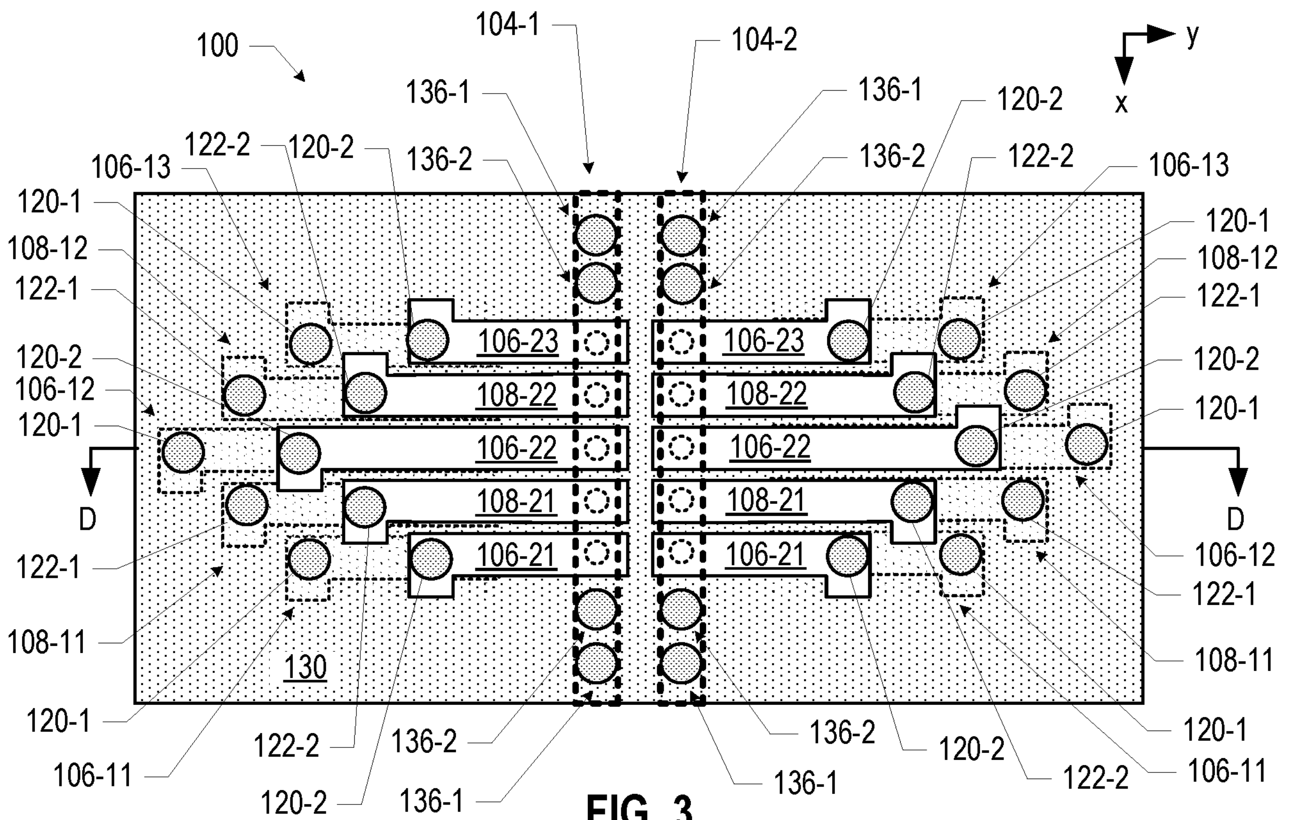


FIG. 3

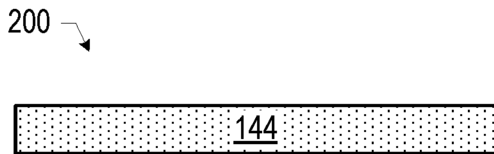


FIG. 4

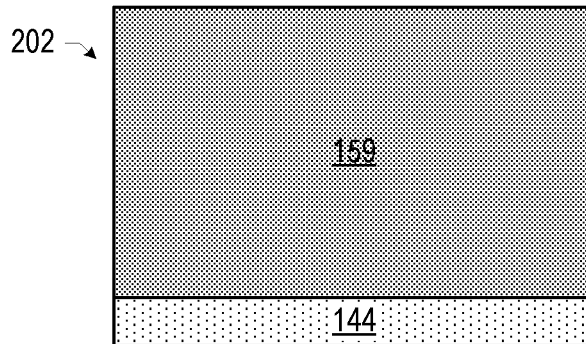


FIG. 5

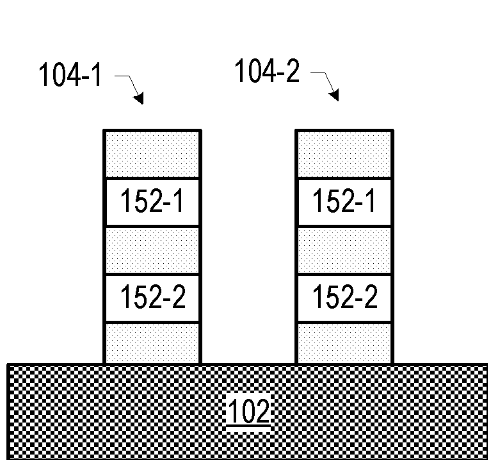


FIG. 6

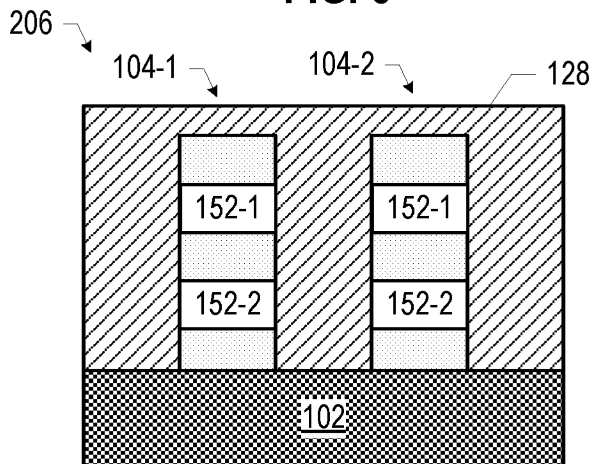


FIG. 7

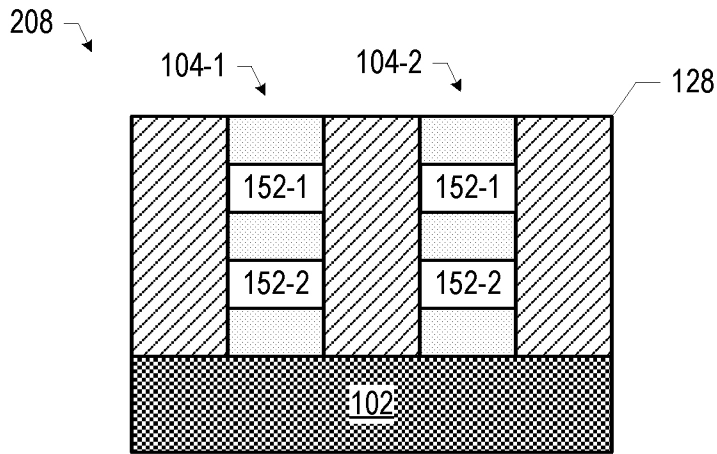


FIG. 8

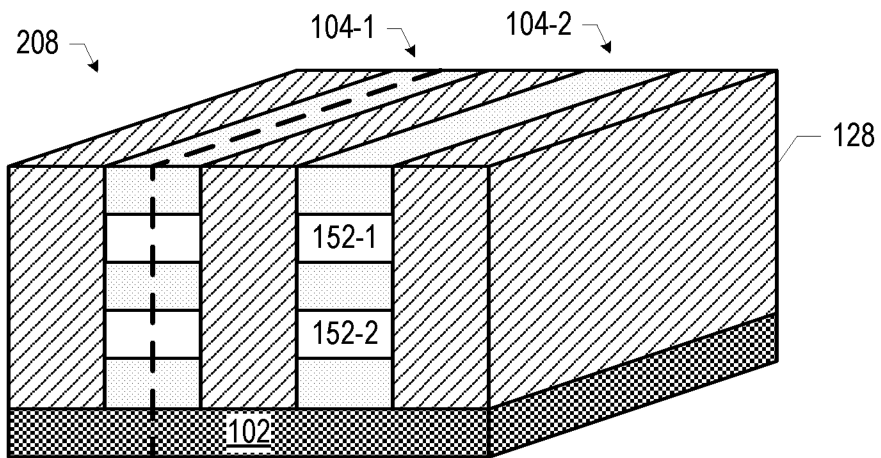


FIG. 9

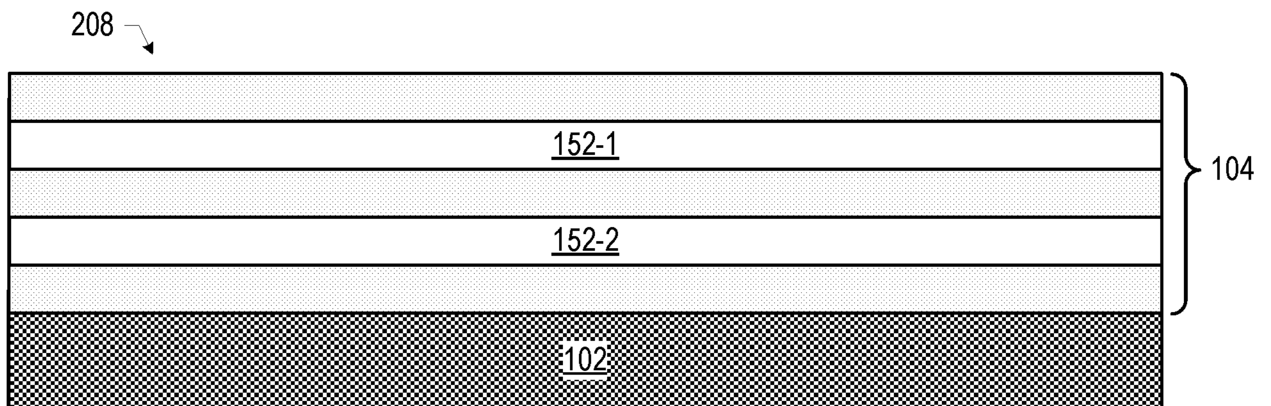


FIG. 10

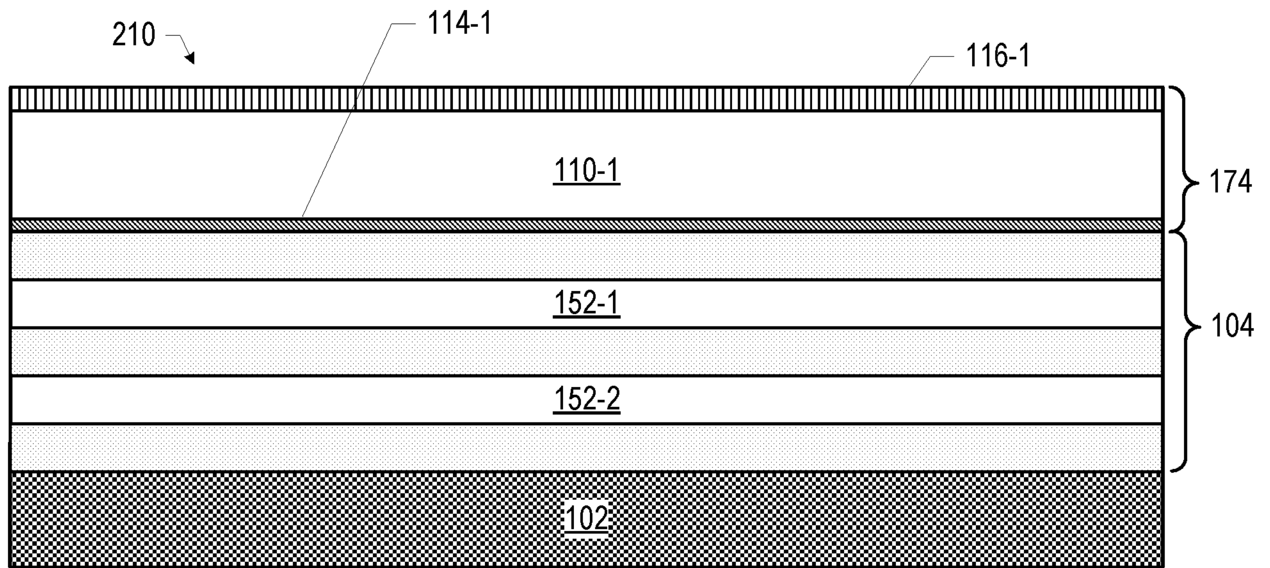


FIG. 11

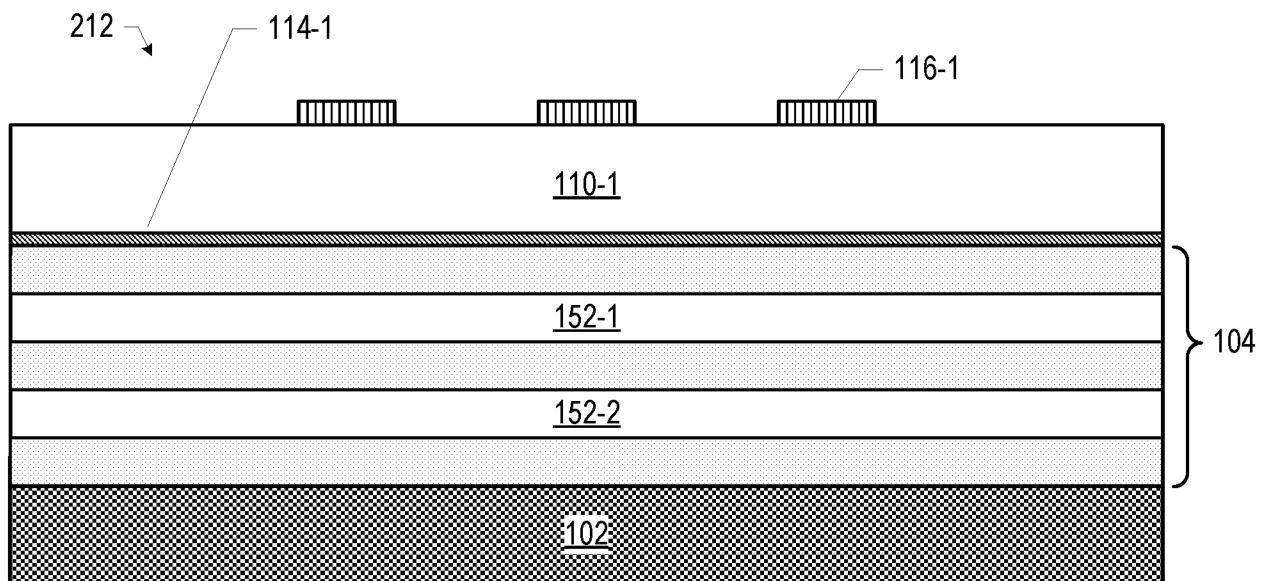


FIG. 12

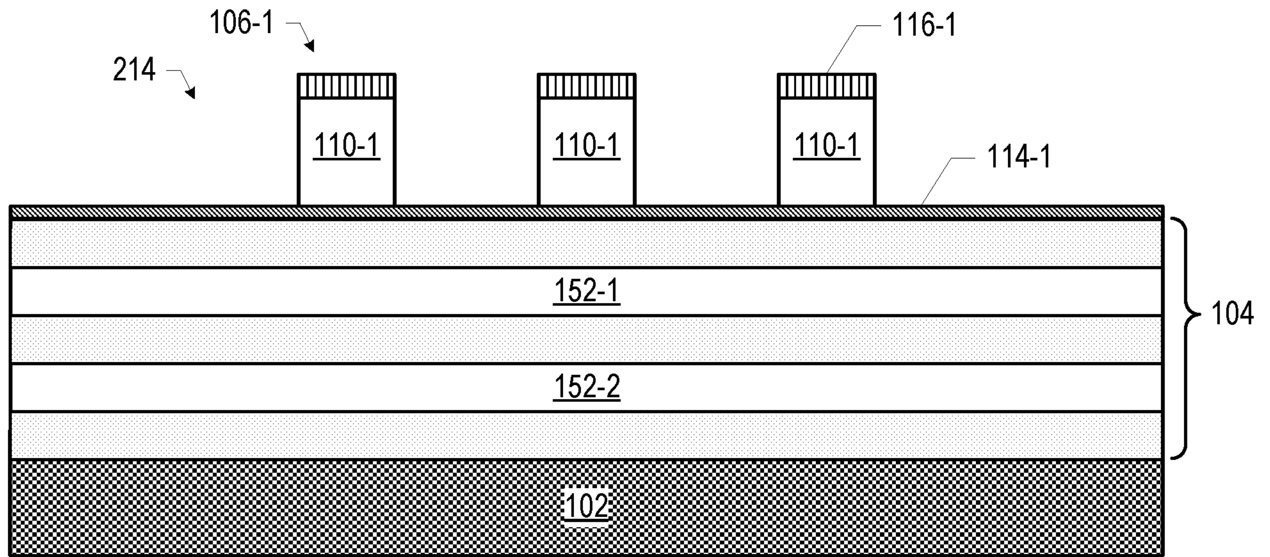


FIG. 13

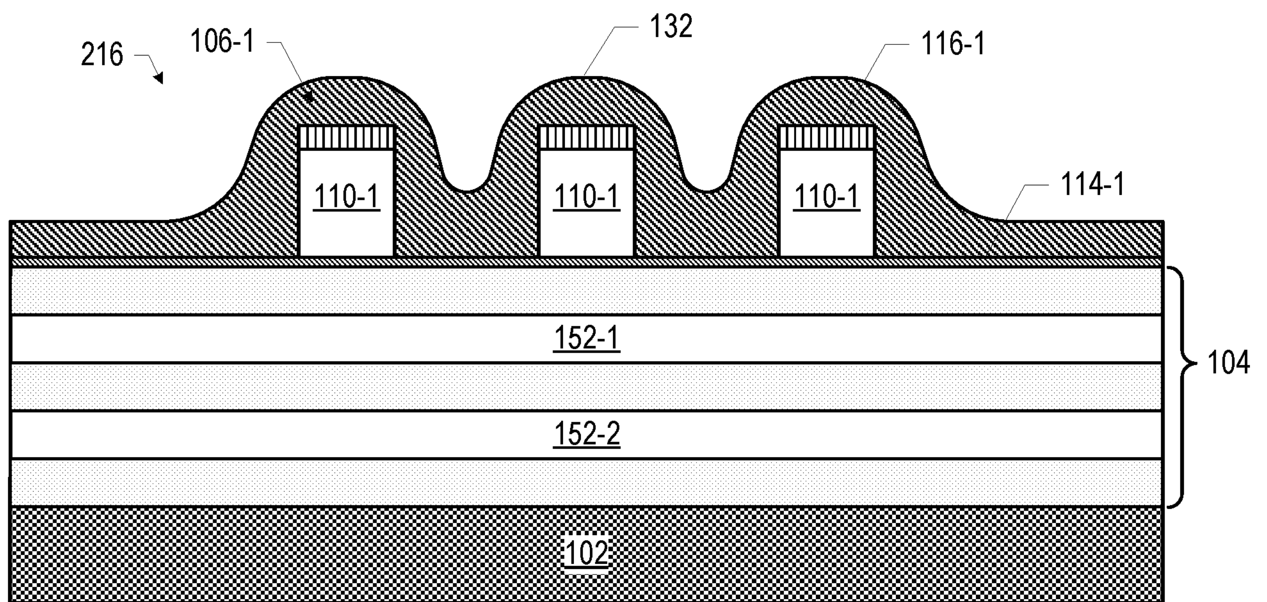


FIG. 14

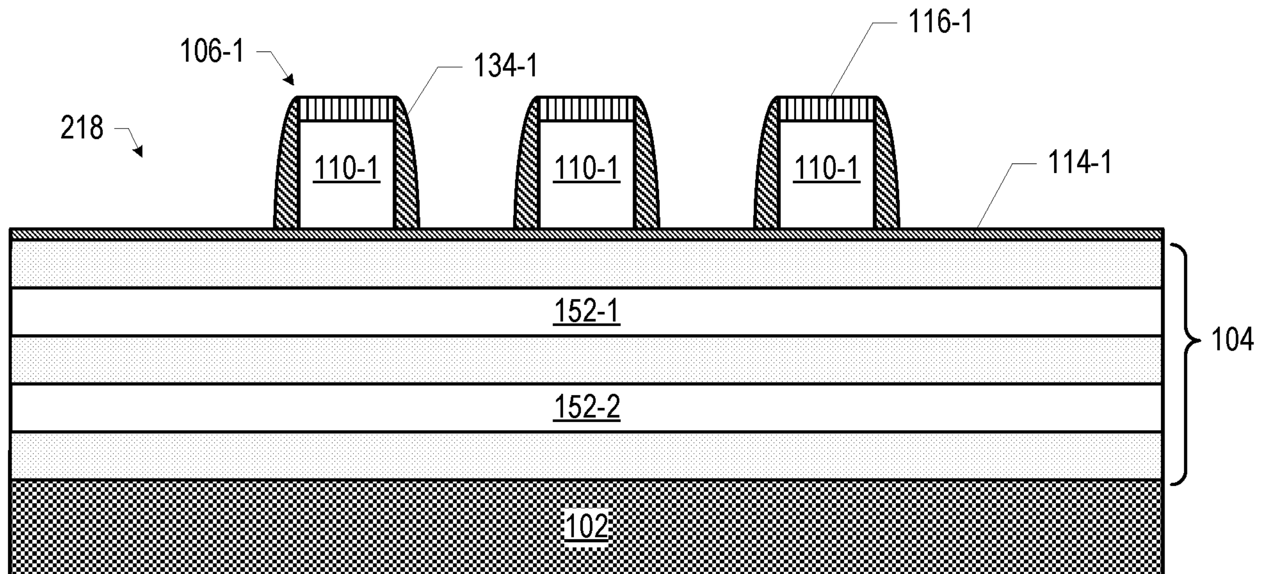


FIG. 15

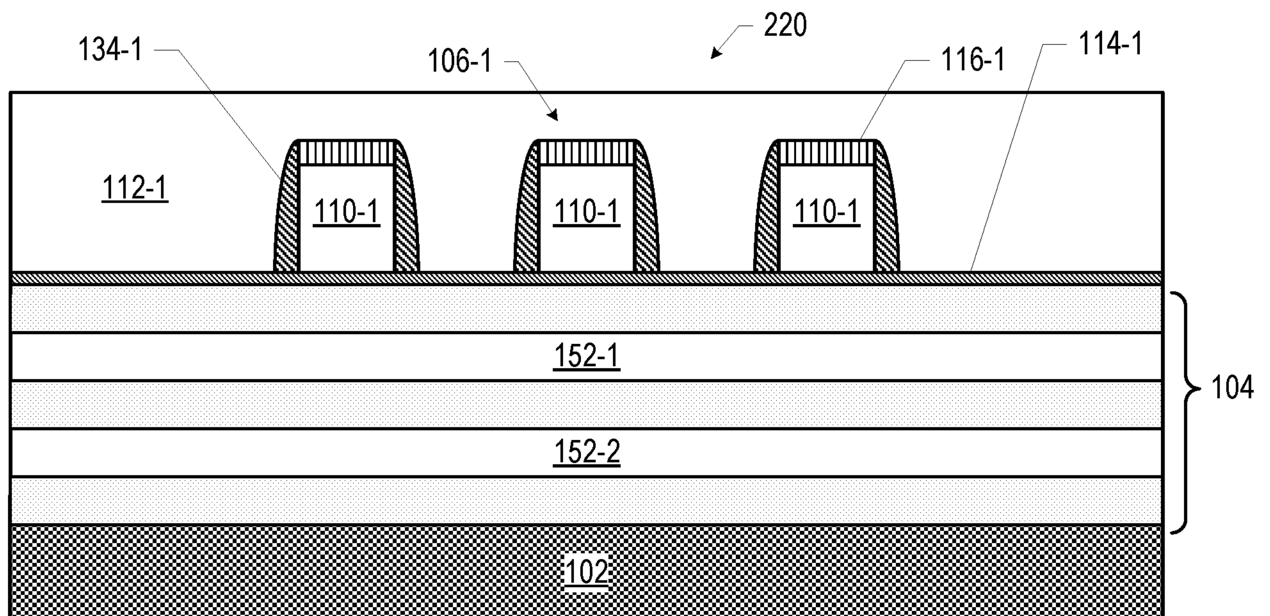


FIG. 16

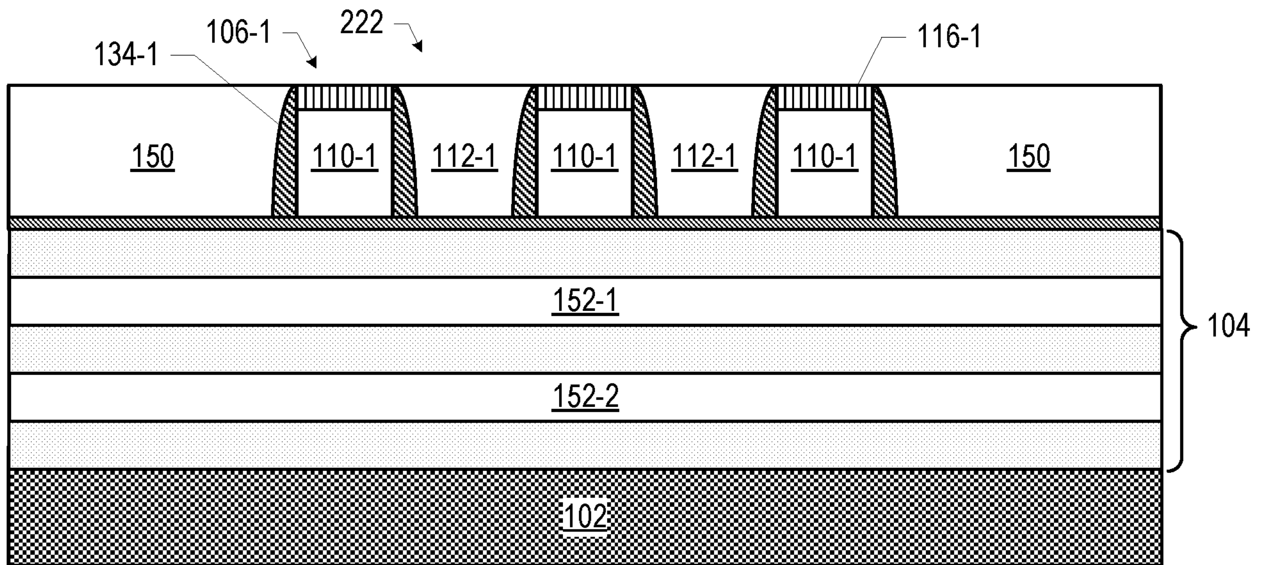


FIG. 17

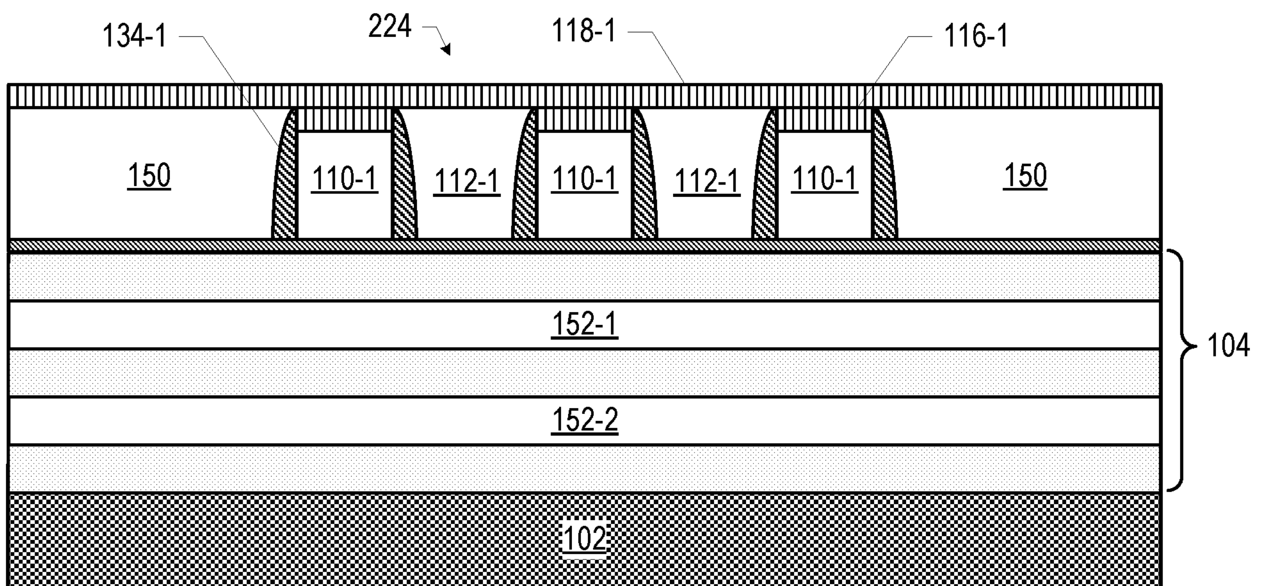


FIG. 18

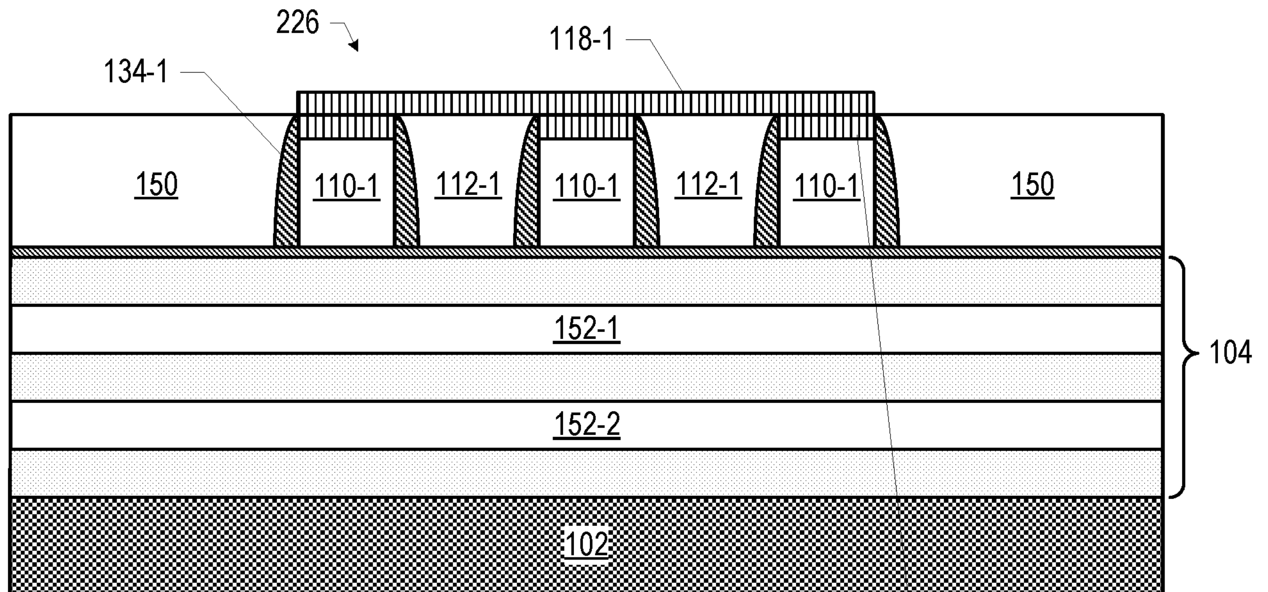


FIG. 19

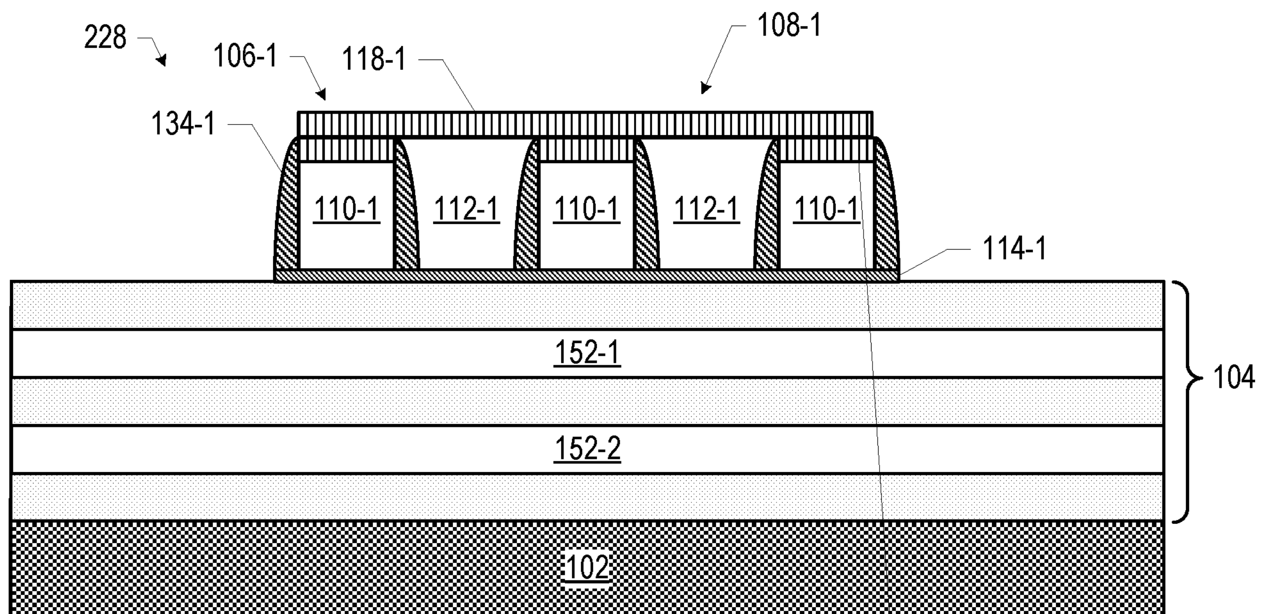


FIG. 20

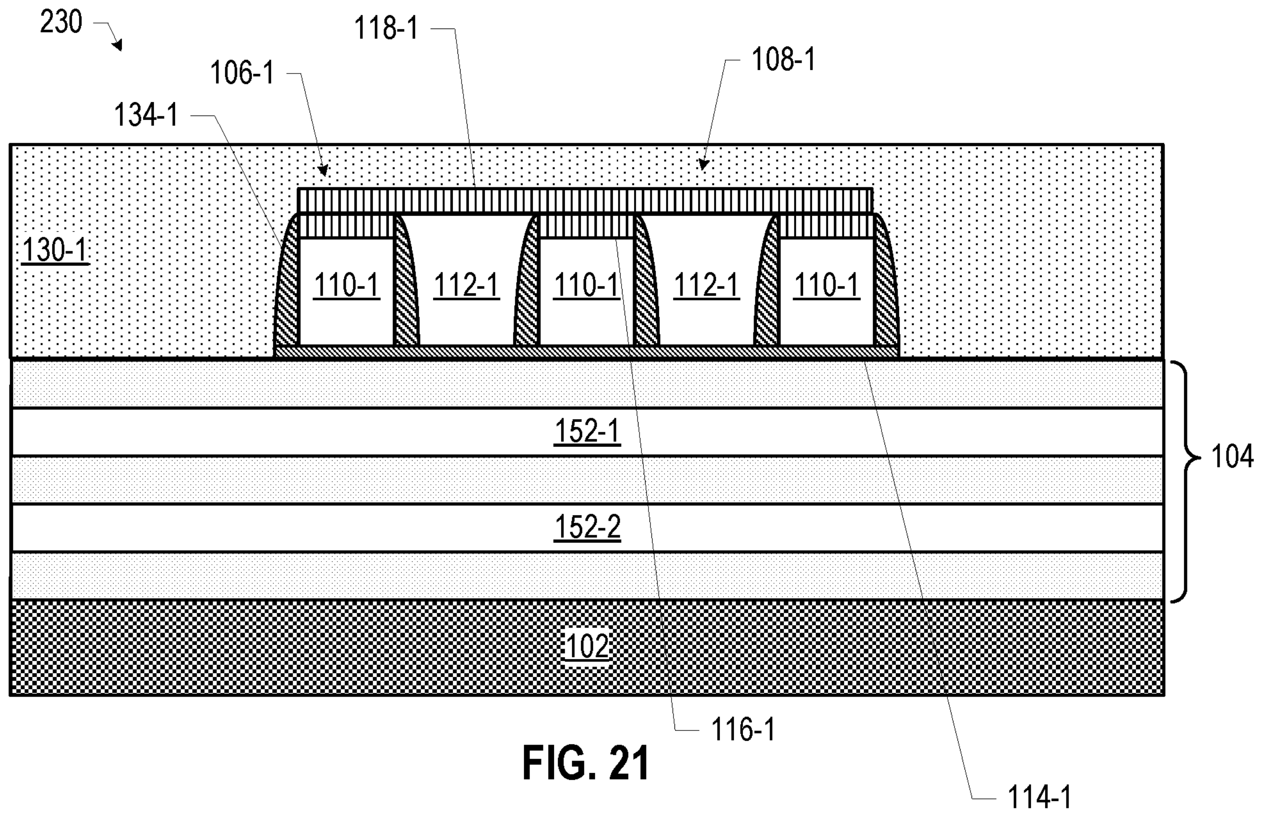


FIG. 21

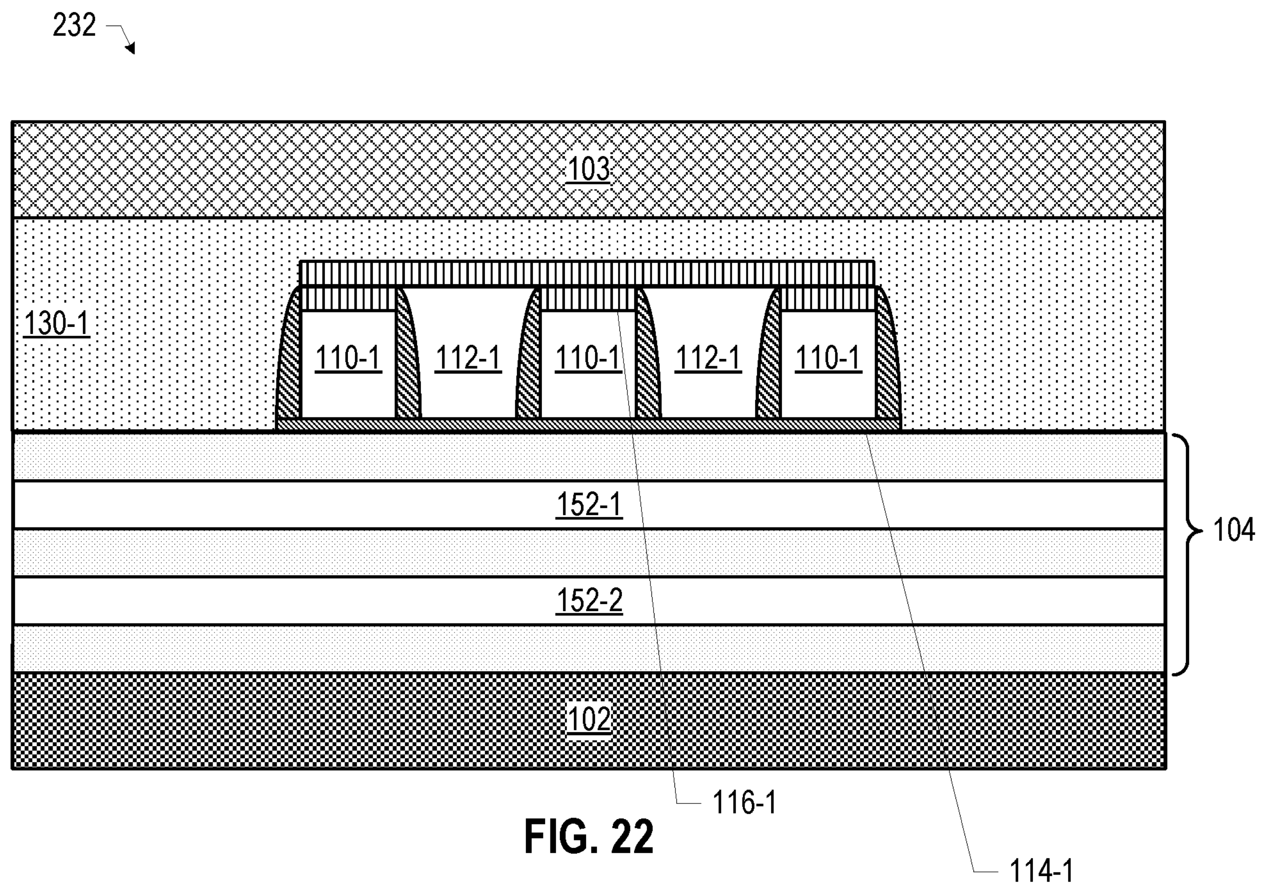


FIG. 22

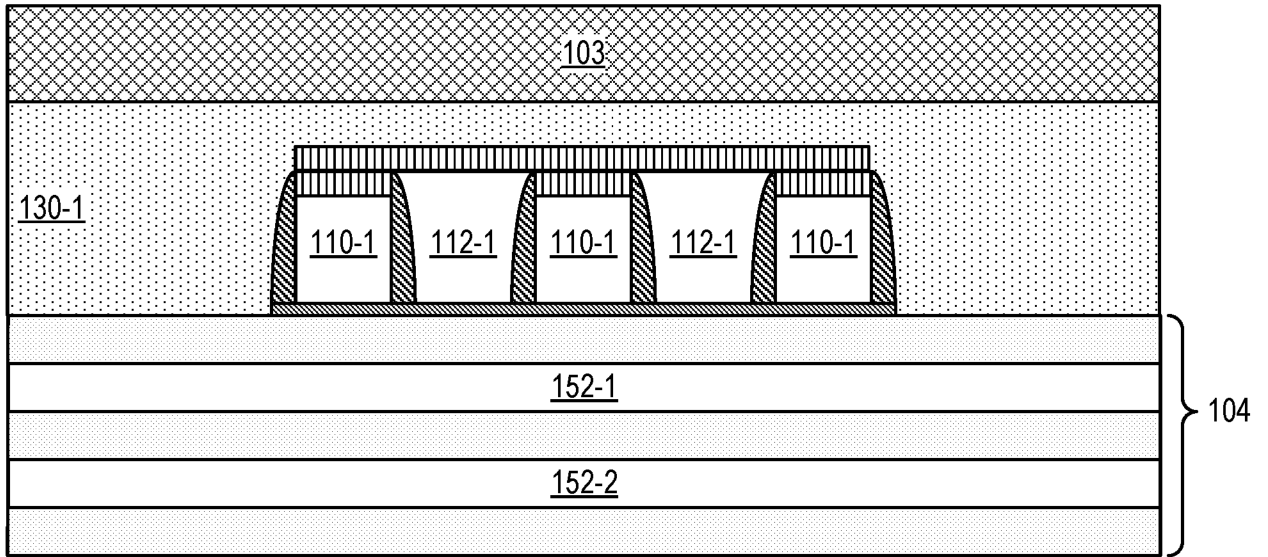


FIG. 23

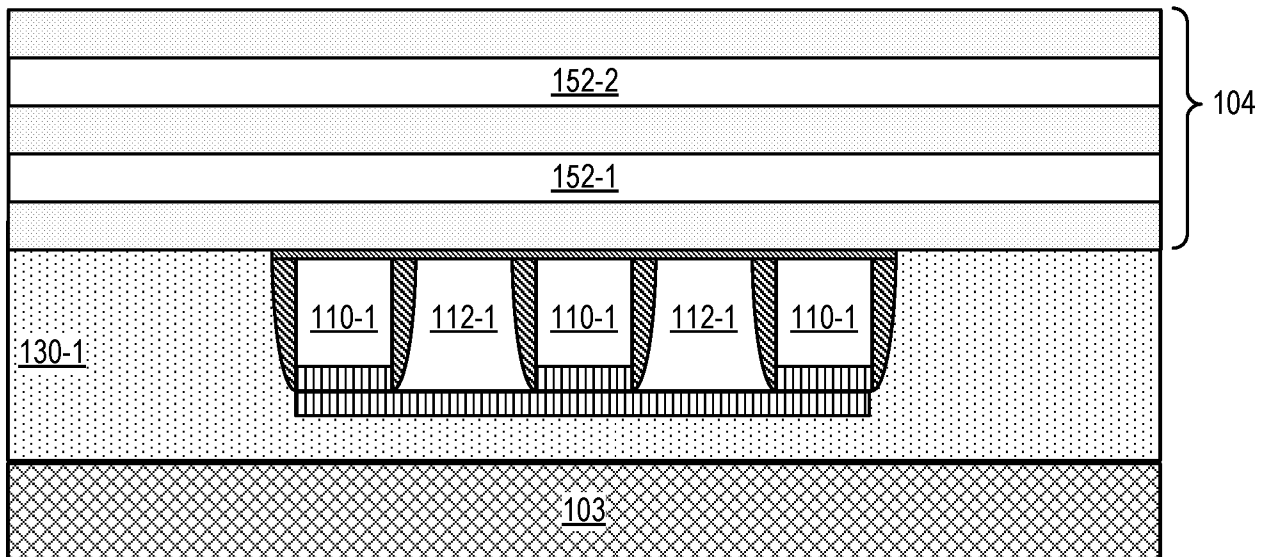


FIG. 24

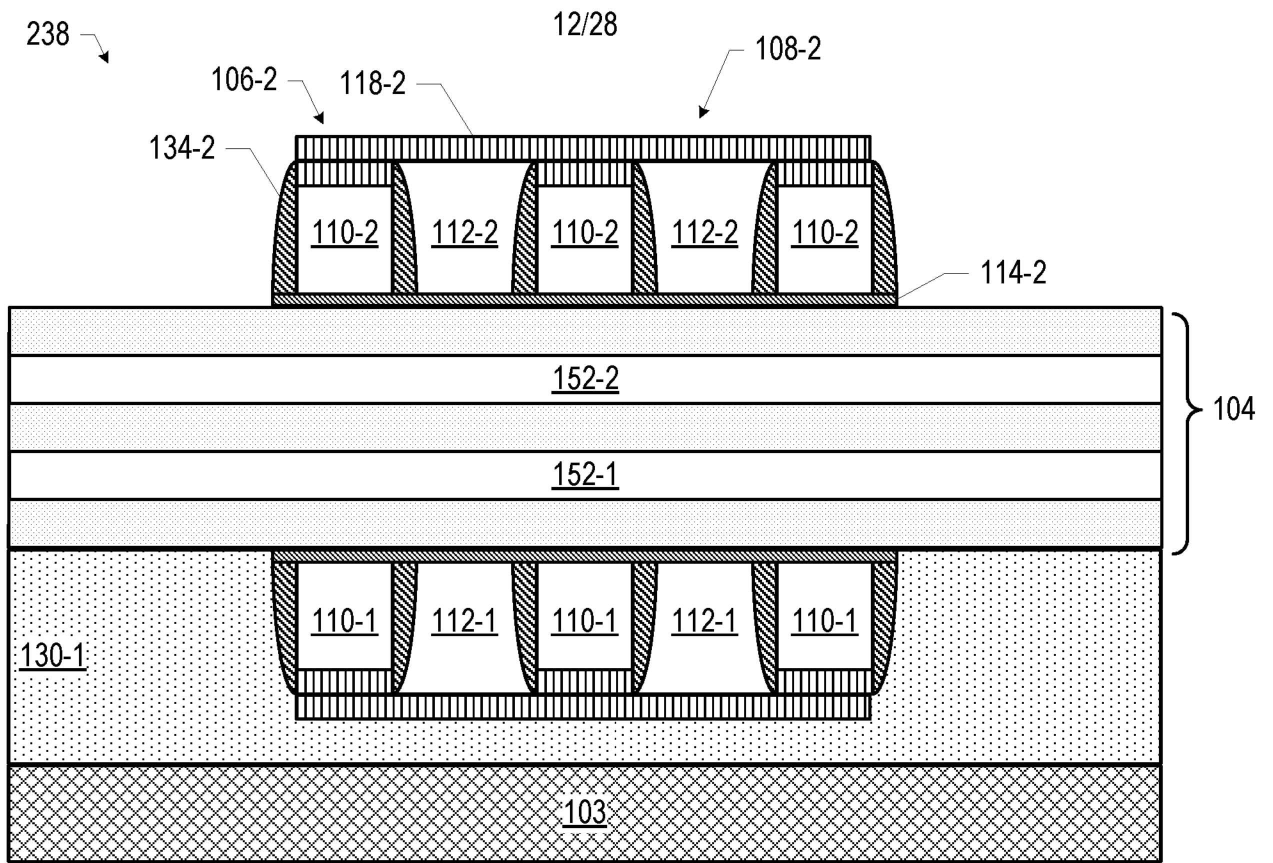


FIG. 25

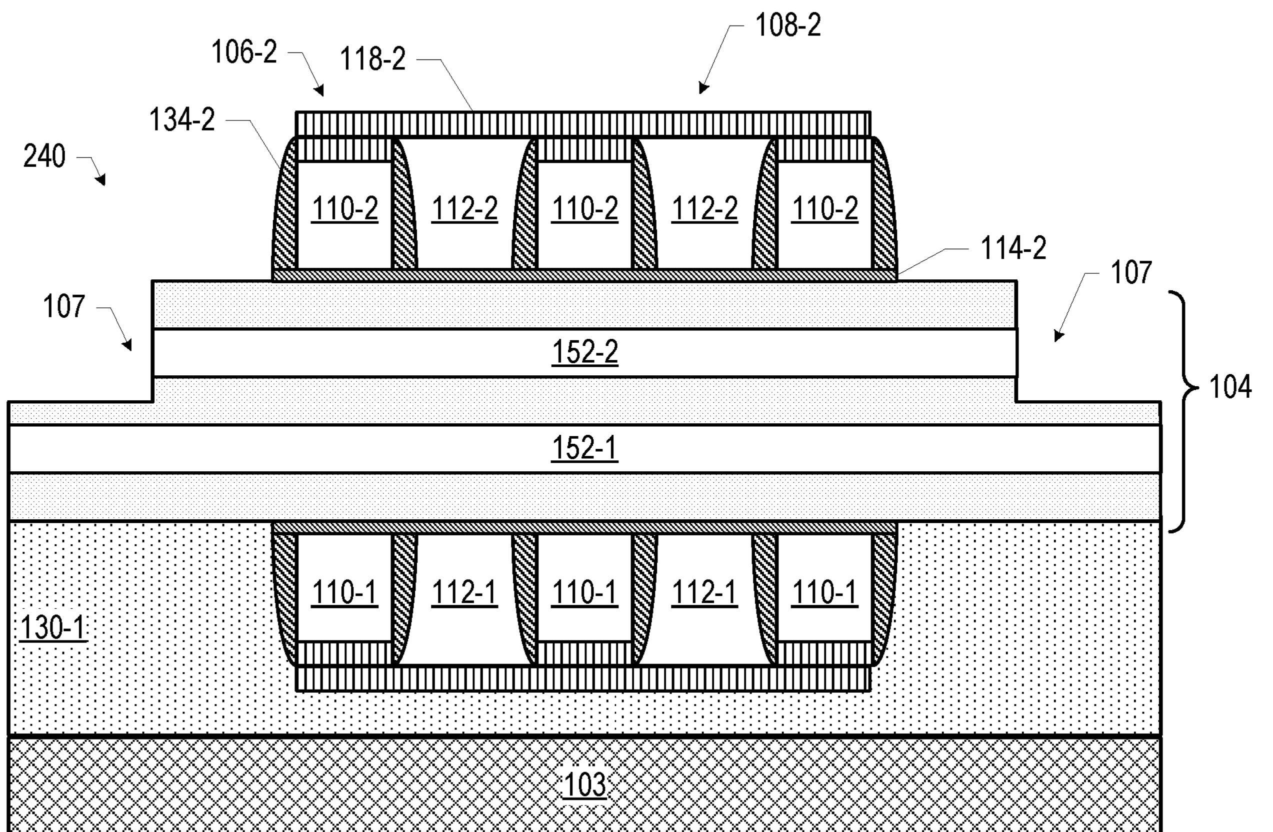


FIG. 26

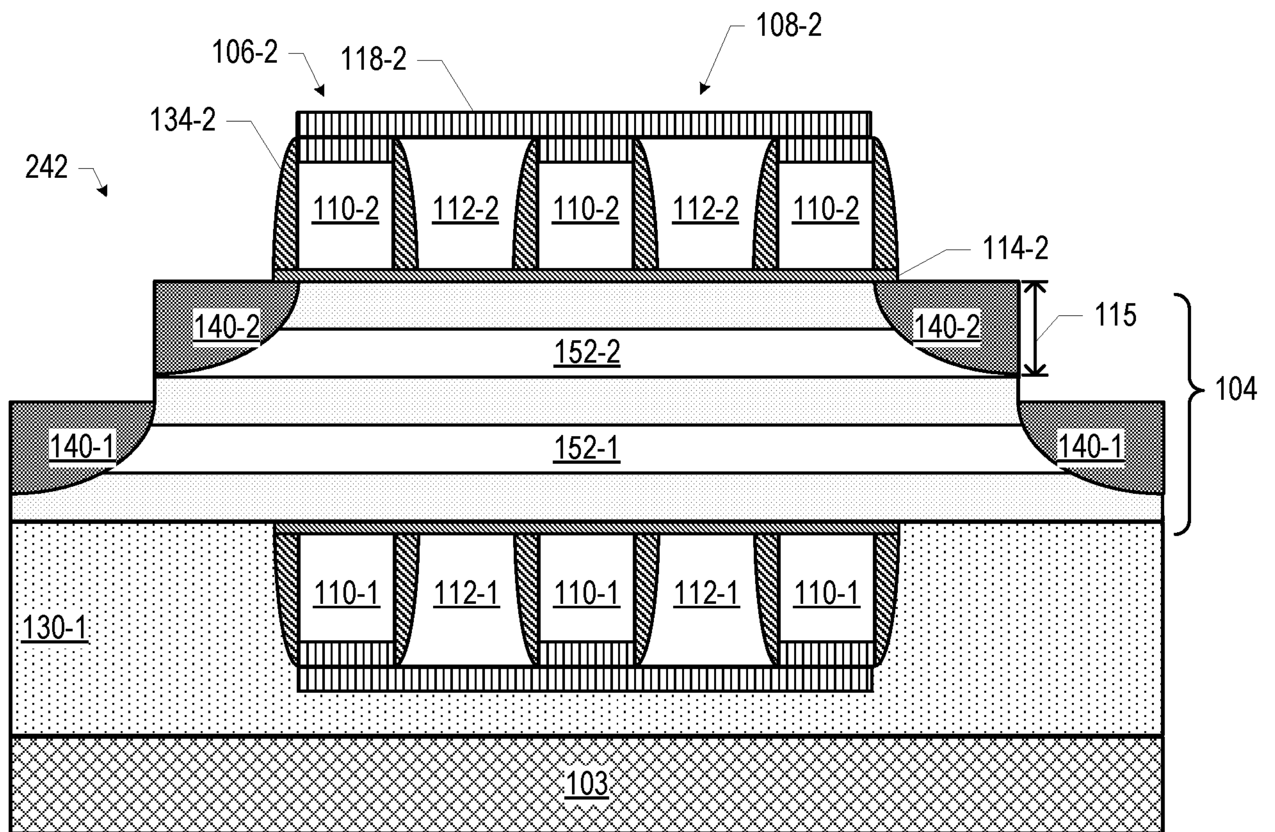


FIG. 27

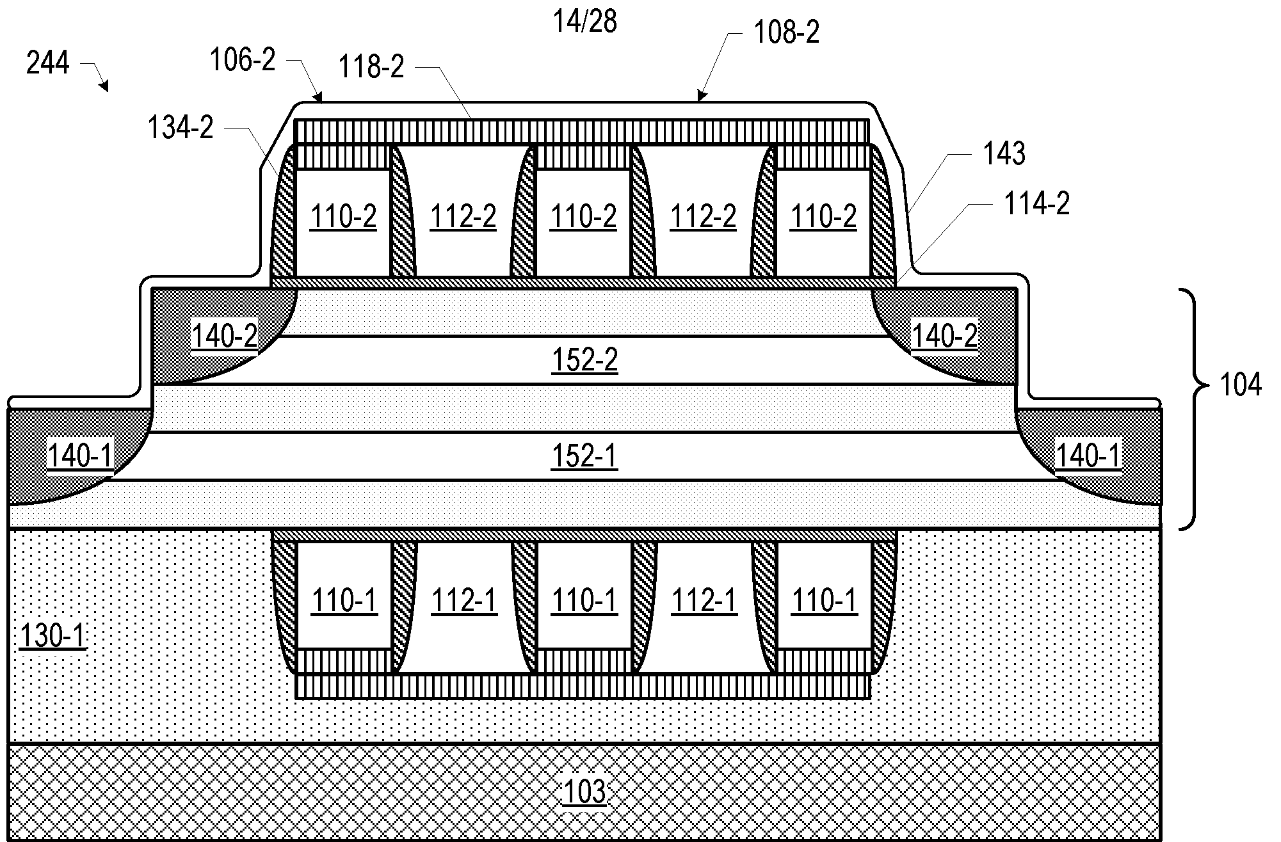


FIG. 28

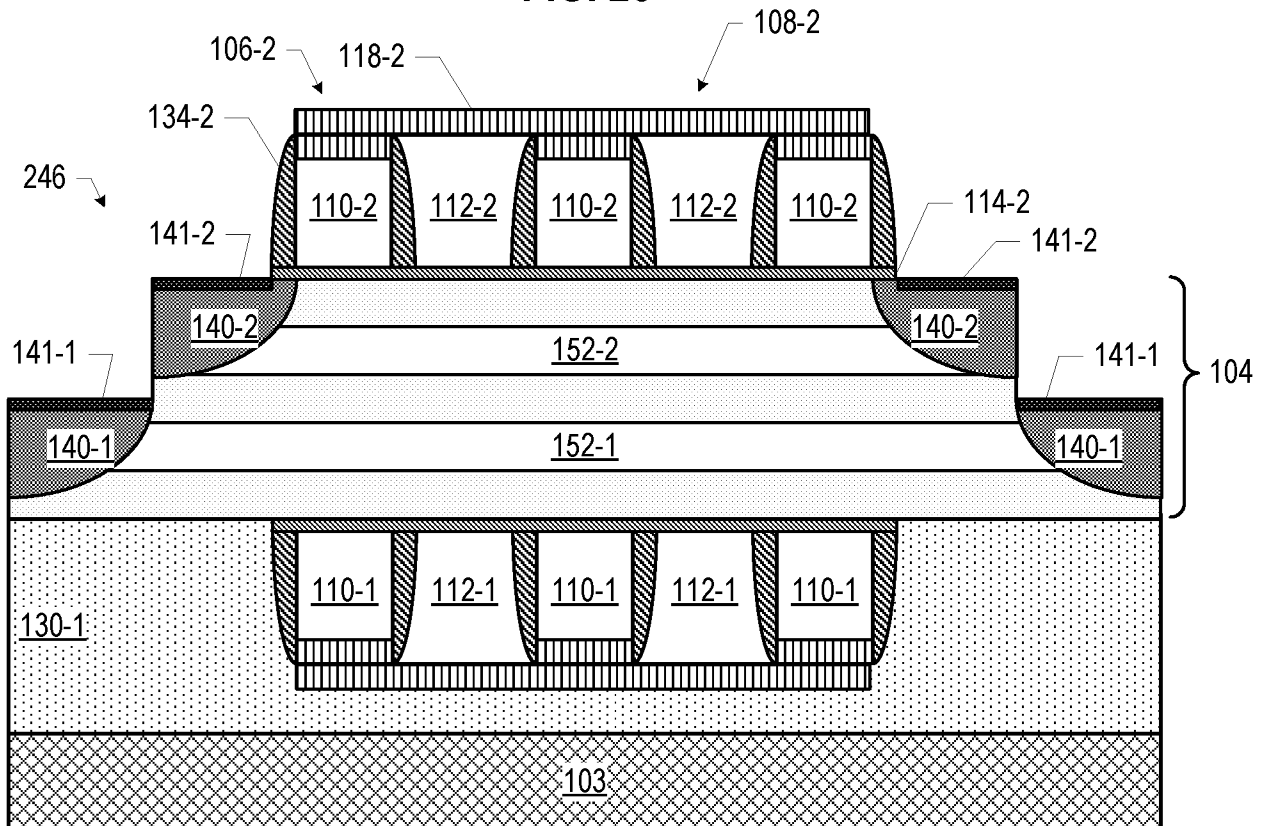


FIG. 29

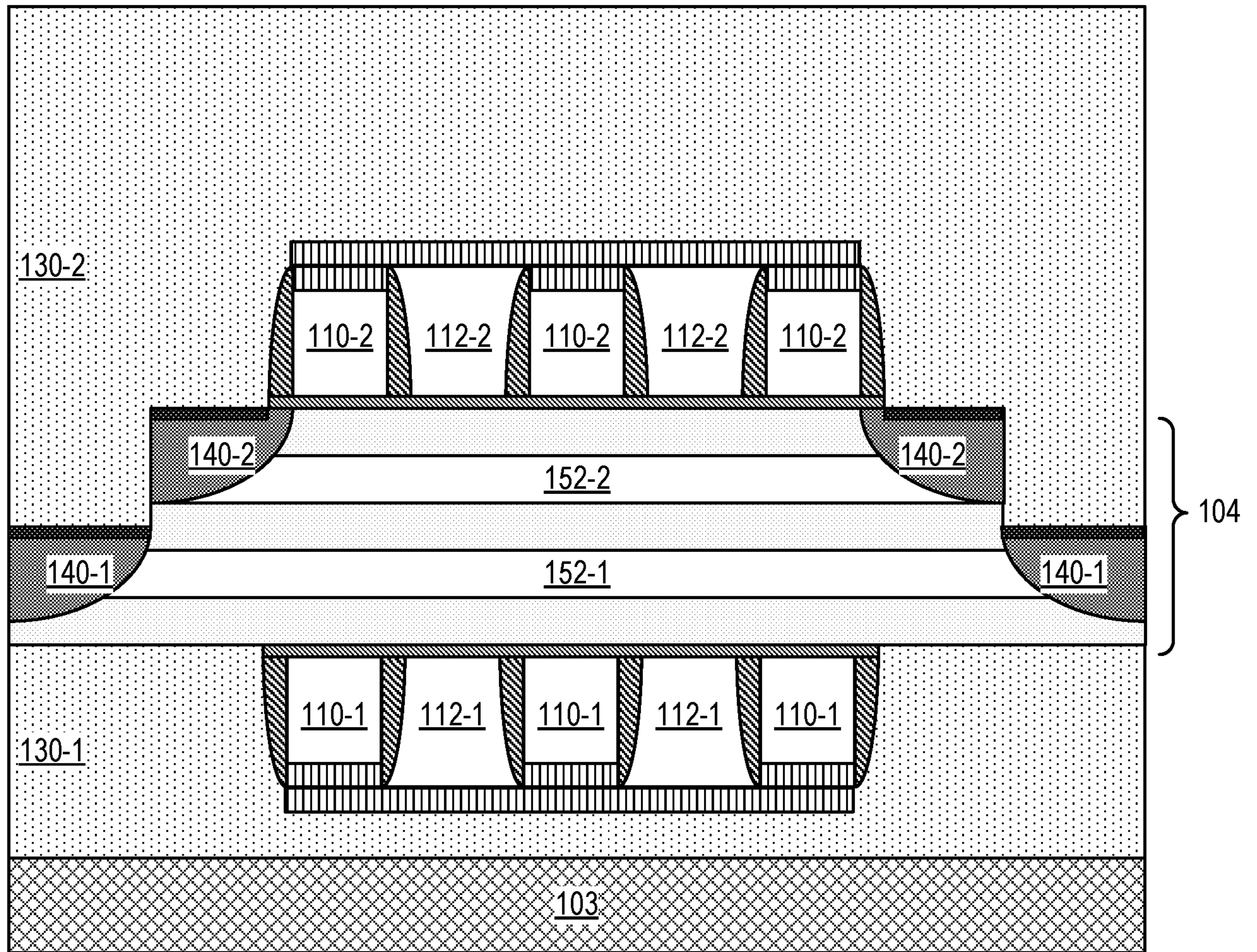


FIG. 30

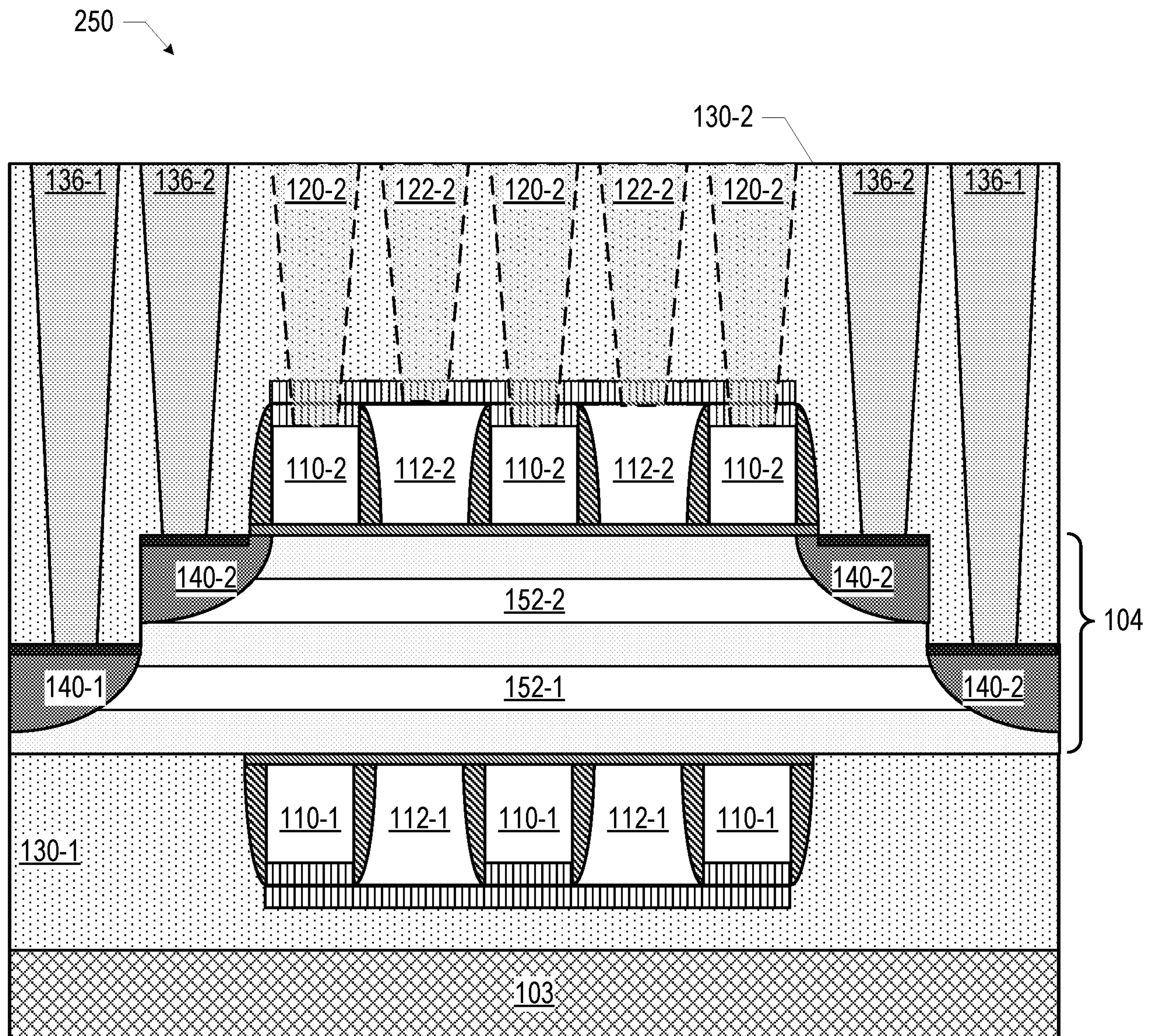


FIG. 31

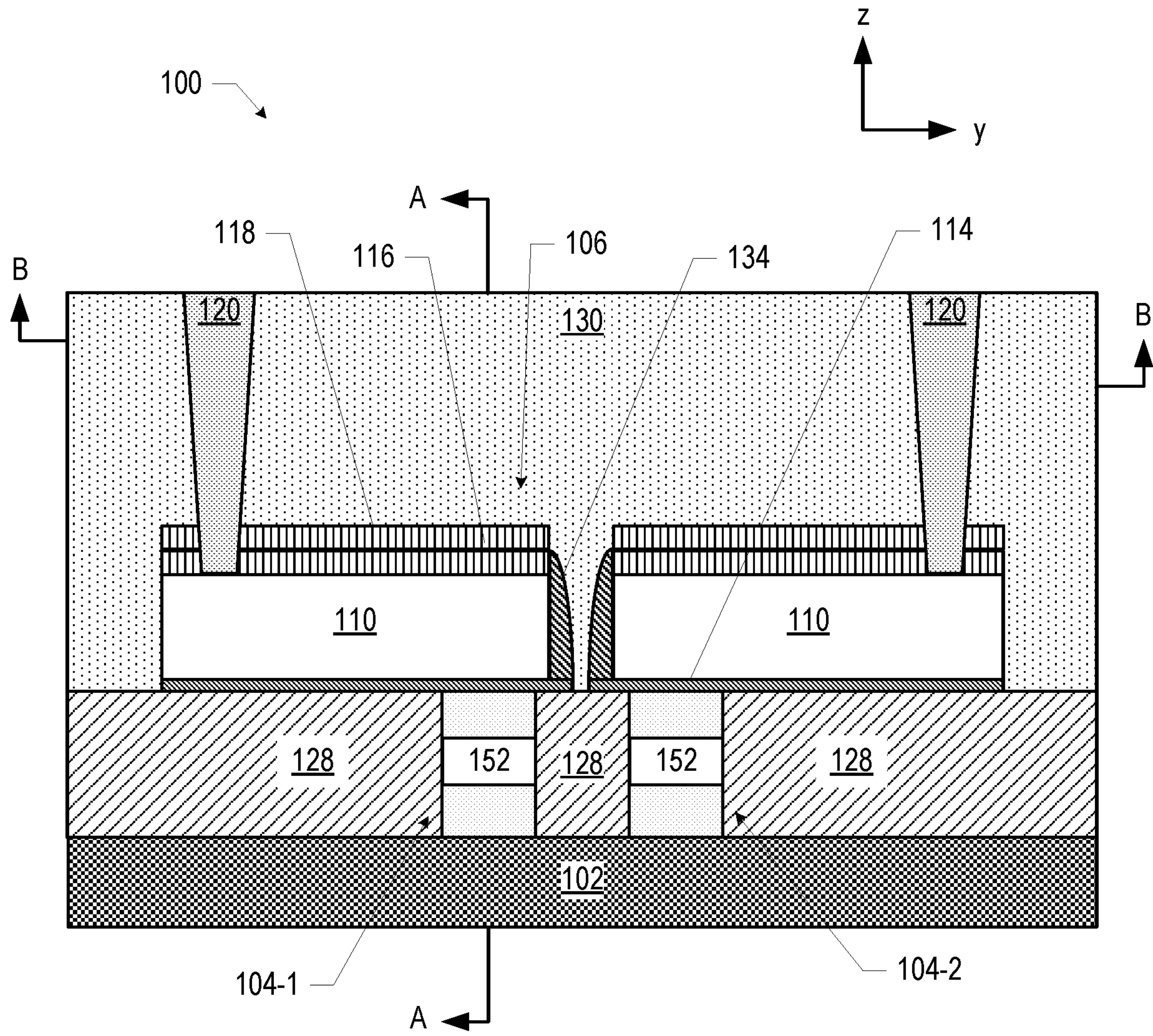


FIG. 32

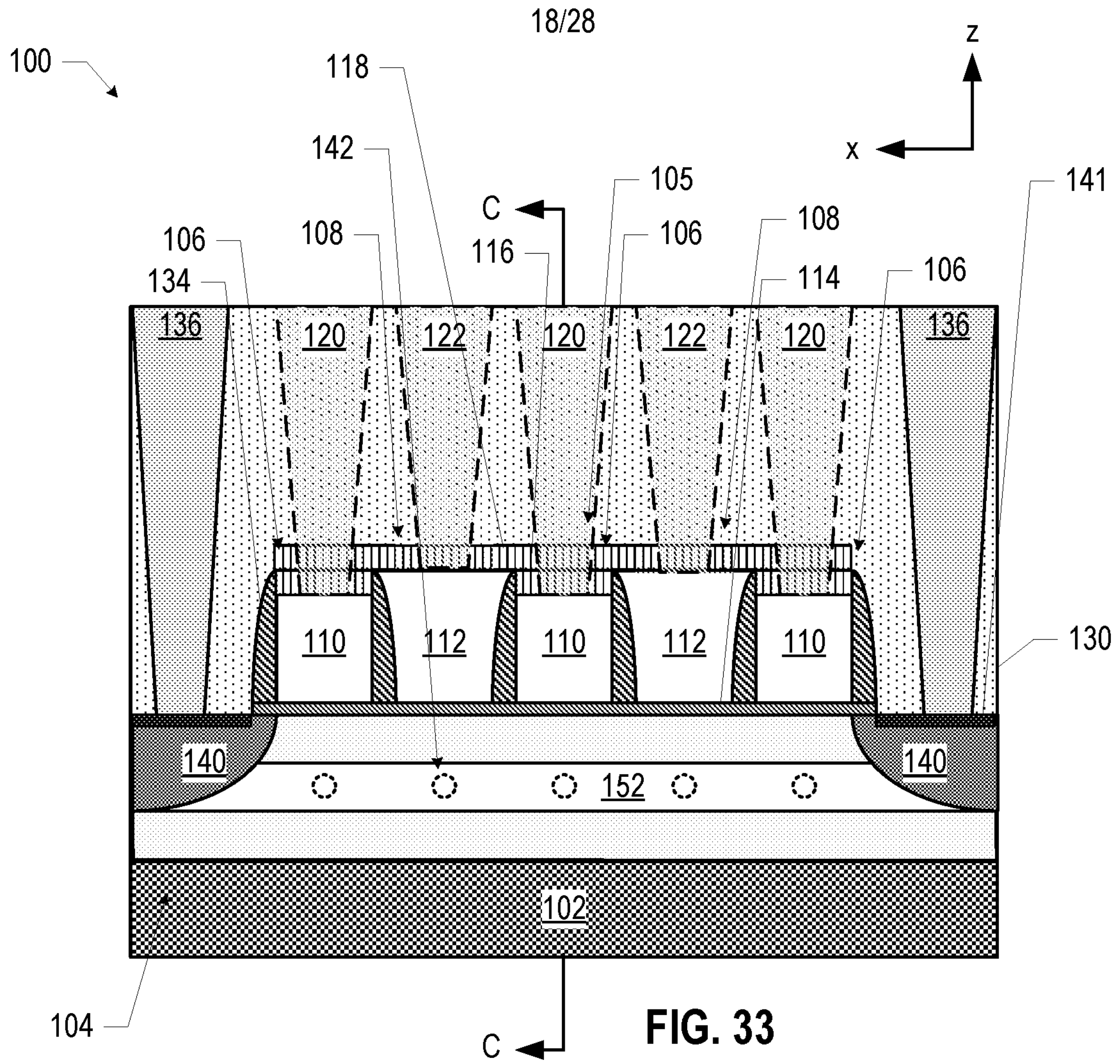


FIG. 33

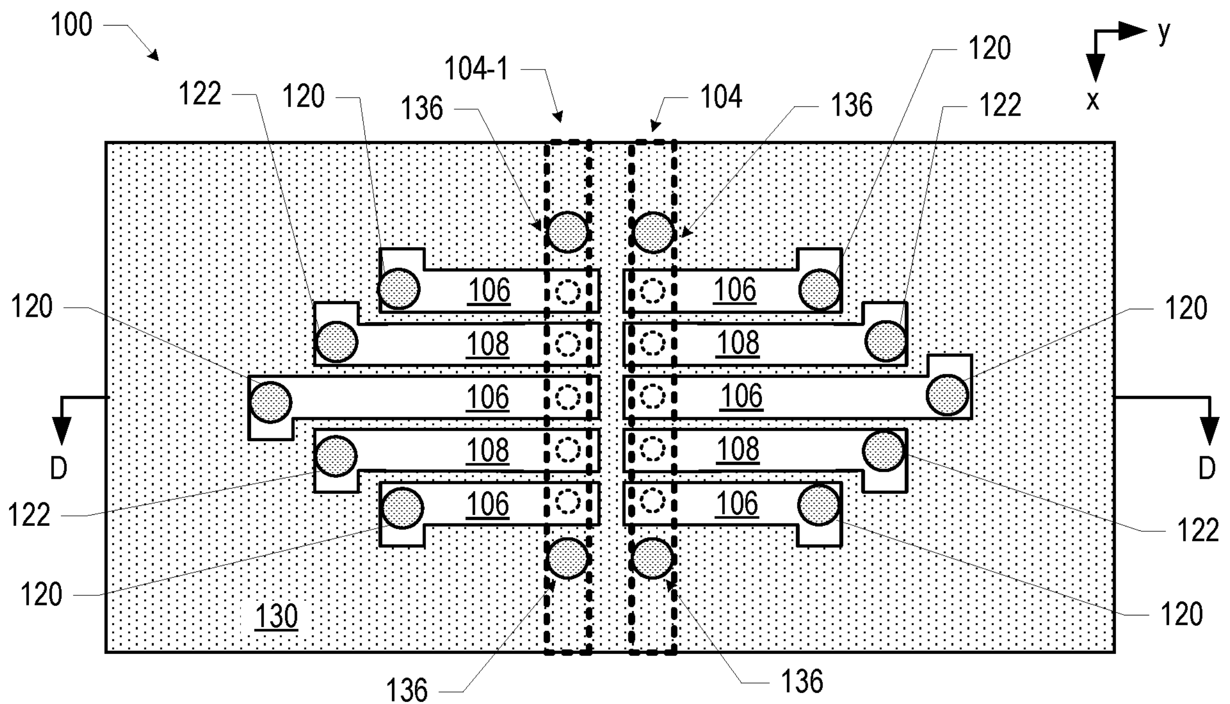


FIG. 34

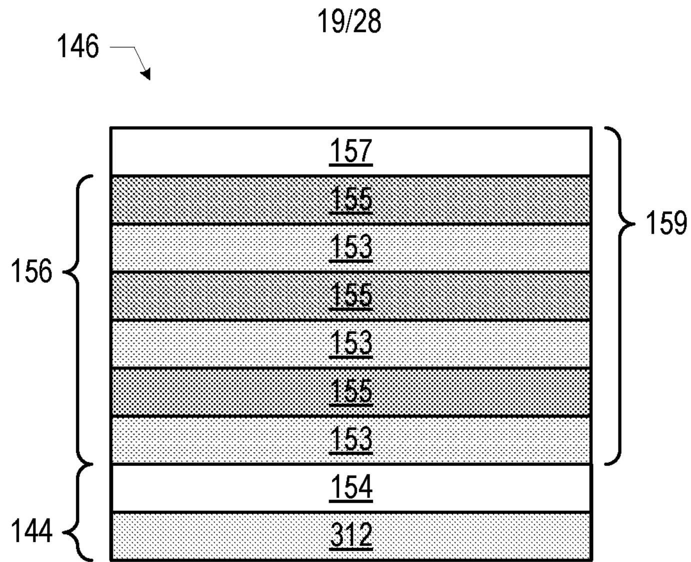


FIG. 35

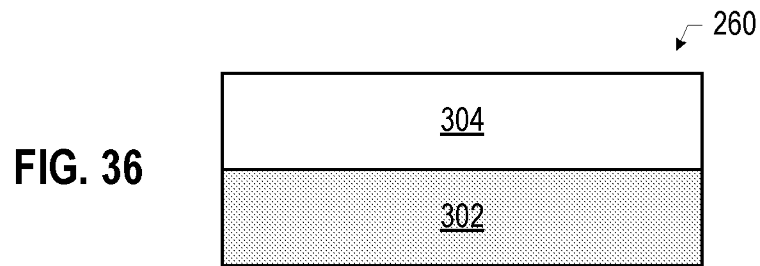


FIG. 36

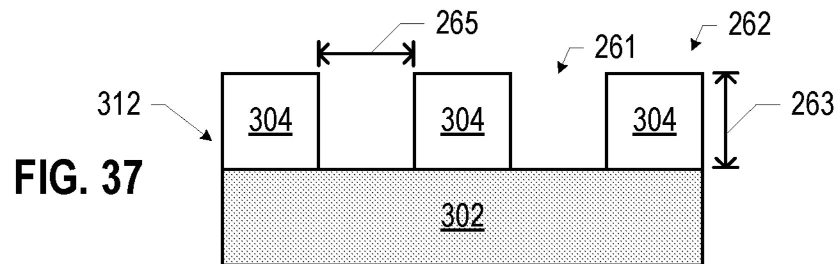


FIG. 37

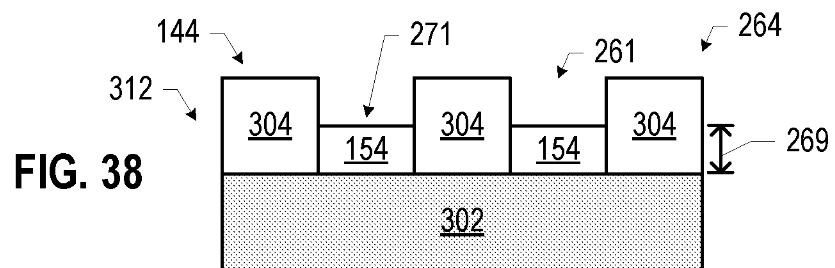


FIG. 38

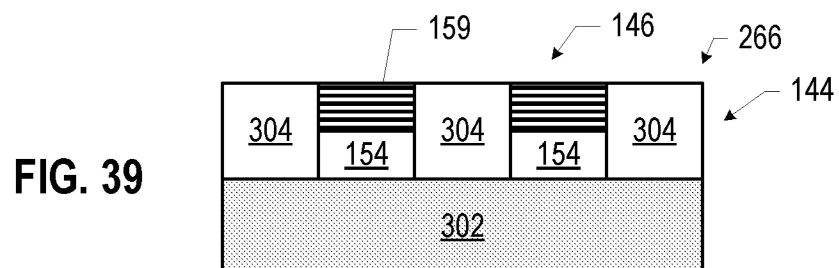


FIG. 39

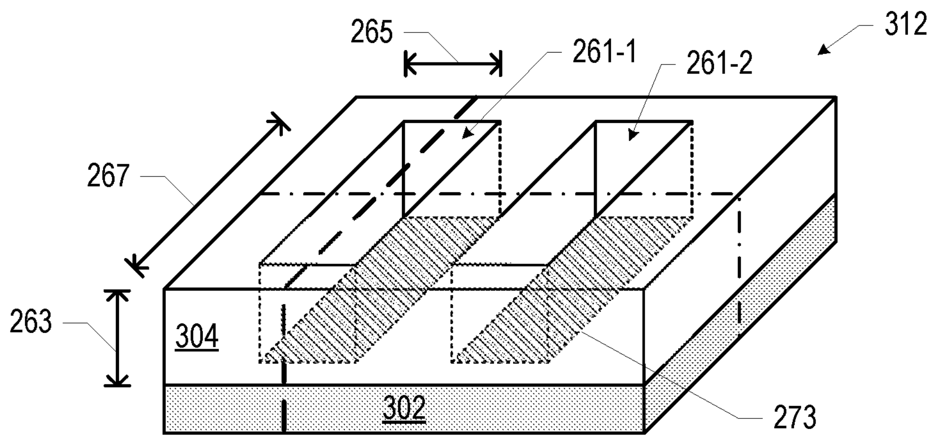


FIG. 40

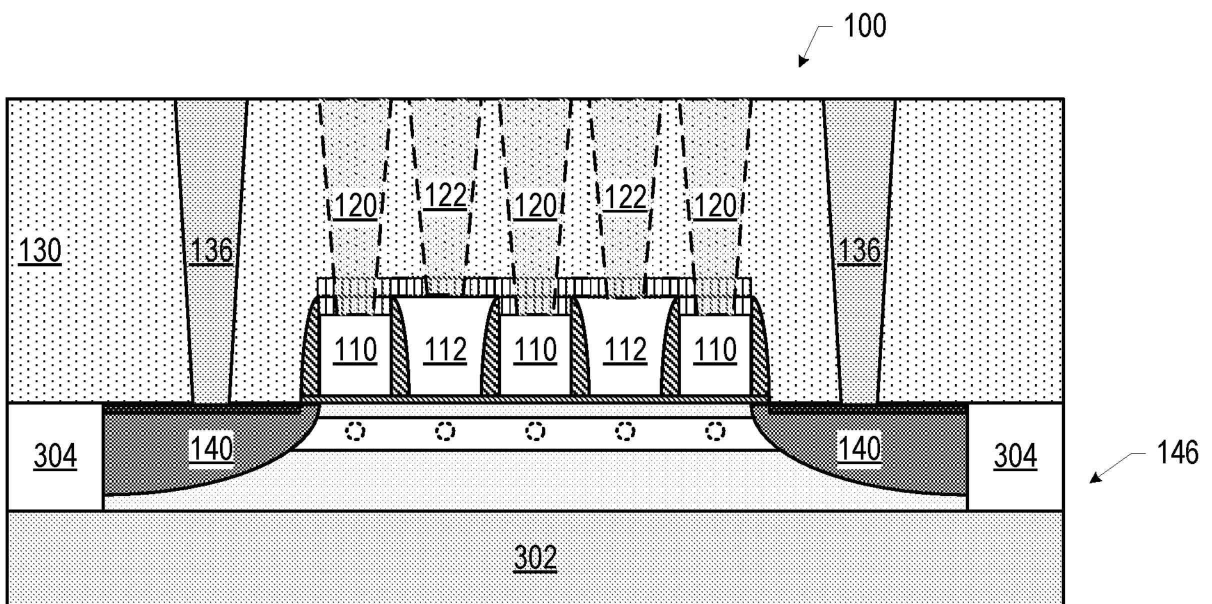


FIG. 41

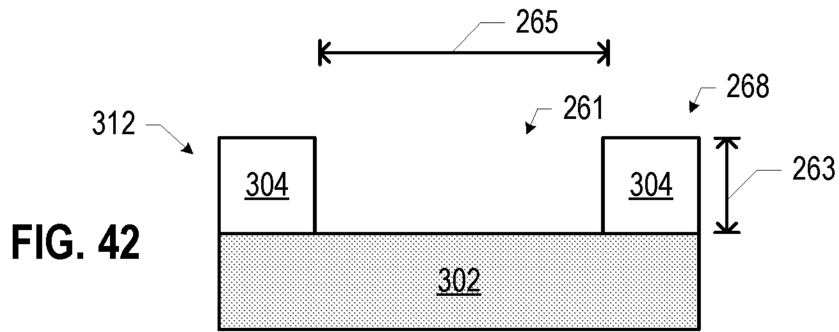


FIG. 42

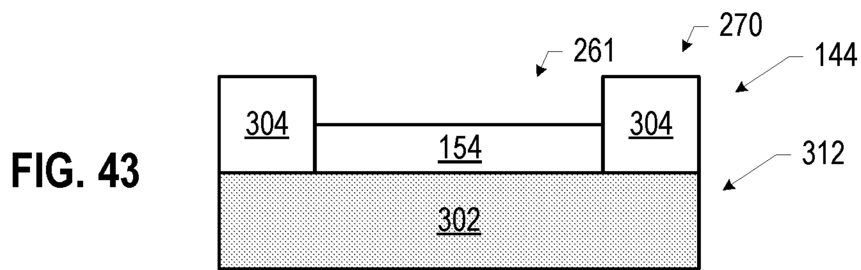


FIG. 43

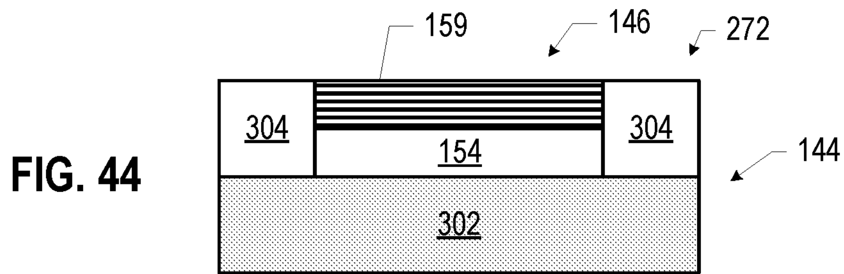


FIG. 44

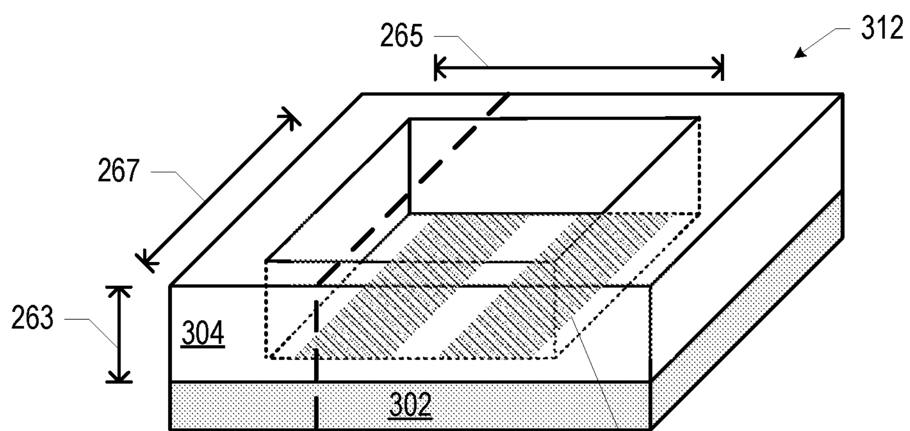


FIG. 45

FIG. 46

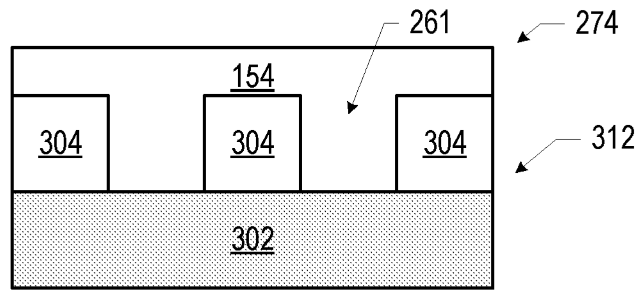


FIG. 47

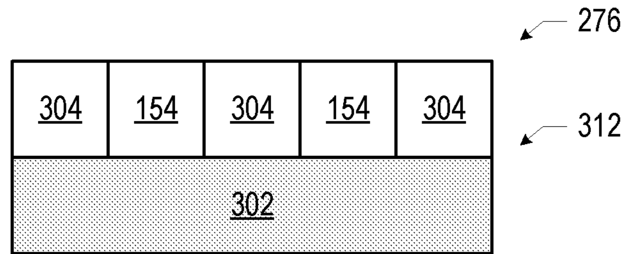


FIG. 48

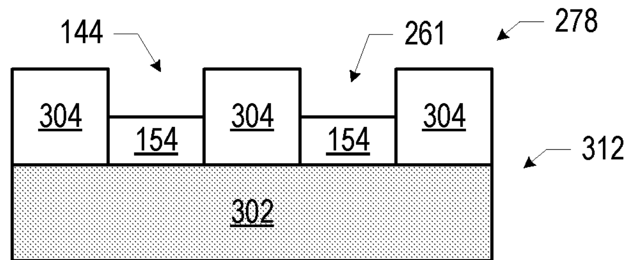


FIG. 49

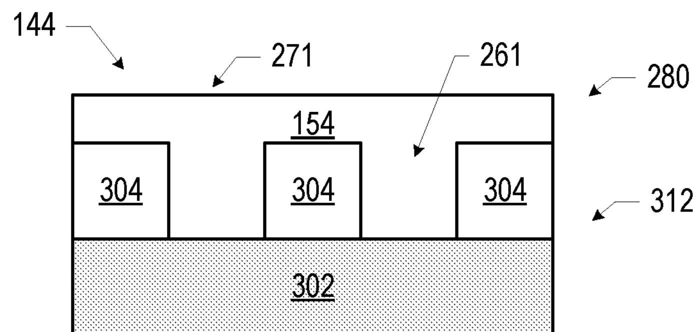
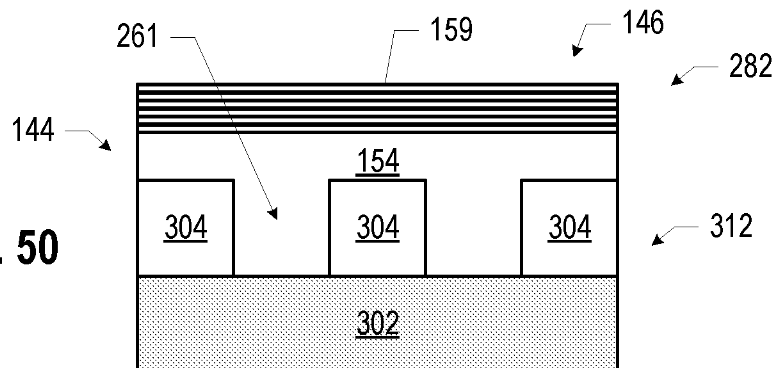


FIG. 50



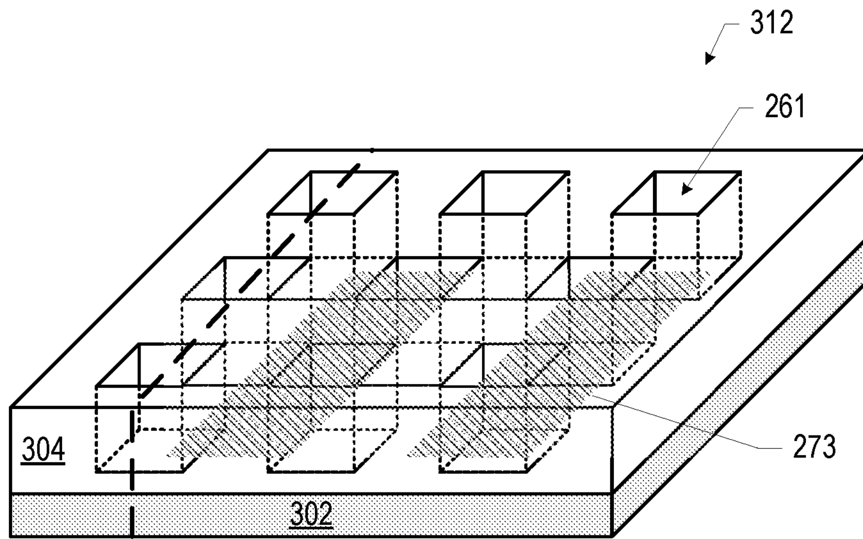


FIG. 51

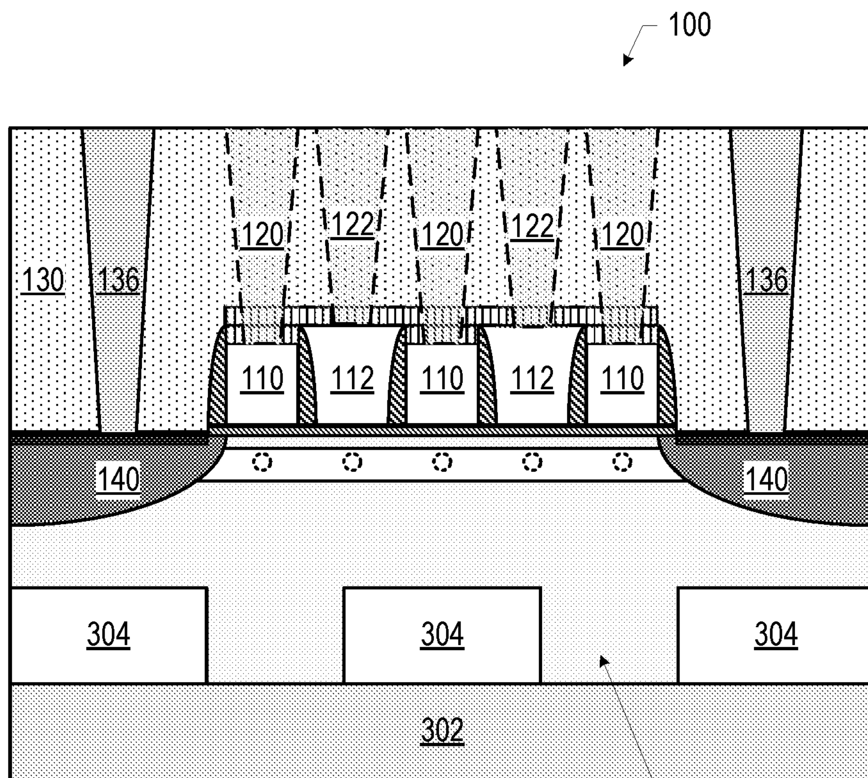


FIG. 52

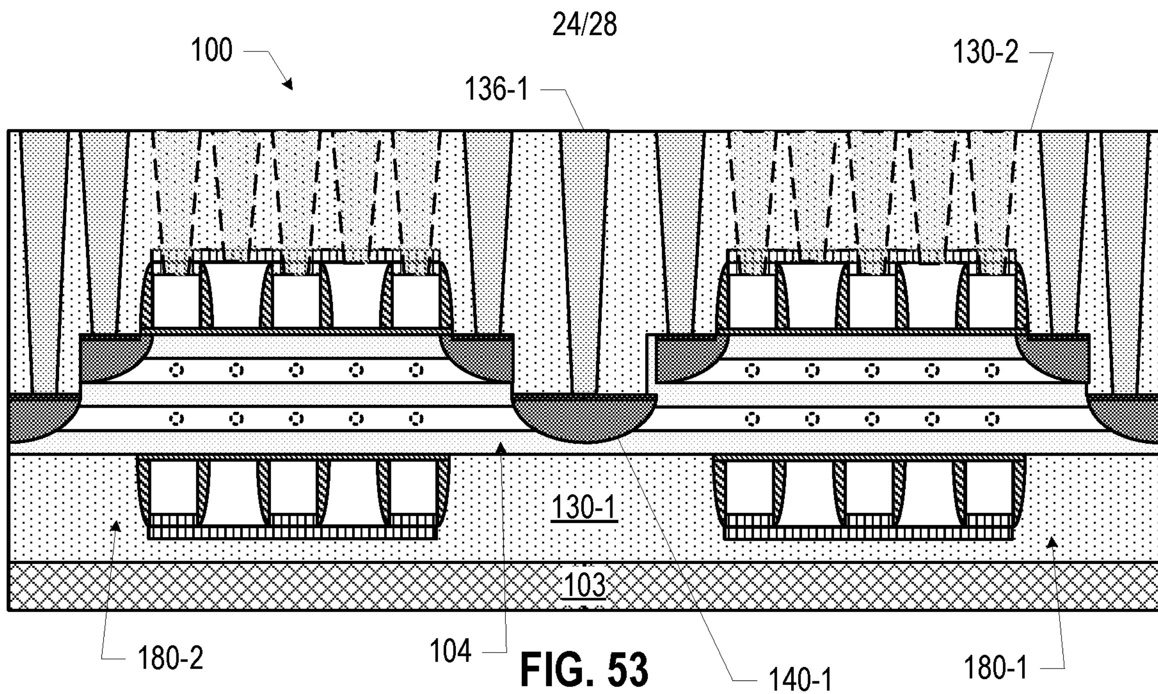


FIG. 53

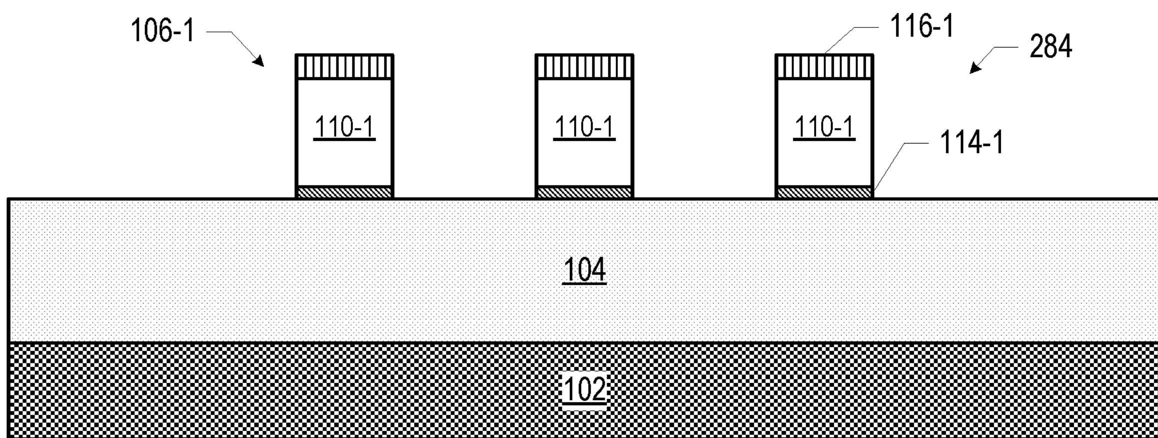


FIG. 54

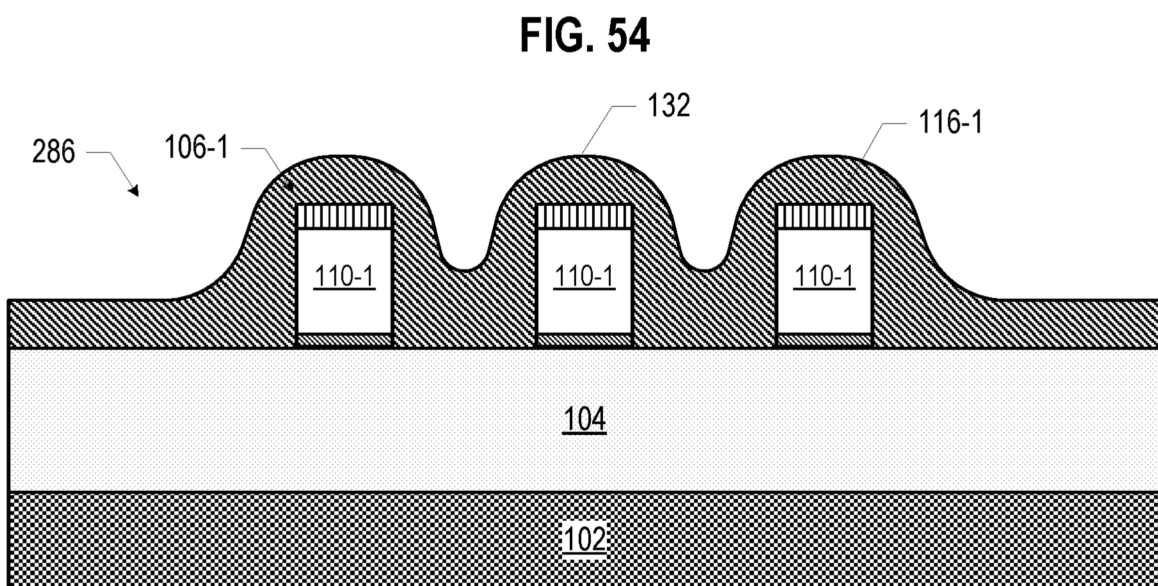


FIG. 55

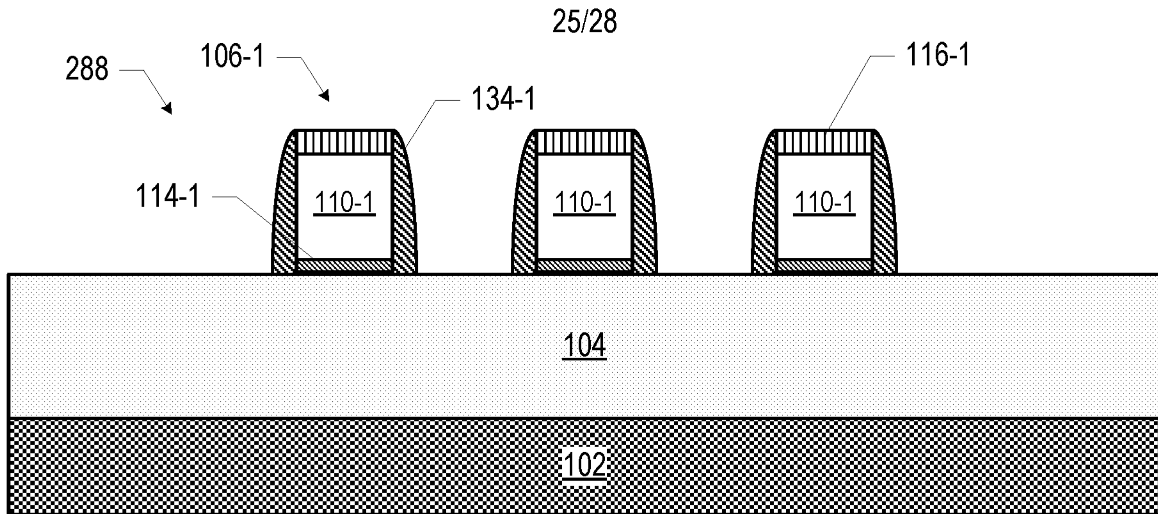


FIG. 56

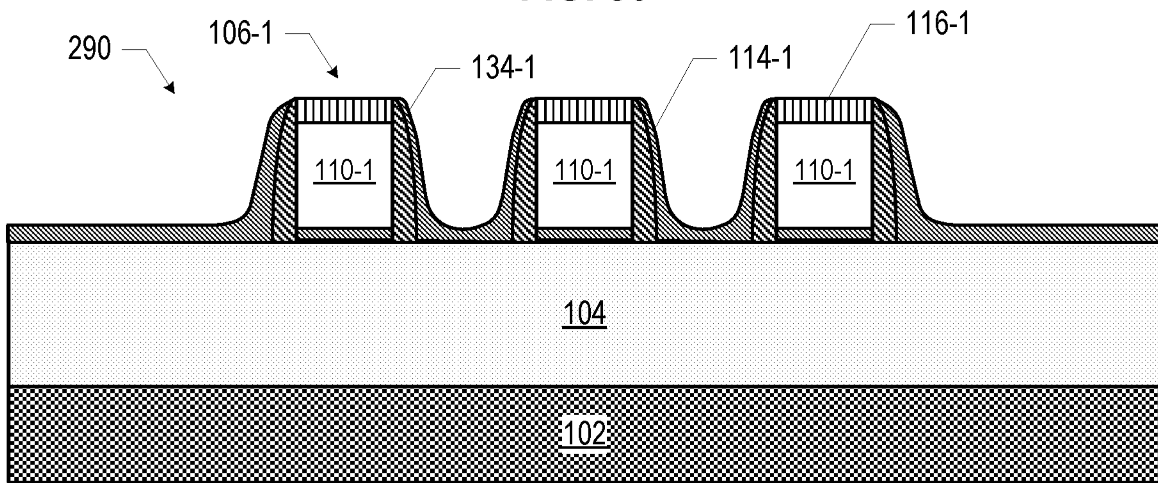


FIG. 57

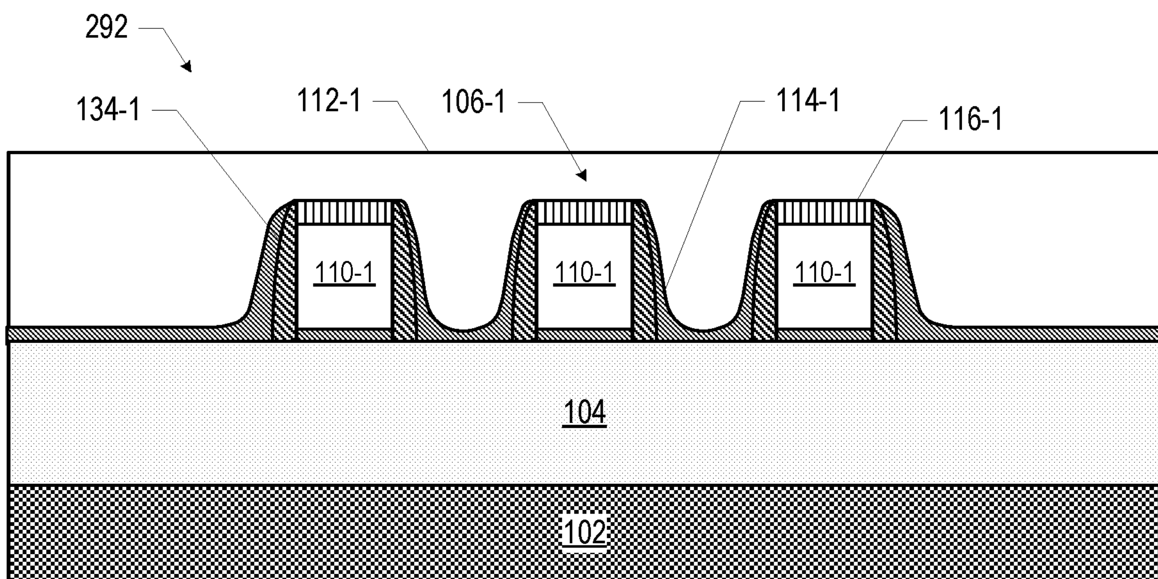


FIG. 58

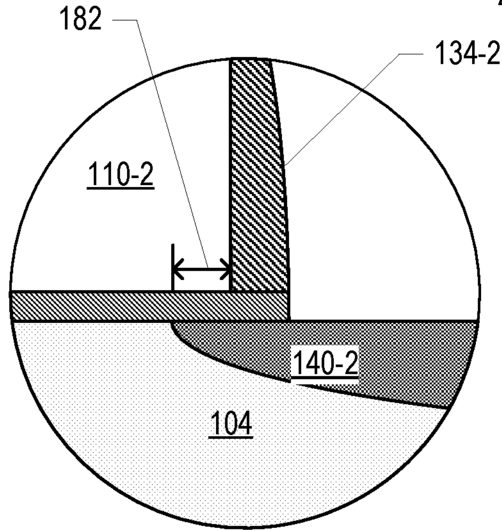


FIG. 59

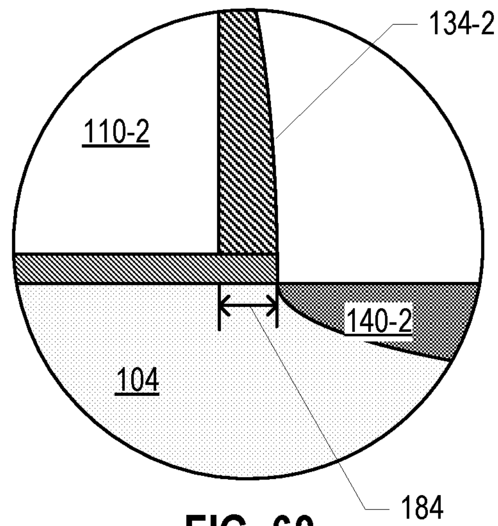


FIG. 60

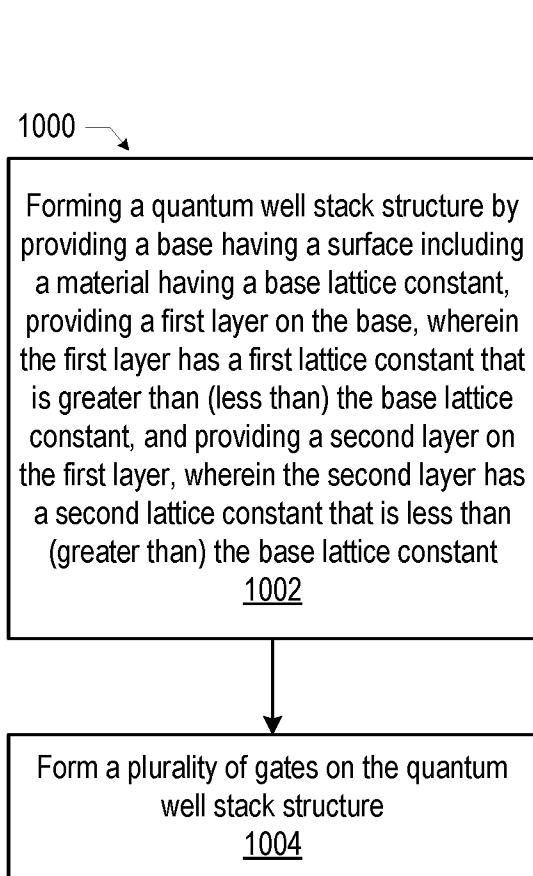


FIG. 61

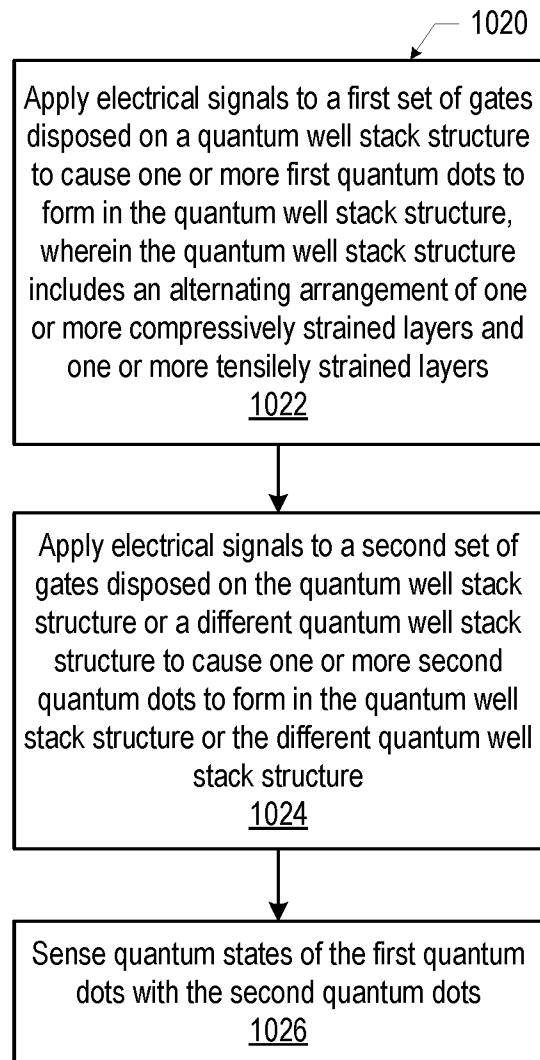
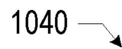


FIG. 62



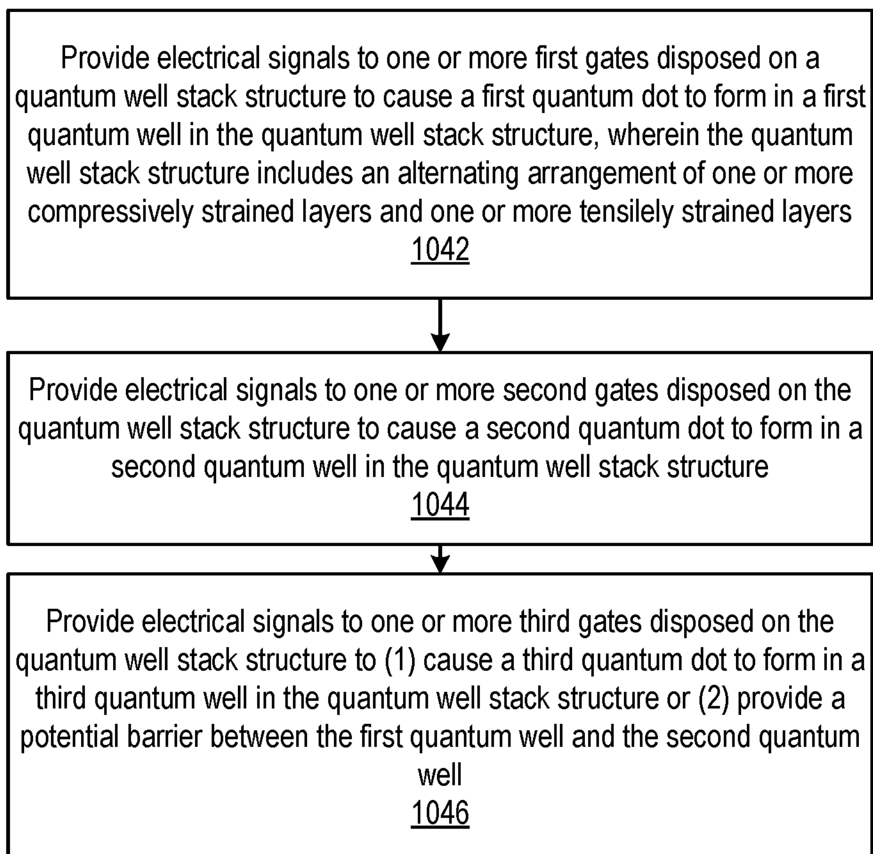


FIG. 63

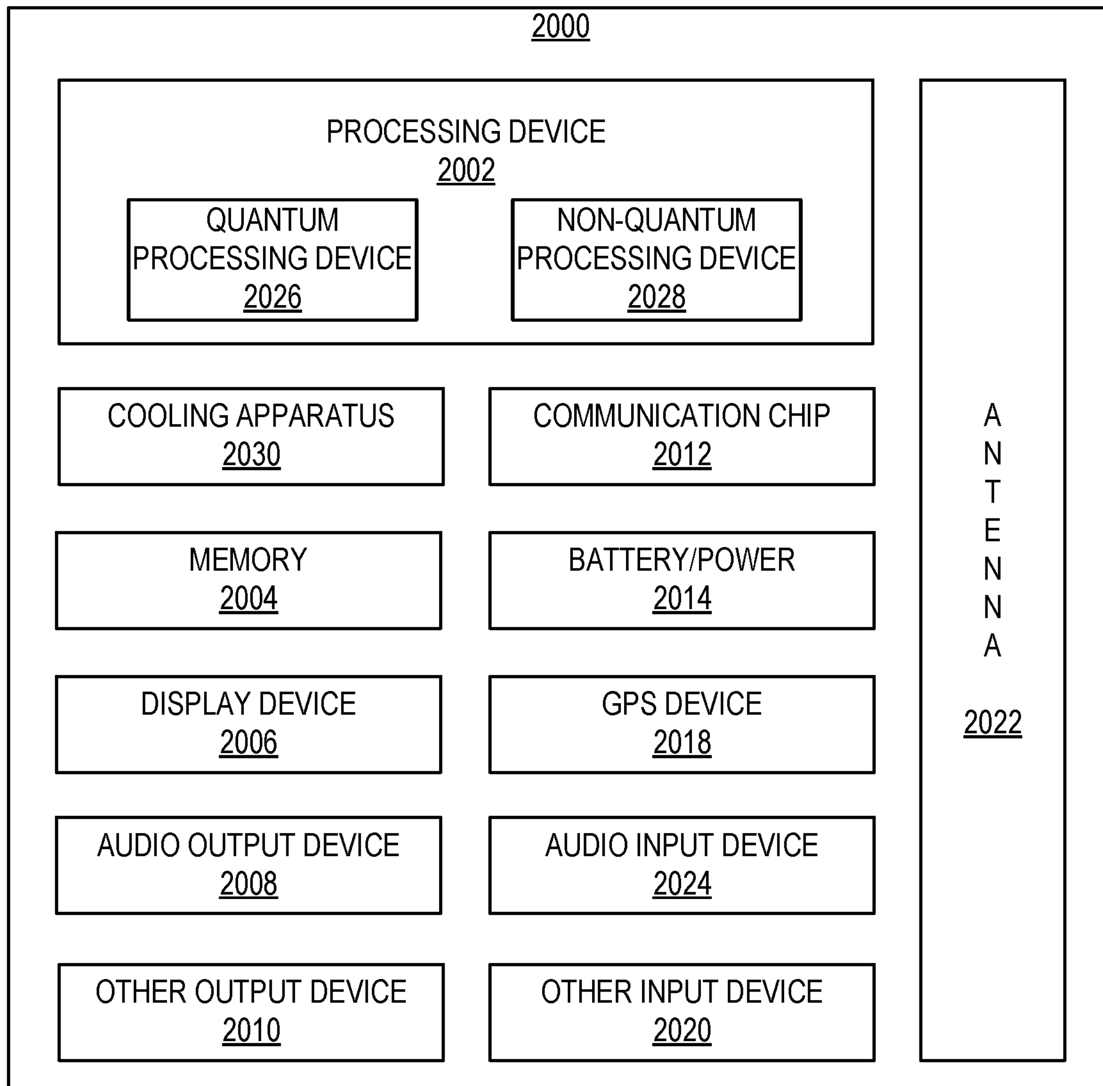


FIG. 64

INTERNATIONAL SEARCH REPORT	International application No. **PCT/US2016/053604**

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/775(2006.01)i, H01L 29/12(2006.01)i, H01L 29/66(2006.01)i, H01L 29/786(2006.01)i, H01L 29/78(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/775; H01L 29/778; H01L 29/165; H01L 29/78; G11C 11/34; H01L 31/0328; H01L 21/336; H01L 29/06; H01L 29/66; G11C 13/00; H01L 29/12; H01L 29/786

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: quantum dot, quantum well, gate, strain

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	US 2002-0179897 A1 (MARK A. ERIKSSON et al.) 05 December 2002 See paragraphs [0035]-[0083] and figures 1-22.	1-10,16,18-19,23,25 12,17,24 11,13-15,20-22
Y	US 2010-0006821 A1 (JUNG BUM CHOI et al.) 14 January 2010 See paragraphs [0084]-[0125] and figures 1-25.	12,17
Y	US 2003-0111659 A1 (ALEXANDER TZALENCHUK et al.) 19 June 2003 See paragraphs [0153]-[0154] and figure 11.	24
A	US 2015-0279981 A1 (WISCONSIN ALUMNI RESEARCH FOUNDATION) 01 October 2015 See paragraphs [0042]-[0057] and figures 4a-4c.	1-25
A	US 7830695 B1 (JEONG-SUN MOON) 09 November 2010 See column 3, line 16 - column 5, line 13 and figures 1-6.	1-25
A	US 6635898 B2 (DAVID ARFON WILLIAMS et al.) 21 October 2003 See column 5, line 34 - column 9, line 25 and figures 1-11.	1-25

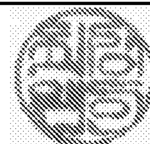
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 August 2017 (21.08.2017)	**21 August 2017 (21.08.2017)**

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHOI, Sang Won

Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/053604

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2002-0179897 A1	05/12/2002	AU 2002-306692 A1	24/09/2002
		CA 2438871 A1	19/09/2002
		CA 2438871 C	04/01/2011
		EP 1386283 A2	04/02/2004
		JP 2004-533107 A	28/10/2004
		US 6597010 B2	22/07/2003
		WO 02-073527 A2	19/09/2002
		WO 02-073527 A3	27/11/2003
US 2010-0006821 A1	14/01/2010	KR 10-0923193 B1	22/10/2009
		KR 10-2008-0032277 A	15/04/2008
		US 8178369 B2	15/05/2012
		WO 2008-044843 A1	17/04/2008
US 2003-0111659 A1	19/06/2003	AU 2002-347173 A1	30/06/2003
		US 2003-0111661 A1	19/06/2003
		US 2003-0146429 A1	07/08/2003
		US 2003-0146430 A1	07/08/2003
		US 6614047 B2	02/09/2003
		US 6791109 B2	14/09/2004
		US 6812484 B2	02/11/2004
		US 6822255 B2	23/11/2004
		WO 03-052687 A1	26/06/2003
US 2015-0279981 A1	01/10/2015	None	
US 7830695 B1	09/11/2010	None	
US 6635898 B2	21/10/2003	EP 1262911 A1	04/12/2002
		JP 2003-086788 A	20/03/2003
		JP 4213892 B2	21/01/2009
		US 2002-0190249 A1	19/12/2002