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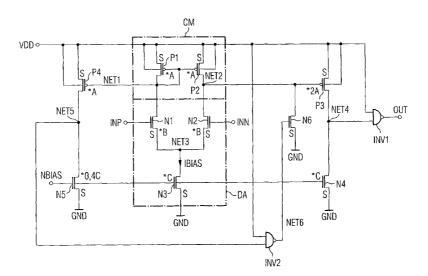
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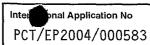


(57) Abstract: The comparator according to the invention comprises a differ-ence amplifier (DA) connected to a current mirror (CM) and a series connection of a first transistor (P4) and a second transistor (N5) connected between a first and a second oper-ating potential (VDD, GND), wherein the control input of the first transistor (P4) is connected to the difference ampli-fier (DA) and the current mirror (CM). The comparator further comprises an inverter (INV2) connected to the first operating potential (VDD) and to the outputs of the first and second transistor (P4, N5). A third transistor (N6) is connected be-tween the second operating potential (GND) and the output (NET2) of the difference amplifier (DA) wherein the control input of the third transistor (N6) is connected to the output of the inverter (INV2).



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT



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