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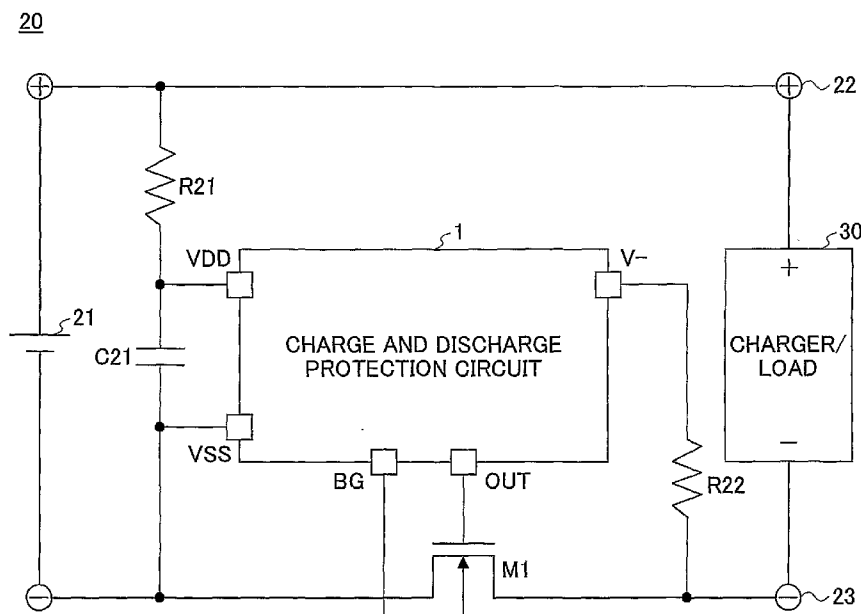
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(54) Title: BACK-GATE VOLTAGE GENERATOR CIRCUIT, FOUR-TERMINAL BACK GATE SWITCHING FET, AND CHARGE AND DISCHARGE PROTECTION CIRCUIT USING SAME



(57) Abstract: A back-gate voltage generator circuit generating a back-gate voltage of a four-terminal back gate switching MOSFET for charge and discharge control is disclosed. The back-gate voltage generator circuit includes first and second n-type MOSFETs connected in series through a common source electrode. A voltage at the common source electrode of the first and second n-type MOSFETs connected in series serves as the back-gate voltage of the four-terminal back gate switching MOSFET, and the back-gate voltage is used as a reference voltage for generating signals for controlling the first and second n-type MOSFETs.

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DESCRIPTION

BACK-GATE VOLTAGE GENERATOR CIRCUIT, FOUR-
TERMINAL BACK GATE SWITCHING FET, AND CHARGE AND
DISCHARGE PROTECTION CIRCUIT USING SAME

5

TECHNICAL FIELD

The present invention relates generally to
techniques related to charge and discharge protection
circuits for secondary batteries such as lithium-ion
10 (Li-ion) secondary batteries, and more particularly
to a technique for enabling protection of a secondary
battery from overcharge, overdischarge, discharge
overcurrent, and charge overcurrent by simply
providing a single four-terminal back gate switching
15 FET in a charge and discharge path.

Specifically, the present invention relates
to a back-gate voltage generator circuit, a four-
terminal back gate switching FET (Field-Effect
Transistor) controlled by the back-gate voltage
20 generator circuit, a charge and discharge protection
circuit for a secondary battery using the four-
terminal back gate switching FET, a battery pack
containing the charge and discharge protection
circuit, and an electronic apparatus such as a
25 cellular phone using the battery pack.

BACKGROUND ART

Li-ion secondary batteries are often used in various portable electronic apparatuses that have
5 been popular in recent years, such as cellular phones; digital cameras; small-size, light-weight audio apparatuses such as portable minidisk units; and game apparatuses. The Li-ion secondary battery involves the risk that metal Li deposits are formed
10 to cause an accident when the battery is overcharged, and also has a problem in that the number of times of repeated charge and discharge use is reduced when the battery is overdischarged.

Accordingly, conventionally, two protection
15 switches, one for overdischarge protection and the other for overcharge protection, are provided in the charge and discharge path between the secondary battery and an apparatus main body, and when the secondary battery is overcharged to be higher than or
20 equal to a predetermined voltage or is overdischarged to be lower than or equal to a predetermined voltage, such overcharge or overdischarge is detected and a corresponding one of the protection switches is
25 turned off, thereby preventing further overcharge or overdischarge.

Thus, the conventional charge and discharge protection circuit for a secondary battery requires a charge control MOSFET (Metal Oxide Silicon Field-Effect Transistor) for charge control and a discharge control MOSFET for discharge control as protection switches, and achieves charge and discharge protection for a battery pack by controlling the gate voltages of the charge control and discharge control MOSFETs. Further, conventionally, each of the charge control MOSFET and the discharge control MOSFET is a three-terminal IC, and the back gate potential is equal to the source potential. Accordingly, there is no need to control the back gate potential.

The source electrode of the charge control MOSFET is connected to the negative terminal of the battery pack, and the source electrode of the discharge control MOSFET is connected to the negative terminal of a battery cell. The direction of the parasitic diode of each MOSFET is fixed.

Japanese Laid-Open Patent Application No. 2006-121900 discloses a battery pack that employs the above-described two MOSFETs for charge control and discharge control.

FIG. 1 is a circuit diagram showing a battery pack 110 disclosed in Japanese Laid-Open

Patent Application No. 2006-121900.

Referring to FIG. 1, the battery pack 110 includes a charge and discharge protection circuit 120, a discharge control FET Q1, a charge control FET
5 Q2, a battery cell 112, capacitors C1, C2, and C3, and resistors r1 and r2.

The charge and discharge protection circuit 120 includes an overcharge detector circuit 122, an overdischarge detector circuit 127, an overcurrent
10 detector circuit 125, delay circuits 126a and 126b, a level shifter 123, an abnormal charger detector circuit 128, a short circuit detector circuit 124, and n-type FETs Q3 and Q4.

The charge and discharge protection circuit
15 120 further includes a VDD terminal to which the positive terminal of the battery cell 112 is connected through the resistor r2, a VSS terminal to which the negative terminal of the battery cell 112 is connected, a V- terminal that detects discharge
20 overcurrent and charge overcurrent, a Cout terminal that turns ON/OFF the charge control MOSFET Q2 that controls charge current, a Dout terminal that turns ON/OFF the discharge control MOSFET Q1 that controls discharge current, and a CT terminal for test
25 shortening.

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The Cout terminal and the Dout terminal are prevented from simultaneously turning OFF the discharge control MOSFET Q1 and the charge control MOSFET Q2. In an overcharged state or a charge
5 overcurrent state, the output level of the Cout terminal output becomes LOW to turn OFF the charge control MOSFET Q2, thereby preventing charging, while the output level of the Dout terminal becomes HIGH to turn ON the discharge control MOSFET Q1, so that it
10 is possible to perform discharge through the parasitic diode of the charge control MOSFET Q2.

Further, in an overdischarged state, a discharge overcurrent state, and a short-circuited state, the output level of the Dout terminal becomes
15 LOW to turn OFF the discharge control MOSFET Q1, thereby preventing discharge, while the output level of the Cout terminal outputs becomes HIGH to turn ON the charge control MOSFET Q2, so that it is possible to perform charging through the parasitic diode of
20 the discharge control MOSFET Q1.

According to the above-described conventional technique, it is possible to control charge and discharge separately, and the direction of the parasitic diode of each of the charge control and
25 discharge control MOSFETs is fixed. Therefore, it is

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possible to provide protection relatively easily.

However, it is low-cost, space-saving products that are now sought after in the marketplace, and products lower in cost and greater in space-
5 saving can be developed by forming a battery pack with one MOSFET capable of controlling both charge and discharge than with two conventional MOSFETs for control.

10 DISCLOSURE OF THE INVENTION

According to one aspect of the present invention, there are provided a back-gate voltage generator circuit that generates a back-gate voltage for performing on-off control on the charge and
15 discharge path of a charge and discharge protection circuit with a single four-terminal back gate switching FET and controlling the direction of the parasitic diode of the four-terminal back gate switching FET in accordance with detection conditions
20 such as overcharge, overdischarge, and overcurrent; a four-terminal back gate switching FET controlled by the back-gate voltage generator circuit; a charge and discharge protection circuit for a secondary battery using the four-terminal back gate switching FET; a
25 battery pack containing the charge and discharge

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protection circuit; and an electronic apparatus such as a cellular phone using the battery pack.

According to one aspect of the present invention, there is provided a back-gate voltage generator circuit generating a back-gate voltage of a
5 four-terminal back gate switching MOSFET for charge and discharge control, the back-gate voltage generator circuit including first and second n-type MOSFETs connected in series through a common source
10 electrode, wherein a voltage at the common source electrode of the first and second n-type MOSFETS connected in series serves as the back-gate voltage of the four-terminal back gate switching MOSFET, and the back-gate voltage is used as a reference voltage
15 for generating signals for controlling the first and second n-type MOSFETS.

According to one aspect of the present invention, there is provided a four-terminal back gate switching MOSFET for charge and discharge
20 control controlled by the back-gate voltage generator circuit as set forth above.

According to one aspect of the present invention, there is provided a charge and discharge protection circuit protecting a secondary battery
25 from overcharge, overdischarge, discharge overcurrent,

and charge overcurrent by detecting the overcharge,
the overdischarge, the discharge overcurrent, and the
charge overcurrent of the secondary battery, the
charge and discharge protection circuit including the
5 four-terminal back gate switching MOSFET for charge
and discharge control as set forth above as an FET
for the charge and discharge control provided in a
charge and discharge path.

According to one aspect of the present
10 invention, there is provided a battery pack including
the charge and discharge protection circuit as set
forth above.

According one aspect of the present
invention, there is provided an electronic apparatus
15 including the battery pack as set forth above.

Examples of the electronic apparatus may
include a cellular phone, a digital camera, an audio
apparatus, and a game apparatus.

Thus, according to embodiments of the
20 present invention, it is possible to provide a back-
gate voltage generator circuit that generates a back-
gate voltage for performing on-off control on the
charge and discharge path of a charge and discharge
protection circuit with a single four-terminal back
25 gate switching FET and controlling the direction of

the parasitic diode of the four-terminal back gate switching FET in accordance with detection conditions such as overcharge, overdischarge, and overcurrent; a four-terminal back gate switching FET controlled by
5 the back-gate voltage generator circuit; a charge and discharge protection circuit for a secondary battery using the four-terminal back gate switching FET; a battery pack containing the charge and discharge protection circuit; and an electronic apparatus such
10 as a cellular phone using the battery pack.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features and advantages of the present invention will become more apparent from
15 the following detailed description when read in conjunction with the accompanying drawings, in which:

FIG. 1 is a circuit diagram showing a conventional battery pack;

FIG. 2 is a schematic circuit diagram
20 showing a battery pack including a charge and discharge protection circuit according to an embodiment of the present invention;

FIG. 3 is a circuit diagram showing a back-gate voltage generator circuit for controlling the
25 back gate of a four-terminal back gate switching FET

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provided in the charge and discharge protection circuit according to the embodiment of the present invention;

FIG. 4 is another circuit diagram showing the battery pack containing a secondary battery protection IC containing the back-gate voltage generator circuit according to the embodiment of the present invention; and

FIG. 5 is a table showing conditions in each operational sequence for illustrating operations according to the embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

A description is given, with reference to the accompanying drawings, of an embodiment of the present invention.

FIG. 2 is a schematic circuit diagram showing a battery pack 20 including a charge and discharge protection circuit 1 and a four-terminal back gate switching FET M1 according to the embodiment of the present invention.

Referring to FIG. 2, the charge and discharge protection circuit 1 according to this embodiment includes a VDD terminal to which the positive terminal of a battery cell 21 is connected

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through a resistor 21; a VSS terminal to which the negative terminal of the battery cell 21 is connected, a V- terminal for detecting discharge overcurrent and charge overcurrent; a BG terminal for controlling the back-gate voltage of the four-terminal back gate switching FET M1, the BG terminal being connected to the back gate of the four-terminal back gate switching FET M1; and an OUT terminal for performing on-off control on the four-terminal back gate switching FET M1, the OUT terminal being connected to the gate terminal of the four-terminal back gate switching FET M1. The charge and discharge protection circuit 1 may further include a test terminal for shortening a delay time.

The battery pack 20 shown in FIG. 2 operates as follows. (See FIG. 5 for the conditions at the time of each operation.)

(a) In an ordinary state (that is, a normal state), the output level of the OUT terminal is HIGH, the BG terminal outputs the V- voltage of the charge and discharge protection circuit, and the four-terminal back gate switching FET M1 is ON. In this state, both charge and discharge are performable.

(b) In an overcharged state, the output level of the OUT terminal is LOW, the BG terminal

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outputs the V- voltage of the charge and discharge protection circuit 1, and the four-terminal back gate switching FET M1 is OFF to stop charging. At this point, the parasitic diode of the four-terminal back gate switching FET M1 is arranged in a direction in which a current flows from the negative terminal of a charger or load (charger/load) 30 to the negative terminal of the battery cell 21, and it is possible to perform discharging.

10 (c) In an overdischarged state, the output level of the OUT terminal is LOW, the BG terminal outputs the VSS voltage of the charge and discharge protection circuit 1, and the four-terminal back gate switching FET M1 is OFF to stop discharging. At this point, the parasitic diode of the four-terminal back gate switching FET M1 is in a direction in which a current flows from the negative terminal of the battery cell 21 to the negative terminal of the charger/load 30, and it is possible to perform charging.

20 (d) In a discharge overcurrent state, the output level of the OUT terminal is LOW, the BG terminal outputs the VSS voltage of the charge and discharge protection circuit 1, and the four-terminal back gate switching FET M1 is OFF to stop discharge.

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At this point, the parasitic diode of the four-terminal back gate switching FET M1 is in the direction in which a current flows from the negative terminal of the battery cell 21 to the negative terminal of the charger/load 30, and it is possible to perform charging.

(e) In a charge overcurrent state, the output level of the OUT terminal is LOW, the BG terminal outputs the V- voltage of the charge and discharge protection circuit 1, and the four-terminal back gate switching FET M1 is OFF to stop charging. At this point, the parasitic diode of the four-terminal back gate switching FET M1 is in the direction in which a current flows from the negative terminal of the charger/load 30 to the negative terminal of the battery cell 21, and it is possible to perform discharging.

FIG. 3 is a circuit diagram showing a back-gate voltage generator circuit 14 for generating a back-gate voltage that controls the back gate of the four-terminal back gate switching FET M1. The back-gate voltage generator circuit 14 is contained in the charge and discharge protection circuit 1.

The back-gate voltage generator circuit 14 includes an n-type MOSFET M10 and an n-type MOSFET

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M20, of which one is selected for the back-gate voltage. The back-gate voltage generator circuit 14 further includes an inverter INV1 and an inverter INV2. The connection (common source electrode) of the n-type MOSFETS M10 and M20 is also connected to each of the inverters INV1 and INV2, so that the gate voltage of each of the n-type MOSFETS M10 and M20 is input using the back-gate voltage as a basis.

In the ordinary state (normal state), when a low-level signal is input as a control signal Sc, the control signal Sc is inverted through the inverter INV1 so that a high-level signal is input to the gate of the n-type MOSFET M10. At the same time, the inverted signal is further inverted through the inverter INV2 so that a low-level signal is input to the gate of the n-type MOSFET M20.

At this point, the n-type MOSFET M10 is ON, and the n-type MOSFET M20 is OFF. At this point, since the four-terminal back gate switching FET M1 is ON, the voltage at the negative terminal of the battery cell 21, the voltage at the negative terminal of the charger/load 30, and the V- voltage through a resistor R22 in FIG. 2 are substantially the same. Accordingly, no current flows through the parasitic diode of the n-type MOSFET M20.

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In the overcharged state, a low-level signal is input as the control signal Sc, so that a high-level signal is input to the gate of the n-type MOSFET M10 and a low-level signal is input to the gate of the n-type MOSFET M20. At this point, the n-type MOSFET M10 is ON, and the n-type MOSFET M20 is OFF. At this point, the four-terminal back gate switching FET M1 is OFF.

Immediately before detection of overcharge, the battery cell 21 has been charged with a charger voltage greater than the voltage of the battery cell 21. Therefore, at the same time that charging is prevented, the relationship between the VSS voltage and the V- voltage becomes " $V_{SS} > V_-$." Accordingly, the direction is opposite, so that no current flows through the parasitic diode of the n-type MOSFET M20.

In the overdischarged state, a high-level signal is input as the control signal Sc, so that a low-level signal is input to the gate of the n-type MOSFET M10 and a high-level signal is input to the gate of the n-type MOSFET M20. At this point, the n-type MOSFET M10 is OFF, and the n-type MOSFET M20 is ON. At this point, the four-terminal back gate switching FET M1 is OFF.

Immediately before detection of

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overdischarge, the battery cell 21 has been discharged because of connection of the battery pack 20 to the load 30. At the same time that discharge is prevented, the V- potential is pulled up to the VDD level inside the charge and discharge protection circuit 1, so that the relationship between the VSS voltage and the V- voltage becomes "VSS < V-." Accordingly, the direction is opposite, so that no current flows through the parasitic diode of the n-type MOSFET M10.

In the discharge overcurrent state, a high-level signal is input as the control signal Sc, so that a low-level signal is input to the gate of the n-type MOSFET M10 and a high-level signal is input to the gate of the n-type MOSFET M20. At this point, the n-type MOSFET M10 is OFF, and the n-type MOSFET M20 is ON. At this point, the four-terminal back gate switching FET M1 is OFF.

Immediately before detection of discharge overcurrent, the battery cell 21 has been discharged because of connection of the battery pack 20 to the load 30. At the same time that discharge is prevented, the discharge path is lost, so that the relationship between the VSS voltage and the V- voltage becomes "VSS < V-." Accordingly, the

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direction is opposite, so that no current flows through the parasitic diode of the n-type MOSFET M10.

In the charge overcurrent state, a low-level signal is input as the control signal S_c , so that a high-level signal is input to the gate of the n-type MOSFET M10 and a low-level signal is input to the gate of the n-type MOSFET M20. At this point, the n-type MOSFET M10 is ON, and the n-type MOSFET M20 is OFF. At this point, the four-terminal back gate switching FET M1 is OFF.

Immediately before detection of charge overcurrent, the battery cell 21 has been charged with a charger voltage greater than the battery cell 21. Therefore, at the same time that charging is prevented, the relationship between the VSS voltage and the V- voltage becomes " $V_{SS} > V_-$." Accordingly, the direction is opposite, so that no current flows through the parasitic diode of the n-type MOSFET M20.

FIG. 4 is another circuit diagram showing the battery pack 20 containing a secondary battery protection IC containing the back-gate voltage generator circuit 14 according to the embodiment of the present invention. In FIG. 4, the same elements as those of FIG. 2 are referred to by the same reference numerals.

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Referring to FIG. 4, the battery pack 20 includes the charge and discharge protection circuit (protection IC having an IC configuration) 1, the four-terminal back gate switching FET M1, which is an n-type MOSFET, the battery cell (secondary battery) 21, a capacitor C21, the resistors R21 and R22, a positive-side terminal 22, and a negative-side terminal 23. The charger/load 30 is a charger at the time of charging or a load device such as a cellular phone; a digital camera; an audio apparatus; or a game apparatus at the time of discharging.

The protection IC 1 includes an overcharge detector circuit 2, an overdischarge detector circuit 3, a charge overcurrent detector circuit 4, a first discharge overcurrent detector circuit 5, a second discharge overcurrent detector circuit 6, a delay time generator circuit 7, a shortening circuit 8, a level shifter 9, an abnormal charger detector circuit 10, a logic circuit 11, the back-gate voltage generator circuit 14 (described in detail with reference to FIG. 3), and the four-terminal n-type MOSFET M1. The delay time generator circuit 7 includes a counter 12 and an oscillator circuit 13.

The protection IC 1 further includes the charge and discharge control terminal OUT for

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controlling the gate voltage of the four-terminal n-type MOSFET M1, the back gate control terminal BG for controlling the back-gate voltage of the four-terminal n-type MOSFET M1, and the current detection terminal V- for detecting charge/discharge current by converting the charge/discharge current into voltage. Although omitted in FIG. 4, the same short circuit detector circuit as the conventional short circuit detector circuit 124 shown in FIG. 1 may be provided so as to input a detection signal to the delay time generator circuit 7 at the time of detecting a short circuit, thereby making it possible to perform protection control at the time of detecting a short circuit as well.

15 The level shifter 9 outputs a gate signal applied to the gate of the four-terminal n-type MOSFET M1 for charge and discharge control and the control signal Sc input to the back-gate voltage generator circuit 14. The control signal Sc is HIGH at the time of the ordinary state, detection of overcharge, and detection of charge overcurrent, and is LOW at the time of detection of overdischarge and detection of discharge overcurrent. The back-gate voltage generator circuit 14 has the configuration described in detail with reference to FIG. 3.

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The outputs of the overcharge detector circuit 2, the overdischarge detector circuit 3, the charge overcurrent detector circuit 4, the first discharge overcurrent detector circuit 5, and the second discharge overcurrent detector circuit 6 are input to the delay time generator circuit 7. Each of these output signals is delayed for a predetermined delay time by the delay time generator circuit 7 to be output to the logic circuit 11, and is thereafter converted into a reference voltage in the level shifter 9. The signal from the level shifter 9 is directly applied to the gate of the four-terminal n-type MOSFET M1. The control signal Sc from the level shifter 9 is input to the back-gate voltage generator circuit 14 to generate a back-gate signal (BG), and the generated back-gate signal (BG) is applied to the back gate of the four-terminal n-type MOSFET M1. Thereby, on-off control is performed on the four-terminal n-type MOSFET M1 and the direction of the parasitic diode of the four-terminal n-type MOSFET M1 is controlled as described above.

The above-described predetermined delay time is not uniform through all the input signals, and takes a predetermined value based on the contents of detection. The details of the delay time are

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described in many patent documents and are well known. Accordingly, a description thereof is omitted.

FIG. 5 shows the above-described operations according to the embodiment of the present invention.

5 FIG. 5 shows a brief list of the conditions of the control signal Sc, the BG output, the terminal voltage, the direction of the parasitic diode, performability of charge and discharge, the gate signal of the four-terminal back gate switching n-

10 type MOSFET M1, and ON/OFF of the four-terminal back gate switching n-type MOSFET M1 in each of the operational sequences at the ordinary (normal) time, at the time of detection of overcharge, at the time of detection of overdischarge, at the time of

15 detection of discharge overcurrent, and at the time of detection of charge overcurrent.

By building the back-gate voltage generator circuit 14 having the above-described configuration into the charge and discharge protection circuit 1, a

20 battery pack using a four-terminal back gate switching MOSFET can be achieved.

Further, the battery pack thus achieved can be applied to a wide range of electronic apparatuses such as cellular phones, digital cameras, audio

25 apparatuses such as small-size, light-weight portable

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minidisk units, and game apparatuses, which have been popular in recent years.

According to one aspect of the present invention, there is provided a back-gate voltage generator circuit generating the back-gate voltage of a four-terminal back gate switching MOSFET for charge and discharge control, the back-gate voltage generator circuit including first and second n-type MOSFETs connected in series through a common source electrode, wherein a voltage at the common source electrode of the first and second n-type MOSFETs connected in series serves as the back-gate voltage of the four-terminal back gate switching MOSFET, and the back-gate voltage is used as a reference voltage for generating signals for controlling the first and second n-type MOSFETs.

According to one aspect of the present invention, there is provided a four-terminal back gate switching MOSFET for charge and discharge control controlled by the back-gate voltage generator circuit as set forth above.

According to one aspect of the present invention, there is provided a charge and discharge protection circuit protecting a secondary battery from overcharge, overdischarge, discharge overcurrent,

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and charge overcurrent by detecting the overcharge, overdischarge, discharge overcurrent, and charge overcurrent of the secondary battery, the charge and discharge protection circuit including the four-
5 terminal back gate switching MOSFET for charge and discharge control as set forth above as an FET for charge and discharge control provided in a charge and discharge path.

According to one aspect of the present
10 invention, there is provided a battery pack including the charge and discharge protection circuit as set forth above.

According one aspect of the present
invention, there is provided an electronic apparatus
15 including the battery pack as set forth above.

Examples of the electronic apparatus may include a cellular phone, a digital camera, an audio apparatus, and a game apparatus.

The back-gate voltage generator circuit as
20 set forth above may further include a first inverter to which a control signal generated from one of detection signals of overcharge, overdischarge, discharge overcurrent, and charge overcurrent of a secondary battery is input; and a second inverter to
25 which the output of the first inverter is input,

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wherein the output of the first inverter may be input to the gate of the first n-type MOSFET, the output of the second inverter may be input to the gate of the second n-type MOSFET, and the back-gate voltage may be used as a ground-side reference potential of each of the first inverter and the second inverter.

Thus, according to embodiments of the present invention, it is possible to provide a back-gate voltage generator circuit that generates a back-gate voltage for performing on-off control on the charge and discharge path of a charge and discharge protection circuit with a single four-terminal back gate switching FET and controlling the direction of the parasitic diode of the four-terminal back gate switching FET in accordance with detection conditions such as overcharge, overdischarge, and overcurrent; a four-terminal back gate switching FET controlled by the back-gate voltage generator circuit; a charge and discharge protection circuit for a secondary battery using the four-terminal back gate switching FET; a battery pack containing the charge and discharge protection circuit; and an electronic apparatus such as a cellular phone using the battery pack.

Further, it is possible to generate an output for back gate control without causing

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unnecessary currents due to the parasitic diodes of the n-type MOS transistors to flow.

The present invention is not limited to the specifically disclosed embodiment, and variations and
5 modifications may be made without departing from the scope of the present invention.

The present application is based on Japanese Priority Patent Application No. 2006-251999, filed on
September 19, 2006, the entire contents of which are
10 hereby incorporated by reference.

CLAIMS

1. A back-gate voltage generator circuit
generating a back-gate voltage of a four-terminal
5 back gate switching MOSFET for charge and discharge
control, the back-gate voltage generator circuit
comprising:

first and second n-type MOSFETs connected in
series through a common source electrode,

10 wherein a voltage at the common source
electrode of the first and second n-type MOSFETS
connected in series serves as the back-gate voltage
of the four-terminal back gate switching MOSFET, and
the back-gate voltage is used as a reference voltage
15 for generating signals for controlling the first and
second n-type MOSFETS.

2. The back-gate voltage generator circuit
as claimed in claim 1, further comprising:

20 a first inverter to which a control signal
generated from one of detection signals of overcharge,
overdischarge, discharge overcurrent, and charge
overcurrent of a secondary battery is input; and

a second inverter to which an output of the
25 first inverter is input,

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wherein the output of the first inverter is input to a gate of the first n-type MOSFET,

an output of the second inverter is input to a gate of the second n-type MOSFET, and

5 the back-gate voltage is used as a ground-side reference potential of each of the first inverter and the second inverter.

3. A four-terminal back gate switching
10 MOSFET for charge and discharge control controlled by the back-gate voltage generator circuit as set forth in claim 1.

4. A charge and discharge protection
15 circuit protecting a secondary battery from overcharge, overdischarge, discharge overcurrent, and charge overcurrent by detecting the overcharge, the overdischarge, the discharge overcurrent, and the charge overcurrent of the secondary battery, the
20 charge and discharge protection circuit comprising:

a four-terminal back gate switching MOSFET for charge and discharge control as an FET for the charge and discharge control provided in a charge and discharge path, the four-terminal back gate switching
25 MOSFET being controlled by the back-gate voltage

generator circuit as set forth in claim 1.

5. A battery pack, comprising:
a charge and discharge protection circuit
5 protecting a secondary battery from overcharge,
overdischarge, discharge overcurrent, and charge
overcurrent by detecting the overcharge, the
overdischarge, the discharge overcurrent, and the
charge overcurrent of the secondary battery, the
10 charge and discharge protection circuit including a
four-terminal back gate switching MOSFET for charge
and discharge control as an FET for the charge and
discharge control provided in a charge and discharge
path, the four-terminal back gate switching MOSFET
15 being controlled by the back-gate voltage generator
circuit as set forth in claim 1.

6. An electronic apparatus, comprising:
a battery pack including a charge and
20 discharge protection circuit protecting a secondary
battery from overcharge, overdischarge, discharge
overcurrent, and charge overcurrent by detecting the
overcharge, the overdischarge, the discharge
overcurrent, and the charge overcurrent of the
25 secondary battery, the charge and discharge

protection circuit including a four-terminal back gate switching MOSFET for charge and discharge control as an FET for the charge and discharge control provided in a charge and discharge path, the
5 four-terminal back gate switching MOSFET being controlled by the back-gate voltage generator circuit as set forth in claim 1.

7. A cellular phone, comprising:
10 a battery pack including a charge and discharge protection circuit protecting a secondary battery from overcharge, overdischarge, discharge overcurrent, and charge overcurrent by detecting the overcharge, the overdischarge, the discharge
15 overcurrent, and the charge overcurrent of the secondary battery, the charge and discharge protection circuit including a four-terminal back gate switching MOSFET for charge and discharge control as an FET for the charge and discharge
20 control provided in a charge and discharge path, the four-terminal back gate switching MOSFET being controlled by the back-gate voltage generator circuit as set forth in claim 1.

25 8. A digital camera, comprising:

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a battery pack including a charge and discharge protection circuit protecting a secondary battery from overcharge, overdischarge, discharge overcurrent, and charge overcurrent by detecting the
5 overcharge, the overdischarge, the discharge overcurrent, and the charge overcurrent of the secondary battery, the charge and discharge protection circuit including a four-terminal back gate switching MOSFET for charge and discharge
10 control as an FET for the charge and discharge control provided in a charge and discharge path, the four-terminal back gate switching MOSFET being controlled by the back-gate voltage generator circuit as set forth in claim 1.

15

9. An audio apparatus, comprising:
a battery pack including a charge and discharge protection circuit protecting a secondary
20 battery from overcharge, overdischarge, discharge overcurrent, and charge overcurrent by detecting the overcharge, the overdischarge, the discharge overcurrent, and the charge overcurrent of the secondary battery, the charge and discharge
25 protection circuit including a four-terminal back gate switching MOSFET for charge and discharge

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control as an FET for the charge and discharge
control provided in a charge and discharge path, the
four-terminal back gate switching MOSFET being
controlled by the back-gate voltage generator circuit
5 as set forth in claim 1.

10. A game apparatus, comprising:
a battery pack including a charge and
discharge protection circuit protecting a secondary
10 battery from overcharge, overdischarge, discharge
overcurrent, and charge overcurrent by detecting the
overcharge, the overdischarge, the discharge
overcurrent, and the charge overcurrent of the
secondary battery, the charge and discharge
15 protection circuit including a four-terminal back
gate switching MOSFET for charge and discharge
control as an FET for the charge and discharge
control provided in a charge and discharge path, the
four-terminal back gate switching MOSFET being
20 controlled by the back-gate voltage generator circuit
as set forth in claim 1.

FIG.1

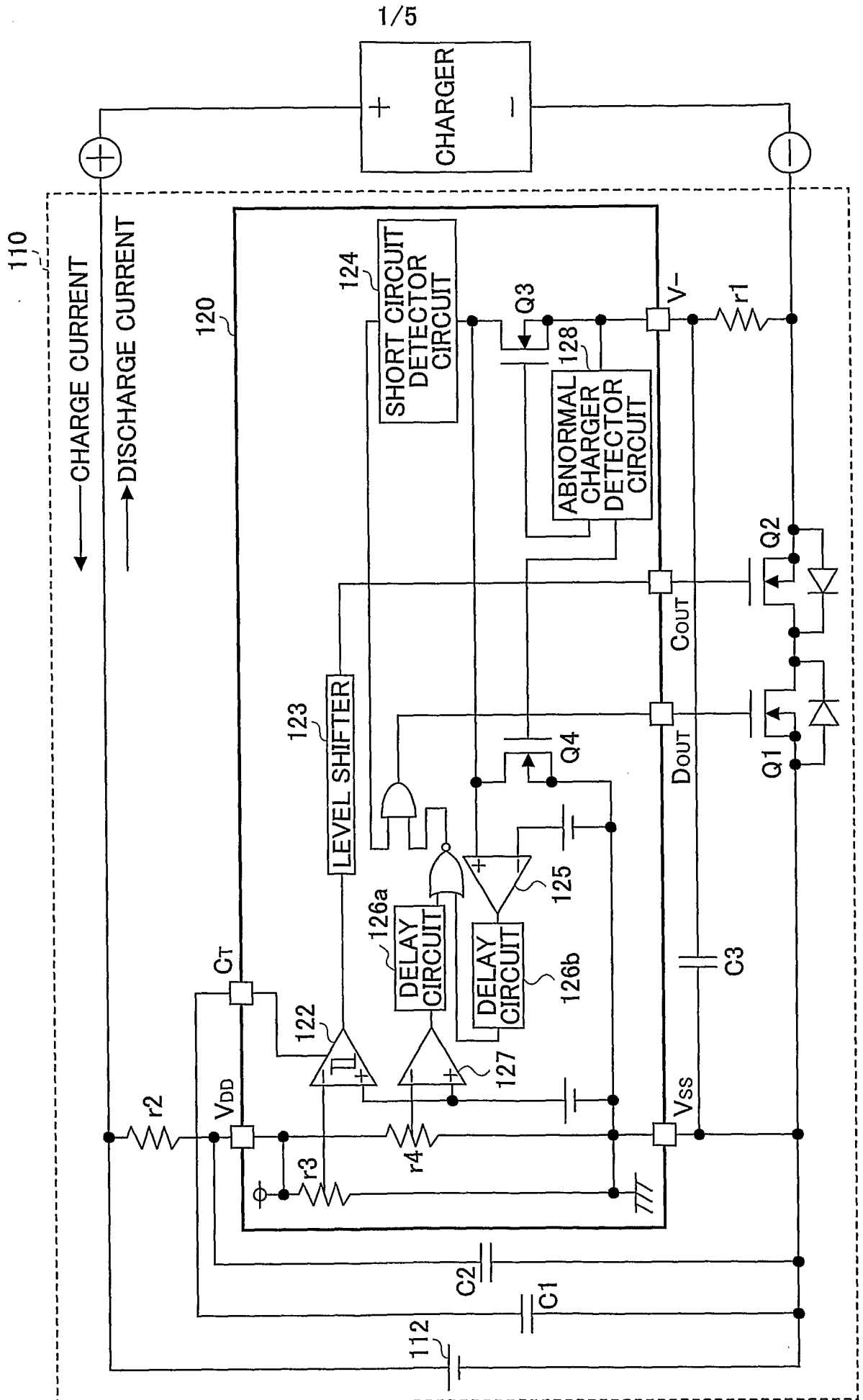


FIG.2

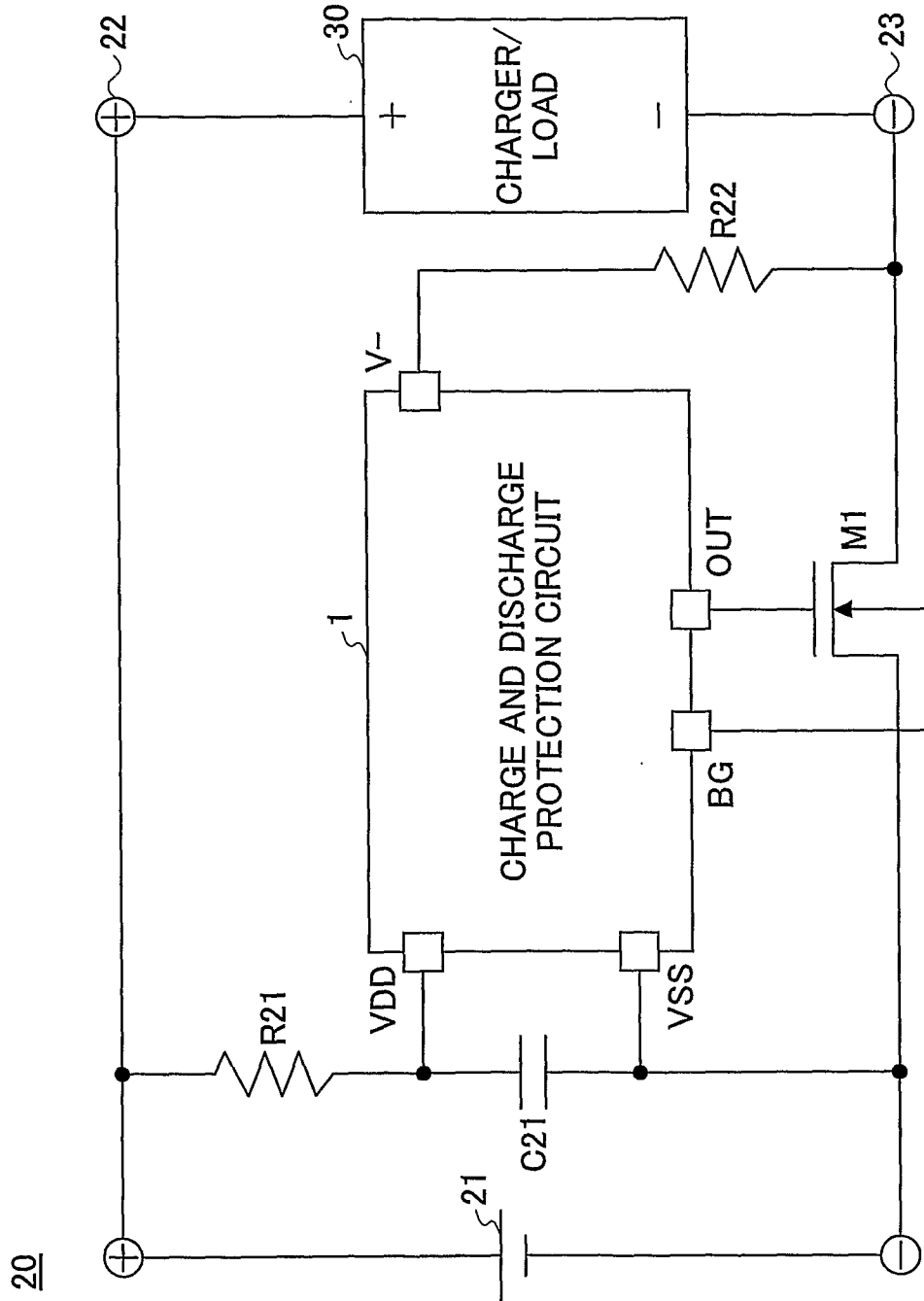
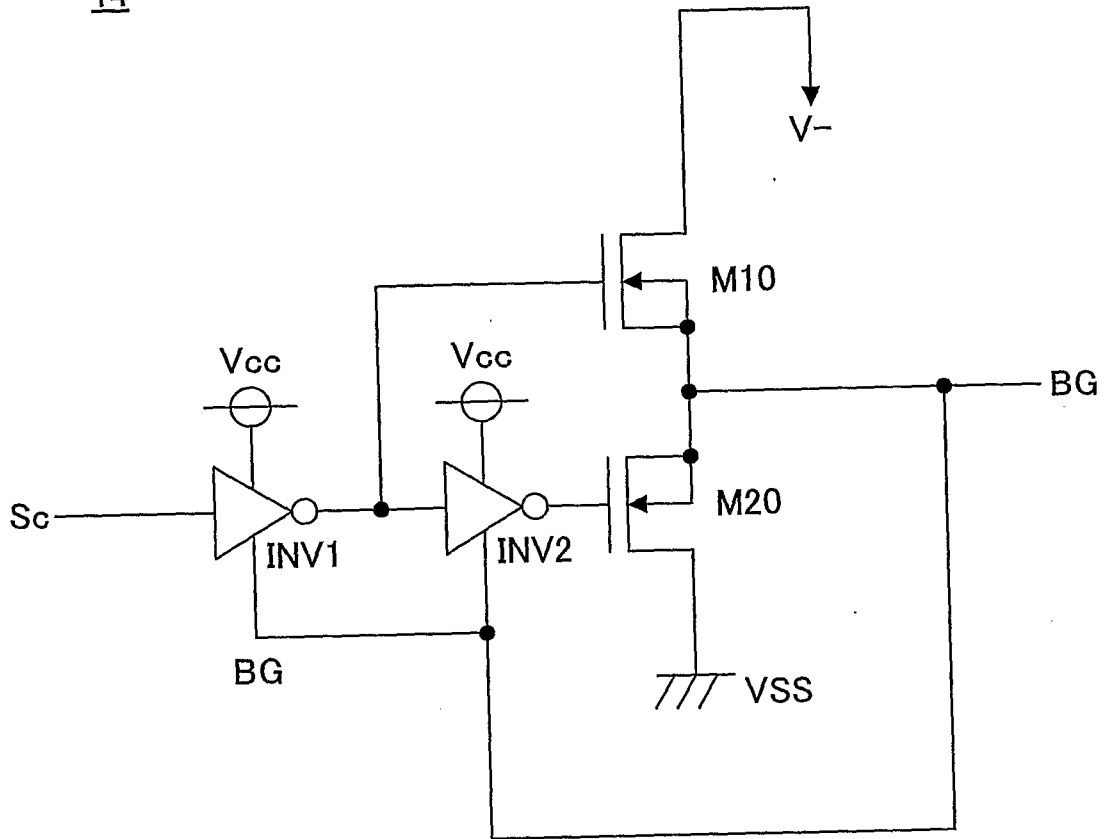


FIG.3

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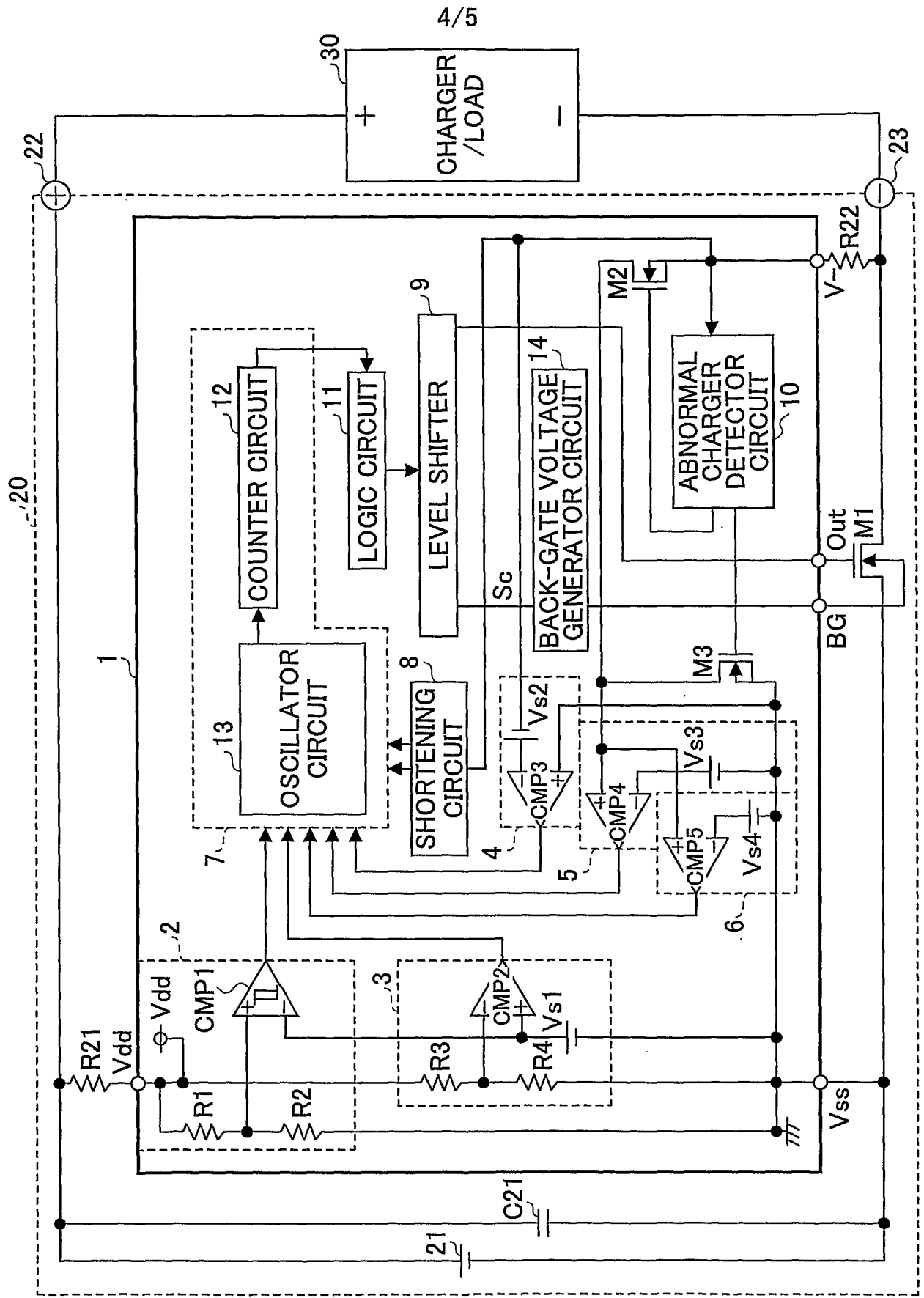


FIG.4

FIG.5

| SEQUENCE | CONTROL SIGNAL | BG OUTPUT | TERMINAL VOLTAGE | PARASITIC DIODE | CHARGE | DISCHARGE | OUT | BACK GATE SWITCHING MOSFET |
|-----------------------|----------------|-----------|------------------|-------------------------|--------|-----------|------|----------------------------|
| ORDINARY | LOW | V- | $V_{ss} = V-$ | $V- \Rightarrow V_{ss}$ | YES | YES | HIGH | ON |
| OVERCHARGED | LOW | V- | $V_{ss} > V-$ | $V- \Rightarrow V_{ss}$ | NO | YES | LOW | OFF |
| OVERDISCHARGED | HIGH | VSS | $V_{ss} < V-$ | $V_{ss} \Rightarrow V-$ | YES | NO | LOW | OFF |
| DISCHARGE OVERCURRENT | HIGH | VSS | $V_{ss} < V-$ | $V_{ss} \Rightarrow V-$ | YES | NO | LOW | OFF |
| CHARGE OVERCURRENT | LOW | V- | $V_{ss} > V-$ | $V- \Rightarrow V_{ss}$ | NO | YES | LOW | OFF |

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2007/066082

| A. CLASSIFICATION OF SUBJECT MATTER | | |
|--|--|--|
| Int.Cl. H02J7/00(2006.01) i, H01M10/44(2006.01) i, H02H7/18(2006.01) i | | |
| According to International Patent Classification (IPC) or to both national classification and IPC | | |
| B. FIELDS SEARCHED | | |
| Minimum documentation searched (classification system followed by classification symbols) | | |
| Int.Cl. H02J7/00, H01M10/44, H02H7/18 | | |
| Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched | | |
| Published examined utility model applications of Japan 1922-1996 Published unexamined utility model applications of Japan 1971-2007 Registered utility model specifications of Japan 1996-2007 Published registered utility model applications of Japan 1994-2007 | | |
| Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) | | |
| C. DOCUMENTS CONSIDERED TO BE RELEVANT | | |
| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
| X A | JP 2006-108568 A(SANYO ELECTRIC CO, LTD.) 2006.04.20, See whole document, Figures 3-4 & US 2006 0076931 A1 & EP 1646148 A2 | 1, 3-10 2 |
| X A | JP 07-227045 A(SONY CORPORATION)1995.08.22 See whole document, Figures 7, 12(Patent Family member(s) NONE) | 1, 3-10 2 |
| A | JP 2000-124780 A(ROHM CO, LTD.)2000.04.28 See 【0002】 - 【0006】 , Figure 3 & WO 2000/022731 A1 | 2 |
| P, A | JP 2007-068390 A(SANYO ELECTRIC CO, LTD.) 2007.03.15, See whole document, Figures 1-8 (Patent Family member(s) NONE) | 1-10 |
| <input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex. | | |
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| Date of the actual completion of the international search | | Date of mailing of the international search report |
| 02.10.2007 | | 16.10.2007 |
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| | | Telephone No. +81-3-3581-1101 Ext. 3568 |

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| C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT | | |
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| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
| A | JP 09-107075 A(Fuji Electric Co, LTD.) 1997.04.22, See whole document, Figures 1-3 (Patent Family member(s) NONE) | 1-10 |