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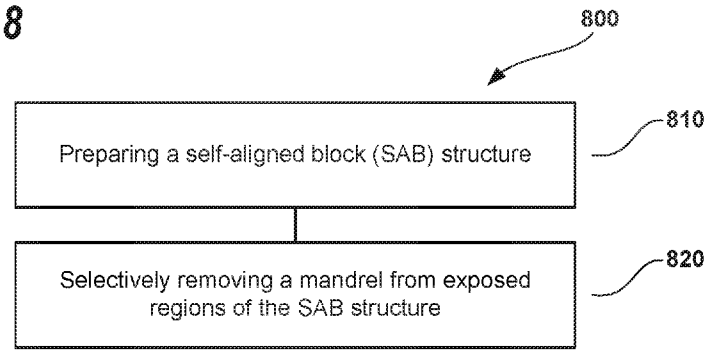
FIG. 8



(57) Abstract: A method of preparing a self-aligned block (SAB) structure is described. The method includes providing a substrate having raised features defined by a first material containing silicon nitride and a second material containing silicon oxide formed on side walls of the first material, and a third material containing an organic material covering some of the raised features and exposing some raised features according to a block pattern formed in the third material. The method further includes forming a first chemical mixture by plasma-excitation of a first process gas, and exposing the first material on the substrate to the first chemical mixture. Thereafter, the method includes forming a second chemical mixture by plasma-excitation of a second process gas, and exposing the first material on the substrate to the second plasma-excited process gas to selectively etch the first material relative to the second and third material.

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METHOD OF ANISOTROPIC EXTRACTION OF SILICON NITRIDE MANDREL FOR FABRICATION OF SELF-ALIGNED BLOCK STRUCTURES

RELATED APPLICATIONS

[0001] The present application claims the benefit of U.S. Provisional Patent Application No. 62/380,603, filed on August 29, 2016, entitled "METHOD OF ANISOTROPIC EXTRACTION OF SILICON NITRIDE MANDREL FOR FABRICATION OF SELF-ALIGNED BLOCK STRUCTURES", which is incorporated herein by reference in its entirety.

FIELD OF INVENTION

[0002] The invention relates to a method for etching, and more particularly, a precision etch technique for etching a thin film for electronic device applications.

BACKGROUND OF THE INVENTION

[0003] The present invention relates to a method of manufacturing a semiconductor device such as an integrated circuit and transistors and transistor components for an integrated circuit. In the manufacture of a semiconductor device (especially on the microscopic scale), various fabrication processes are executed such as film-forming depositions, etch mask creation, patterning, material etching and removal, and doping treatments, are performed repeatedly to form desired semiconductor device elements on a substrate. Historically, with microfabrication, transistors have been created in one plane, with wiring/metallization formed above, and have thus been characterized as two-dimensional (2D) circuits or 2D fabrication. Scaling efforts have greatly increased the number of transistors per unit area in 2D circuits, yet scaling efforts are running into greater challenges as scaling enters single digit nanometer semiconductor device fabrication nodes. Semiconductor device fabricators have expressed a desire for three-dimensional (3D) semiconductor devices in which transistors are stacked on top of each other.

[0004] As device structures densify and develop vertically, the need for precision material etch becomes more compelling. Trade-offs between selectivity, profile,

ARDE (aspect ratio dependent etching), and uniformity in plasma etch processes become difficult to manage. Current approaches to patterning and pattern transfer by balancing these trade-offs is not sustainable. The root cause for these trade-offs is the inability to control ion energy, ion flux, and radical flux independently. However, self-limiting processes, such as atomic layer etching (ALE), offer a viable route to escape these trade-offs by decoupling the etch process into sequential steps of surface modification and removal of modified surface regions, thereby allowing the segregation of the roles of radical flux and ion flux and energy.

SUMMARY

[0005] Techniques herein pertain to device fabrication using precision etch techniques.

[0006] A method of preparing a self-aligned block (SAB) structure is described. The method includes providing a substrate having raised features defined by a first material containing silicon nitride and a second material containing silicon oxide formed on side walls of the first material, and a third material containing an organic material covering some of the raised features and exposing some raised features according to a block pattern formed in the third material. The method further includes forming a first chemical mixture by plasma-excitation of a first process gas containing H and optionally a noble gas, and exposing the first material on the substrate to the first chemical mixture. Thereafter, the method includes forming a second chemical mixture by plasma-excitation of a second process gas containing N, F, O, and optionally a noble element, and exposing the first material on the substrate to the second plasma-excited process gas to selectively etch the first material relative to the second and third material.

[0007] Of course, the order of discussion of the different steps as described herein has been presented for clarity sake. In general, these steps can be performed in any suitable order. Additionally, although each of the different features, techniques, configurations, etc. herein may be discussed in different places of this disclosure, it is intended that each of the concepts can be executed independently of each other or in combination with each other. Accordingly, the present invention can be embodied and viewed in many different ways.

[0008] Note that this summary section does not specify every embodiment and/or incrementally novel aspect of the present disclosure or claimed invention. Instead, this summary only provides a preliminary discussion of different embodiments and corresponding points of novelty over conventional techniques. For additional details and/or possible perspectives of the invention and embodiments, the reader is directed to the Detailed Description section and corresponding figures of the present disclosure as further discussed below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] In the accompanying drawings:

[0010] FIG. 1 illustrates a schematic representation of a method of etching a thin film on a substrate according to an embodiment;

[0011] FIG. 2 provides a flow chart illustrating a method of etching a substrate according to an embodiment;

[0012] FIG. 3 illustrates a result obtained using the method of etching depicted in FIGs. 1 and 2;

[0013] FIGs. 4 and 5 illustrate additional results obtained using the method of etching depicted in FIGs. 1 and 2;

[0014] FIGs. 6A through 6D illustrate various exemplary fabrication sequences to which the method of etching depicted in FIGs. 1 and 2 can be applied according to several embodiments;

[0015] FIGs. 7A and 7B illustrate a schematic representation of a method of etching a thin film on a substrate according to another embodiment;

[0016] FIG. 8 provides a flow chart illustrating a method of etching a substrate according to yet another embodiment; and

[0017] FIGs. 9A through 9D provide schematic illustrations of plasma processing systems for performing the method of etching according to various embodiments.

DETAILED DESCRIPTION

[0018] Techniques herein pertain to device fabrication using precision etch techniques. Several instances manifest in semiconductor manufacturing in both front end of line (FEOL, e.g., transistor fabrication) through to the back end of line

(BEOL, e.g., interconnect fabrication), where oxide and nitride films (typically silicon-containing, in nature) need to be etched with a high degree of precision.

[0019] Numerous fabrication sequences in semiconductor manufacturing demand precision etch techniques. Examples, which will be discussed later, include: (1) gate spacer etch for both 2D (two-dimensional) and 3D (three-dimensional) device structures, (2) spacer etch for sidewall image transfer (SIT) for multi-patterning, (3) mandrel removal from a post-spacer etch SIT structure, and (4) liner etch from a raised structure.

[0020] As another example, fabrication of self-aligned block (SAB) structures has become a critical step in self-aligned double patterning (SADP), self-aligned quadruple patterning (SAQP), and other variations of self-aligned multiple patterning (SAMP). As part of an SAB flow, a silicon nitride mandrel is anisotropically etched with selectivity to an oxide spacer. Current approaches to etch silicon nitride mandrel do not have the required selectivity, which exceeds 15 (i.e., the etch rate of silicon nitride is 15 times greater than the etch rate of silicon oxide) to etch the mandrel without damaging the oxide spacer.

[0021] This invention relates to development of an anisotropic process that can etch silicon nitride mandrel with extremely high selectivity (e.g., > 15, or >20, or >30, or >50, or >80, and even >100) to oxide spacer, thereby enabling SAB fabrication flows.

[0022] According to several embodiments, FIGs. 1 and 2 illustrate a method of etching a thin film. The method, depicted as flow chart 200, includes providing a substrate having a first material 100 containing silicon nitride and a second material (not shown) that is different from the first material 100, forming a first chemical mixture by plasma-excitation of a first process gas containing H and optionally a noble gas in step 210, and exposing the first material on the substrate to the first chemical mixture in step 220, the combination of which is depicted as 102 in FIG. 1. Thereafter, the method includes forming a second chemical mixture by plasma-excitation of a second process gas containing N, F, O, and optionally a noble element in step 230, and exposing the first material 100 on the substrate to the second plasma-excited process gas to selectively etch the first material 100 relative to the second material in step 240, the combination of which is depicted as 104 in FIG. 1.

[0023] The first material 100, to be etched, contains, consists essentially of, or consists of silicon nitride, expressed as Si_3N_4, or more generically Si_xN_y, wherein x and y are real number greater than zero. The second material (not shown) can include silicon oxide, e.g., SiO_2, or other silicon-containing material, a metal or metal-containing material, or an organic material, such as an organic planarization layer (OPL), resist, or antireflective coating (ARC).

[0024] As set forth above, the first chemical mixture is formed from the plasma excitation of a first process gas. The first process gas contains hydrogen (H), and can include atomic hydrogen (H), molecular hydrogen (H_2), metastable hydrogen, hydrogen radical, or hydrogen ions, or any combination of two or more thereof. In one embodiment, the first process gas includes H_2, or H_2 and Ar. In another embodiment, the first process gas consists essentially of or consists of H_2. In yet another embodiment, the first process gas consists essentially of or consists of H_2 and Ar.

[0025] As also set forth above, the second chemical mixture is formed from the plasma excitation of a second process gas. The second process gas contains nitrogen (N), fluorine (F), and oxygen (O), and can optionally include a noble element, such as Ar (argon). In one embodiment, the second process gas includes NF_3, O_2, and Ar. In another embodiment, the second process gas consists essentially of or consists of NF_3, O_2, and Ar.

[0026] The plasma-excitation of the first process and/or the second process gas can be performed in-situ (i.e., the first and/or second chemical mixture is formed within a gas-phase, vacuum environment in proximate contact with the substrate), or ex-situ (i.e., the first and/or second chemical mixture is formed within a gas-phase, vacuum environment remotely located relative to the substrate). FIGs. 9A through 9D provide several plasma generating systems that may be used to facilitate plasma-excitation of a process gas. FIG. 9A illustrates a capacitively coupled plasma (CCP) system, wherein plasma is formed proximate a substrate between an upper plate electrode (UEL) and a lower plate electrode (LEL), the lower electrode also serving as an electrostatic chuck (ESC) to support and retain the substrate. Plasma is formed by coupling radio frequency (RF) power to at least one of the electrodes. As shown in FIG. 9A, RF power is coupled to both the upper and lower electrodes, and the power coupling may include differing RF frequencies.

Alternatively, multiple RF power sources may be coupled to the same electrode. Moreover, direct current (DC) power may be coupled to the upper electrode.

[0027] FIG. 9B illustrates an inductively coupled plasma (ICP) system, wherein plasma is formed proximate a substrate between an inductive element (e.g., a planar, or solenoidal/helical coil) and a lower plate electrode (LEL), the lower electrode also serving as an electrostatic chuck (ESC) to support and retain the substrate. Plasma is formed by coupling radio frequency (RF) power to the inductive coupling element. As shown in FIG. 9B, RF power is coupled to both the inductive element and lower electrode, and the power coupling may include differing RF frequencies.

[0028] FIG. 9C illustrates a surface wave plasma (SWP) system, wherein plasma is formed proximate a substrate between a slotted plane antenna and a lower plate electrode (LEL), the lower electrode also serving as an electrostatic chuck (ESC) to support and retain the substrate. Plasma is formed by coupling radio frequency (RF) power at microwave frequencies through a waveguide and coaxial line to the slotted plane antenna. As shown in FIG. 9C, RF power is coupled to both the slotted plane antenna and lower electrode, and the power coupling may include differing RF frequencies.

[0029] FIG. 9D illustrates remote plasma system, wherein plasma is formed in a region remote from a substrate and separated from the substrate by a filter arranged to impede the transport of charged particles from the remote plasma source to a processing region proximate the substrate. The substrate is supported by a lower plate electrode (LEL) that also serves as an electrostatic chuck (ESC) to retain the substrate. Plasma is formed by coupling radio frequency (RF) power to a plasma generating device adjacent the remotely located region. As shown in FIG. 9D, RF power is coupled to both the plasma generating device adjacent the remote region and lower electrode, and the power coupling may include differing RF frequencies.

[0030] The plasma processing systems of FIGs. 9A through 9D are intended to be illustrative of various techniques for implementing the stepped ion/radical process described. Other embodiments are contemplated including both combinations and variations of the systems described.

[0031] Turning now to FIG. 3 and Table 1, a silicon nitride film, deposited by chemical vapor deposition (CVD) (CVD Sin), is exposed to several etching processes together with an adjacent silicon oxide film. In a first example, the two

films are exposed to a hydrogen (H_2) plasma only, according to the conditions provided in Table 1. In this ion-driven, hydrogen plasma the two films are not etched and no selectivity between films is observed. In a second example, the two films are exposed to plasma composed of NF_3 and O_2. In this radical-driven plasma, eleven (11) Angstroms are etched from the silicon nitride film and only one (1) Angstrom is etched from the silicon oxide film, thus, leading to an etch selectivity of 11-to-1. In a third example, the two films are sequentially exposed to the hydrogen (H_2) plasma, and then exposed to the plasma composed of NF_3 and O_2. In this radical and ion-driven sequential plasma, sixty one (61) Angstroms are etched from the silicon nitride film and substantially no etching is observed of the silicon oxide film, thus, leading to an etch selectivity exceeding 60-to-1.

Tool: CCP, ICP, RLSA H2 plasma:20-100mT, HF 0W, LF 25-100W, 500H2/50Ar,15C,15-60sec NF3-O2 plasma:100-500mT, HF 0-1000W, LF 15-100W, 480NF3/160O2/1000Ar,15C,5-60sec				
Step	Dominant plasma species	Etch Amount (Å)		Selectivity
		CVD SiN	Oxide	SiN-Oxide
H2 plasma only	Ion-driven	-0.6	-3	No sputtering
NF3-O2 plasma only	Radical-driven	11	1	>11
H2+NF3-O2 plasma		61	-1	>60

Table 1

[0032] The inventors surmise that hydrogen ions during the hydrogen plasma step enrich a surface region of the silicon nitride and the silicon oxide, leading to elevated sub-surface hydrogen concentrations; see FIGs. 4 and 5. As shown in FIG. 5, the hydrogen content increases in region 1 (heavily modified sub-surface region) to a maximum, then decays through moderate concentration levels in region 2 (moderately modified sub-surface region), until it decays to low levels in region 3 (pristine or original material). Then, the NF_3 and O_2 plasma creates radicals that selectively react with the hydrogenated silicon nitride and volatilize at a rate greater than with the second material, e.g., silicon oxide or organic material. FIG. 3 illustrates the etch amounts achieved with each exemplary process. And, as shown in FIG. 4, the etch amount achieved during the NF_3 and O_2 step decreases (or the etch rate decays) as the etching proceeds through the sub-surface regions from relatively high hydrogen concentration to relatively low hydrogen concentration.

[0033] In FIGs. 6A through 6D, several examples are provide of fabrication sequences in semiconductor manufacturing that demand precision etch techniques. In each example, it is necessary to remove silicon nitride with high selectivity to other materials, and the examples include: (1) gate spacer etch for both 2D (two-dimensional) and 3D (three-dimensional) device structures, (2) spacer etch for sidewall image transfer (SIT) for multi-patterning, (3) mandrel removal from a post-spacer etch SIT structure, and (4) liner etch from a raised structure. FIG. 6A illustrates selectively removing a silicon nitride 615 from the cap region of the gate structure 610. FIG. 6B illustrates selectively removing a silicon nitride 625 from a cap region and footer region surrounding a mandrel 620 utilized in a self-aligned multi-patterning (SAMP) scheme. FIG. 6C illustrates selectively removing a silicon nitride mandrel 635 from a post-spacer etch structure 630 to leave behind double patterned spacer structures. FIG. 6D illustrates selectively removing silicon nitride liners 645 to leave behind a raised feature 640.

[0034] In yet another example, the fabrication of self-aligned block (SAB) structures has become a critical step in self-aligned double patterning (SADP), self-aligned quadruple patterning (SAQP), and other variations of self-aligned multiple patterning (SAMP). As part of an SAB flow, a silicon nitride mandrel is anisotropically etched with selectivity to an oxide spacer. Current approaches to etch silicon nitride mandrel do not have the required selectivity, which exceeds 15 (i.e., the etch rate of silicon nitride is 15 times greater than the etch rate of silicon oxide) to etch the mandrel without damaging the oxide spacer.

[0035] As shown in FIG. 7A, a substrate 700 can include a patterned layer 720 overlying a film stack 710, including one or more optional layers 712, 714, 716 to be etched or patterned. The patterned layer 720 can define an open feature pattern overlying one or more additional layers. The substrate 700 further includes device layers. The device layers can include any thin film or structure on the workpiece into which a pattern is to be transferred, or a target material is to be removed. Furthermore, the patterned layer 720 can include a retention layer 722, and a target layer 724 to be removed.

[0036] The target layer 724 can be composed of silicon nitride. As shown in FIG. 7A, the target layer 724 fills a trench or via 725 within retention layer 722, the trench or via 725 has a depth (D) 727, a width (W) 726, and an aspect ratio (D/W). The aspect ratio can be greater than 3, 4, or 5. For some structures, the aspect ratio can

be greater than 10, 15, or even 20. The width (W) 726 can be less than 50 nm, 40 nm, 30 nm, or 20 nm. In some applications, the width (W) 726 is less than 10 nm. The retention layer 722 can be composed of material selected from the group consisting of silicon oxide (SiO_x), silicon oxynitride (SiO_xN_y), transition metal oxide (e.g., titanium oxide (TiO_x)), transition metal nitride (e.g., titanium oxide (TiN_y)), and silicon-containing organic material having a silicon content ranging from 15% by weight to 50% by weight silicon.

[0037] As an example, the patterned layer 720 in FIG. 7A can include a spacer layer surrounding a mandrel layer used in multi-patterning schemes. Alternatively, for example, the patterned layer 720 in FIG. 1A can include a dummy silicon nitride layer filling a region to be replaced with an advanced gate structure, such as a metal gate structure.

[0038] The substrate 700 can include a bulk silicon substrate, a single crystal silicon (doped or un-doped) substrate, a semiconductor-on-insulator (SOI) substrate, or any other semiconductor substrate containing, for example, Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP, as well as other III/V or II/VI compound semiconductors, or any combination thereof (Groups II, III, V, VI refer to the classical or old IUPAC notation in the Periodic Table of Elements; according to the revised or new IUPAC notation, these Groups would refer to Groups 2, 13, 15, 16, respectively). The substrate 700 can be of any size, for example, a 200 mm (millimeter) substrate, a 300 mm substrate, a 450 mm substrate, or an even larger substrate. The device layers can include any film or device structure into which a pattern can be transferred.

[0039] Organic layer 721 blankets various regions of substrate 700, and exposes block regions within which the silicon nitride mandrel is to be removed from high aspect ratio features. In FIG. 7B, the silicon nitride mandrel 714 is selectively removed with minimal impact to the silicon oxide spacers and the organic fill layer 721.

[0040] FIG. 8 depicts a flow chart 800 for etching a substrate according to another embodiment. In 810, a self-aligned block (SAB) structure is prepared. And, in 820, a mandrel is removed from an exposed region of the SAB structure. FIG. 2 depicts a method of selectively etching a silicon nitride mandrel from a high expect ratio feature to leave behind silicon oxide spacers. The aspect ratio can exceed ten (10, and the etch selectivity for removing the silicon nitride mandrel relative to other

materials, e.g., silicon oxide and organic material, can exceed 20-to-1, or 50-to-1, or even 100-to-1.

[0041] In the claims below, any of the dependents limitations can depend from any of the independent claims.

[0042] In the preceding description, specific details have been set forth, such as a particular geometry of a processing system and descriptions of various components and processes used therein. It should be understood, however, that techniques herein may be practiced in other embodiments that depart from these specific details, and that such details are for purposes of explanation and not limitation. Embodiments disclosed herein have been described with reference to the accompanying drawings. Similarly, for purposes of explanation, specific numbers, materials, and configurations have been set forth in order to provide a thorough understanding. Nevertheless, embodiments may be practiced without such specific details. Components having substantially the same functional constructions are denoted by like reference characters, and thus any redundant descriptions may be omitted.

[0043] Various techniques have been described as multiple discrete operations to assist in understanding the various embodiments. The order of description should not be construed as to imply that these operations are necessarily order dependent. Indeed, these operations need not be performed in the order of presentation. Operations described may be performed in a different order than the described embodiment. Various additional operations may be performed and/or described operations may be omitted in additional embodiments.

[0044] "Substrate" or "target substrate" as used herein generically refers to an object being processed in accordance with the invention. The substrate may include any material portion or structure of a device, particularly a semiconductor or other electronics device, and may, for example, be a base substrate structure, such as a semiconductor wafer, reticle, or a layer on or overlying a base substrate structure such as a thin film. Thus, substrate is not limited to any particular base structure, underlying layer or overlying layer, patterned or un-patterned, but rather, is contemplated to include any such layer or base structure, and any combination of layers and/or base structures. The description may reference particular types of substrates, but this is for illustrative purposes only.

[0045] Those skilled in the art will also understand that there can be many variations made to the operations of the techniques explained above while still achieving the same objectives of the invention. Such variations are intended to be covered by the scope of this disclosure. As such, the foregoing descriptions of embodiments of the invention are not intended to be limiting. Rather, any limitations to embodiments of the invention are presented in the following claims.

CLAIMS

1. A method of preparing a self-aligned block (SAB) structure, comprising:

providing a substrate having raised features defined by a first material containing silicon nitride and a second material containing silicon oxide formed on side walls of the first material, and a third material containing an organic material covering some of the raised features and exposing some raised features according to a block pattern formed in the third material;

forming a first chemical mixture by plasma-excitation of a first process gas containing H and optionally a noble gas;

exposing the first, second, and third materials on the substrate to the first chemical mixture;

thereafter, forming a second chemical mixture by plasma-excitation of a second process gas containing N, F, O, and optionally a noble element; and

exposing the first, second, and third materials on the substrate to the second plasma-excited process gas to selectively etch the first material relative to the second and third materials.

2. The method of claim 1, wherein the first process gas contains H_2.

3. The method of claim 1, wherein the first process gas consists of H_2.

4. The method of claim 1, wherein the first process gas consists of H_2 and Ar.

5. The method of claim 1, wherein the second process gas contains NF_3, O_2, and Ar.

6. The method of claim 1, wherein the second process gas consists of NF_3, O_2, and Ar.

7. The method of claim 1, wherein the first chemical mixture contains hydrogen ions.

8. The method of claim 1, wherein the second chemical mixture contains substantially charge-neutral species.

9. The method of claim 1, wherein the second material is selected from the group consisting of SiO_2 and organic materials.

10. The method of claim 1, wherein the first material includes raised features on the substrate, the second material forms sidewall spacers on the vertical portions of the raised features, and wherein the exposing removes the raised features of the first material but not the sidewall spacers.

11. The method of claim 1, wherein the plasma excitation of the first process gas or the second process gas includes generating plasma using a capacitively coupled plasma source containing an upper plate electrode, and a lower plate electrode supporting the substrate.

12. The method of claim 1, wherein the plasma excitation of the first process gas or the second process gas includes generating plasma using an inductively coupled plasma source containing an inductive element, and a lower plate electrode supporting the substrate.

13. The method of claim 1, wherein the plasma excitation of the first process gas or the second process gas includes generating plasma using a remote plasma source that creates a high radical to ion flux ratio.

14. The method of claim 1, further comprising:

repeating the steps of forming the first chemical mixture, exposing the first material to the first chemical mixture, forming the second chemical mixture, and exposing the first material to the second chemical mixture to incrementally remove additional portions of the first material.

15. The method of claim 1, wherein the first material is removed at an etch selectivity of greater than 100-to-1 relative to the second and third materials.

16. The method of claim 1, wherein the raised feature is a mandrel in a self-aligned multi-patterning process.

17. The method of claim 16, wherein an aspect ratio of the raised feature exceeds 10.

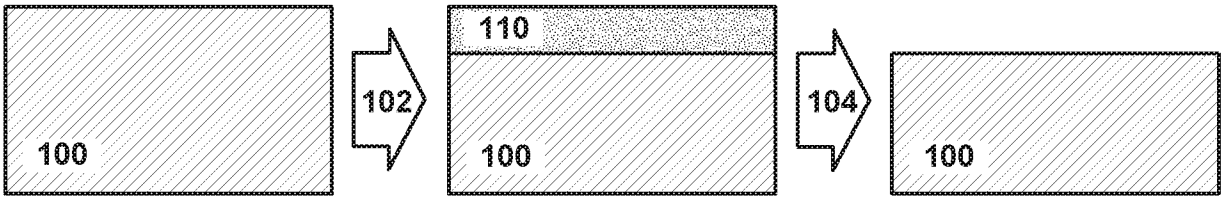

FIG. 1

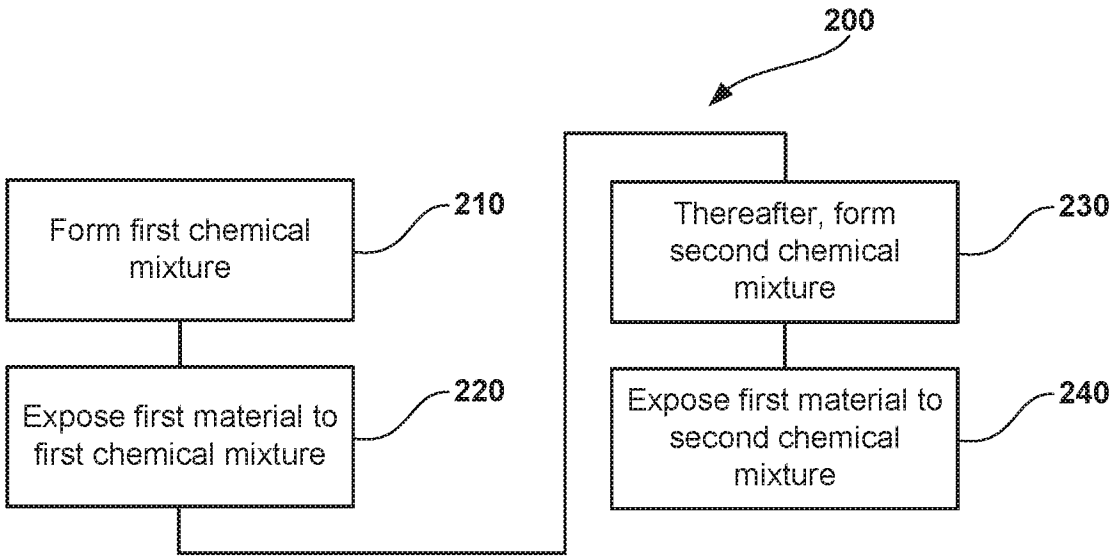

FIG. 2

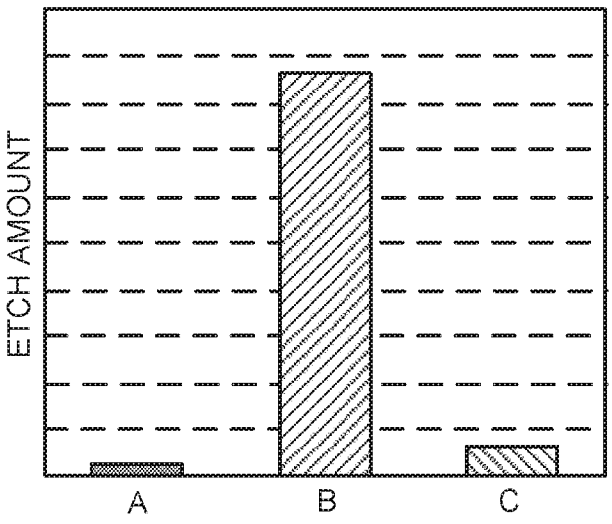

FIG. 3

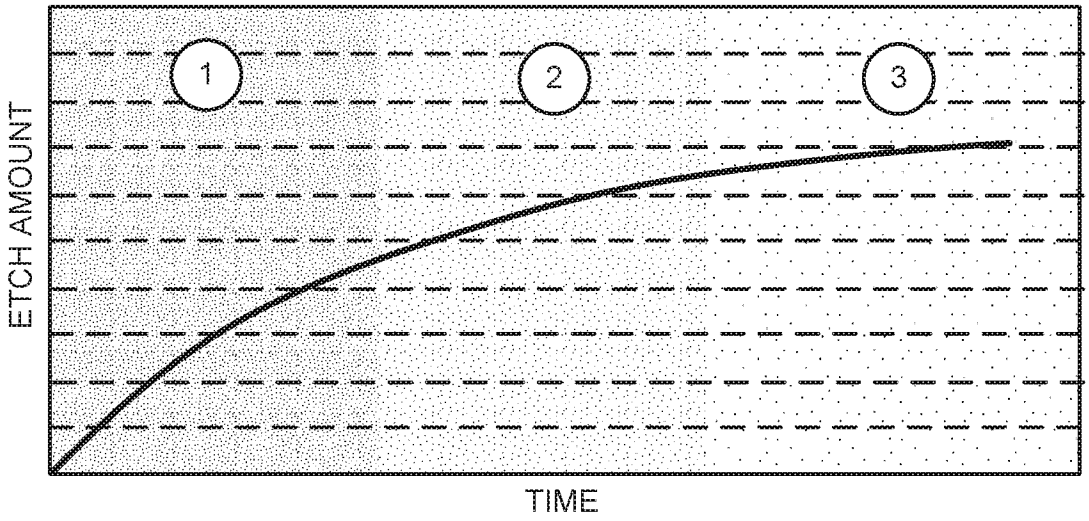

FIG. 4

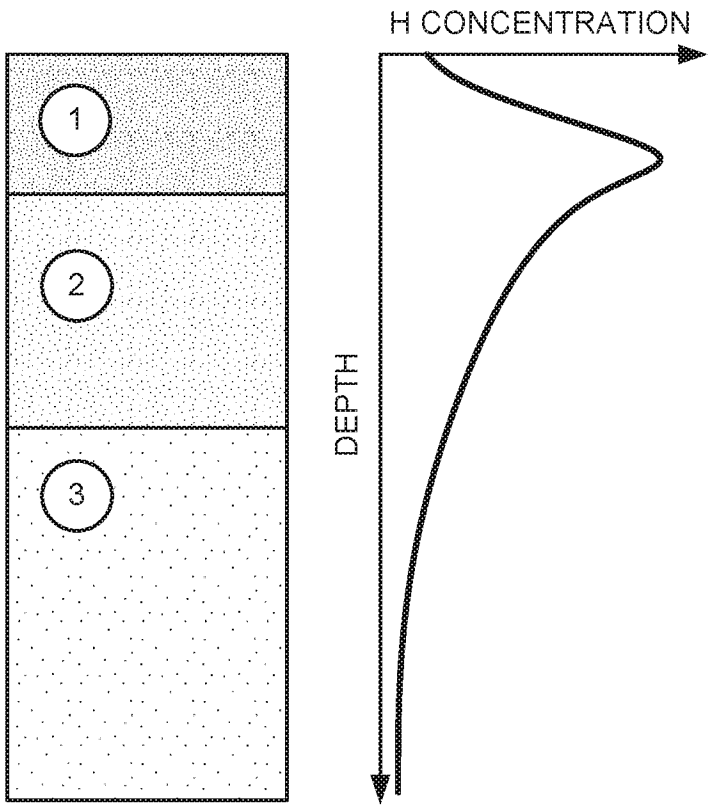

FIG. 5

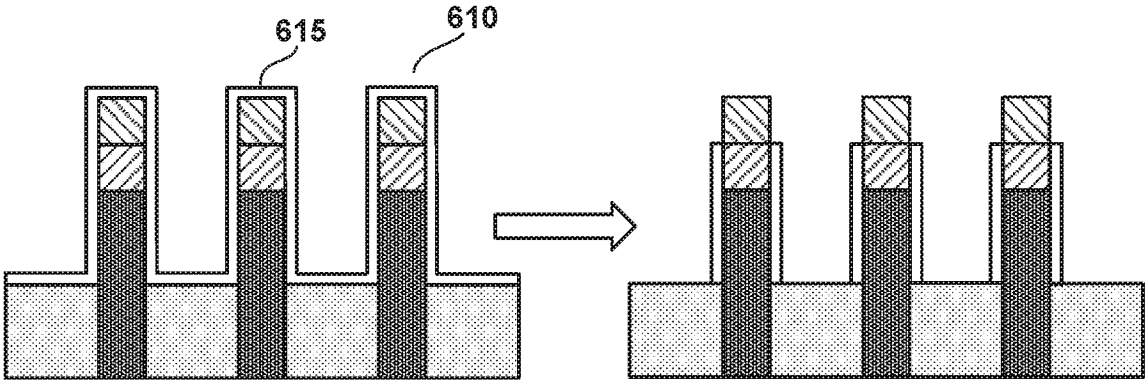

FIG. 6A

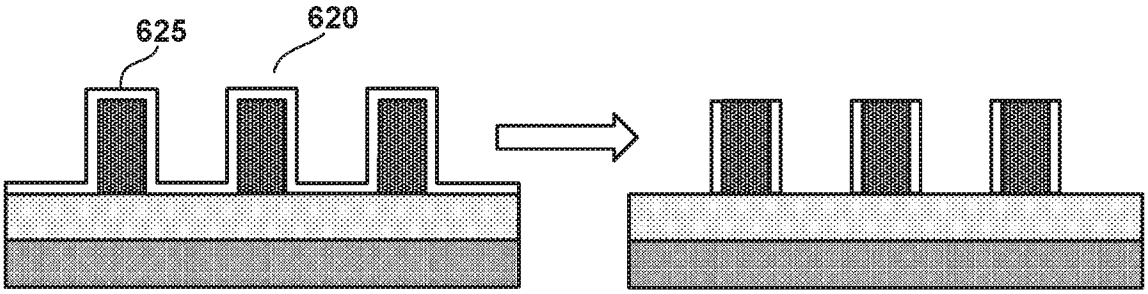

FIG. 6B

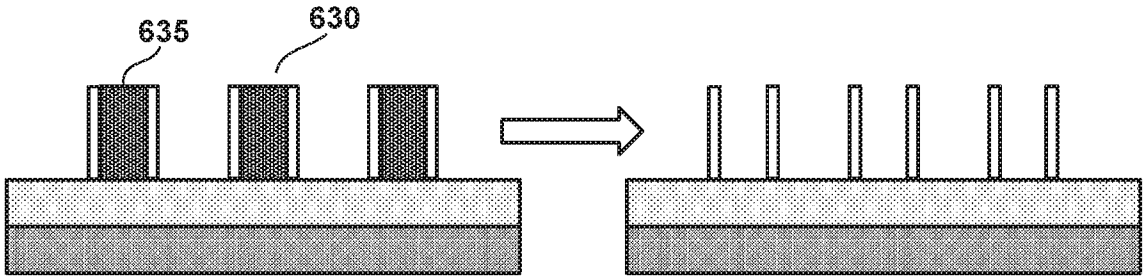

FIG. 6C

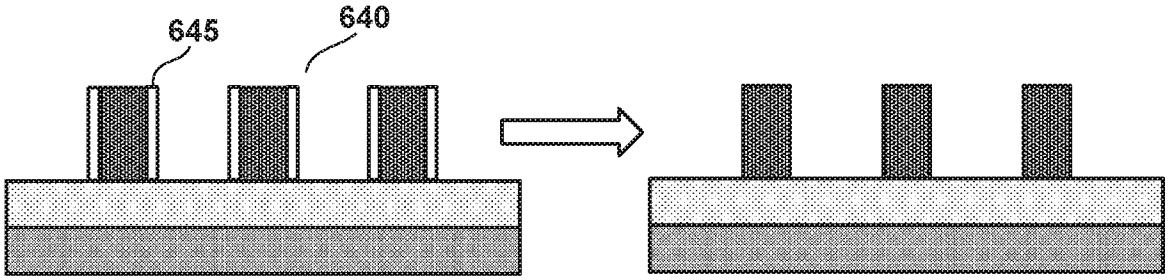

FIG. 6D

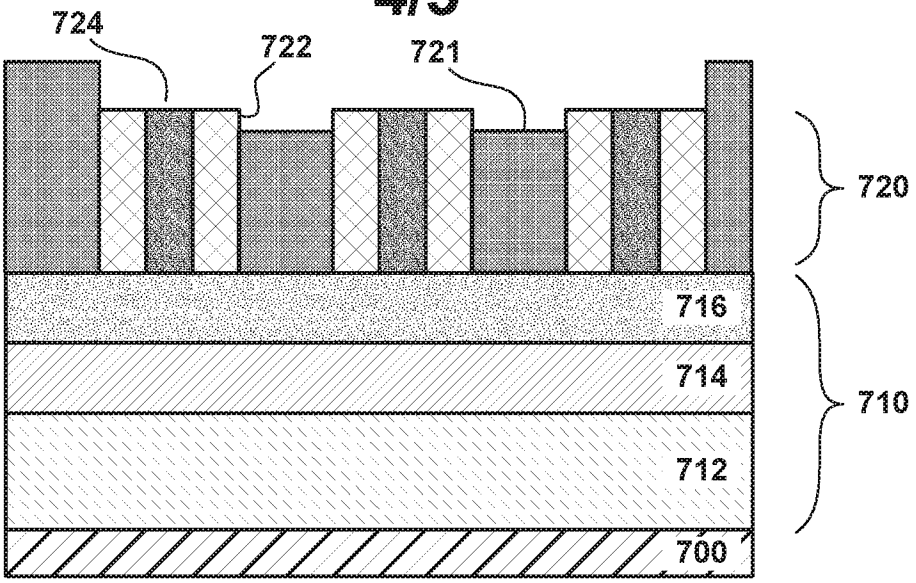

FIG. 7A

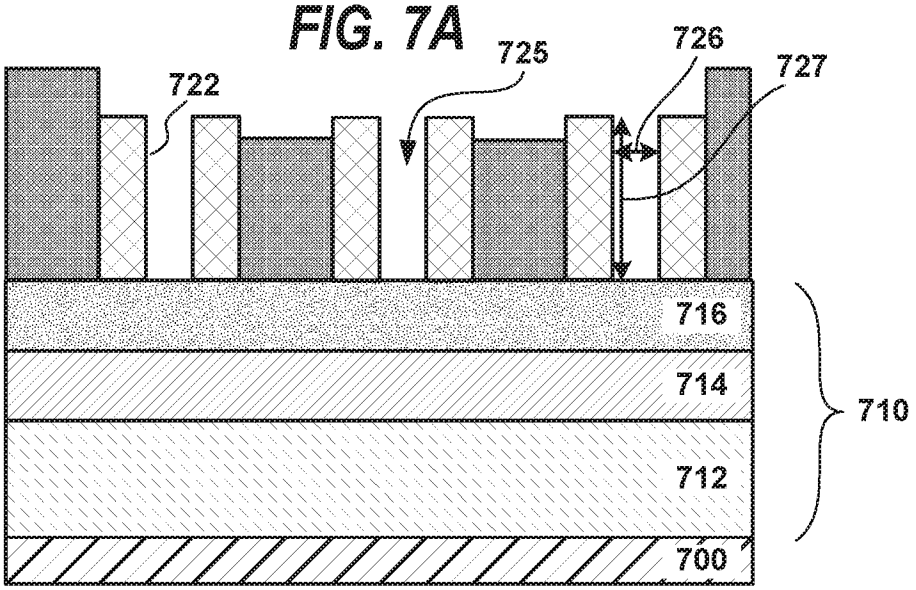

FIG. 7B

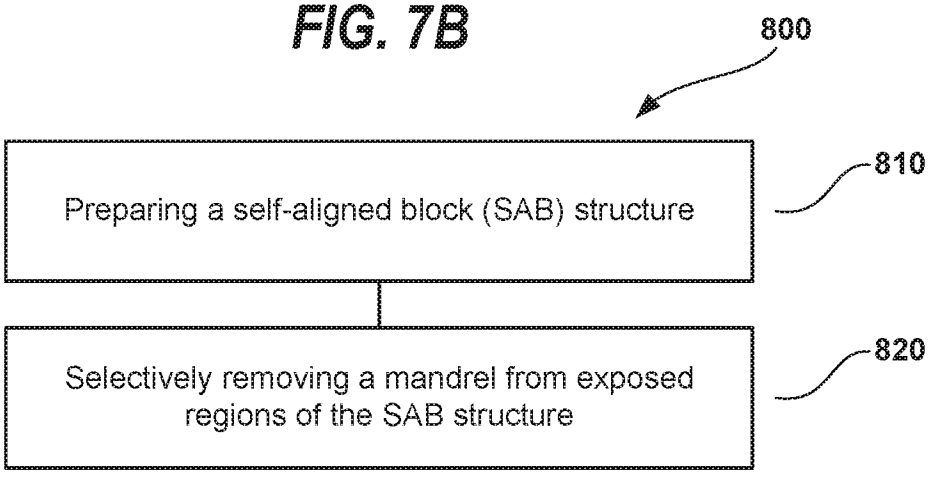

FIG. 8

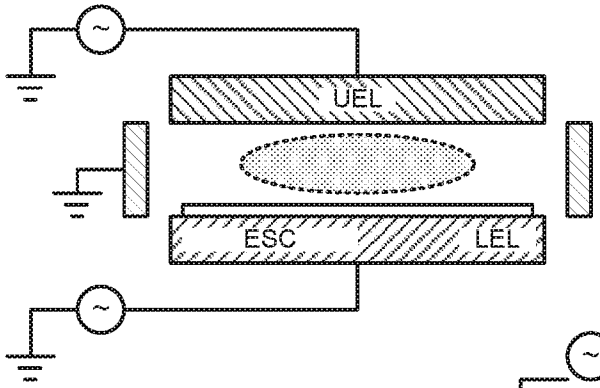

FIG. 9A

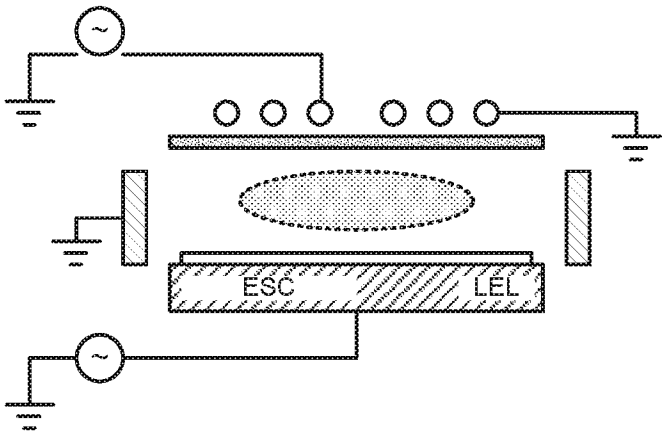

FIG. 9B

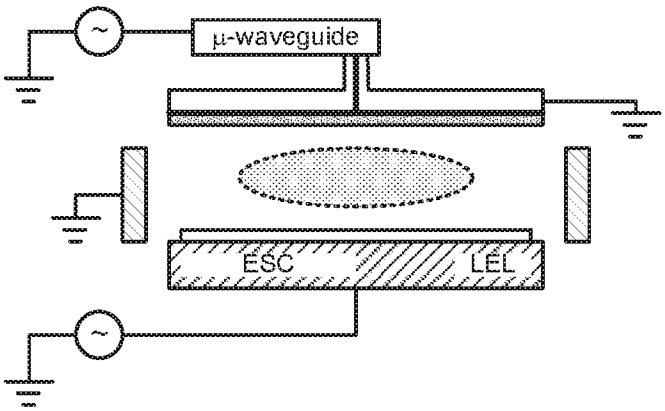

FIG. 9C

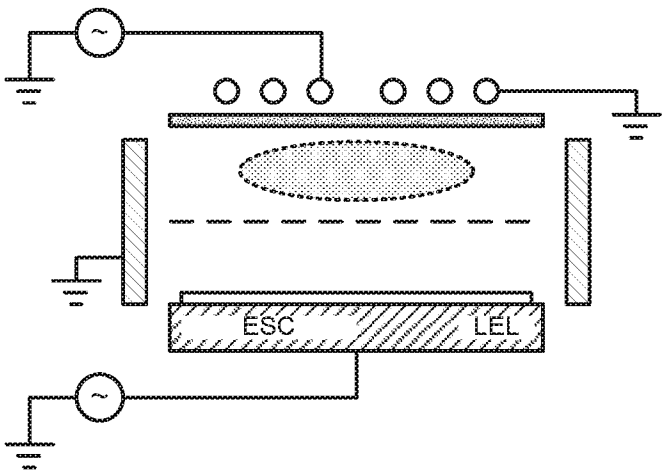

FIG. 9D

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/048689

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/3065(2006.01)i, H01L 21/3213(2006.01)i, H01L 21/311(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/3065; H01L 21/302; H01L 21/311; H01L 21/336; H01L 21/483; H01L 21/214; H01L 21/461; H01L 21/00; H01L 21/3213

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords:self aligned block, silicon nitride, silicon oxide, etch selectivity

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7709396 B2 (CHRISTOPHER DENNIS BENCHER et al.) 04 May 2010 See claims 1, 8, 10, 12 and figure 3H.	1-17
A	US 7977249 B1 (XINYE LIU et al.) 12 July 2011 See column 2, lines 4-11, claims 1, 12, 16 and figure 1.	1-17
A	US 9384997 B2 (APPLIED MATERIALS, INC.) 05 July 2016 See column 3, lines 4-13.	1-17
A	JP 5706946 B2 (TOKYO ELECTRON LTD.) 22 April 2015 See paragraphs [0049]-[0060] and figures 7, 8.	1-17
A	US 9257293 B2 (APPLIED MATERIALS, INC.) 09 February 2016 See claims 1, 4.	1-17

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
05 December 2017 (05.12.2017)	**05 December 2017 (05.12.2017)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/048689

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		WO 2011-108663 A1	09/09/2011
US 9257293 B2	09/02/2016	US 2014-0273292 A1	18/09/2014