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(54) **SELF-ALIGNED SI RICH NITRIDE CHARGE TRAP LAYER ISOLATION FOR CHARGE TRAP FLASH MEMORY**

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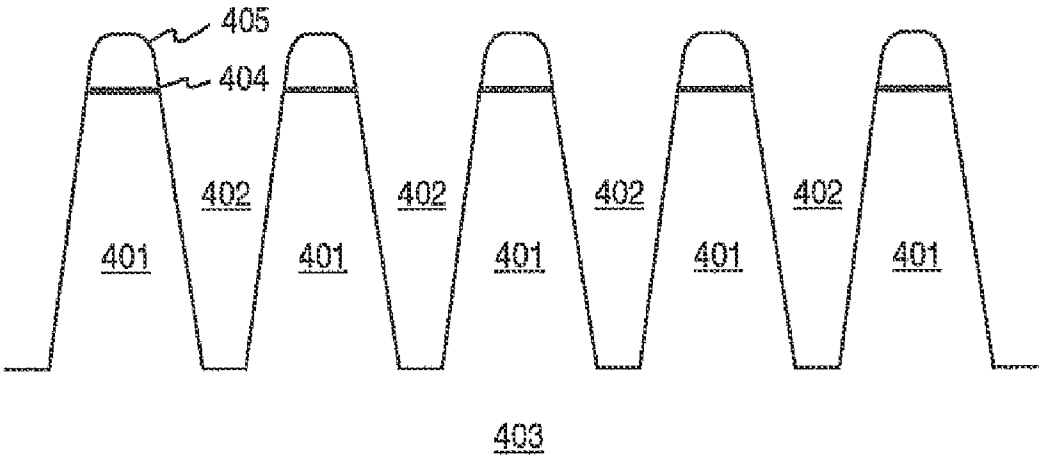
USPC **257/324**

(57) **ABSTRACT**

A method for fabricating a memory device with U-shaped trap layers over rounded active region corners is disclosed. In the present invention, an STI process is performed before the charge-trapping layer is formed. Immediately after the STI process, the sharp corners of the active regions are exposed, making them available for rounding. Rounding the corners improves the performance characteristics of the memory device. Subsequent to the rounding process, a bottom oxide layer, nitride layer, and sacrificial top oxide layer are formed. An organic bottom antireflective coating applied to the charge trapping layer is planarized. Now the organic bottom antireflective coating, sacrificial top oxide layer, and nitride layer are etched, without etching the sacrificial top oxide layer and nitride layer over the active regions. After the etching the charge trapping layer has a cross-sectional U-shape appearance. U-shaped trap layer edges allow for increased packing density and integration while maintaining isolation between trap layers.



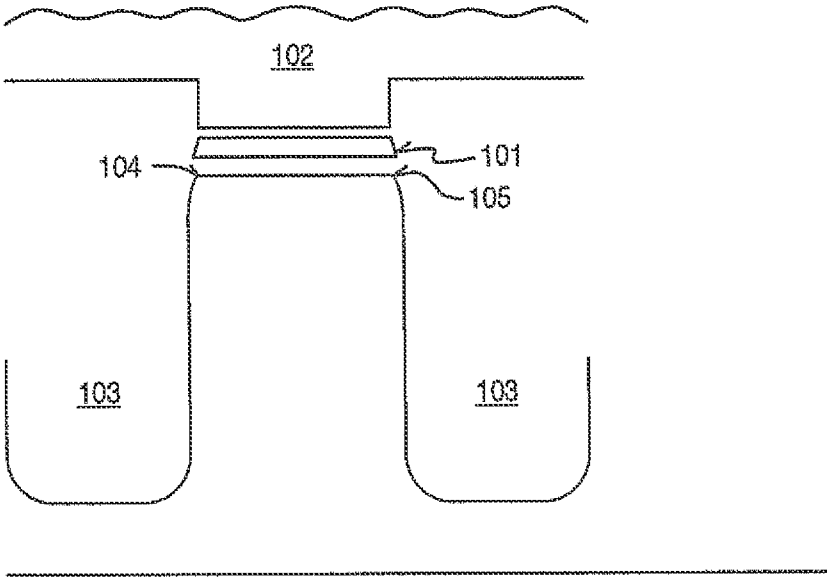


Figure 1
(Prior Art)

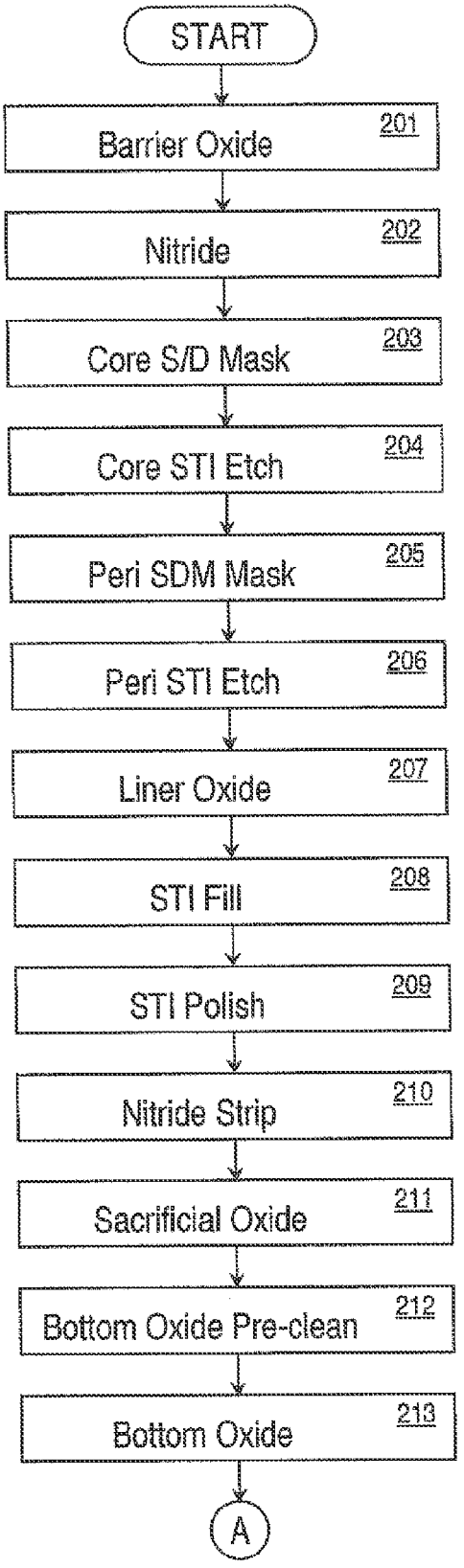

START
Barrier Oxide
201
Nitride
202
Core S/D Mask
203
Core STI Etch
204
Peri SDM Mask
205
Peri STI Etch
206
Liner Oxide
207
STI Fill
208
STI Polish
209
Nitride Strip
210
Sacrificial Oxide
211
Bottom Oxide Pre-clean
212
Bottom Oxide
213
A

Figure 2

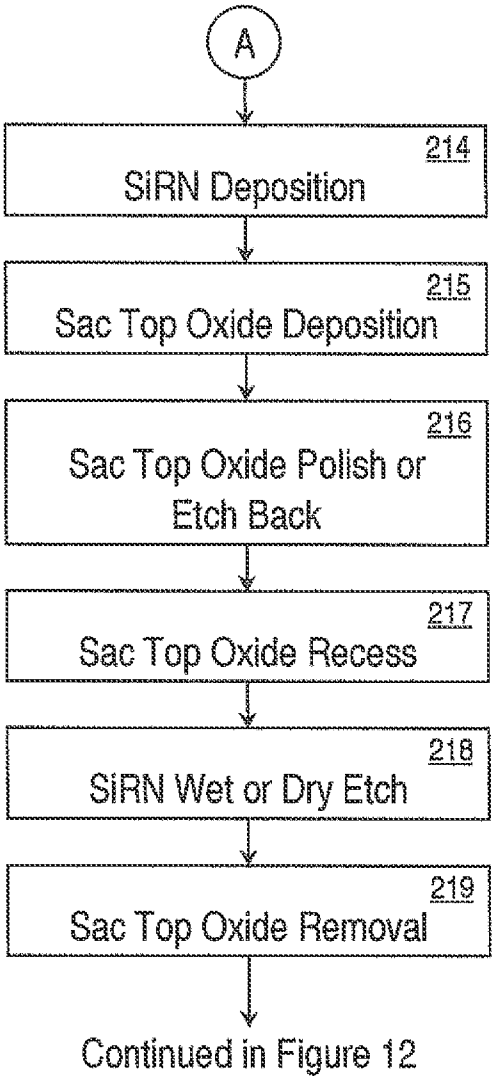

A
214
SiRN Deposition
215
Sac Top Oxide Deposition
216
Sac Top Oxide Polish or Etch Back
217
Sac Top Oxide Recess
218
SiRN Wet or Dry Etch
219
Sac Top Oxide Removal
Continued in Figure 12

Figure 3

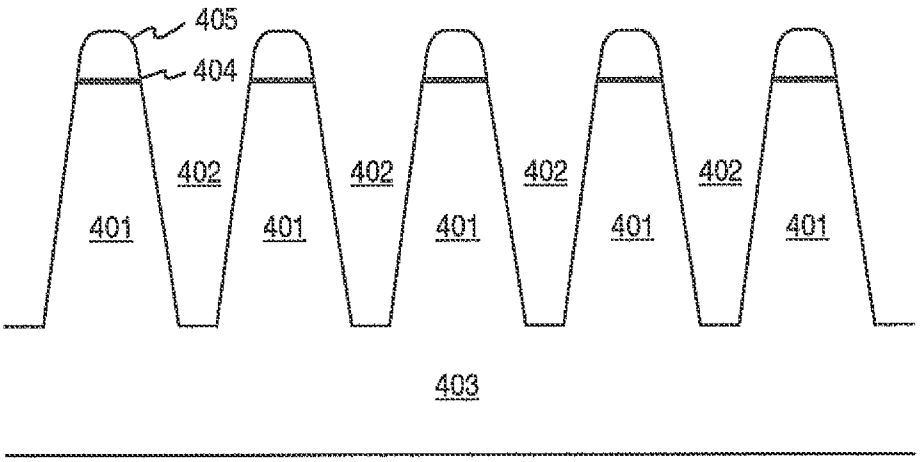


Figure 4

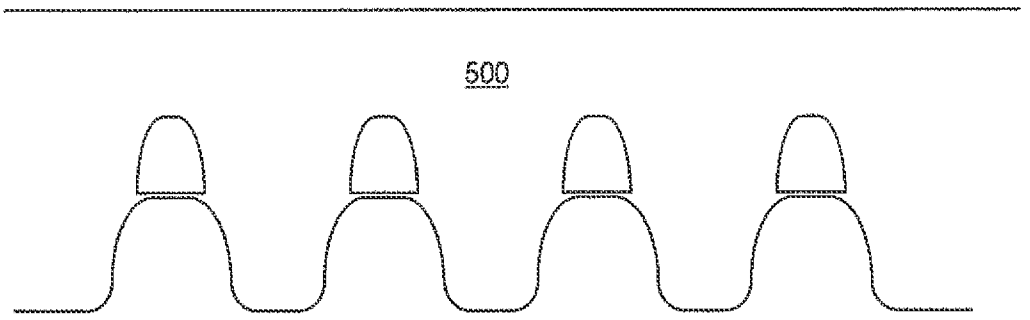


Figure 5

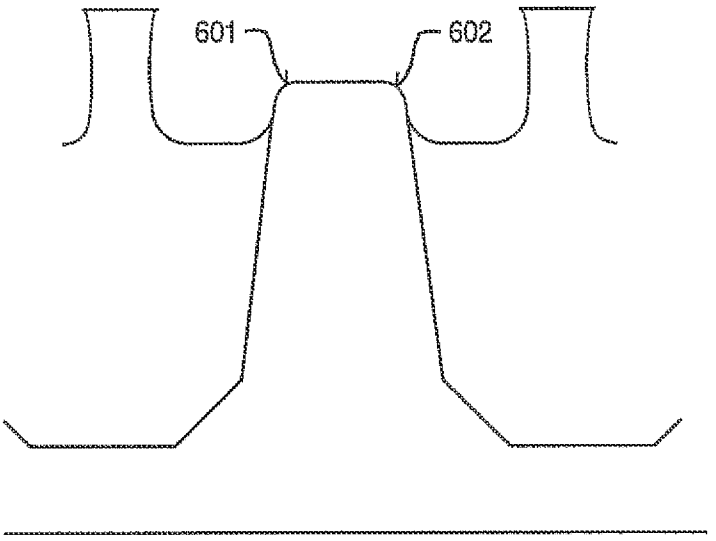


Figure 6

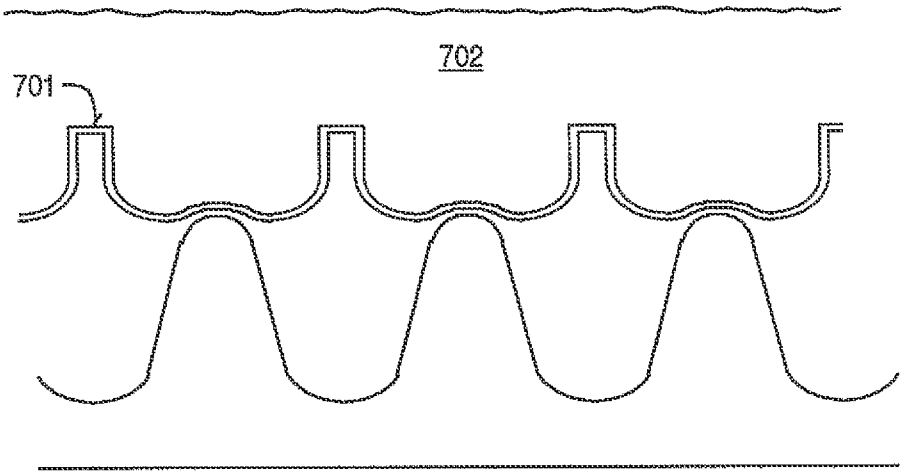


Figure 7

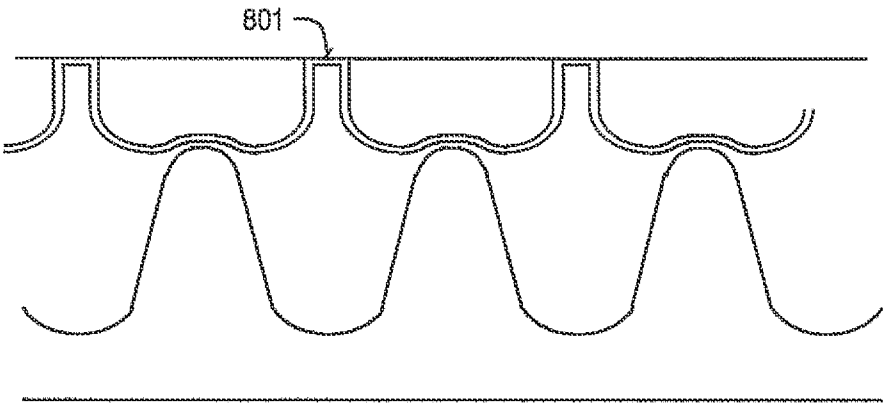


Figure 8

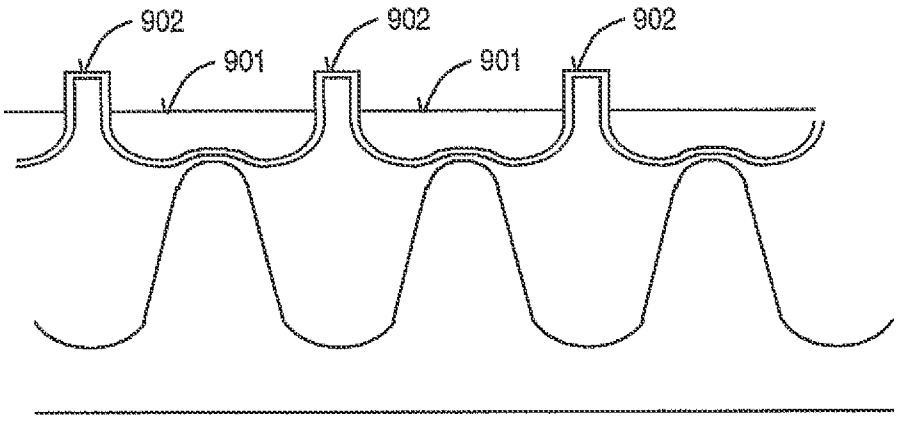


Figure 9

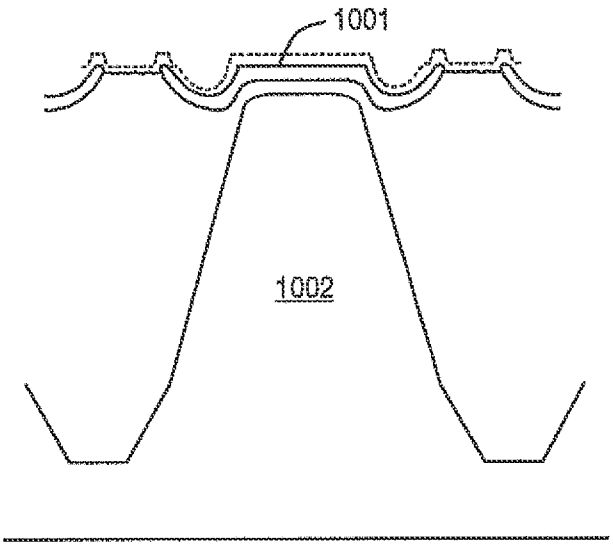


Figure 10

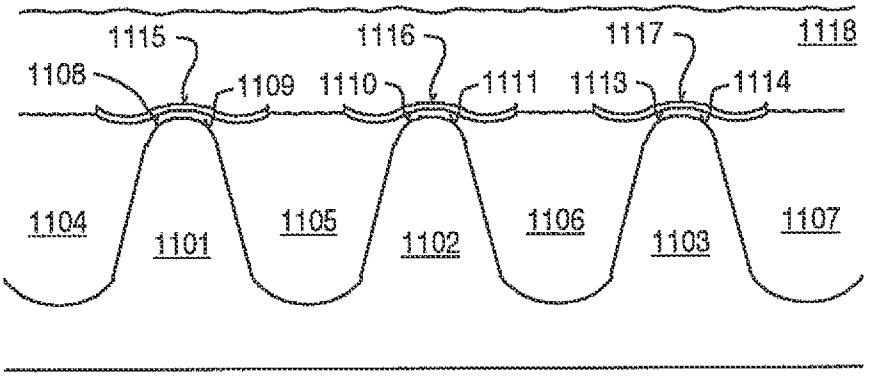

1115
1116
1117
1118
1108
1109
1110
1111
1113
1114
1104
1101
1105
1102
1106
1103
1107

Figure 11

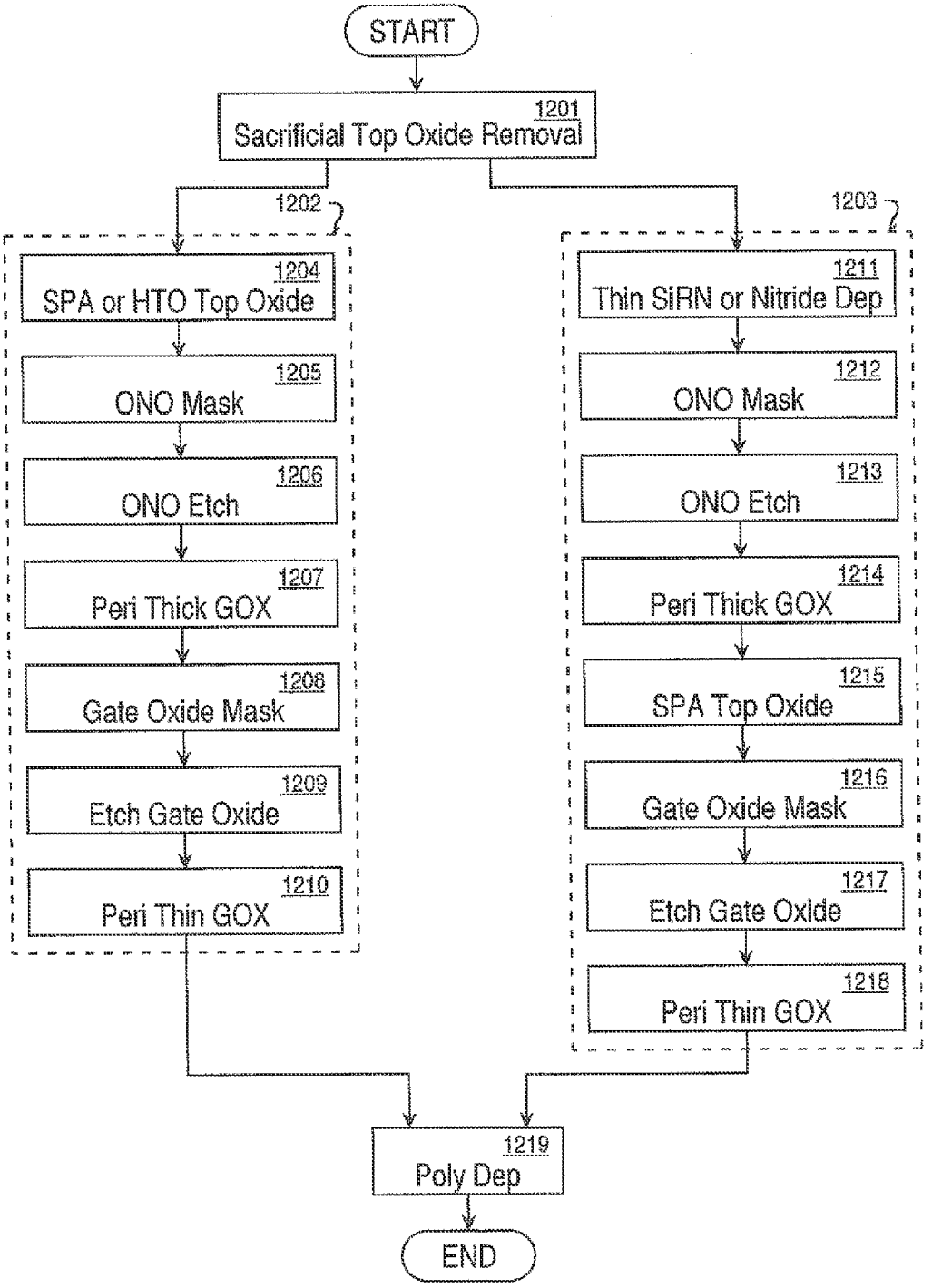

START
1201
Sacrificial Top Oxide Removal
1202
1204
SPA or HTO Top Oxide
1205
ONO Mask
1206
ONO Etch
1207
Peri Thick GOX
1208
Gate Oxide Mask
1209
Etch Gate Oxide
1210
Peri Thin GOX
1203
1211
Thin SiRN or Nitride Dep
1212
ONO Mask
1213
ONO Etch
1214
Peri Thick GOX
1215
SPA Top Oxide
1216
Gate Oxide Mask
1217
Etch Gate Oxide
1218
Peri Thin GOX
1219
Poly Dep
END

Figure 12

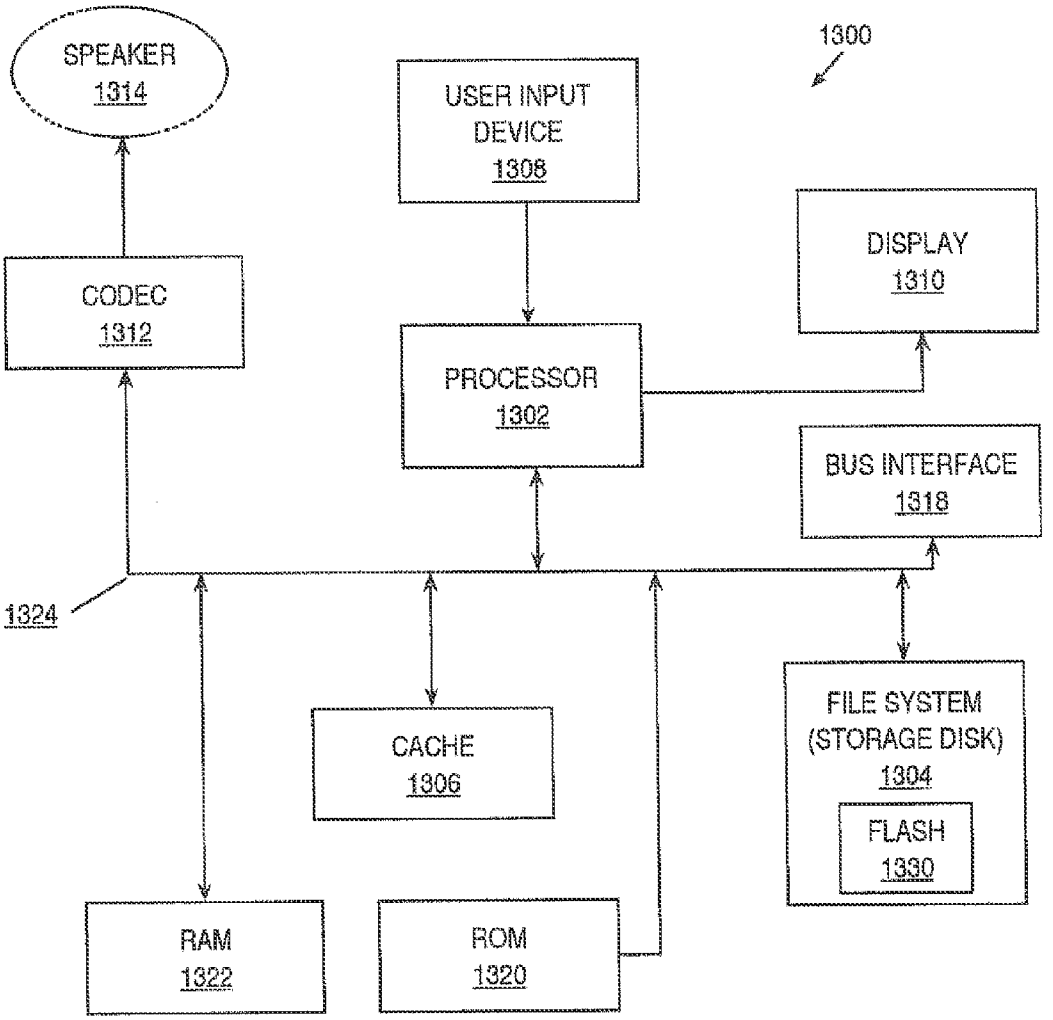

1300
SPEAKER
1314
USER INPUT
DEVICE
1308
DISPLAY
1310
CODEC
1312
PROCESSOR
1302
BUS INTERFACE
1318
1324
CACHE
1306
FILE SYSTEM
(STORAGE DISK)
1304
FLASH
1330
RAM
1322
ROM
1320

Figure 13

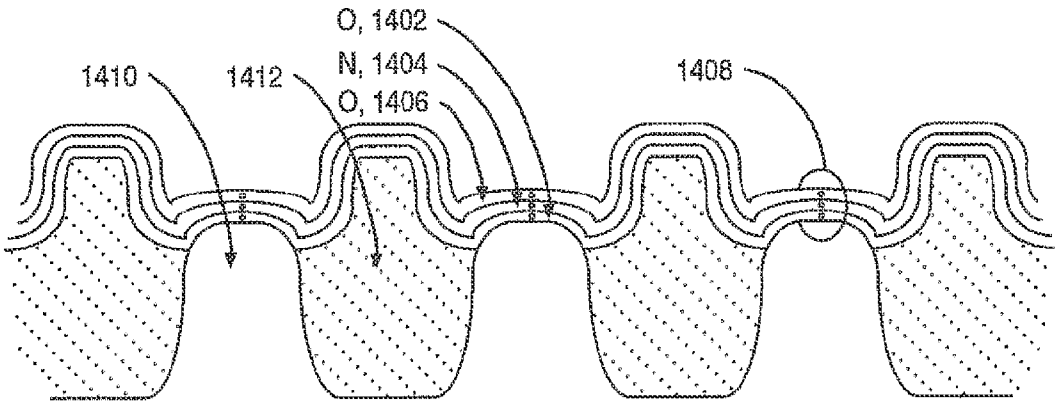


Figure 14

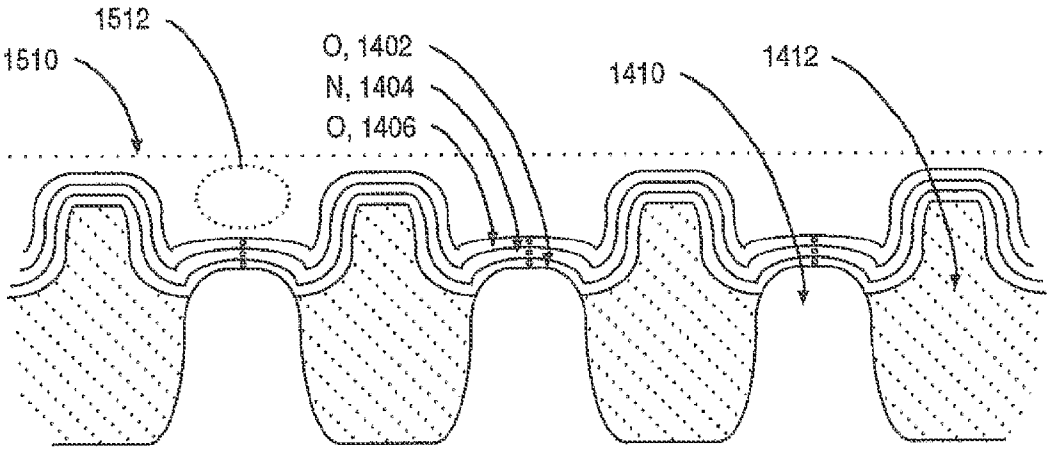


Figure 15

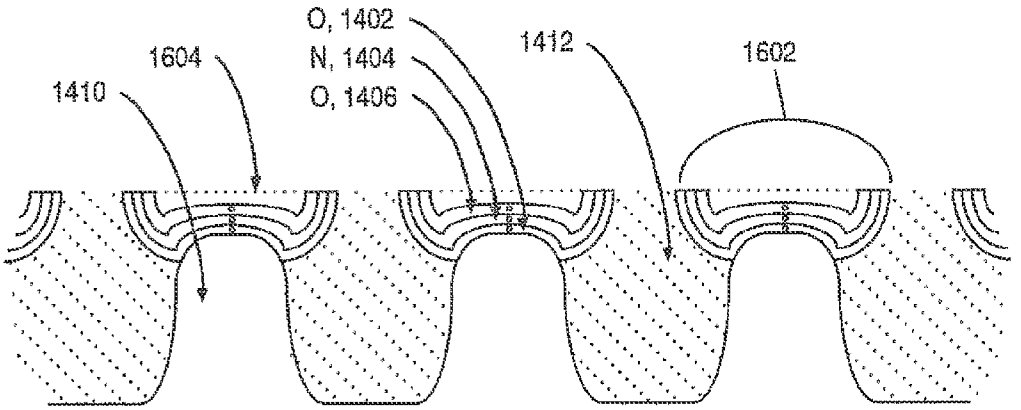


Figure 16

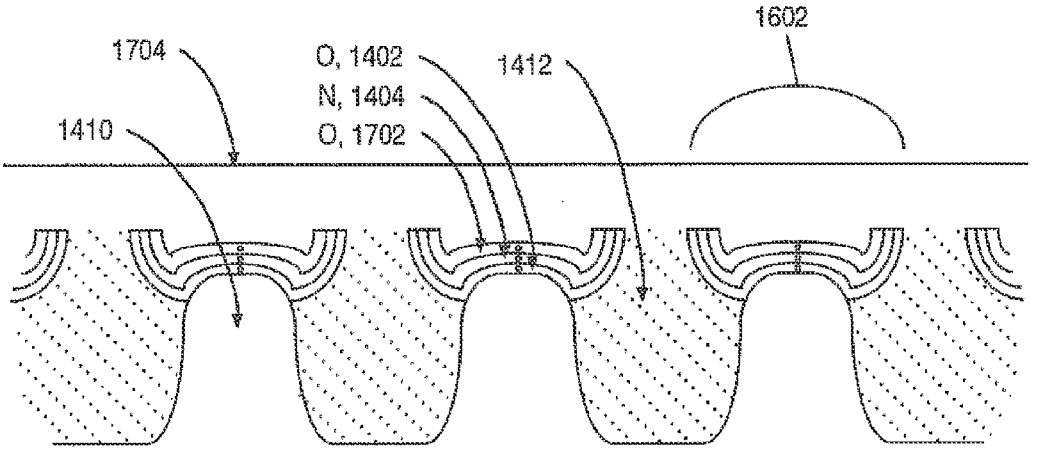


Figure 17

SELF-ALIGNED SI RICH NITRIDE CHARGE TRAP LAYER ISOLATION FOR CHARGE TRAP FLASH MEMORY

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application is a Continuation-in-Part of U.S. patent application Ser. No. 11/639,667, filed Nov. 7, 2006, entitled "SELF-ALIGNED STI WITH SINGLE POLY FOR MANUFACTURING A FLASH MEMORY DEVICE."

FIELD OF THE INVENTION

[0002] The present invention relates, in general, to semiconductor memory devices.

BACKGROUND OF THE INVENTION

[0003] Data is digitally stored in semiconductor memory devices. These semiconductor memory devices fall into one of two categories. Volatile memory devices retain their data only when they are powered on; whereas, non-volatile memory chips can retain the data even if no external power is being supplied to the memory device. One popular form of non-volatile memory device is flash memory. Flash memory is versatile because it can be erased and programmed multiple times. Furthermore, flash memory is relatively inexpensive compared to other types of non-volatile memory devices. Consequently, flash memory is ideal for applications that demand significant amounts of non-volatile, solid-state storage. Examples of applications employing flash memory include USB flash drives, digital audio players, digital cameras and camcorders, mobile phones, automotive control systems, gaming consoles, etc.

[0004] Flash memory is typically made up of an array of floating gate transistors, commonly referred to as memory "cells." One or more bits of data are stored as charge by each memory cell. For example, dual bit memory devices use a silicon-oxide-nitride-oxide-silicon (SONOS) type architecture in which a lower layer of silicon oxide is formed over a semiconductor substrate that is typically silicon. A layer of silicon nitride is formed on the lower layer of silicon oxide, an upper layer of silicon oxide is formed on the layer of silicon nitride and a layer of an electrically conductive material is formed on the upper layer of silicon oxide. The combination of the lower silicon oxide layer, the silicon nitride layer, and the upper silicon oxide layer are capable of trapping charge and are commonly referred to as a charge trapping dielectric structure or layer. It should be noted that the charge trapping structure is defined as a stack of ONO. When more than one bit of information is stored in the charge trapping structure, the memory device is referred to as a dual bit memory device. Bit lines are typically formed in the portion of the semiconductor substrate that is below the charge trapping structure and word lines may be formed from the layer of electrically conductive material that is disposed on the charge trapping structure. In a dual bit memory device, two bits are stored per cell by biasing the bit line, the word line, the source, and the drain of the memory cell such that a bit and a complementary bit are stored. This arrangement enables flash memory cells to be manufactured efficiently and economically.

[0005] FIG. **1** shows a conventional memory cell. In a conventional flash memory fabrication process, the tunnel oxide, the charge-trapping layer, and top charge block oxide **101** (e.g., oxide-nitride-oxide ONO layer) and one or more polysilicon layers **102** are formed before the shallow trench isolation (STI **103**) definition. It should be noted that the nitride layer can be comprised of nitride, silicon rich nitride, a combination of nitride on top of silicon rich nitride or multiple layers with different percentages of silicon content. After the STI **103** formation, another polysilicon layer can be deposited on the previous polysilicon layer. Subsequently, the word line is defined. Unfortunately, this conventional approach produces sharp corners **104-105** because the nature of the STI process produces near vertical sides. These sharp corners directly contribute to device degradation in performance and reliability. Simply going back and rounding off the sharp corners cannot solve these associated problems due to the increase in oxide encroachment which detrimentally impacts the erase and programming of the memory cell. Furthermore, rounding off the sharp corners would reduce the core cell current by a smaller effective channel width, which is highly undesirable.

[0006] Furthermore, various semiconductor fabrication processes use masks to help align the memory cells. Aligning the cells produces a more organized and compact design. Although masking techniques properly align the cells, scaling becomes an issue. It becomes harder to place the cells closer together. It is important to place the cells as close together without impacting their functionality because denser cells can hold more data for a given semiconductor area. In other words, tighter tolerances allow for greater memory capacity at reduced cost.

SUMMARY OF THE INVENTION

[0007] A method for fabricating a memory device with a self-aligned charge trapping layer and an active region with rounded corners is disclosed. An STI process is performed before any of the charge-trapping and top-level layers are formed. Immediately after the STI process, the sharp corners of the active regions are exposed. Because these sharp corners are exposed at this time, they are available to be rounded through any number of known rounding techniques. Rounding the corners improves the performance characteristics of the memory device. Subsequent to the rounding process, the charge-trapping structure and other layers are formed through a self-aligned process. In one embodiment, a sacrificial top oxide, polish, recess, nitride etch, sacrificial top oxide etch, and top oxide process flow makes the charge trapping layer self-aligned.

[0008] In an additional embodiment, subsequent to the rounding process, when the charge trapping layer is formed a bottom oxide layer, nitride layer, and sacrificial top oxide layer are formed. The sacrificial top oxide layer is a thin conformal layer of 20-100 angstroms. This is followed by an organic bottom antireflective coating applied to the charge trapping layer. This organic bottom antireflective coating is planarized. Now the organic bottom antireflective coating, top oxide layer, and nitride layer are etched, without etching the top oxide layer and nitride layer over the active regions. In this way, the top oxide and nitride layer are only etched over the trenches. After the etching, the charge trapping layer in a cross-sectional view, has a U-shaped appearance. U-shaped trap layer edges allow for increased packing density and integration while maintaining isolation between trap layers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The present invention will be better understood from a reading of the following detailed description, taken in

conjunction with the accompanying drawing figures in which like reference characters designate like elements and in which:

[0010] FIG. **1** shows a conventional memory cell.

[0011] FIG. **2** shows the process flow for fabricating the memory device according to one embodiment of the present invention.

[0012] FIG. **3** shows the continued process flow for fabricating the memory device according to one embodiment of the present invention.

[0013] FIG. **4** shows the patterning after the STI process is performed.

[0014] FIG. **5** shows a cross-sectional side view of one embodiment of the memory device after STI fill.

[0015] FIG. **6** shows a cross-sectional view of one embodiment of the memory device after the nitride strip, sacrificial oxide and bottom oxide pre-cleaning.

[0016] FIG. **7** shows a cross-sectional view of the memory device as it exists after the sacrificial top oxide deposition.

[0017] FIG. **8** shows a cross-sectional view of an embodiment of the memory device using a CMP or etch back technique whereby the top oxide layers are polished back or etched back to the boundary of the SiRN layer.

[0018] FIG. **9** shows the cross-sectional view of an embodiment of the memory device after sacrificial top oxide recess.

[0019] FIG. **10** shows the cross-sectional view of the memory device after performing the HDP recess and sacrificial top oxide removal.

[0020] FIG. **11** shows the cross-sectional view of the self-aligned memory device with rounded corners according to one embodiment of the present invention.

[0021] FIG. **12** is a flow diagram showing the process for two periphery integration schemes.

[0022] FIG. **13** shows a system according to embodiments of the present invention.

[0023] FIG. **14** shows the cross-sectional view of the memory device after the bottom oxide layer deposition, nitride layer deposition, and sacrificial top oxide layer deposition according to an embodiment of the present invention.

[0024] FIG. **15** shows the cross-sectional view of the memory device after the organic bottom antireflective coating deposition and planarization according to an embodiment of the present invention.

[0025] FIG. **16** shows the cross-sectional view of the memory device after performing the organic bottom antireflective coating etch, the sacrificial top oxide layer etch, and the nitride layer etch according to an embodiment of the present invention.

[0026] FIG. **17** shows the cross-sectional view of the self-aligned memory device with a substantially U-shaped trapping layer over an active region with rounded corners according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0027] The following embodiments are described in sufficient detail to enable those skilled in the art to make and use the invention, and it is to be understood that other embodiments would be evident based on the present disclosure and that process or mechanical changes may be made without departing from the scope of the present invention.

[0028] In the following description, numerous specific details are given to provide a thorough understanding of the invention. However, it will be apparent that the invention may be practiced without these specific details. In order to avoid obscuring the present invention, some well-known system configurations and process steps are not disclosed in detail. Likewise, the drawings showing embodiments of the invention are semi-diagrammatic and not drawn to scale, and particularly, some of the dimensions are for the clarity of presentation and are shown exaggerated in the Figures.

[0029] Generally, the present invention provides a method for manufacturing a self-aligned memory device with generally rounded polysilicon and STI corners. Semiconductor non-volatile memory devices, such as NOR-type and NAND-type flash memories, can be constructed using oxide/nitride/oxide (ONO) configurations. The nitride layer (e.g., silicon nitride, silicon rich nitride, or multiple layers with different percentages of Si content) closest to the semiconductor substrate in an ONO configuration acts as the charge trapping layer and is typically programmed and erased by the tunneling of electrons into and out of this layer. FIGS. **2** and **3** show the process flows for fabricating the memory device according to one embodiment of the present invention. Initially, a barrier oxide layer is formed on a silicon substrate, step **201**. The barrier oxide can be grown or deposited over the substrate. A nitride layer is then formed in step **202**. In step **203**, a core source/drain mask is patterned. The core STI etch then follows, step **204**. FIG. **4** shows the STI profile after the STI etch is performed. The STI process defines a number of active regions **401** separated by trenches **402** over a common substrate **403**. The oxide **404** and nitride **403** from steps **201** and **202** reside on active regions **401**. Active regions **401** are regions where the transistor action occurs. Substrate **403** can be fabricated from silicon, silicon based composites, or other known semiconductor materials including, but not limited to polysilicon, germanium, silicon germanium, Semiconductor-On-Insulator (SOI) material, etc. It should be noted that the conductivity type of substrate **403** is not a limitation of the present invention. In accordance with one embodiment, the conductivity type is chosen to form an N-channel insulated gate field effect transistor. However, the conductivity type can be selected to form a P-channel insulated gate semiconductor device or a complementary insulated gate semiconductor device (e.g., CMOS).

[0030] Next, a peripheral source/drain masking (SDM) step **205** is performed. The peripheral STI etching step **206** follows. The peripheral SDM and STI etch can be combined with core SDM and STI etch, respectively. In step **207**, one or more liner oxide layers are formed with or without wet etch of existing oxide before each liner oxide to round up the STI corners, and in step **208**, an STI fill is performed. It is the combination of one or more liner oxide and/or cleaning processes which causes the corners of the STI to become rounded. It should be noted that other known processes for rounding the corners can be employed at this time. In the prior art, the STI trench was cut after substantially all the layers (including the charge-trapping layers) were formed. This resulted in a near-vertical planar cut which resulted in sharp STI corners. In contrast, one embodiment of the present invention performs the STI before the charge-trapping and other top layers are formed. This exposes the sharp corners of the STI active region so that some type of rounding process can be performed to round out those now-exposed sharp corners. FIG. **5** shows a cross-sectional side view of one embodiment of the memory device after STI fill step **208**. The filling **500** can be an insulator material, such as an oxide formed by a high density plasma process. This trench fill material **500** is polished back in step **209**. The nitride is

stripped in step **210**. One or more sacrificial oxide layers with or without wet etch of existing oxide before each sacrificial oxide are performed in step **211**. The sacrificial oxide can also be skipped. The sacrificial oxide or the barrier oxide in case that sacrificial oxide is skipped, is then removed by a bottom oxide pre-clean step **217**. The oxide removal can be done in a variety of ways. It can be accomplished, for example, by means of wet or dry etch, sputtering, plasma techniques, or by other means. FIG. **6** shows a cross-sectional view of one embodiment of the memory device after the nitride strip, sacrificial oxide and bottom oxide pre-cleaning. It should be noted that the corners **601** and **602** are now rounded.

[0031] At this point, a charge trapping structure is fabricated. In one embodiment, this entails growing a bottom oxide layer, as indicated by step **213**. A silicon-rich nitride (SiRN) or multiple layers of nitride with different percentages of Si content are deposited on top of the bottom oxide layer in step **214**. A sacrificial top oxide process is then performed over the SiRN layer in step **215**. FIG. **7** shows a cross-sectional view of the memory device as it exists after the sacrificial top oxide deposition/process of step **215**. The silicon-rich nitride (SiRN) is depicted as layer **701**. The sacrificial top oxide is **702**. Note that the sacrificial top oxide will be completely etched off in step **219**. The top oxide will be formed in step **1204** or **1215** described below in reference to FIG. **12**. It should be noted that any charge trapping structure, including but not limited to ONO, can be utilized within the scope of the present invention. Other charge trapping structures can include three or more dielectric layers disposed on the active regions. For example, the top and bottom dielectric layers may be silicon dioxide layers that are oxygen-rich silicon dioxide layers; one or both of which may be thermally grown or deposited oxide layers. Alternatively, one or both of the bottom and top dielectric layers may be silicon dioxide layers that are nitrided oxide layers. The middle dielectric layer may be a silicon-rich silicon nitride layer or a combination of multiple layers with different percentages of Si content.

[0032] It should be understood that the charge trapping structure is not limited to being a three layer structure or a structure limited to silicon dioxide and silicon nitride. The charge trapping structure may be any dielectric layer or layers capable of trapping charge or that facilitate charge trapping. Other suitable materials include an oxide/nitride bilayer dielectric, a nitride/oxide bilayer dielectric, an oxide/tantalum oxide bilayer dielectric (SiO_2/Ta_2O_5), an oxide/tantalum oxide/oxide trilayer dielectric ($SiO_2/Ta_2O_5/SiO_2$), an oxide/strontium titanate bilayer dielectric ($SiO_2/SrTiO_3$), an oxide/barium strontium titanate bilayer dielectric ($SiO_2/BaSrTiO_2$), an oxide/strontium titanate/oxide trilayer dielectric, an oxide/strontium titanate/oxide trilayer dielectric ($SiO_2/SrTiO_3/BaSrTiO_2$), and oxide/hafnium oxide/oxide trilayer dielectric, and the like. A tunnel oxide may be formed between the semiconductor substrate and charge trapping structure. Although any charge trapping structure can be used, it is of significance that the charge trapping structure and any polysilicon deposition occurs after the STI is formed and the STI corners are rounded.

[0033] In step **216**, the sacrificial top oxide is polished back by CMP or etched back by plasma dry etch. For example, a chemical mechanical planarization (CMP) technique can be used to polish back the oxide layers to stop at the SiRN layer with or without partially removing SiRN. Other suitable planarization techniques include electropolishing, electrochemical polishing, chemical polishing, and chemically enhanced planarization. FIG. **8** shows a cross-sectional view of an embodiment of the memory device using a CMP technique whereby the sacrificial top oxide layers are polished back to the boundary **801** of the SiRN layer. In one embodiment, the SiRN layer is approximately 60 to 130 angstroms thick as deposit and final thickness can be approximately 30 to 100 angstroms thick. A sacrificial top oxide recess is performed in step **217**. The recess can be performed by either a wet or dry etching process. FIG. **9** shows the cross-sectional view of an embodiment of the memory device after recess. As shown, the oxide **901** is now recessed below the tops **902** of the SiRN layer over the active regions. Next, the SiRN is wet or dry etched, step **218**. This is done to separate the SiRN layers for each memory cell. In other words, the top portions of the SiRN layers are etched off so that each active region has its own separate SiRN layer. A sacrificial top oxide removal is performed in step **219**. The cross-sectional view of the memory device after performing the sacrificial top oxide removal is shown in FIG. **10**. It can be seen that the SiRN portion **1001** is segmented over the active region **1002**. Furthermore, the combination of the sacrificial top oxide, polish and wet etch of the nitride makes the new integration scheme self-aligned according to this embodiment of the present invention. It should be noted that TEOS is one of the films that can be used for the sacrificial top oxide.

[0034] Usually a thick (200-400 A) and a thin (20-100 A) gate oxide are needed for periphery transistors of NAND or NOR flash memory. Two approaches for periphery transistor gate oxide are shown in FIG. **12** and described later below. After HTO or SPA top oxide, an ONO mask opens the periphery area. Dry or wet or a combination of dry and wet etch removes ONO layers in the periphery. A dry thick gate oxide is grown first. Gate oxide mask opens thin gate oxide area and a wet or dry etch removes the thick oxide and then a thin gate oxide is grown.

[0035] The other approach is for wet periphery thick oxide. Since during the wet oxidation oxygen diffuses through oxide in core STI area and encroaches core S/D, a thin (20-30 A) SiRN or nitride is deposited first to block the steam oxide. An ONO mask opens the periphery area. Dry or wet or a combination of dry and wet etch removes ONO layers in the periphery. A thick steam gate oxide grows first and is followed by SPA top oxide. This SPA top oxide adds the thickness to the steam oxide and also consumes all the thin SiRN or nitride on core STI. Gate oxide mask opens thin gate oxide area and a wet or dry etch removes the thick oxide and then a thin gate oxide is grown.

[0036] FIG. **11** shows the cross-sectional view of the self-aligned memory device with rounded corners according to one embodiment of the present invention. Each active region **1101-1103** is separated on each side by trenches **1104-1107**. The trenches are formed through an STI process as described above. Right after the STI process, the corners of these active regions **1101-1103** are sharp due to the way the trenches are vertically cut. Immediately upon forming the trenches **1104-1107**, the corners are rounded. It is advantageous to round the corners at this time because they are exposed. The rounding process can be done in may different ways, such as by means of known cleaning/polishing and/or sacrificial oxide placement/removal. The corners **1108-1114** are rounded before any additional layers are formed. After the corners have sufficiently been rounded, any number or combination of layers can be deposited or grown over the active region. For example, a tunnel oxide layer (optional), ONO (ONO stands

for tunnel oxide-nitride-top oxide) stacks **1115-1117**, polysilicon layer(s) **1118**, etc. can be formed after the rounding process.

[0037] It should be noted that steps **213-219** shown in the flow diagram of FIG. **2** is of particular relevance because these steps depict the process of forming self-aligned ONO stacks. In particular, the steps start with a bottom oxide. This is followed by depositing the SiRN. A sacrificial top oxide deposition is performed. The sacrificial top oxide is polished or etched back. A sacrificial oxide recess is performed, and a SiRN wet or dry etch is performed. This results in a self-aligned process which greatly improves scalability.

[0038] FIG. **12** is a flow diagram showing the process for two periphery integration schemes. Upon forming the self-aligned ONO stacks, a sacrificial oxide removal step **1201** is performed. Note that step **1202** is the same step as step **219** of FIG. **3**. A first periphery integration scheme **1202** includes process steps **1204-1210**. In process step **1204**, an SPA or high temperature oxidation (HTO) is used to form a top oxide. An ONO masking is performed in step **1205**. The ONO is etched in step **1206**. A periphery thick gate oxide is fabricated in step **1207**. Next, the gate oxide is masked in step **1208**. The gate oxide is then etched in step **1209**. And a periphery thin gate oxide is fabricated in step **1210**.

[0039] A second periphery integration scheme **1203** includes process steps **1211-1218**. In step **1211**, a thin SiRN or Nitride layer is deposited. An ONO masking step **1212** is then performed. The ONO is then etched in step **1213**. A periphery thick gate oxide layer is fabricated in step **1214**. An SPA top oxide is fabricated in step **1215**. The gate oxide is then masked in step **1216**. The gate oxide is etched in step **1217**. And a periphery thin gate oxide is fabricated in step **1218**. After either of the two periphery integration schemes has been performed, a polysilicon layer is deposited in step **1219**.

[0040] FIG. **13** shows a system according to embodiments of the present invention. The system **1300** can be a portable multimedia device, media player, communications device, networking devices, computing device, consumer electronic device, mobile computing device, image capture device, audio/visual device, gaming console, etc. System **1300** includes a process **1302** that pertains to a microprocessor or controller for controlling the overall processing of data in system **1300**. Digital data is stored in a file system **1304** and a cache memory **1306**. The file system **1304** typically provides high capacity storage capability for system **1300**. File system **1304** can include a non-volatile flash memory **1330**. Flash memory **1330** has rounded STI corners and is manufactured as described above. The system **1300** also includes volatile random access memory (RAM) **1320** and non-volatile read-only memory (ROM) **1322** for storing digital data. System **1300** also includes a user input device **1308**, such as a button, keypad, dial, scroll wheel, touch sensitive pad, etc. A display **1310** is used to display visual information to the user. A data bus **1324** transfers data between the various components via a bus interface **1318**. A compression-decompression (CODEC) chip can be used to facilitate data storage and transfers. A speaker **1314** is used to play back songs, voice messages, and other audio streams.

A Further Embodiment of the Present Invention with a U-Shaped Charge Trapping Layer Over Rounded STI Corners

[0041] Generally, this embodiment discloses a method for manufacturing a self-aligned memory device with a substantially U-shaped charge trapping structure over an active region with rounded trench corners. FIGS. **14-17** illustrate a not-to-scale cross-section of a memory device undergoing the process steps according to an embodiment of the present invention. Further, aspects of the memory device of FIGS. **14-17** may be exaggerated for clarity. By virtue of having substantially U-shaped charge trapping portions over active regions with rounded corners, the present invention mitigates the disadvantageous attributes corresponding to the sharp trench corners as well as the flatter charge trapping portions resulting from conventional fabrication techniques. Moreover, the present invention has greater scalability due to the fact that it is self-aligned with U-shaped charge trapping portions, allowing the structures to be placed closer together.

[0042] Initially, the process steps as disclosed in FIGS. **1-6** are carried out up to and including the deposition of the nitride layer over the bottom oxide layer of step **214** in FIG. **3** for the charge trapping layer. The nitride layer of the charge trapping layer may be silicon-rich nitride (SiRN) or multiple layers of nitride with different percentages of Si content. FIG. **14** illustrates the bottom oxide layer **1402** underlying the nitride layer **1404** as well as a sacrificial top oxide layer **1406** deposited over the nitride layer **1402**. This sacrificial top oxide layer **1406** is a conformal coating of oxide only 20-100 angstroms (Å) thick, rather than the thicker oxide deposition **702**, as illustrated in FIG. **7**. The sacrificial top oxide layer **1406**, nitride layer **1404**, and bottom oxide layer **1402** make up the layer **1408** overlying each active region **1410** and each isolation region **1412**. The active regions are separated on each side by trenches or isolation regions **1412**. The trenches **1412** are formed through the shallow trench isolation (STI) process described above. The trenches may also be STI field oxide (FOX) structures.

[0043] FIG. **15** illustrates the next step in the process. An organic bottom antireflective coating (oBARC) **1510** is spun-on over the sacrificial top oxide layer **1406**. As illustrated in FIG. **15**, the oBARC overlay **1510** is then planarized. The planarized oBARC **1510** is of a depth sufficient to fill gaps **1512** between the trench structures **1410** as well as thinly covering the trench structures **1410** themselves. In an embodiment of the invention, the planarized oBARC **1510** in the gap **1512** is 400-500 angstroms (Å) thick. Further, any suitable planarization coating material may be used. For example, other than using oBARC, another material such as a spin-on glass may be used instead.

[0044] FIG. **16** illustrates the results of an etching step in the process. The etching step isolates the charge trapping layer **1408** into charge trapping portions **1602** over the active regions **1410**. In isolating portions **1602** of the charge trapping layer **1408**, the oBARC layer **1510**, top oxide layer **1406**, and nitride layer **1404** are etched above the trenches without etching the nitride layer **1404** and top oxide layer **1406** above the active regions **1410**. As shown in FIG. **16**, a small quantity of oBARC material **1604** remains in the gaps **1512** above each charge trapping portion **1602**. A photo mask may be used before the etching step, if blocking etching is needed in some areas, e.g. periphery areas.

[0045] As illustrated in FIG. **17**, the remaining oBARC material **1604** is now removed. The remaining oBARC material **1602** may be removed through any available method for removing antireflective coatings, such as the organic bottom antireflective coating used in this embodiment. After removing the remaining oBARC material **1604**, the sacrificial top oxide **1406** is removed by a wet etch and the surface is cleaned

to prevent any contamination or damage of the oBARC and etch. Note that the sacrificial top oxide **1406** may be removed as in step **1202** and step **219** of FIG. **12** and FIG. **3** above, respectively. Then, as discussed above, and illustrated in FIG. **17**, a top oxide **1702** is formed and a further layer of polysilicon **1704** is deposited. The top oxide formation may be accomplished through thermal growth or CVD deposition. FIG. **17** shows the cross-sectional view of the self-aligned memory device with substantially U-shaped charge trapping portions **1602** overlying active regions **1410** with rounded STI corners. Substantially U-shaped charge trapping portions **1602** are defined as U-shaped as seen from a cross-sectional view of the semiconductor device. Further, "substantially U-shaped" is defined as a shape approaching an actual U-shape with vertical ends. While not necessarily reaching true vertical orientation, a substantially U-shape refers to those shapes with edges or ends that steeply sloop upwards approaching or reaching an orthogonal relationship to the substrate below, as illustrated in the charge trapping portions **1602** of FIGS. **16** and **17**. While other embodiments may include charge trapping portions with edges that slope upwards with shallower slopes, a steeper slope as defined by "substantially U-shaped" is the preferred embodiment.

[0046] This method benefits from using a conformal sacrificial top oxide layer **1406** rather than the top oxide layer **702** deposited in FIG. **7**. The U-shaped charge trapping portions **1602**, as viewed in the cross-section of a semiconductor device, allow the charge trapping portions **1602** to be moved closer together while maintaining isolation between the charge trapping portions **1602**. The U-shape of the charge trapping portions **1602** provides a steeper upward slope on the edges of the charge trapping portions **1602**, rather than shallow sloping edges of other embodiments. Tighter dimensions and smaller devices make polishing a thicker sacrificial oxide layer difficult and risks damaging the nitride layer over the active regions. As the semiconductor structures are scaled smaller, the working margins are lost and a thick sacrificial oxide layer with polishing may be replaced in favor of a thin top oxide layer with oBARC and etching in accordance with embodiments of the present invention.

[0047] Therefore, a non-volatile, self-aligned semiconductor memory device having a substantially U-shaped charge trapping portion over a rounded active region and a method for manufacturing the device has been disclosed. In particular, the STI process is performed before the ONO and polysilicon deposition steps. This enables the STI corners to be rounded after the STI process but before the ONO and polysilicon deposition steps. This is in contrast to the conventional method of forming ONO and polysilicon before the STI definition. In the conventional method, after the STI formation, another polysilicon layer is deposited on the previous polysilicon layer and then the word line is defined. This conventional method results in sharp polysilicon and STI corners which degrades device performance and reliability. By virtue of having substantially U-shaped charge trapping portions over rounded active region corners, the present invention mitigates the disadvantageous attributes corresponding to the sharp corners as well as flatter charge trapping portions resulting from conventional fabrication techniques. Moreover, the present invention has greater scalability due to the fact that it is self-aligned with U-shaped charge trapping portions. This is accomplished by means of a conformal or thin sacrificial top oxide layer, an oBARC deposition, and etch of the oBARC, sacrificial top oxide layer, and nitride layer, while avoiding etching the sacrificial top oxide and nitride layers over the active regions, as opposed to embodiments that provide for a thick sacrificial top oxide layer, polish, and wet etch of the nitride, as well as the ONO structures formed before the STI structures are formed. The process using a conformal sacrificial top oxide, oBARC layer with etching provides a U-shaped charge trapping layer over an active region with rounded corners as opposed to the shallower, wider portions seen in embodiments using the thick sacrificial top oxide layer, polish, and wet etch of the nitride, which may or may not have rounded active region corners. Although not shown, it should be appreciated that source and drain regions are formed in active regions of the substrate and that additional processing is performed to form a metallization system including contact structures. Further, the non-volatile flash memory **1330** of FIG. **13** may include a charge trapping portion or structure **1602** with substantially U-shaped edges.

[0048] Although certain preferred embodiments and methods have been disclosed herein, it will be apparent from the foregoing disclosure to those skilled in the art that variations and modifications of such embodiments and methods may be made without departing from the spirit and scope of the invention. It is intended that the invention shall be limited only to the extent required by the appended claims and the rules and principles of applicable law.

1-11. (canceled)

12. A memory device, comprising:

a semiconductor substrate;

a plurality of active regions;

a plurality of trenches separating the active regions;

a plurality of self-aligned charge trapping structures disposed over the plurality of active regions, wherein the charge trapping structures are substantially U-shaped.

13. The memory device of claim **12**, wherein the self-aligned charge trapping structures are formed through a sacrificial top oxide, organic bottom antireflective coating planarization, organic bottom antireflective coating etch back, sacrificial top oxide etch, nitride etch, organic bottom antireflective coating removal and cleaning, sacrificial top oxide removal and cleaning, top oxide formation and polysilicon deposit, wherein the sacrificial top oxide and nitride are not etched over the active regions.

14. The memory device of claim **12**, wherein the active regions have had corners which underwent a rounding process before the plurality of charge trapping structures were formed.

15. The memory device of claim **14**, wherein the corners are rounded through a liner oxide process.

16. The memory device of claim **12**, wherein the charge trapping structures comprise an oxide-nitride-oxide structure.

17. The memory device of claim **16**, wherein the nitride of the oxide-nitride-oxide structure is comprised of silicon rich nitride.

18. The memory device of claim **16**, wherein the nitride of the oxide-nitride-oxide structure is comprised of nitride on top of silicon rich nitride.

19. The memory device of claim **16**, wherein the nitride of the oxide-nitride-oxide structure is comprised of a plurality of nitride layers having different amounts of silicon.

20. The memory device of claim **13**, wherein the organic bottom antireflective coating is replaced with other materials suitable for use in planarization.

21. The memory device of claim **13**, wherein the sacrificial top oxide layer is between 20-100 angstroms (Å) thick.

22. A system comprising:

a processor;

a bus coupled to the processor;

a non-volatile memory coupled to the bus, wherein the non-volatile memory comprises:

a semiconductor substrate;

a plurality of active regions;

a plurality of trenches separating the active regions;

a plurality of self-aligned charge trapping structures disposed over the plurality of active regions, wherein the charge trapping structures are substantially U-shaped.

23. The system of claim **22**, wherein the self-aligned charge trapping structures are formed through a sacrificial top oxide, organic bottom antireflective coating planarization, organic bottom antireflective coating etch back, sacrificial top oxide etch, nitride etch, organic bottom antireflective coating removal and cleaning, sacrificial top oxide removal and cleaning, top oxide formation and polysilicon deposit, wherein the sacrificial top oxide and nitride are not etched over the active regions.

24. The system of claim **22**, wherein the active regions have rounded corners.

25. The system of claim **22**, wherein the processor, bus, and non-volatile memory comprise an image capture device.

26. The system of claim **22**, wherein the processor, bus, and non-volatile memory comprise a communications device.

27. The system of claim **22**, wherein the processor, bus, and non-volatile memory comprise a computing device.

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