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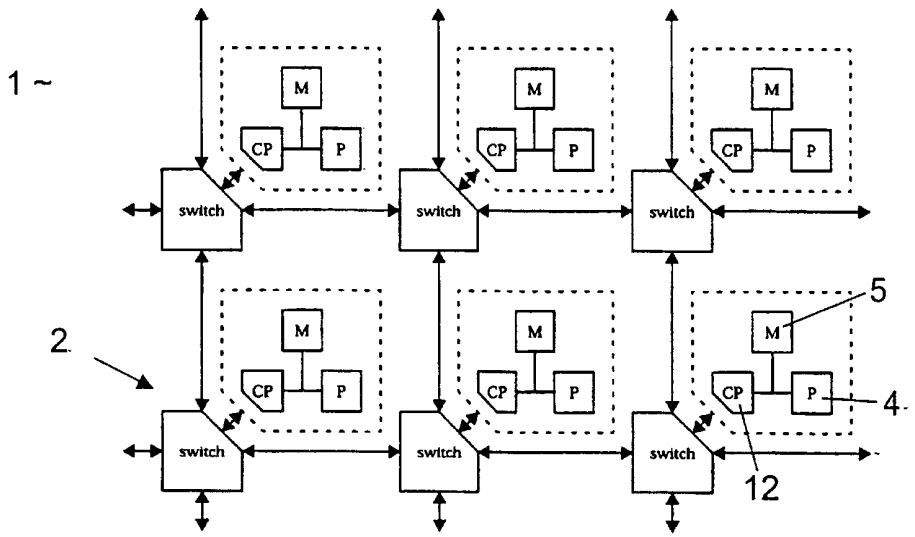
(54) **Title:** AN ARRAY OF PARALLEL PROGRAMMABLE PROCESSING ENGINES AND DETERMINISTIC METHOD OF OPERATING THE SAME



(57) **Abstract:** The present invention provides an array of parallel programmable processing engines interconnected by a switching network. At least some of the processing engines execute a thread, and at least some threads communicate with each other through communication objects either internally within one processing engine or through the network. A scheduling step of the parallel programmable processing engines is initiated by one or more events, an event being defined by a change of a state variable of a communication object. The array comprises: means for scheduling a scheduling step of the processing engines, the scheduling means comprising means for executing at least a first set of threads in parallel, means for updating state values of communications objects in response to the parallel executing step, and means for repeatedly and sequentially scheduling the executing means and the updating means until no more events occur. The present invention also provides a deterministic method of operating such an array.

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F17/50 G06F9/44

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, IBM-TDB, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 00 42535 A (CHAN TERENCE) 20 July 2000 (2000-07-20) page 5, line 6 - line 32 page 11, line 27 -page 12, line 22 figure 7 --- -/--	1,3,10, 18,21, 23,28

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Guingale, A

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	SERNEC R ET AL: "Multithreaded systolic/SIMD DSP array processor-MUS2DAP" 1997 IEEE WORKSHOP ON SIGNAL PROCESSING SYSTEMS. SIPS 97 DESIGN AND IMPLEMENTATION FORMERLY VLSI SIGNAL PROCESSING (CAT. NO.97TH8262), 1997 IEEE WORKSHOP ON SIGNAL PROCESSING SYSTEMS. SIPS 97 DESIGN AND IMPLEMENTATION FORMERLY VLSI SIGNAL PROCESSING,, pages 448-457, XP002189868 1997, New York, NY, USA, IEEE, USA ISBN: 0-7803-3806-5 abstract ---	1,10,18, 21,23,28
A	SAKURAI R ET AL: "A scheduling method for synchronous communication in the Bach hardware compiler" PROCEEDINGS OF THE ASP-DAC '99 ASIA AND SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE 1999 (CAT. NO.99EX198), PROCEEDINGS OF THE ASP-DAC '99 ASIAN AND SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE 1999, WANCHAI, HONG KONG, 18-21 JAN. 1999, pages 193-196 vol.1, XP010326328 1999, Piscatatway, NJ, USA, IEEE, USA ISBN: 0-7803-5012-X abstract -----	1,3,10, 18,21, 23,28

INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 0042535 A	20-07-2000	AU 2505200 A	01-08-2000
		WO 0042535 A1	20-07-2000