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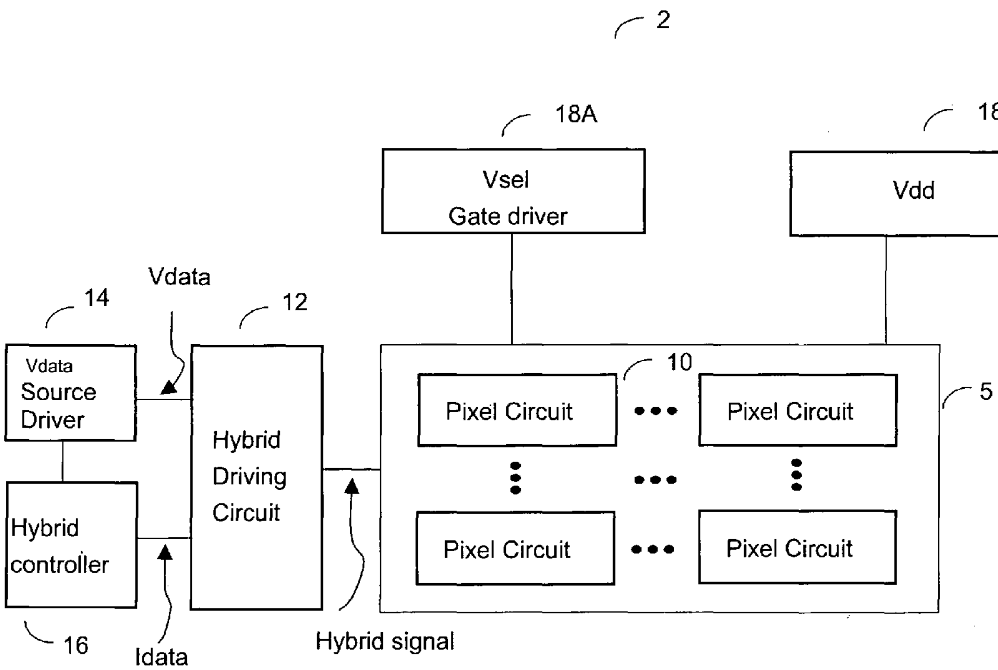
(54) **Title:** VOLTAGE-PROGRAMMING SCHEME FOR CURRENT-DRIVEN AMOLED DISPLAYS



(57) **Abstract:** A system and method for driving an AMOLED display is provided. The AMOLED display includes a plurality of pixel circuits. A voltage-programming scheme, a current-programming scheme or a combination thereof is applied to drive the display. Threshold shift information, and/or voltage necessary to obtain hybrid driving circuit may be acquired. A data sampling may be implemented to acquire a current/voltage relationship. A feedback operation may be implemented to correct the brightness of the pixel.

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Voltage-Programming Scheme For Current-Driven AMOLED Displays

FIELD OF INVENTION

[0001] The present invention relates to a display technique, and more specifically to technology for driving pixel circuits.

BACKGROUND OF THE INVENTION

[0002] Active matrix organic light emitting diode (AMOLED) displays are well known in the art. The AMOLED displays have been increasingly used as a flat panel in a wide variety of tools.

[0003] The AMOLED displays are classified as either a voltage-programmed display or a current-programmed display. The voltage-programmed display is driven by a voltage-programmed scheme where data is applied to the display as a voltage. The current-programmed display is driven by a current-programmed scheme where data is applied to the display as a current.

[0004] The advantage of the current-programming scheme is that it can facilitate pixel designs where the brightness of the pixel remains more constant over time than with voltage programming. However, the current-programming requires longer time of charging capacitors associated with the column.

[0005] Therefore, there is a need to provide a new scheme for driving a current-driven AMOLED display, which ensures high speed and high quality.

SUMMARY OF THE INVENTION

[0006] The present invention relates to a system and method of driving a pixel circuit in an AMOLED display.

[0007] The system and method of the present invention uses Voltage-Programming Scheme For Current-Driven AMOLED Displays.

[0008] In accordance with an aspect of the present invention there is provided a system for driving a display which includes a plurality of pixel circuits, each having a plurality of thin film transistors (TFTs) and an organic light emitting diode (OLED), which includes: a voltage driver for generating a voltage to program the pixel circuit; a programmable current source for generating a current to program the pixel circuit; and a switching network for selectively connecting the data driver or the current source to one or more pixel circuits.

[0009] In accordance with a further aspect of the present invention there is provided a system for driving a pixel circuit having a plurality of thin film transistors (TFTs) and an organic light emitting diode (OLED), which includes: a pre-charge controller for pre-charging and discharging a data node of the pixel circuit to acquire threshold voltage information of the TFT from the data node; and a hybrid driving circuit for programming the pixel circuit based on the acquired threshold voltage information and video data information displayed on the pixel circuit.

[0010] In accordance with a further aspect of the present invention there is provided a system for driving a pixel circuit having a plurality of thin film transistors (TFTs) and an organic light emitting diode (OLED), which includes: a sampler for sampling, from a data node of the pixel circuit, a voltage required to program the pixel circuit; and a programming circuit for programming the pixel circuit based on the sampled voltage and video data information displayed on the pixel circuit.

[0011] In accordance with a further aspect of the present invention there is provided a method of driving a pixel circuit having a plurality of thin film transistors (TFTs) and an organic light emitting diode (OLED), which includes the steps of: selecting a pixel circuit and pre-charging a data node of the pixel circuit; allowing the pre-charged data node to be discharged; extracting a threshold voltage of the TFT through the discharging step; and programming the pixel circuit, including compensating a programming data based on the extracted threshold voltage.

[0012] This summary of the invention does not necessarily describe all features of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings wherein:

[0014] Figure 1 is a block diagram showing a system for driving an AMOLED display in accordance with an embodiment of the present invention;

[0015] Figure 2 is a schematic diagram showing one example of a pixel circuit of Figure 1;

[0016] Figure 3 is a schematic diagram showing an example of a hybrid driving circuit, which is applicable to Figure 1;

[0017] Figure 4 is an exemplary flow chart for showing the operation of the hybrid driving circuit of Figure 3;

[0018] Figure 5 is an exemplary timing chart for showing the operation of the hybrid driving circuit of Figure 3;

[0019] Figure 6 is a schematic diagram showing a further example of a hybrid driving circuit, which is applicable to Figure 1;

[0020] Figure 7 is an exemplary flow chart for showing the operation of the hybrid driving circuit of Figure 6;

[0021] Figure 8 is a schematic diagram showing a further example of a hybrid driving circuit, which is applicable to Figure 1;

[0022] Figure 9 is an exemplary flow chart for showing the operation of the hybrid driving circuit of Figure 8;

[0023] Figure 10 is an exemplary timing chart for showing the operation of the hybrid driving circuit of Figure 8;

[0024] Figure 11 is a schematic diagram showing a further example of the pixel circuit of Figure 1;

[0025] Figure 12 is a block diagram showing a system for driving an AMOLED display in accordance with a further embodiment of the present invention;

[0026] Figure 13 is an exemplary flow chart for showing the operation of the system of Figure 12;

[0027] Figure 14 is an exemplary flow chart for showing the operation of the system of Figure 12;

[0028] Figure 15 is an exemplary timing chart for showing the operation of the system of Figure 12;

[0029] Figure 16 is an exemplary flow chart for a hidden refresh operation of the system of Figure 12;

[0030] Figure 17 is a diagram showing an example of a sample of the current/voltage correction curve;

[0031] Figure 18 is a diagram showing the current/voltage correction curve of Figure 17 and an example of a newly measured data point:

[0032] Figure 19 is a diagram showing an example of a new current/voltage correction curve based on the measured point of Figure 18;

[0033] Figure 20 is a block diagram showing a further example of a programming circuit for implementing a combined current and voltage-programming technique;

[0034] Figure 21 is a block diagram showing a system for driving an AMOLED display in accordance with a further embodiment of the invention;

[0035] Figure 22 is a schematic diagram showing an example of a switch network of Figure 21; and

[0036] Figure 23 is a schematic diagram showing a system for correcting the current/voltage information of the pixel circuit.

DETAILED DESCRIPTION

[0037] Embodiments of the present invention are described using an AMOLED display. Drive scheme described below is applicable to a current programmed (driven) pixel circuit and a voltage programmed (driven) pixel circuit.

[0038] In addition, hybrid technique described below can be applied to any existing driving scheme, including a) any drive schemes that use sophisticated timing of the data, select, or power inputs to the pixels to achieve increased brightness uniformity, b) any drive schemes that use current or voltage feedback, c) any drive schemes that use optical feedback.

[0039] The light emitting material of the pixel circuit can be any technology, specifically organic light emitting diode (OLED) technology, and in particular, but not limited to, fluorescent, phosphorescent, polymer, and dendrimer materials.

[0040] Referring to Figure 1, there is illustrated a system 2 for driving an AMOLED display 5 in accordance with an embodiment of the present invention. The AMOLED display 5 includes a plurality of pixel circuits. In Figure 1, four pixel circuits 10 are shown as an example.

[0041] The system 2 includes a hybrid driving circuit 12, a voltage source driver 14, a hybrid programming controller 16, a gate driver 18A and a power-supply 18B. The pixel circuit 10 is selected by the gate driver 18A (Vsel), and is programmed by either voltage mode using a node Vdata or current mode using a node Idata. The hybrid driving circuit 12 selects the mode of programming, and connects it to the pixel circuit 10 through a hybrid signal. A pre-charge signal (Vp) is applied to the pixel circuit 10 to acquire threshold Vt information (or Vt shift information) from the pixel circuit 10. The hybrid driving circuit 12 controls the pre-charging, if pre-charging technique is used. The pre-charge signal (Vp) may be generated within the hybrid driving circuit 12, which depends on the operation condition. The power-supply 18B (Vdd) supplies the current required to energize the display 5 and to monitor the power consumption of the display 5.

[0042] The hybrid controller 16 controls the individual components that make up the entire hybrid programming circuit. The hybrid controller 16 handles timing and controls the order in which the required functions occur. The hybrid controller 16 may generate data Idata and supplied to the hybrid driving circuit 12. The system 2 may have a reference current source, and the Idata may be supplied under the control of the hybrid controller 16.

[0043] The hybrid driver 12 may be implemented either as a switching matrix, or as the hybrid driving circuit(s) of Figure 3, 6, 8 or 20 or combination thereof.

[0044] In the description, Vdata refers to data, a data signal, a data line or a node for supplying the data or data signal Vdata, or a voltage on the data line or the node. Similarly, Idata refers to data, a data signal, a data line or a node for supplying the data or data signal Idata, or a current on the data line or the node. Vp refers to a pre-charge signal, a pre-charge pulse, a pre-charge voltage for pre-charging/discharging, a line or a node for supplying the pre-charge signal, pre-charge pulse or pre-charge voltage Vp. Vsel refers to a pulse or a signal for selecting a pixel circuit or a line or a node for supplying the pulse or signal Vs. The terms "hybrid signal", "hybrid signal node", and "hybrid signal line" may be used interchangeably.

[0045] The pixel circuit 10 includes a plurality of TFTs, and an organic light emitting diode (OLED). The TFT may be an n-type TFT or a p-type TFT. The TFT is, for example, but not limited to, an amorphous silicon (a-Si:H) based TFT, a polycrystalline silicon based TFT, a crystalline silicon based TFT, or an organic semiconductor based TFT. The OLED may be regular (P-I-N) stack or inverted (N-I-P) stack. The OLED can be located in the source or the drain of one or more driving TFTs.

[0046] Figure 2 illustrates an example of the pixel circuit 10 of Figure 1. The pixel circuit of Figure 2 includes four thin film transistors (TFTs) 20-26, a capacitor Cs 28 and an organic light emitter diode (OLED) 30. The TFT (Tdrive) 26 is a drive TFT that is connected to the OLED 30 and the capacitor Cs 28. The pixel circuit of Figure 2 is selected by the select line Vsel, and is programmed by a data line DL. The data line DL is controlled by the hybrid signal output from the hybrid driving circuit 12 of Figure 1.

[0047] In Figure 2, four TFTs are illustrated. However, the pixel circuit 10 of Figure 1 may include less than four TFTs or more than four TFTs.

[0048] In the description, the terms "data line DL" and "data node DL" may be used interchangeably.

[0049] Referring to Figures 1-2, the data node DL is pre-charged and discharged to acquire the threshold Vt of a drive TFT (e.g., Tdrive 26 of Figure 2) or the threshold Vt shift. In the description, Vt shift, Vt shift information, Vt, and Vt information may be used interchangeably. The pixel circuit 10 is then consecutively programmed by the source driver 14 using voltage-programming. The acquired Vt shift information is utilized to compensate for degradation of the pixel circuit 10, thus maintaining uniform brightness of the display 5.

[0050] The process of acquiring Vt starts by applying Vsel to T1 20 and T2 22 to the pixel circuit illustrated in Figure 2. Such action causes the drain and gate of T3 24 to be at the same voltage. This allows the Vt of T3 24 to be extracted by first applying the pre-charge voltage Vp to the data line DL, which is than allowed to be discharged. The rate of discharge is a function of Vt. Thus, by measure of the rate of discharge, Vt can be obtained.

[0051] Figure 3 illustrates an example of a hybrid driving circuit, which is applicable to the hybrid driving circuit 12 of Figure 1. The hybrid driving circuit 12A of Figure 3 implements voltage programming technique.

[0052] The hybrid driving circuit 12A of Figure 3 includes a charge programming capacitor Cc 32. The charge programming capacitor Cc 32 is provided between the data line Vdata and the data node DL. The pre-charge line Vp is also connected to the data node DL.

[0053] The hybrid driving circuit 12A is provided to a pixel circuit 10A having four TFTs (such as the pixel circuit of Figure 2). However, the pixel circuit 10A may include more than four TFTs or less than four TFTs.

[0054] The charge programming capacitor Cc 32 is provided to program the pixel circuit 10A with a voltage that is equal to the sum of threshold Vt of the TFT and Vdata, scaled by a constant K. The constant is determined by the voltage division network formed by the charge storage capacitor (e.g. Cs 28 of Figure 2) and the charge programming capacitor Cc 32.

[0055] Figure 4 illustrates an exemplary flow chart for showing the operation of the hybrid driving circuit 12A of Figure 3. At step S10, pre-charge mode is enabled. At step S12, a pixel circuit is selected and pre-charging (Vp) is started. At step S14, Vt acquisition mode is enabled, and at step S16, discharging (Vp) starts. The Vt information is acquired through Cc 32. Then at step S18, writing mode is enabled.

[0056] Figure 5 illustrates an exemplary timing chart for showing the operation of the hybrid driving circuit 12A of Figure 3. In the drawings, Vdata0 represents voltage at the data node (e.g. DL of Figure 2) of the pixel circuit; Idata0 represents current at the data node (e.g. DL of Figure 2) of the pixel circuit.

[0057] The programming procedure starts by selecting the pixel to be programmed with the pulse Vsel. At the same time, the pre-charge pulse Vp is applied to the pixel circuit's data input (e.g. DL of Figure 2).

[0058] During the Vt acquisition phase, voltage on the data line (DL) is allowed to be discharged through the pixel circuit, which is in a current mirror connection with the Vsel line held high. The data line (DL) is discharged to a certain voltage, and the Vt of a drive TFT is extracted from that voltage. The voltage at Vdata is at ground.

[0059] During the programming (writing) phase, the calculated compensated voltage is applied to the data input line (DL) of the pixel circuit. The programming routine finishes with the lowering of the Vsel signal.

[0060] The calculated compensated voltage is obtained through analog means of a charge programming capacitor Cc32. However, any other analog means for obtaining compensated voltage may be used. Further, any (external) digital circuit (e.g. 50 of Figure 7) may be used to obtain the calculated compensated voltage.

[0061] The source driver (14 of Figure 1) supplies Vdata to the capacitor Cc 32. When Vdata is increased from ground to the desired voltage level, the voltage at Idata is equal to (Vt+Vdata)*K.

[0062] The structure of Figure 3 is simple, and is easily implemented.

[0063] Figure 6 illustrates a further example of a hybrid driving circuit, which is applicable to the hybrid driving circuit 12 of Figure 1. The hybrid driving circuit 12B of Figure 6 implements voltage programming technique.

[0064] The hybrid driving circuit 12B includes a summer 40, a sample and hold (S/H) circuit 42 and a switching element 44. The S/H circuit 42 samples Idata and holds it for a certain period. The summer 40 receives Vdata and the output of the S/H circuit 42.

The switching element 44 connects the output of the summer 40 to the data node DL in response to a programming control signal 46.

[0065] The hybrid driving circuit 12B utilizes the summer 40, instead of the charge coupling capacitor Cc 32, to produce programming voltage that is equal to the sum of Vt and Vdata. As the hybrid driving circuit 12B does not utilize a capacity, programming voltage is not affected by the parasitic capacitance, and it has less charge feed-through effect. As the hybrid driving circuit 12B does not utilize a charge storage capacitor, programming voltage is not affected by the charge storage capacitance. As the hybrid driving circuit 12B does not utilize a charge programming capacitor, it achieves faster Vt acquisition time. Removal of the charge programming capacitor eliminates the charge dependency of the programming scheme. Thus the programming voltage is not affected by the charge being shared between the charge storage capacitor and the parasitic capacitance of the system. This results in a higher effective programming voltage.

[0066] Figure 7 illustrates an exemplary flow chart for showing the operation of the hybrid driving circuit 12B of Figure 6. During the Vt acquisition mode, the Vt is sampled at step S20, and new data is produced at step S22. When writing mode is enabled, the new data is supplied to the pixel circuit in response to the programming control signal (46) at S24. It is noted that the operation of the system having the hybrid driving circuit 12B is not limited to Figure 7. The new data may be produced after step S18. The control signal 46 may be enabled before step S18.

[0067] During the Vt acquisition cycle, Vdata is at ground, and the voltage at the data node DL is equal to Vt of the TFT by the pre-charging/discharging operation (Vp). The voltage on the data node DL is sampled and holed by the S/H circuit 42. The Vt is provided to the summer 40 through the S/H circuit 42. When Vdata is increased from ground to the desired voltage level, the summer 40 outputs the sum of Vt and Vdata. The switch 44 turns on in response to the programming control signal 46. The voltage at the data node DL goes to (Vt +Vdata). Timing chart for showing the operation of the system 2 having the hybrid driving circuit 12B is similar to that of Figure 5.

[0068] Figure 8 illustrates a further example of a hybrid driving circuit, which is applicable to the hybrid driving circuit 12 of Figure 1. The hybrid driving circuit 12C of Figure 8 implements voltage programming technique.

[0069] The hybrid driving circuit 13C is a direct digital hybrid driving circuit. The direct digital programming circuit 13C includes a microComputer uC 50 which receives digital data (Vdada), a digital to analog (D/A) converter 52, a voltage follower 54 for increasing current without affecting voltage, and an analog to digital (A/D) converter 56.

[0070] The threshold Vt of the drive TFT may increase slowly. Thus, it may not be necessary to acquire the threshold Vt of the drive TFT every programming cycle. This effectively hides the Vt acquisition for the majority of the programming cycle. In the direct digital hybrid driving circuit 13C, the threshold Vt acquired from the pixel circuit 10A is digitalized at the A/D converter 56, and is stored in memory contained in the uC 50. The digital data that defines the brightness of the pixel is added to the Vt in the uC 50. The resulting voltage is then converted back to an analog value at the D/A 52, which is programmed into the pixel circuit 10A. This programming method is designed to compensate for the slow process of the Vt acquisition.

[0071] Figure 9 illustrates an exemplary flow chart for showing the operation of the hybrid driving circuit 12C of Figure 8. At the Vt acquisition mode, the Vt is sampled and recorded at step S30. When writing mode is enabled, new data is provided based on the recorded data. It is noted that the operation of the system having the hybrid driving circuit 12C of Figure 8 is not limited to Figure 9. At the writing mode, the data which have been recorded may be used without implementing the Vt acquisition.

[0072] Figure 10 illustrates an exemplary timing chart for showing the operation of the hybrid driving circuit 12C of Figure 8. During the Vt acquisition, sampling by the A/D converter 56 is implemented. In a next cycle, the hybrid driving circuit 13C may use the Vt that has been previously acquired and has been recorded in the uC 50.

[0073] The conversion of the output on the data node DL by A/D can remove the requirements of having to acquire the Vt every programming cycle. The Vt of the pixel circuit 10A may be acquired once every second or less. Thus, it may acquire Vt for only one row of the display per frame cycle. This effectively increases the amount of time for the pixel programming cycle. Less frequent need of Vt acquisition ensures faster programming time.

[0074] In the above description, Figure 2 is used to describe the pixel circuit 10 of Figure 1. However, the pixel circuit 10 is not limited to that of Figure 2. The pixel circuit 10 may be a pixel circuit illustrated in Figure 11 (J. Kanichi, J.-H. Kim, J.Y. Nahm, Y. He and R. Hattori "Amorphous Silicon Thin-Film Transistor Based Active-Matrix Organic Light Emitting Display" Asia Display IDW 2001 pp. 315). The pixel circuit of Figure 11 includes four TFTs 64-70, a capacitor C_{ST} 72 and an OLED 74. The TFT 78 is a drive TFT that is connected to the OLED 74 and the capacitor C_{ST} 72. The pixel circuit of Figure 11 is selected by Vselect1 and Vselect2, and is programmed by Idata. The voltage acquired is a combination of the voltage across the OLED 74 and T3 68. The technique compensates the voltage change of both the Vt and the OLED 74. Idata of Figure 11 corresponds to the data node DL of Figure 2.

[0075] Figure 12 illustrates a system for driving an AMOLED display in accordance with a further embodiment of the invention. The system 82 of Figure 12 includes a hybrid programming circuit having a correction table 80, a source driver 14 for implementing a voltage-programming scheme and a reference current source 94 for implementing a current-programming scheme. The system 82 drives a display having a plurality of pixel circuits using the voltage-programming scheme and the current-programming scheme.

[0076] A hybrid controller 98 is provided to control each component. In Figure 12, the hybrid controller 98 is placed between the A/D converter 96 and the correction table 80, as an example. The hybrid controller 98 is similar to the hybrid controller 16 of Figure 1.

[0077] The pixel circuit driven by the system 82 may be the pixel circuit 10 of Figure 1, and may be a current programmed pixel circuit or a voltage programmed pixel circuit. The pixel circuit driven by the system 82 may be implemented by Figure 2 or Figure 11, however, is not limited to those of Figures 2 and 11.

[0078] The hybrid programming circuit includes a correction calculation module 92 for correcting data from the data source 90 based on the correction table 80 and an A/D converter 96. The data corrected by the correction calculation module 92 is applied to the source driver 14. The source driver 14 generates Vdata based on the corrected data output from the correction calculation module 92. Vdata from the source driver 14 and Idata from the reference current source 94 are supplied to the hybrid driver 12.

[0079] The data source 90 is, for example, but not limited to, a DVD. The hybrid driver 12 may be implemented either as a switching matrix, or as the digital programming circuit(s) of Figure 8, 20 or combination thereof. The A/D converter 96 may be the A/D converter 56 of Figure 8. The system 82 may implement the Vt acquisition technique described above using the A/D converter 96 (56).

[0080] The correction table 80 is a lookup table. The correction table 80 records the relationship between current required to program the pixel circuit and voltage necessary to obtain that current. The correction table 80 is built for every pixel in the entire display.

[0081] In the description, the relationship between the current required to program the pixel circuit and the voltage necessary to obtain that programming current, is referred to as "current/voltage correction information", "current/voltage correction curve", or "current/voltage information", or "current voltage curve".

[0082] In Figure 12, the correction table 80 is illustrated separately from the correction calculation module 92. However, the correction table 80 may be included in the correction calculation module 92.

[0083] The operation of the system of Figure 12 has two modes, namely display mode and calibration mode. In the display mode, the data from the data source 90 is corrected using the data in the correction table 80, and is applied to the source driver 14. The hybrid driver 12 is not involved in the display mode. In the calibration mode, the current from the reference current source 94 is applied to the pixel circuit, and the voltage associated with the current is read from the pixel circuit. The voltage is converted to a digital data by the A/D converter 96. The correction table 80 is updated with the correct value based on the digital data.

[0084] During the display mode, a voltage-programming scheme is implemented. The voltage on the data line (e.g. DL of Figure 2) of the pixel circuit determines the brightness of the pixels. The voltage required to program the pixel circuit is calculated from the pixel brightness to be displayed (from the incoming video information) combined with the current/voltage correction information stored in the correction table 80. The information on the correction table 80 is combined with incoming video information to ensure that each pixel will maintain a constant brightness over long-term use.

[0085] After the display has been used for a fixed period of time, the display enters the calibration mode. The current source 94 is connected to the data input node (DL) of the pixel circuit via the hybrid driver 12. Each pixel is programmed through a current-programming scheme (where the level of current on the data line determines the brightness of the pixel), and the voltage required to achieve that current is read by the A/D converter 96.

[0086] The voltage required to program the pixel current is sampled at multiple current points by the A/D converter 96. The multiple points may be a subset of the possible current levels (e.g. 256 possible levels for 8-bit, or 64 levels for 6-bit). This subset of voltage measurements is used to construct the correction table 80 that is interpolated from the measurement points.

[0087] The calibration mode may be entered either through user's command or may be combined with the normal display mode so that the calibration takes place during the display refresh period.

[0088] In one example, the entire display may be calibrated at once. The display may stop showing incoming video information for a short period of time while each pixel was programmed with a current and the voltage recorded.

[0089] In a further example, a subset of the pixels may be calibrated, such as one pixel every fixed number of frames. This is virtually transparent to the user, and the correction information may still be acquired for each pixel.

[0090] When a conventional voltage-programming scheme is utilized, a pixel circuit is programmed in an open loop configuration, where there is no feedback from the pixel circuit regarding the threshold voltage shift of the TFTs. When a conventional current-programming scheme is utilized, the brightness of the pixel may remain constant over time. However, the current programming scheme is slow. Thus, the table lookup technique combines the technique of the current-programming scheme with the technique of the voltage-programming scheme. The pixel circuit is programmed with a current through a current-programming scheme. A voltage to maintain that current is read and is stored at a lookup table. The next time that particular level of current is applied to the pixel circuit, instead of programming with a current, the pixel circuit is programmed based on information on the lookup table. Accordingly, it attains the compensation inherent in the current programming scheme while attaining the fast programming time that is only possible with voltage-programming scheme.

[0091] In the above description, the correction table (lookup table) 80 is used to correct the current/voltage correction information. However, the system 82 of Figure 12 may use the lookup table to correct the Vt shift and the current/voltage correction information at the same time in combination with the hybrid driving circuit of Figure 3, 6, 8 or 20.

[0092] For example, several voltage measurements are captured at many different current points by the A/D converter 96 (56). The hybrid controller 98 extracts the Vt shift information by extending the voltage versus current curve to zero current point. The Vt shift information is stored in an array of tables (correction table 80) which is applied to incoming display data.

[0093] The uC 50 of Figure 8 or 20 may utilize the lookup table to generate appropriate voltage and program the pixel circuit.

[0094] The hybrid circuits 12A of Figure 3 and 12B of Figure 6 may be integrated into the system of Figure 12.

[0095] Figures 13-14 illustrate exemplary flow charts for showing the operation of the system of Figure 12. Referring to Figure 13, at step S40, calibration mode is enabled. At step S42, a pixel circuit is selected and current programming is implemented to the selected pixel circuit. At step S44, a switch matrix enable signal is enabled. Then the connection to the pixel circuit is changed. The Vt is sampled at step s46, and then the correction table is created/corrected at step S48. Referring to Figure 14, at step S50, video data are corrected based on the correction table. Then at step S52, new Vdata is produced based on the corrected data.

[0096] It is noted that the writing mode may be implemented based on the previously created correction table without implementing the calibration mode. It is noted that the operation of the system of Figure 12 is not limited to Figures 13-14.

[0097] Figure 15 illustrates an exemplary timing chart for showing a combination of the Vt shift acquisition and the current/voltage correction. A switch matrix enable signal in Figure 15 represents a control signal for the hybrid driver 12 of Figure 12.

[0098] Referring to Figures 12 and 15, the calibration mode (i.e. the current-programming scheme) is enabled when the switch matrix enable signal is high. The programming mode (i.e. the voltage-programming scheme) is enabled when the switch matrix enable signal is low. However, the calibration mode may be enabled when the switch matrix enable signal is low. The programming mode may be enabled when the switch matrix enable signal is high.

[0099] A/D sampling is implemented during the calibration mode. During the calibration mode, the current from the reference current source 94 is applied to the pixel circuit. The voltage on the data input node is converted to a digital voltage by the A/D converter 56. Based on the digital voltage and current associated with the digital voltage, current/voltage correction information is recorded at the lookup table. The Vt shift information is generated based on the data in the correction table 80 or the output from the A/D converter 96.

[00100] The system 82 of Figure 12 may implement hidden refresh technique for refreshing current/voltage correction information in addition to the table lookup technique described above.

[00101] Under the hidden refresh operation, new current/voltage correction information is constructed while completely hidden from user's perception. This

technique utilizes the information that is currently displayed on the screen (i.e. the incoming video data). By obtaining the pixel characteristics from the full calibration routine that has been performed during the manufacturing process of the display, the current/voltage correction information for each pixel in the display is known. During the display's usage, the current/voltage correction curve may shift due to the change in Vt. By measuring a single point along the current/voltage correction curve (which is the data currently displayed, that is part of the video image), a new current/voltage correction curve is extrapolated from the point so that it is fitted to the measured point. Based on the new current/voltage correction curve, the Vt shift information is extracted which is used to compensate for the shift in Vt.

[00102] Figure 16 illustrates an exemplary flow chart for the hidden refresh operation of the system of Figure 12. First, a current/voltage correction curve is produced during the calibration process that is implemented during the manufacturing of the display (step S62). Figure 17 illustrates an example of a sample of the current voltage correction curve.

[00103] Referring to Figure 16, the next step is to measure a point along the curve during the usage of the display. This point can be any point along the curve, so any data that the user currently has on the display can be used for calibration (step S64). Figure 18 illustrates the current voltage correction of Figure 17 and an example of a newly measured data point.

[00104] Referring to Figure 16, the last step is to shift the current/voltage correction curve to fit the point of voltage verses current relationship that is measured (step S66). Figure 19 illustrates an example of a new current voltage correction curve based on the measured point of Figure 18.

[00105] The process associated with Figures 17-19 is implemented in the hybrid controller 98 of Figure 12.

[00106] The system 82 of Figure 12 may implement a combined current and voltage-programming technique. Figure 20 illustrates one example of a hybrid driving circuit for implementing the combined current and voltage-programming technique.

The hybrid driving circuit of Figure 20 may be included in the hybrid driver 12 of Figure 12.

[00107] In the hybrid driving circuit of Figure 20, the digital hybrid driving circuit 12C and a current source 100 are provided to the data line DL of the pixel circuit.

[00108] To enhance the circuit's ability to compensate for a change in the current/voltage correction curve due to temperature, threshold voltage shift, or other factors, the pixel circuit programming is divided into two phases.

[00109] During the writing mode, the pixel circuit 10A is voltage-programmed first to set the gate voltage of the driving TFT to an approximate value, then followed by a current programming phase. The current programming phase can then fine-tune the output current. The system of Figure 20 is faster than current programming and has the compensation capabilities of the current programming scheme.

[00110] In Figure 20, the digital hybrid driving circuit 12C is provided. However, the combined current and voltage-programming technique may be implemented by combining the hybrid driving circuit 12A of Figure 3 or 12B of Figure 6 with the current source 100. The current source 100 may be the reference current source 94 of Figure 12.

[00111] The system 2 of Figure 1 may implement the hidden refresh technique described above. The system 2 of Figure 1 may implement the combined current and voltage-programming technique. The system 2 of Figure 1 may include the hybrid driving circuit of Figure 20 to implement the combined current and voltage-programming technique.

[00112] Extension of the direct digital programming scheme is now described in detail. The direct digital programming scheme (Figures 6, 8 and 20) can be extended to drive an OLED array (e.g. a 4T OLED array) using voltage programmed column drivers, such as those used for driving Active Matrix Liquixd Crystal Display (AMLCD), or voltage-programmed Active-Matrix Organic Light Emitting Diode (AMOLED) displays, or any other voltage-output display driver.

[00113] Figure 21 illustrates a system for driving an AMOLED array having a plurality of pixel circuits in accordance with a further embodiment of the invention. The system 105 of Figure 21 includes a voltage column driver 112, a programmable current source 114, a switching network 116, an A/D converter 118 and a row driver 120.

[00114] The voltage column driver 112 is a voltage programmed column driver. Each of the voltage column driver 112 and the row driver 120 may be any driver that has a voltage output, such as those designed for the AMLCD. The voltage column driver 112 and the programmable current source 114 are connected to an OLED array 110 through the switching network 116. The OLED array 110 forms an AMOLED display, and contains a plurality of pixel circuits (such as 10 of Figure 1). The pixel circuit may be a current programmed pixel circuit or a voltage programmed pixel circuit.

[00115] The A/D converter 118 is an interface that allows an analog signal (i.e. current driving the display 110) to be read back as a digital signal. The digital signal associated with the current can than be processed and/or stored. The A/D converter 118 may be the A/D converter 56 of Figures 8 and 20. The column driver 112 may be the source driver 14 of Figures 1 and 12.

[00116] The system 105 of Figure 21 implements the calibration mode and the display mode as described above.

[00117] Figure 22 illustrates an example of the switch network 116 of Figure 21. The switching network 116 of Figure 22 includes two MOSFET switches 122 and 124 that can switch the column of the display (110) from connecting to the column driver (112) to the combination of the current source (114) and the A /D converter (118), and vice versa. A shift register 126 is a source of the digital control signal that controls the operation of the MOS switches 122 and 124. An inverter 128 inverts an output from the shift register 126. Thus, when the switch 122 is on (off), the switch 124 is off (on).

[00118] The switching network 116 may be located either off the glass in the column driver (112) or directly on the glass using TFT switches.

[00119] Referring to Figures 21-22, the system 105 uses only one current source 114. The voltage-programming drivers (such as, AMLCD drivers, or any other voltage-output drivers) drive the rest of the display 110. The switching matrix (switching network 116) allows different pixels within the array of pixels to be connected to a single current source (114) through a time division method. This allows a single current source to be applied to the entire display. This lowers the cost of the driver circuit and speeds up the programming time for the pixel circuit.

[00120] The system 105 uses the A/D converter 118 to convert an analog output of the data node (e.g. DL of Figure 2) of the pixel circuit to digital data. The conversion by the A/D converter 118 removes the requirements of having to acquire the Vt every programming cycle. The Vt of the pixel circuit may be acquired once every few minutes. Thus it may acquire one column of the panel every refresh cycle.

[00121] Only one A/D 118 may be implemented for all the columns. The circuit acquires only one pixel per frame refresh. For example, for a 320 by 240 panel, the number of pixels is 76, 8000. For a frame rate of 30Hz, the time required to acquire Vt from all pixels for the entire frame is 43 minutes. This may be acceptable for some applications, providing that Vt does not shift substantially in an hour.

[00122] The parasitics only affect the amount of time to discharge the capacitor to acquire Vt. Since the circuit is voltage-programmed, it is not affected by the parasitics. Since Vt is only acquired one column per frame time, it can be long. For example, for a display with 320 columns that has a frame rate of 30Hz, each frame time is 33mS. For voltage programming, it is possible to program a pixel in 70uS. For 320 columns, the time to update the display is 22mS, which still leave 11mS to complete a charge/discharge cycle.

[00123] The system 105 may implement the lookup table technique to compensate for Vt shift and/or to correct the current/voltage information as described above

[00124] The system 105 may implement the hidden refresh technique to acquire the Vt shift information and current/voltage correction information of each pixel circuit (10) in the display 110. This current/voltage correction information is used to populate

a lookup table (e.g. a correction table 80 of Figure 12) that will then be used to compensate for the degradation in the pixel circuit, which is caused by aging. To reduce cost, the number of current-programmed circuits has been reduced so there is only one per display instead of one per column driver.

[00125] The system 105 may implement the combined current and voltage-programming technique as described above.

[00126] The current/voltage information of the pixel circuit can be further corrected by implementing a system illustrated in Figure 23. Figure 23 illustrates a system for correcting the current/voltage information of the pixel circuit. In Figure 23, a display 130 is depicted as a 2T or 4T OLED array. However, the display 130 may include a plurality of pixel circuits, each having three or more than four transistors. The display 130 may include voltage-driven pixel circuits or current-driven pixel circuits. The system of Figure 23 is applicable to the systems 2, 82 and 105 of Figures 1, 12 and 22.

[00127] As illustrated in Figure 23, a switch 132 is provided to disconnect the common electrode of the OLED. It is well known that two electrodes are provided for the OLED. One is connected to the pixel circuit, and the other is a common electrode connected to all OLEDs. It is noted that the common electrode may be Vdd or GND depending on the type of OLED. The switch 132 connects the common electrode of the OLED into a current sensing network 134 utilizing a high side common mode sensor (such as, INA168 by TI). The current sensing network 134 measures the current through the common electrode.

[00128] During the calibration phase, each pixel is lit individually and the current consumed is acquired by the sensing network 134. The acquired current is used to correct the lookup table (e.g. the correction table 80 of Figure 12) populated by the direct digital hybrid driving circuit of Figure 8 or 20.

[00129] A dark display current may be acquired to include the effect of dead pixel and leakage current of the array. During this procedure, all pixels are turned off, and the current (i.e. dark display current) is measured.

[00130] According to the embodiments of the present invention, the major issue with current-programmed pixel circuits, which is the slow programming time, is solved. The concept of using feedback to compensate the pixel circuit enhances the uniformity and stability of the display while retaining the fast programming capability of the voltage programmed drive scheme.

[00131] The present invention has been described with regard to one or more embodiments. However, it will be apparent to persons skilled in the art that a number of variations and modifications can be made without departing from the scope of the invention as defined in the claims.

WHAT IS CLAIMED IS:

1. A system for driving a display which includes a plurality of pixel circuits, each having a plurality of thin film transistors (TFTs) and an organic light emitting diode (OLED), comprising:

a voltage driver for generating a voltage to program the pixel circuit;

a programmable current source for generating a current to program the pixel circuit; and

a switching network for selectively connecting the data driver or the current source to one or more pixel circuits.

2. A system according to claim 1, wherein the switching network includes:

a first switch for connecting the voltage driver to one or more pixel circuits, and

a second switch for connecting the current source to one or more pixel circuits.

3. A system according to claim 2, wherein the switching network includes:

a shift register for controlling the operation of the first and second switches.

4. A system according to claim 1, further comprising:

a analog/digital converter for sampling a voltage on a data node of the pixel circuit.

5. A system according to claim 1, further comprising:

a lookup table for storing a current/voltage information representing a relationship between a program current and a program voltage associated with the program current.

6. A system according to claim 5, further comprising:

a current sensing network for sensing a current consumed in the pixel circuit to correct the lookup table.

7. A system according to claim 5, further comprising:

a module for correcting the current/voltage information during the current-based programming or the voltage-based programming.

8. A system according to claim 1, further comprising:

a programming circuit for acquiring the threshold voltage of the TFT from the pixel circuit, having an analog to digital converter for converting an analog threshold voltage information to a digital threshold voltage information, and for programming the pixel circuit based on the digital threshold voltage information and the voltage associated with incoming video information.

9. A system for driving a pixel circuit having a plurality of thin film transistors (TFTs) and an organic light emitting diode (OLED), comprising:

a pre-charge controller for pre-charging and discharging a data node of the pixel circuit to acquire threshold voltage information of the TFT from the data node; and

a hybrid driving circuit for programming the pixel circuit based on the acquired threshold voltage information and video data information displayed on the pixel circuit.

10. A system according to claim 9, wherein the hybrid driving circuit includes a capacitor coupled to the data node.

11. A system according to claim 9, wherein the hybrid driving circuit includes:

a sampling circuit for sampling the threshold voltage information on the data node,

a summer for summing the video data voltage and the sampled voltage threshold information, and

a switch for selectively connecting the output of the summer to the data node.

12. A system according to claim 9, wherein the hybrid driving circuit includes:

an analog to digital converter for converting the threshold voltage information to a digital threshold voltage information,

a microcomputer for storing the digital threshold voltage information and summing the digital threshold voltage information and the voltage, and

a digital to analog converter for converting the summing result output from the microcomputer to an analog data and providing the analog data to the data node.

13. A system according to claim 9, further comprising:

a programming circuit for providing a current on the data node to program the pixel circuit.

14. A system according to claim 9, wherein the hybrid driving circuit includes a switching matrix for selecting one of a voltage programming mode and a current programming mode to program the pixel by the selected programming mode.

15. A system for driving a pixel circuit having a plurality of thin film transistors (TFTs) and an organic light emitting diode (OLED), comprising:

a sampler for sampling, from a data node of the pixel circuit, a voltage required to program the pixel circuit;

a programming circuit for programming the pixel circuit based on the sampled voltage and video data information displayed on the pixel circuit.

16. A system according to claim 15, further comprising:

a current source for providing current to the pixel circuit during a calibration mode; and

a lookup table for storing a current/voltage information representing a relationship between the current and the sampled voltage associated with the current.

17. A systems according to claim 16, wherein the lookup table is created to each pixel circuit.

18. A system according to claim 16, further comprising:

a correction calculation module for correcting data from a data source based on the current/voltage information,

during a writing mode, a voltage associated with the corrected data being applied to the pixel circuit.

19. A system according to claim 16, further comprising:

a module for extracting a threshold voltage shift of the TFT based on the sampled voltage.

20. A system according to claim 15, further comprising:

a lookup table for storing a current/voltage curve representing a relationship between a current and a voltage necessary to program the current into the pixel circuit;

a module for correcting the current/voltage curve based on the sampled voltage associated with information currently displayed on the pixel circuit,

during a writing mode, a voltage to be programmed being determined based on the current/voltage curve.

21. A systems according to claim 20, wherein the lookup table is created to each pixel circuit.

22. A system according to claim 20, further comprising:

a module for extracting a threshold voltage shift of the TFT based on the corrected current/voltage curve.

23. A system according to any one of claims 1-22, wherein the system is applicable to a current-programmed pixel circuits and a voltage-programmed pixel circuit.

24. A system according to any one of claims 1-22, wherein the TFT includes amorphous silicon, polysilicon (n-type or p-type), crystalline silicon, or organic based TFT.

25. A system according to any one of claims 1-22, wherein the OLED includes NIP or PIN OLED, and is locatable in the source or the drain of one or more driving TFTs.

26. A method of driving a pixel circuit having a plurality of thin film transistors (TFTs) and an organic light emitting diode (OLED), comprising:

selecting a pixel circuit and pre-charging a data node of the pixel circuit;

allowing the pre-charged data node to be discharged;

extracting a threshold voltage of the TFT through the discharging step; and

programming the pixel circuit, including compensating a programming data based on the extracted threshold voltage.

27. A method according to claim 26, wherein the extracting step includes:

sampling the threshold voltage, and

recording the sampled threshold voltage, the compensating step utilizing the recorded sampled threshold voltage.

28. A method according to claim 27, wherein the programming step includes:

subsequently programming the pixel circuit based on the recorded threshold voltage.

29. A method according to claim 26, wherein the programming step includes:

programming information on the pixel circuit with a current-programming scheme and a voltage-programming scheme.

30 A method of driving a pixel circuit having a plurality of thin film transistors (TFTs) and an organic light emitting diode (OLED), comprising:

sampling, from a data node of the pixel circuit, a voltage required to program the pixel circuit;

programming the pixel circuit based on the sampled voltage and information displayed on the pixel circuit.

31. A method according to claim 30, further comprising:

enabling a calibration mode, and implementing a current-programming scheme to the pixel circuit,

the sampling step implementing sampling operation during the calibration mode.

32. A method according to claim 31, further comprising:

creating, based on the sampling, a lookup table storing a current/voltage correction information representing the current and the sampled voltage associated with the current,

the programming step including the step of correcting data from a data source based on the current/voltage correction information.

33. A method according to claim 30, further comprising:

storing a current/voltage correction information representing a current and a voltage necessary to program the current into the pixel circuit, and

correcting the current/voltage correction information based on the sampled voltage associated with information currently displayed on the pixel circuit.

34. A method according to claim 32, further comprising:

sensing a current consumed in the pixel circuit,

correcting the current/voltage correction information based on the sensed current.

35. A method according to claim 33, further comprising:

sensing a current consumed in the pixel circuit, the correcting step correcting the current/voltage correction information based on the sensed current.

36. A hybrid driving circuit for implementing the switching network according to claim 1, wherein the hybrid driving circuit is applicable to driving scheme, including drive schemes that use timing of the data, select or power inputs to the pixel circuits to achieve increased brightness uniformity, drive schemes that use current or voltage feedback, and drive schemes that use optical feedback.

37. A hybrid driving circuit for implementing the system according to claim 9 or 15, wherein the hybrid driving circuit is applicable to any driving scheme, including drive schemes that use timing of the data, select or power inputs to the pixel circuits to achieve increased brightness uniformity, drive schemes that use current or voltage feedback, and drive schemes that use optical feedback.

38. A system according to any one of claims 1-22, wherein the OLED material includes fluorescent, phosphorescent, polymer, or dendrimer.

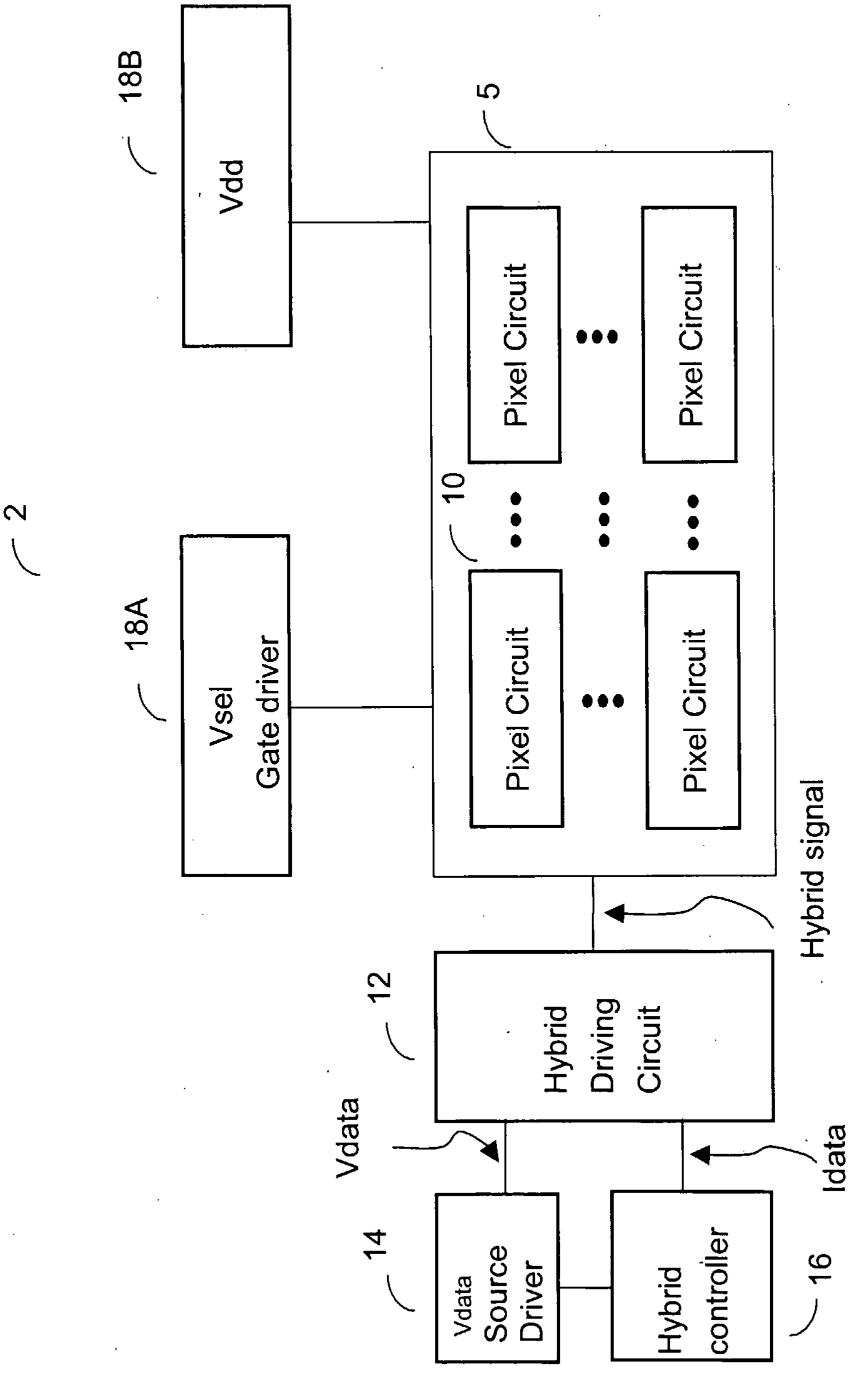

2
18B
Vdd
18A
Vsel
Gate driver
5
Pixel Circuit
Pixel Circuit
Pixel Circuit
Pixel Circuit
10
Hybrid signal
12
Hybrid
Driving
Circuit
Vdata
Idata
14
Vdata
Source
Driver
Hybrid
controller
16

FIG.1

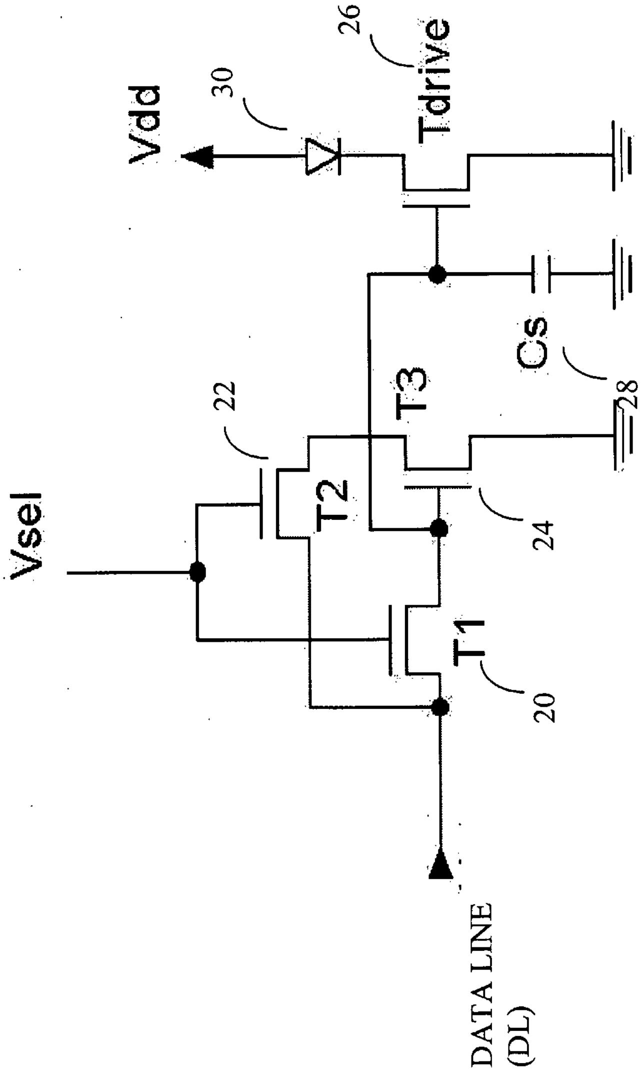


FIG.2

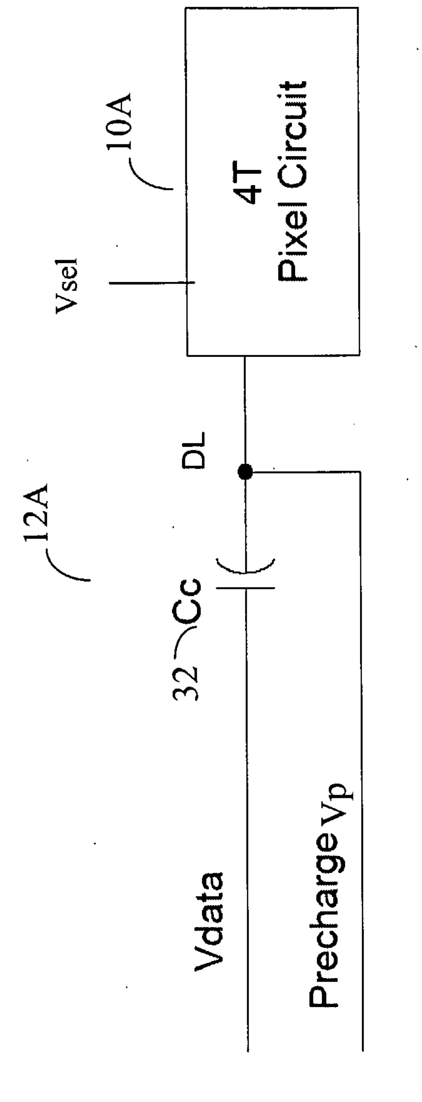


FIG.3

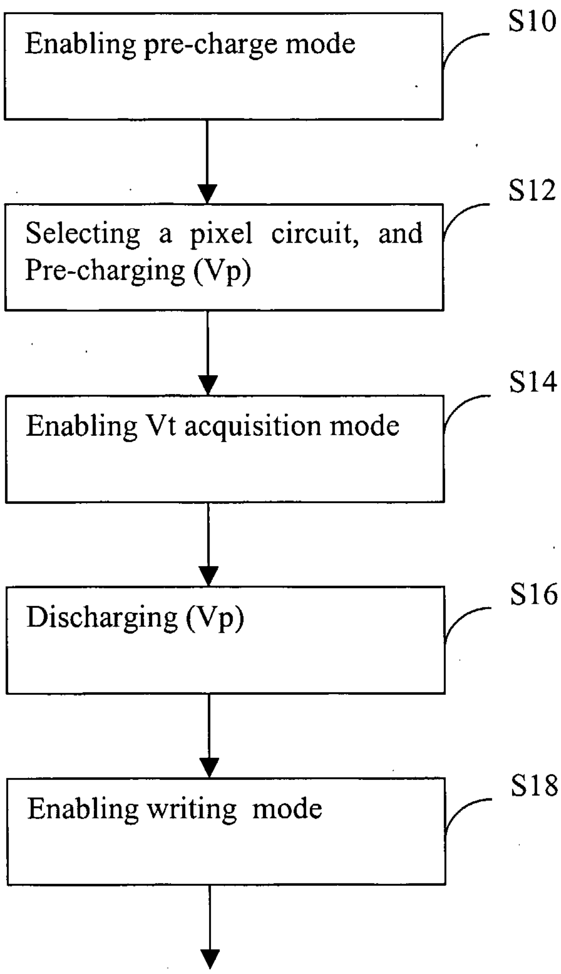

Enabling pre-charge mode
S10
Selecting a pixel circuit, and Pre-charging (Vp)
S12
Enabling Vt acquisition mode
S14
Discharging (Vp)
S16
Enabling writing mode
S18

FIG. 4

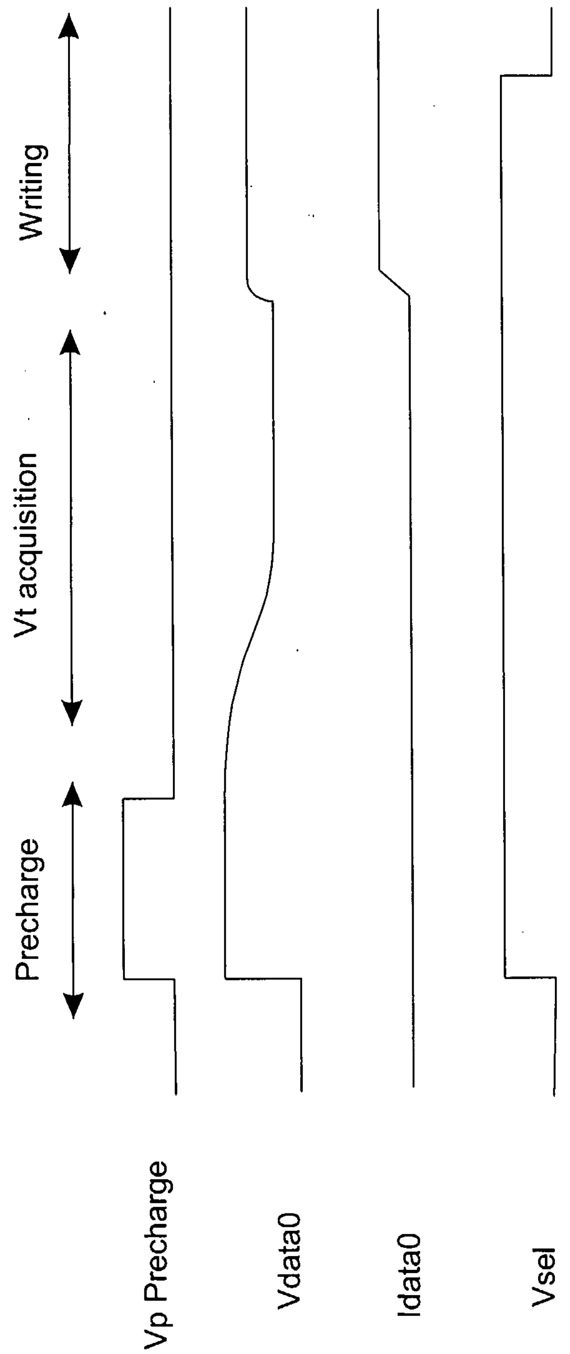

Writing
Vt acquisition
Precharge
Vp Precharge
Vdata0
Idata0
Vsel

FIG.5

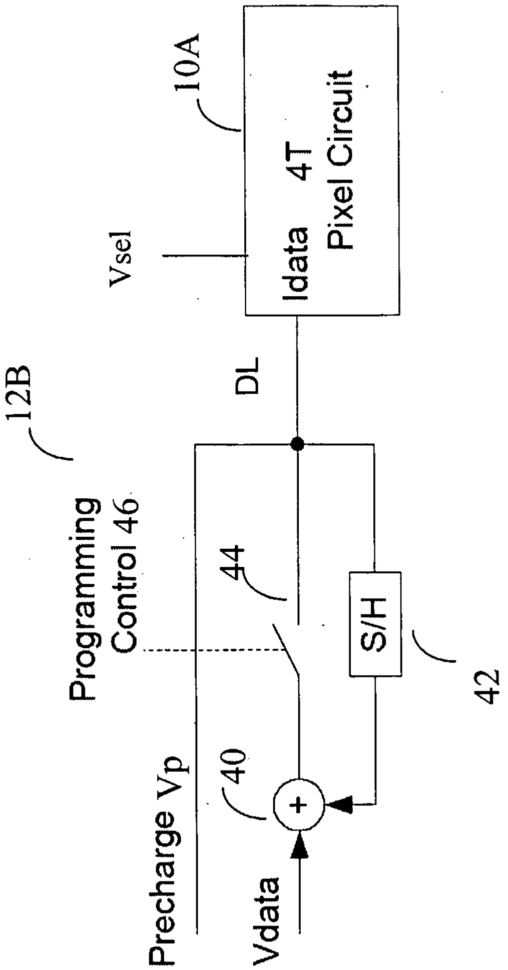

10A
Idata
4T
Pixel Circuit
Vsel
DL
12B
Programming
Control 46
44
S/H
42
Precharge Vp
40
+
Vdata

FIG.6

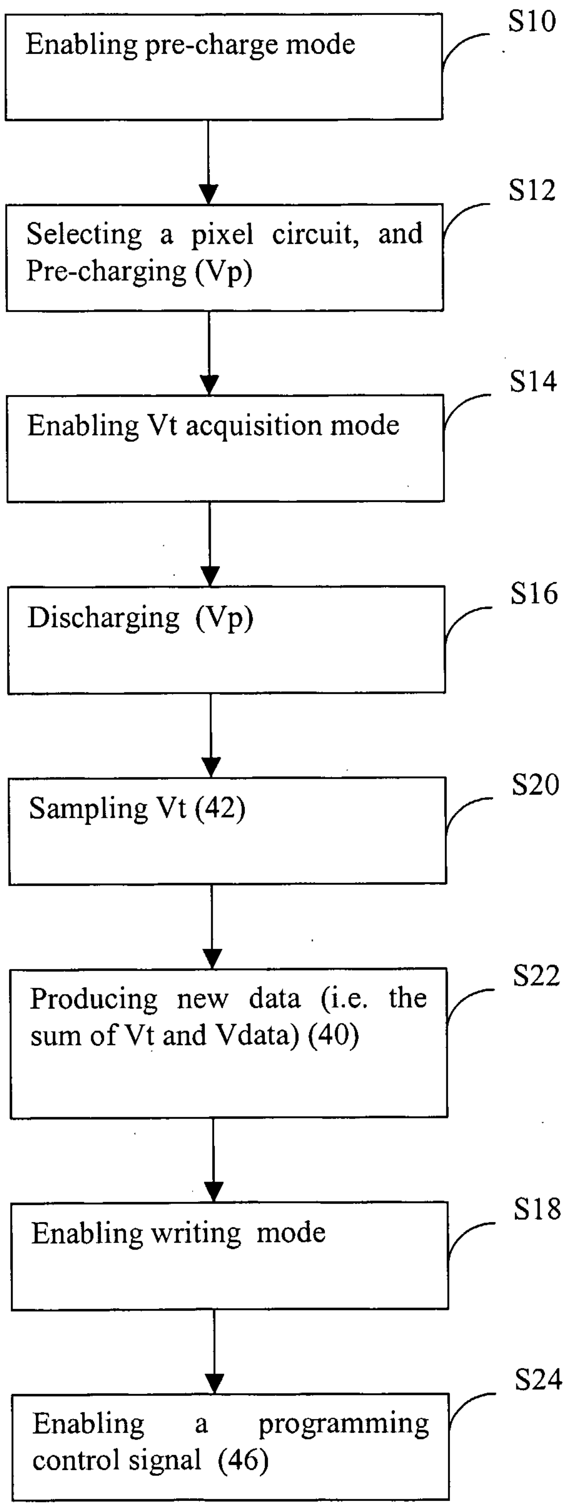

Enabling pre-charge mode
S10
Selecting a pixel circuit, and Pre-charging (Vp)
S12
Enabling Vt acquisition mode
S14
Discharging (Vp)
S16
Sampling Vt (42)
S20
Producing new data (i.e. the sum of Vt and Vdata) (40)
S22
Enabling writing mode
S18
Enabling a programming control signal (46)
S24

FIG. 7

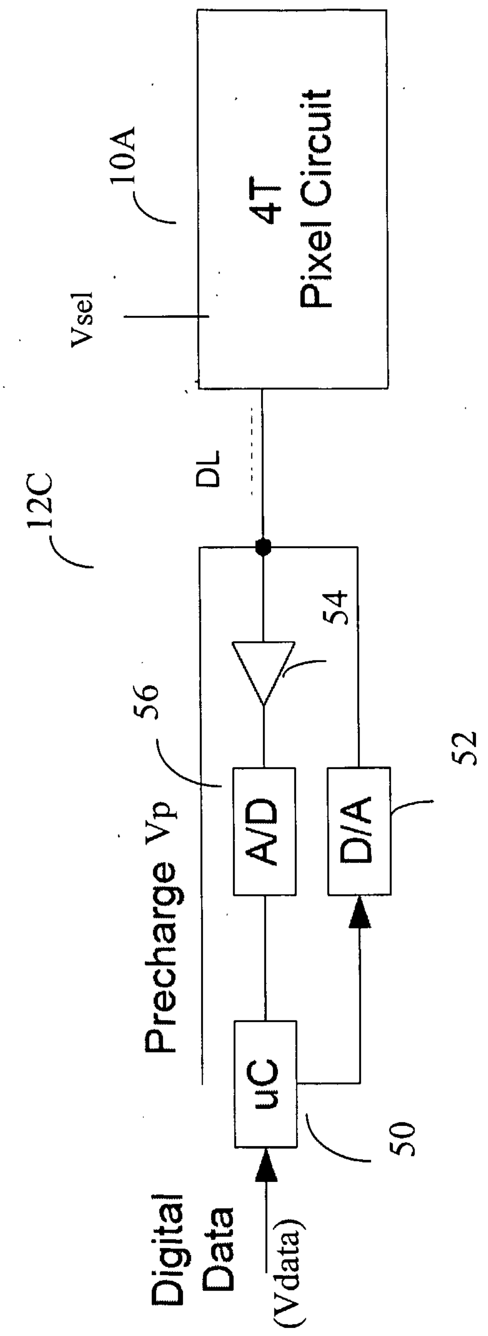

4T
Pixel Circuit
10A
Vsel
DL
12C
54
56
Precharge Vp
A/D
D/A
52
uC
50
Digital
Data
(Vdata)

FIG.8

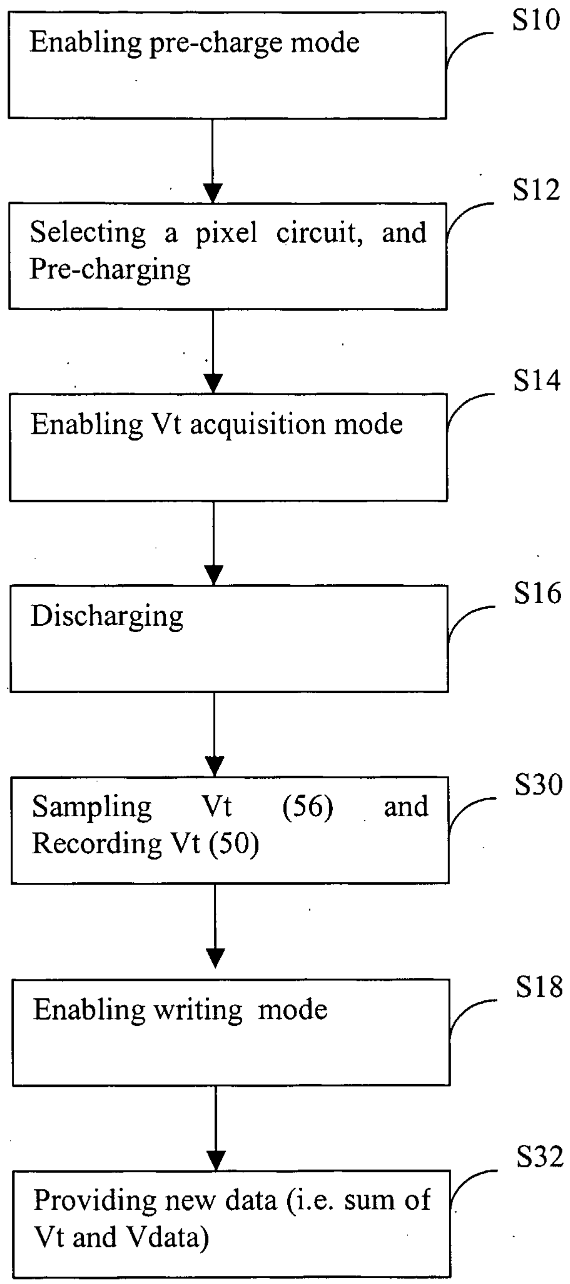

Enabling pre-charge mode
S10
Selecting a pixel circuit, and Pre-charging
S12
Enabling Vt acquisition mode
S14
Discharging
S16
Sampling Vt (56) and Recording Vt (50)
S30
Enabling writing mode
S18
Providing new data (i.e. sum of Vt and Vdata)
S32

FIG. 9

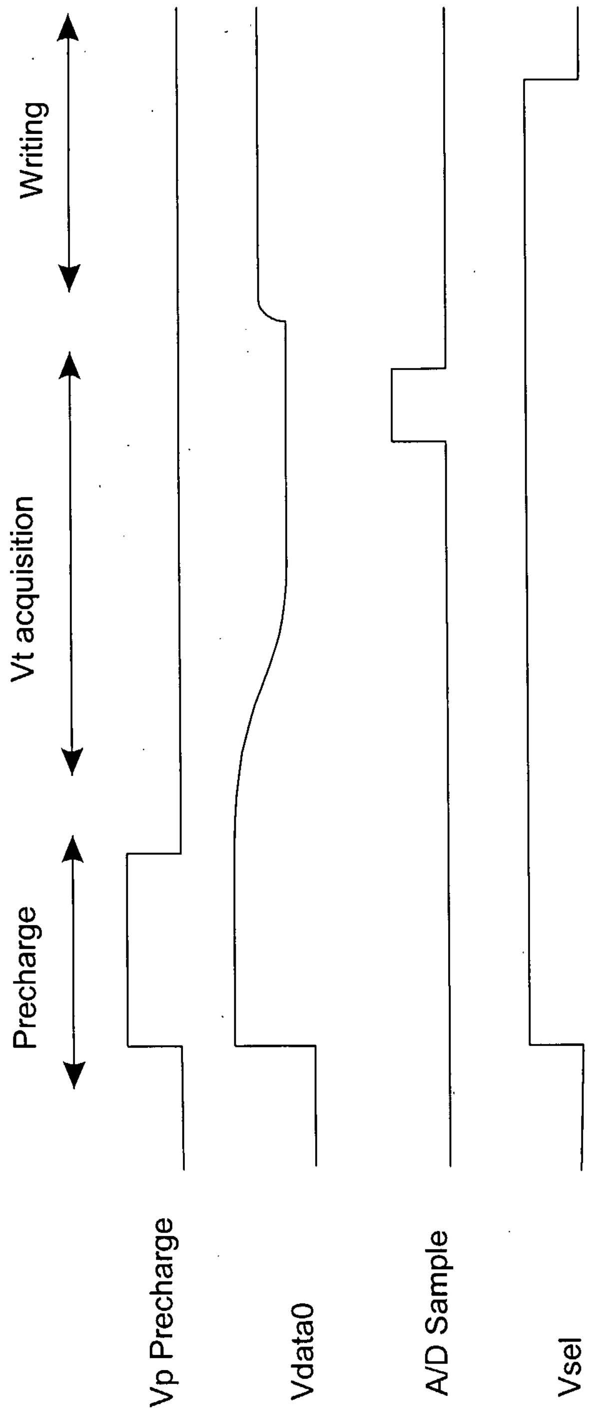

Writing
Vt acquisition
Precharge
Vp Precharge
Vdata0
A/D Sample
Vsel

FIG.10

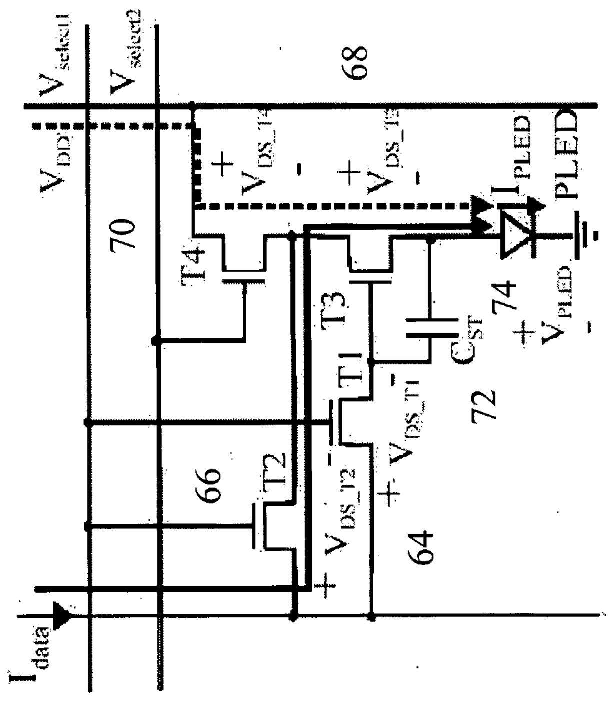

Vselect1
Vselect2
68
VDD
70
T4
VDS_T4
VDS_T3
IPLED
PLED
T3
74
CST
VPLED
T1
VDS_T1
72
66
T2
VDS_T2
64
Idata

FIG.11

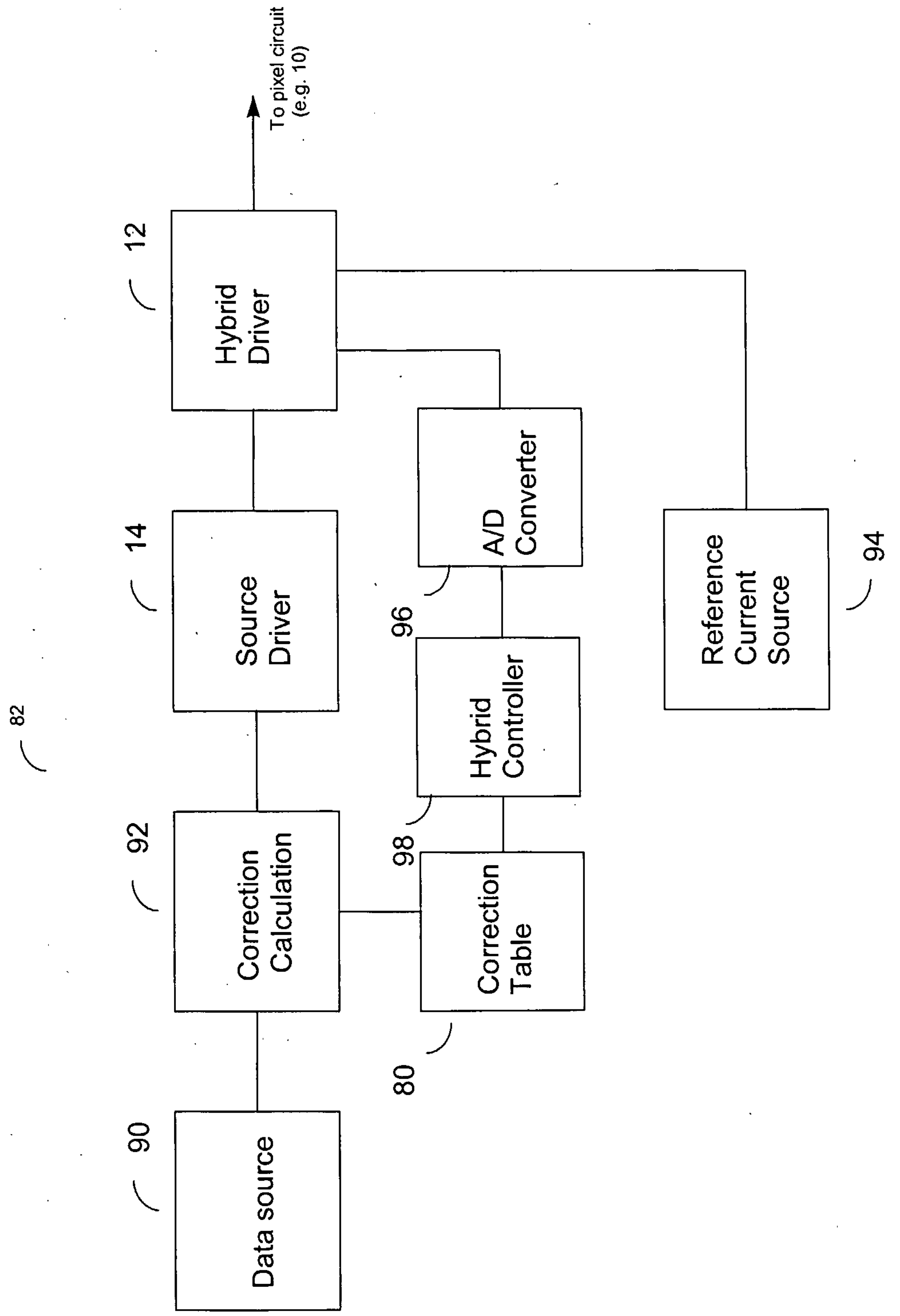

To pixel circuit
(e.g. 10)
Hybrid
Driver
12
Source
Driver
14
Correction
Calculation
92
Data source
90
82
A/D
Converter
96
Hybrid
Controller
98
Correction
Table
80
Reference
Current
Source
94

FIG. 12

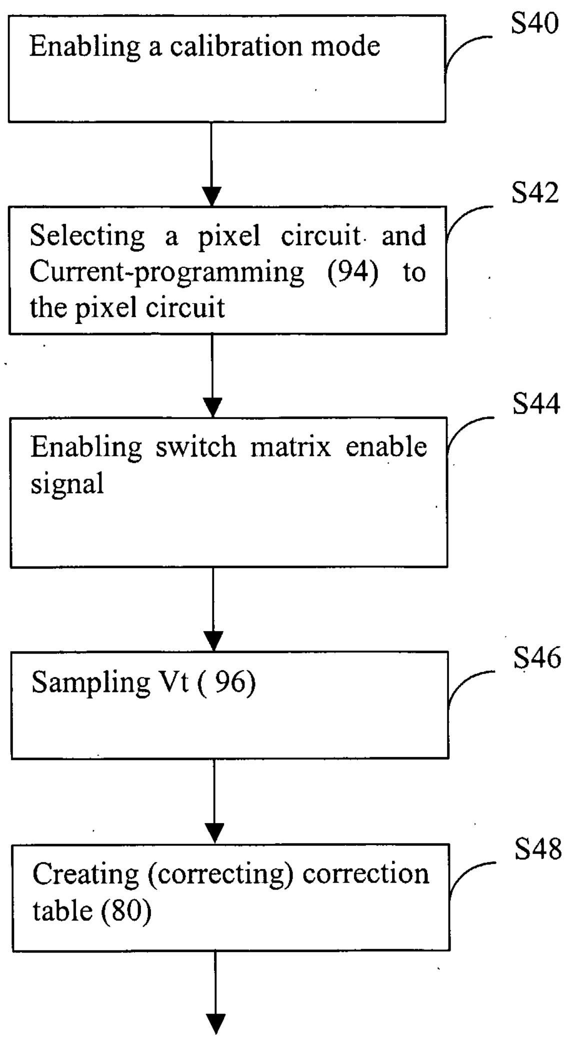

Enabling a calibration mode
S40
Selecting a pixel circuit and Current-programming (94) to the pixel circuit
S42
Enabling switch matrix enable signal
S44
Sampling Vt (96)
S46
Creating (correcting) correction table (80)
S48

FIG. 13

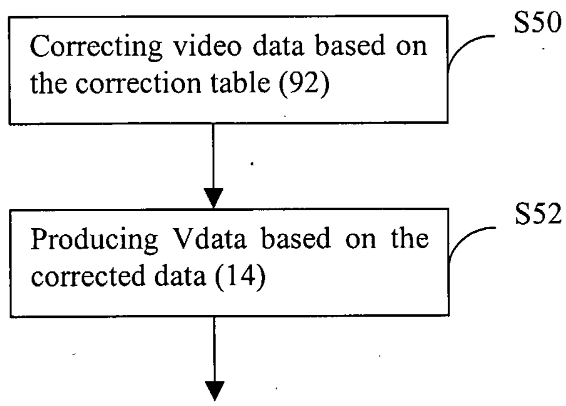

Correcting video data based on the correction table (92)
S50
Producing Vdata based on the corrected data (14)
S52

FIG. 14

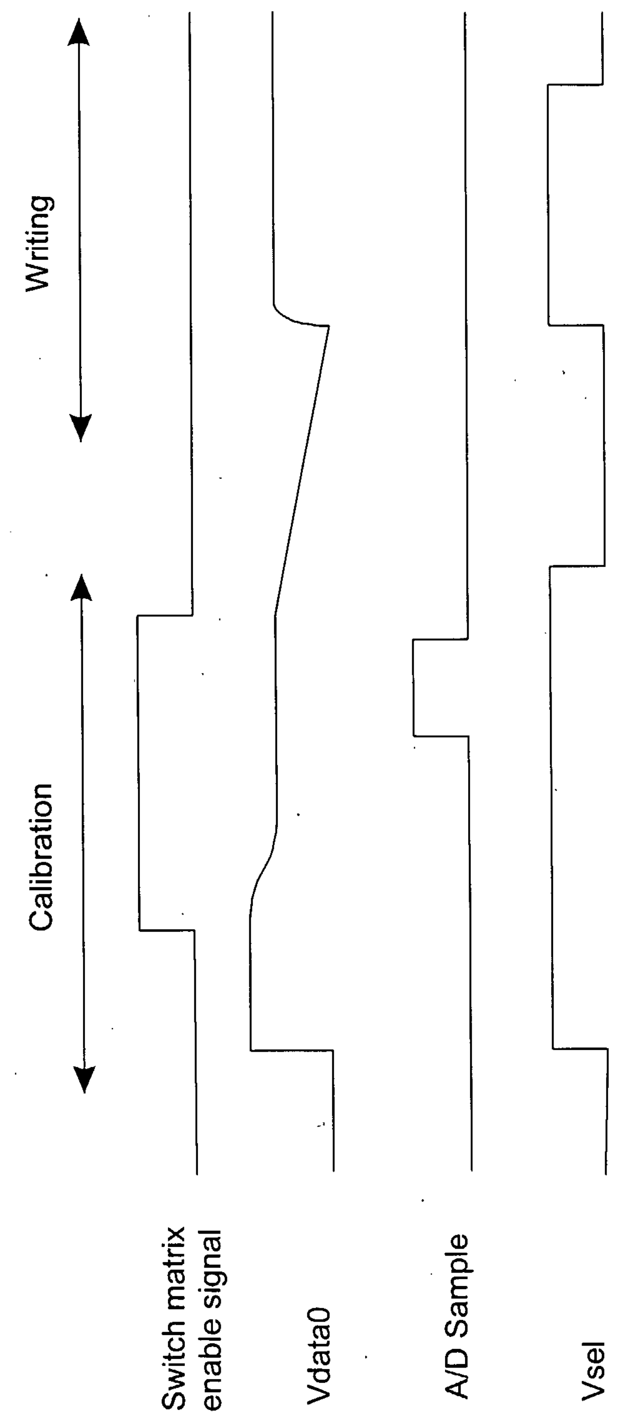

Writing
Calibration
Switch matrix enable signal
Vdata0
A/D Sample
Vsel

FIG. 15

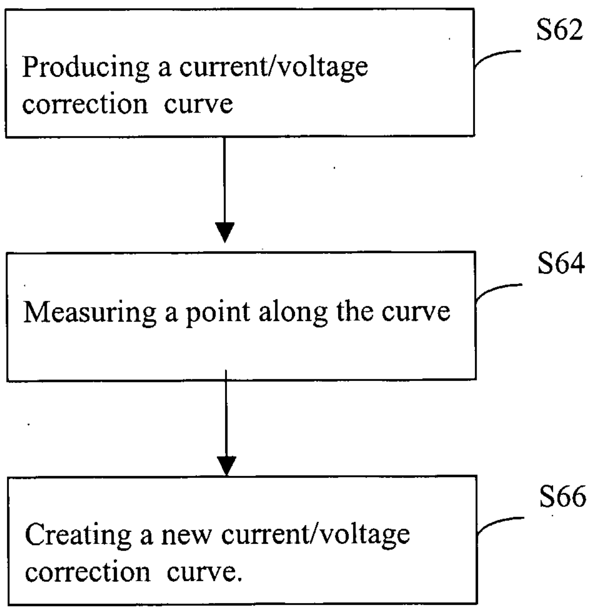

Producing a current/voltage correction curve
S62
Measuring a point along the curve
S64
Creating a new current/voltage correction curve.
S66

FIG.16

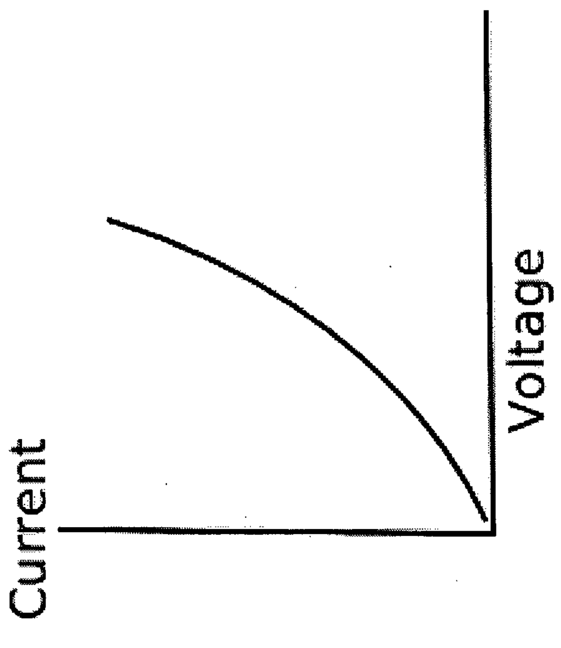


FIG. 17

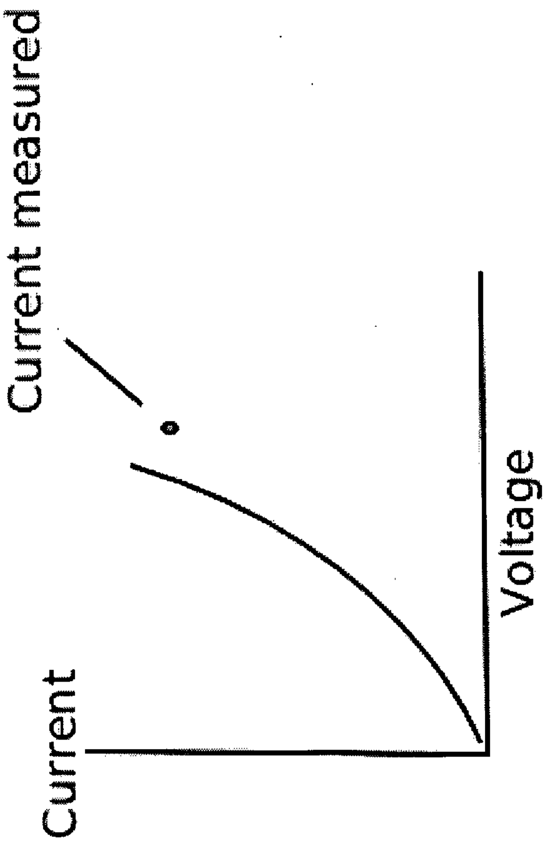


FIG. 18

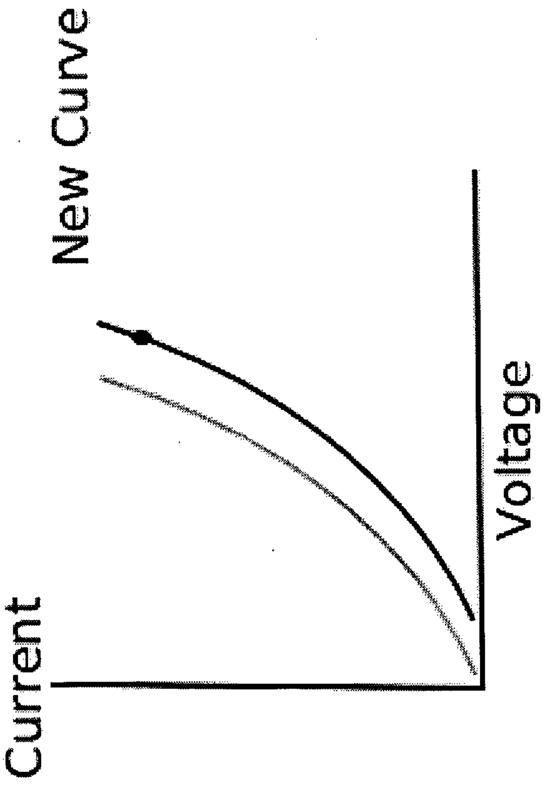


FIG. 19

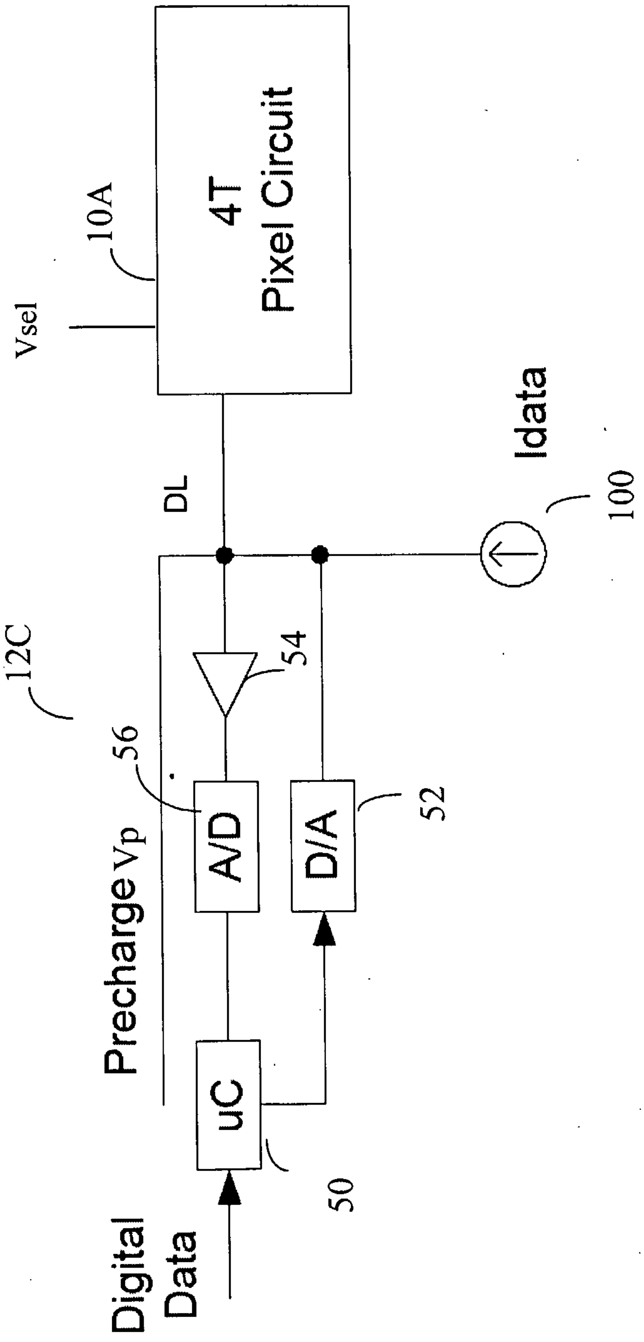

4T
Pixel Circuit
Vsel
10A
DL
Idata
100
12C
54
56
Precharge Vp
A/D
D/A
52
uC
50
Digital
Data

FIG. 20

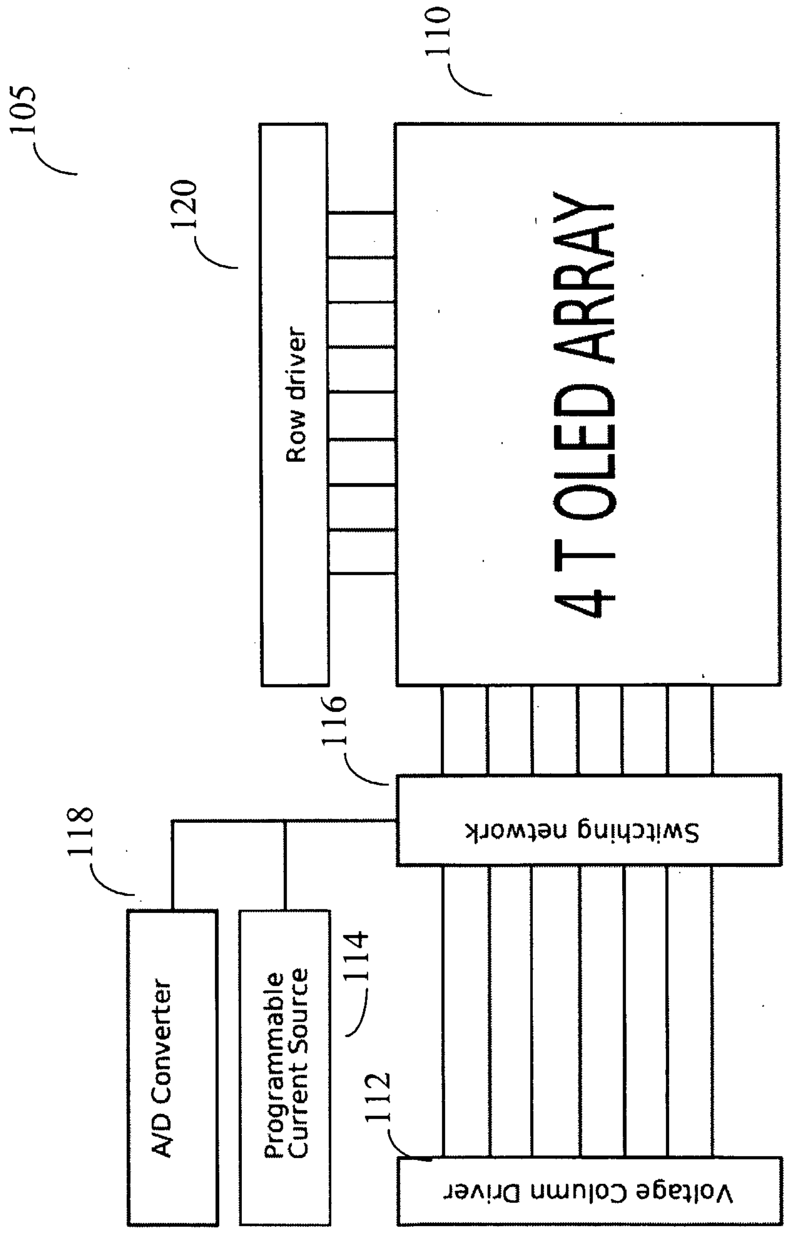

105
110
120
Row driver
4 T OLED ARRAY
116
Switching network
118
A/D Converter
Programmable Current Source
114
112
Voltage Column Driver

FIG. 21

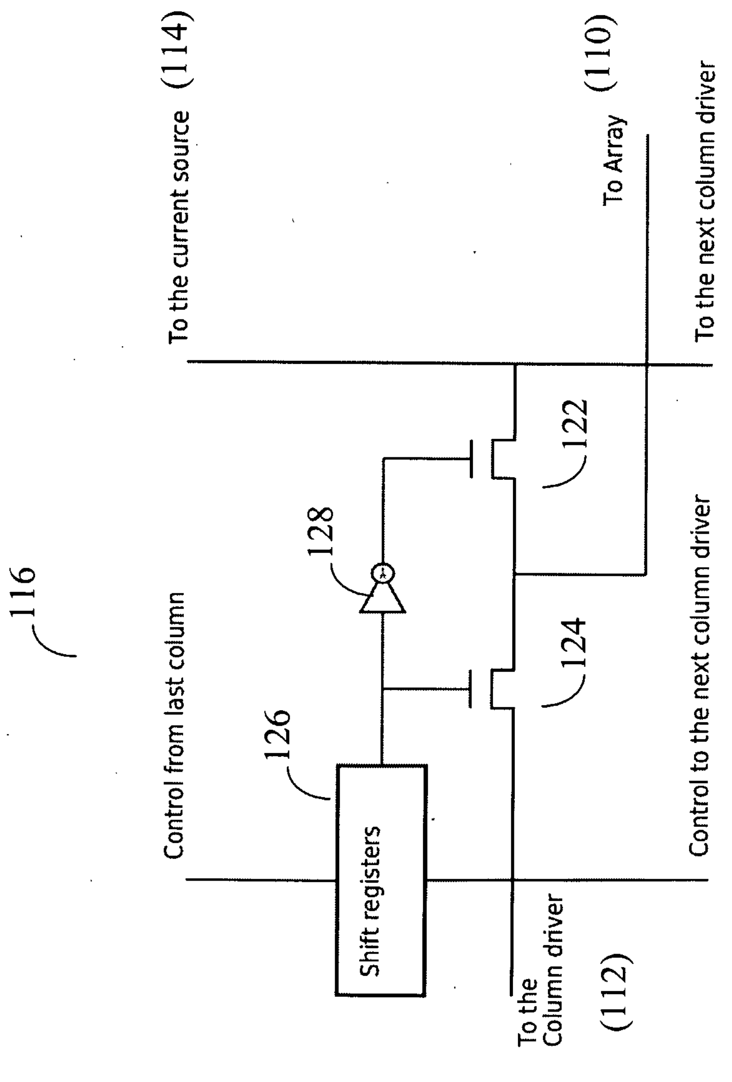
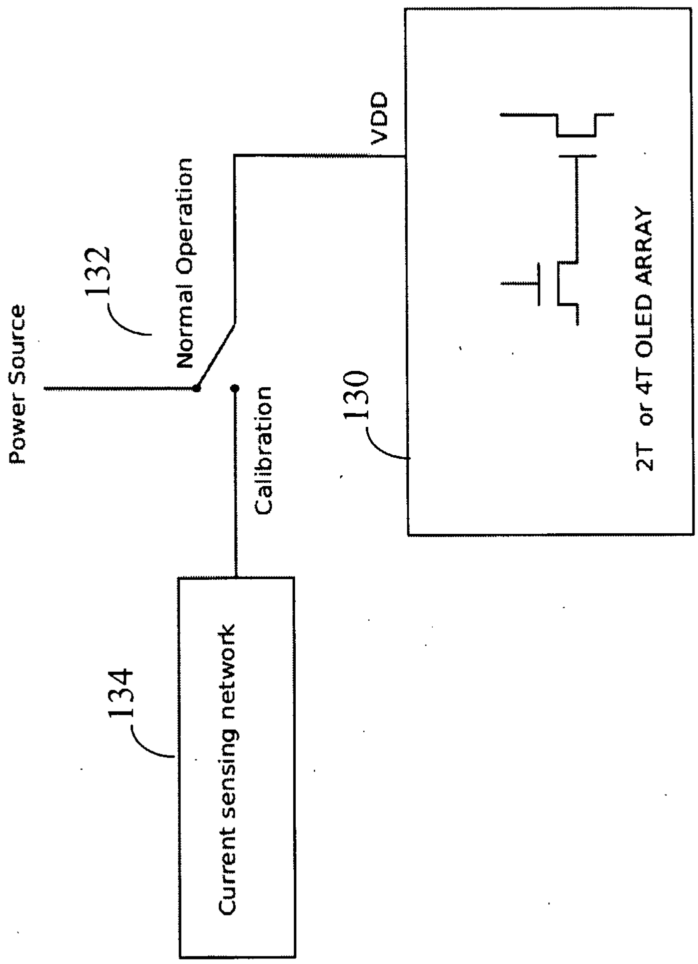

116
To the current source (114)
To Array (110)
To the next column driver
122
128
124
126
Control from last column
Shift registers
Control to the next column driver
To the
Column driver
(112)

FIG. 22



Power Source
132
Normal Operation
Calibration
VDD
130
2T or 4T OLED ARRAY
134
Current sensing network

FIG. 23

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2005/001007

1. CLASSIFICATION OF SUBJECT MATTER

IPC(7) G09G-3/32

2. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC^7 G09G-3/32; CANADIAN 375/1 - 375/18; 375/33 - 375/36; 375/40

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base, and, where practicable, search terms used) :

Databases : Delphion, West, USPTO, Espacenet, Canadian Patent Database
Keywords : voltage driver; current programming; active matrix; TFT; OLED; threshold voltage; hybrid circuit; pre-charge; DAC; polymer; fluorescent; phosphorescent; dendrimer

3. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6618030 (KANE et al.) 9 September 2003 (09.09.2003), Columns 1-5, 12-13; Figs. 9, 13	1-2, 4-35
Y		3, 37, 38
X	CA 2498136 (STEVENSON et al.) 18 March 2004 (18.03.2004), abstract; pages 1, 27; figs. 15, 16	1, 2, 36
Y		37
Y	US 6594606 (EVERITT) 15 July 2003 (15.07.2003), abstract, columns 3-4	3
Y	US 6687266 (MA et al.) 3 February 2004 (03.02.2004), abstract, column 1	38

Further documents are listed in the continuation of Box C. Patent family members are listed in annex. [X]

* Special categories of cited documents :
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international-type search
03 September 2005 (03-09-2005)

Date of mailing of the international-type search report
18 October 2005 (18-10-2005)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/CA2005/001007

Patent Document Cited in the Search Report		Publication Date (dd.mm.yyyy)	Patent Family Members	Publication Date(s) (dd.mm.yyyy)
X	US 6618030	09.09.2003	US 6229508	08.05.2001
			JP 11219146 A2	10.08.1999
			EP 905673 A1	31.03.1999
X	CA 2498136	18.03.2004	WO 04/23443 A2	18.03.2004
			US 20040183759 A1	23.09.2004
			EP 1537557 A2	08.06.2005
			AU 3266011 AA	29.03.2004
Y	US 6594606	15.07.2003	WO 03/34389 A2	24.04.2003
			WO 02/91344 A2	14.11.2002
			WO 02/91342 A2	14.11.2002
			WO 02/91032 A2	14.11.2002
Y	US 6687266	03.02.2004	WO 04/45002 A1	27.05.2004
			EP 1561240 A1	10.08.2005
			AU 3291370 AA	03.06-2004