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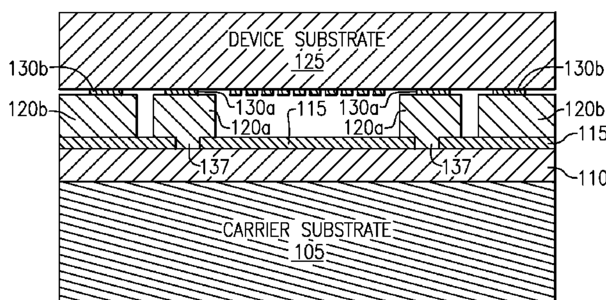

FIG.3F

(57) Abstract: According to various aspects and embodiments, a method for forming a packaged electronic device is provided. In accordance with one embodiment, the method comprises depositing a layer of temporary adhesive material on at least a portion of a surface of a first substrate having a coefficient of thermal expansion, depositing a layer of dielectric material on at least a portion of the layer of temporary adhesive material, forming at least one seal ring on at least a portion of the layer of dielectric material, providing a second substrate having a coefficient of thermal expansion that is substantially the same as the coefficient of thermal expansion of the first substrate, the second substrate having at least one bonding structure attached to a surface of the second substrate, and aligning the at least one seal ring to the at least one bonding structure and bonding the first substrate to the second substrate.

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DEVICE PACKAGING USING A RECYCLABLE CARRIER SUBSTRATE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of priority under 35 U.S.C. § 119(e) to co-pending
5 U.S. Provisional Application No. 62/293,987 filed on February 11, 2016, which is herein incorporated herein by reference in its entirety for all purposes.

BACKGROUND

FIELD OF INVENTION

10 The present disclosure relates generally to the field of semiconductor wafer processing technology. In particular, aspects and embodiments of the present invention relate to a recyclable carrier substrate that can be used in packages for electronic devices, such as semiconductor devices.

15 ### DISCUSSION OF RELATED ART

Many types of electronic devices incorporate the use of thin and/or fragile materials, or are designed to have features that themselves are fragile and susceptible to damage during processing. For example, some forms of MEMS devices or acoustic wave devices, such as surface acoustic wafer (SAW) filters or bulk acoustic wave (BAW) filters, are formed on
20 piezoelectric substrates, such as lithium tantalate ($LiTaO_3$). These substrates are fragile, making them difficult to handle during wafer processing.

SUMMARY

According to one aspect of the present invention, a method of forming a packaged
25 electronic device is provided. In one embodiment, the method comprises depositing a layer of temporary adhesive material on at least a portion of a surface of a first substrate having a coefficient of thermal expansion, depositing a layer of dielectric material on at least a portion of the layer of temporary adhesive material, forming at least one seal ring on at least a portion of the layer of dielectric material, providing a second substrate having a coefficient of thermal
30 expansion that is substantially the same as the coefficient of thermal expansion of the first

substrate, the second substrate having at least one bonding structure attached to a surface of the second substrate, and aligning the at least one seal ring to the at least one bonding structure and bonding the first substrate to the second substrate.

In some embodiments, the method further comprises thinning the second substrate.
5 According to a further embodiment, the second substrate has a thickness in a range of about 150 to 200 microns.

In some embodiments, the method further comprises removing the first substrate from the second substrate by removing the layer of temporary adhesive material. According to another embodiment, the method further comprises forming at least one via opening in the layer of
10 dielectric material before forming the at least one seal ring. According to another embodiment, the method further comprises depositing a layer of polymer material on at least a portion of the layer of dielectric material. According to another embodiment, the method further comprises forming at least one via opening in the layer of polymer material. According to another embodiment, the method further comprises forming at least one conductive pad, including
15 portions disposed in the at least one via opening of the layer of polymer material. According to another embodiment, the method further comprises depositing solder material onto the at least one conductive pad and reflowing the solder material. According to another embodiment, the method further comprises depositing a metal seed layer including portions disposed in the at least one via opening of the layer of polymer material. According to some embodiments, the method
20 further comprises mounting the packaged electronic device in electronic device modules. In some embodiments, the method further comprises mounting the electronic device modules in electronic devices.

In some embodiments, the method further comprises reusing the first substrate for forming multiple packaged electronic devices.

25 In accordance with another aspect of the present invention, a recyclable carrier substrate for use in forming a packaged electronic device is provided. According to at least one embodiment, the recyclable carrier substrate comprises a substrate having a coefficient of thermal expansion that is substantially the same as a coefficient of thermal expansion of a substrate of the electronic device used in forming the packaged electronic device, a layer of
30 temporary adhesive material disposed on at least a portion of a surface of the substrate, a layer of

dielectric material disposed on at least a portion of the layer of temporary adhesive material, and at least one seal ring formed on at least a portion of the layer of dielectric material.

In some embodiments, the at least one seal ring is further formed on at least a portion of the temporary adhesive material. According to some embodiments, the at least one seal ring is formed on portions of the temporary adhesive material through one or more openings formed in the layer of dielectric material.

In some embodiments, the at least one seal ring comprises an inner seal ring and an outer seal ring. According to some embodiments, the inner seal ring includes a binary alloy of two metal materials having a first ratio, and the outer seal ring includes the binary alloy of two metal materials having a second ratio that is different than the first ratio.

In accordance with another aspect of the invention, a packaged electronic device is provided. According to at least one embodiment, the packaged electronic device comprises a substrate, at least one bonding structure disposed on a surface of the substrate, at least one seal ring formed on the at least one bonding structure, a layer of dielectric material disposed on at least a portion of the at least one seal ring, a layer of polymer material disposed on at least a portion of the dielectric layer and at least a portion of the at least one seal ring, at least one conductive via formed on at least a portion of the polymer material and extending through openings formed in the polymer material and the layer of dielectric material to the at least one seal ring, and at least one electronic device disposed on the substrate and within a cavity that is at least partially defined by the at least one seal ring.

In some embodiments, the thickness of the packaged electronic device is less than 250 microns.

In some embodiments, the substrate is sapphire, lithium tantalite, lithium niobate, zirconium dioxide, zinc oxide, or quartz.

In some embodiments, the cavity is further defined by a portion of the layer of dielectric material and the surface of the substrate.

In some embodiments, the packaged electronic device further comprises interdigital (IDT) electrodes of an acoustic wave filter disposed on a surface of the substrate within the cavity. According to some embodiments, the packaged electronic device is included in an electronic device module. According to another embodiment, the packaged electronic device is

included in an RF device. According to another embodiment, the electronic device module is a radio frequency (RF) device module. According to another embodiment, the electronic device module is included in a duplexer.

In accordance with another aspect of the invention, a method for using a recyclable carrier substrate is provided. According to at least one embodiment, the method comprises depositing a layer of temporary adhesive material on at least a portion of a surface of a recyclable carrier substrate having a first coefficient of thermal expansion, depositing a layer of dielectric material on at least a portion of the layer of temporary adhesive material, forming at least one seal ring on at least a portion of the layer of dielectric material, aligning and bonding the at least seal ring to at least one bonding structure attached to a surface of a first device substrate having a second coefficient of thermal expansion that is substantially the same as the first coefficient of thermal expansion of the recyclable carrier substrate, and removing the recyclable carrier substrate by removing the layer of temporary adhesive material.

In some embodiments, the method further comprises repeating the depositing of the layer of temporary adhesive material, the depositing of the layer of dielectric material, and the forming of the at least one seal ring using the removed recyclable carrier substrate, and aligning and bonding the at least one seal ring to at least one bonding structure attached to a surface of a second device substrate having a third coefficient of thermal expansion that is substantially the same as the first coefficient of thermal expansion of the removed recyclable carrier substrate. In some embodiments, the method further comprises thinning the first device substrate prior to removing the recyclable carrier substrate.

Still other aspects, embodiments, and advantages of these example aspects and embodiments, are discussed in detail below. Moreover, it is to be understood that both the foregoing information and the following detailed description are merely illustrative examples of various aspects and embodiments, and are intended to provide an overview or framework for understanding the nature and character of the claimed aspects and embodiments. Embodiments disclosed herein may be combined with other embodiments, and references to “an embodiment,” “an example,” “some embodiments,” “some examples,” “an alternate embodiment,” “various embodiments,” “one embodiment,” “at least one embodiment,” “this and other embodiments,” “certain embodiments,” or the like are not necessarily mutually exclusive and are intended to

indicate that a particular feature, structure, or characteristic described may be included in at least one embodiment. The appearances of such terms herein are not necessarily all referring to the same embodiment.

BRIEF DESCRIPTION OF DRAWINGS

Various aspects of at least one embodiment are discussed below with reference to the accompanying figures, which are not intended to be drawn to scale. The figures are included to provide an illustration and a further understanding of the various aspects and embodiments, and are incorporated in and constitute a part of this specification, but are not intended as a definition of the limits of any particular embodiment. The drawings, together with the remainder of the specification, serve to explain principles and operations of the described and claimed aspects and embodiments. In the figures, each identical or nearly identical component that is illustrated in various figures is represented by a like numeral. For purposes of clarity, not every component may be labeled in every figure. In the figures:

FIG. 1A is a cross-sectional side view of a first example of a packaged electronic device;

FIG. 1B is a cross-sectional side view of a second example of a packaged electronic device;

FIG. 2A is a flow chart illustrating an embodiment of a method of forming at least a portion of the electronic devices of FIGS. 1A and 1B;

FIG. 2B is a flow chart illustrating alternative embodiments of the method of FIG. 2A;

FIG. 3A illustrates an act in the method of FIG. 2A;

FIG. 3B illustrates an act in the method of FIG. 2A;

FIG. 3C illustrates an act in the method of FIG. 2A;

FIG. 3D illustrates an act in the method of FIG. 2A;

FIG. 3E illustrates an act in the method of FIG. 2A;

FIG. 3F illustrates an act in the method of FIG. 2A;

FIG. 3G illustrates an act in the method of FIG. 2A;

FIG. 3H illustrates an act in the method of FIG. 2A;

FIG. 3I illustrates an act in the method of FIG. 2A;

FIG. 3J illustrates an act in the method of FIG. 2A;

FIG. 3K illustrates an act in the method of FIG. 2A;

FIG. 3L illustrates an act in the method of FIG. 2A;

FIG. 3M illustrates an act in the method of FIG. 2A;

FIG. 3N illustrates an act in the method of FIG. 2A;

5 FIG. 4 is a block diagram of one example of an antenna duplexer incorporating a packaged electronic device according to aspects of the present invention;

FIG. 5 is a block diagram of one example of a module incorporating a packaged electronic device according to aspects of the present invention; and

FIG. 6 is a block diagram of one example of a communications device incorporating the
10 antenna duplexer of FIG. 4, according to aspects of the present invention.

DETAILED DESCRIPTION

Aspects and embodiments are directed to a method of forming a packaged electronic device using a recyclable carrier substrate. The processes and devices disclosed herein are
15 capable of providing a low cost structure, while still maintaining functional, mechanical, and hermetic requirements. According to various aspects, the carrier substrate, otherwise referred to herein as a carrier wafer, has substantially the same coefficient of thermal expansion (CTE) as the device substrate, otherwise referred to herein as a device wafer. This minimizes wafer bow, stress, and cracks that can occur during certain manufacturing processes, such as during wafer
20 bonding processes. The carrier substrate is also reusable and therefore offers cost savings.

At least one embodiment is directed to a recyclable carrier substrate that may be used in a surface acoustic wafer (SAW) filter package manufacturing process. The carrier substrate may provide mechanical support to the fragile SAW filter substrate, during certain manufacturing steps, such as during processes in which the SAW filter substrate is thinned. According to some
25 embodiments, this allows the total thickness of the finished SAW filter package to be less than 250 microns.

The aspects disclosed herein in accordance with the present invention are not limited in their application to the details of construction and the arrangement of components set forth in the following description or illustrated in the accompanying drawings. These aspects are capable of
30 assuming other embodiments and of being practiced or of being carried out in various ways.

Examples of specific implementations are provided herein for illustrative purposes only and are not intended to be limiting. In particular, acts, components, elements, and features discussed in connection with any one or more embodiments are not intended to be excluded from a similar role in any other embodiments.

5 Also, the phraseology and terminology used herein is for the purpose of description and should not be regarded as limiting. Any references to examples, embodiments, components, elements or acts of the systems and methods herein referred to in the singular may also embrace embodiments including a plurality, and any references in plural to any embodiment, component, element or act herein may also embrace embodiments including only a singularity. References 10 in the singular or plural form are not intended to limit the presently disclosed systems or methods, their components, acts, or elements. The use herein of "including," "comprising," "having," "containing," "involving," and variations thereof is meant to encompass the items listed thereafter and equivalents thereof as well as additional items. References to "or" may be construed as inclusive so that any terms described using "or" may indicate any of a single, more 15 than one, and all of the described terms.

In accordance with various aspects, FIG. 1A illustrates a first example of a packaged electronic device, indicated generally at 100a. As used herein, the terms "electronic device" and "device" are used interchangeably and are to be understood to encompass semiconductor die, MEMS devices, and other electrical components that may be used according to one or more 20 embodiments of the present invention. In certain instances, the electronic device may include or be part of a larger system, as discussed further below. Non-limiting examples of electronic devices include MEMS or acoustic wave devices, such as surface acoustic wafer (SAW) filters or bulk acoustic wave (BAW) filters, or other similar acoustic wave components. The electronic device includes a device substrate 125, and according to various embodiments, the device 25 substrate 125 may be a material suitable for piezoelectric devices that are used as electronic components in cellular phones, such as SAW filters. Non-limiting examples of materials suitable for forming the device substrate 125 include piezoelectric single crystal materials, such as sapphire, lithium tantalite ($LiTaO_3$), lithium niobate ($LiNbO_3$), zirconium dioxide (ZrO_2), zinc oxide (ZiO), and quartz. It is to be appreciated that although the embodiments discussed herein 30 reference a SAW filter device, aspects of the present invention may be applied to other types of

electronic devices, including other types of acoustic wave devices. Interdigital transducer (IDT) electrodes 155 of a SAW filter may be provided on the device substrate 125 within a cavity 160 defined in the package 100a. As shown in FIG. 1A, the packaged SAW filter 100a may also include one or more bonding structures 130a and 130b, also referred to herein as electrodes, that
5 are each attached to a respective seal ring 120a and 120b (discussed in further detail below) formed from sealing material, which in certain instances surrounds the cavity 160 to provide a hermetic seal. For example, in some embodiments the seal rings 120a and 120b (and thus the bonding structures 130a, 130b) fully circumscribe the cavity 160 and may be circular, square, rectangular, or any other desired shape suitable to hermetically seal the cavity 160. A layer of
10 dielectric material 115 and a layer of polymer material 135 are further provided to seal the cavity 160. Metal contacts are also provided, which in this particular example includes a metal seed layer 150 comprising copper plating material.

FIG. 1B illustrates a second example of a packaged electronic device, generally indicated at 100b. The packaged electronic device 100b may be a SAW filter, and as shown in FIG. 1B is
15 similar in structure to the packaged SAW filter 100a of FIG. 1A, but features an alternative packaging option. According to this embodiment, the packaged SAW filter 100b includes contacts formed from pad material 140 (also referred to herein as a “conductive pad”) and solder material 145 instead of the copper material 150 shown in FIG. 1A.

According to certain aspects and embodiments, FIG. 2A illustrates a flow diagram of one
20 example of a method 200 of forming at least a portion of the packaged electronic devices of FIGS. 1A and 1B. Process 200 will be described with reference to FIGS. 3A-3N. Although the discussion below references single devices formed in a single package, it is to be understood that the method may be applied to forming multiple devices on a common substrate or wafer. For example, step 260 includes singulation, where the substrate may be diced to individually separate
25 the packaged electronic devices from one another.

A first step 202 includes providing a carrier substrate 105 (see FIG. 3A). According to at least one embodiment, the carrier substrate 105 has a coefficient of thermal expansion (CTE) that is substantially the same as that of the corresponding substrate of the device that is to be packaged. As used herein, the expression “substantially the same” when used in reference to the
30 CTE of the carrier substrate and the corresponding device substrate means that the difference

between the two CTE values is sufficiently small such that the device substrate and the carrier substrate expand and contract approximately the same amount when subjected to changes in temperature. According to various aspects, the carrier substrate is selected so as to achieve the lowest CTE mismatch possible. For example, sapphire (CTE of 6.95 ppm/°C) may be paired with Al_2O_3 (CTE of 8 ppm/°C), or with GaAs (CTE of 6.86 ppm/°C), whereas pairing $LiTaO_3$ (CTE of 14 ppm/°C) with either Si (2.6 ppm/°C) or GaAs creates too large of a CTE mismatch. In accordance with certain aspects, having the CTE values be substantially the same allows the carrier substrate 105 and the device substrate 125 to expand and contract by approximately the same amount during one or more processing steps.

In certain instances, the carrier substrate 105 may be made from the same material as the substrate of the corresponding device. According to one embodiment, the carrier substrate 105 may be made of a piezoelectric single crystal such as, for example, sapphire, lithium tantalite, lithium niobate, quartz crystal, and the like. Other non-limiting examples of suitable carrier substrate 105 materials include zirconium dioxide (ZrO_2), zinc oxide (ZiO), and Al_2O_3. According to some embodiments, the device substrate 125 may be formed from gallium (Ga) based materials, such as gallium arsenide (GaAs). Further, in accordance with various aspects, the thickness of the carrier substrate 105 may be chosen such that the material forming the carrier substrate 105 doesn’t experience mechanical failure, i.e., crack or break, during one or more processing steps. According to a further aspect, the thickness of the carrier substrate 105 may be chosen such that it provides additional mechanical support to the device substrate 125 during one or more processing steps. For instance, the device substrate 125 may bow in one direction during a processing step, and the carrier substrate 105 may bow in the same manner and thereby function to counteract or otherwise compliment the bowing of the device substrate 125. Listed below in Table 1 are CTE values for different types of materials used in semiconductor manufacturing. As stated above, according to some embodiments, the carrier substrate 105 may be made from the same material as the corresponding device substrate, but in alternative embodiments, the carrier substrate 105 may be made from a different material than the corresponding device substrate 125. For example, in certain instances the carrier substrate 105 may be sapphire, while the device substrate 125 may be gallium arsenide GaAs. Other suitable

examples or materials that may be paired together include sapphire and Al_2O_3, Pyrex and Si_3N_4, Si and GaN, and AlN and SiC.

Table 1: Thermal Expansion Coefficients at 20 °C

Material	CTE (ppm/°C)	Material	CTE (ppm/°C)
Polymers	55-200	Al_2O_3	8
Epoxy	55	Sapphire	6.95
E-glass	54	GaAs	6.86
Benzocyclobutene (BCB)	42	AlAs	4.9
Sn-Pb solder	27	InP	4.75
Copper	16.7	AlN	4.6
$LiNbO_3$	15.4	SiC	4.5
Au-Sn solder	14.7	Pyrex	3.2
$LiTaO_3$	14	Si_3N_4	3.2
Gold	14	GaN	2.8
ZrO_2	10	Si	2.6

5

In step 205, and as illustrated in FIG. 3B, a layer of temporary adhesive material 110 may be deposited on at least a portion of a surface of the carrier substrate 105. According to some embodiments, the temporary adhesive material 110 is an adhesive material such as WaferBOND® HT-10.10 temporary bonding material available from Brewer Science, Inc.,
10 Rolla, MO or any other temporary wafer bonding material known in the art. According to various aspects, the layer of temporary adhesive material may have a thickness, for example, of between about 5 microns and about 20 microns. According to some embodiments, the layer of temporary adhesive material 110 may be deposited using a spin coating process, although other deposition techniques are also within the scope of this disclosure, such as screen printing. In
15 some embodiments, the adhesive material 110 is a high temperature temporary bonding material, meaning that it can withstand processing steps that stay below a certain target temperature. For

instance, according to some embodiments, the temporary adhesive material 110 may be used in process steps that do not exceed 220 °C.

In step 210, and as illustrated in FIG. 3C, a layer of dielectric material 115 may be deposited on at least a portion of the layer of temporary adhesive material 110. Non-limiting examples of dielectric material 115 include insulation materials such as silicon oxide (SiO_x), silicon nitride (Si_3N_4), and the like. According to some embodiments, the layer of dielectric material 115 may be deposited using a low temperature processing method, such as a spin coating or physical vapor deposition (PVD) processes. For example, according to one embodiment, the layer of dielectric material 115 is deposited using a deposition method conducted at temperatures that are below about 300 °C.

In step 215, a via opening 137 may be formed in the layer of dielectric material 115 (FIG. 3D). As discussed in further detail below, the via opening 137 may be used to allow for electric current to pass through to the electronic devices disposed on the device substrate 125, as shown in FIGS. 1A and 1B. Via opening 137 formed in the layer of dielectric material 115 may be formed using an etch process, such as a wet etch technique or a dry etch technique.

As shown in FIGS. 3E-3N, an inner seal ring 120a and an outer seal ring 120b are each formed from a layer of sealing material that is deposited on at least a portion of the layer of dielectric material 115 in step 220 (FIG. 3E). In accordance with various aspects, the inner and outer seal rings 120a and 120b function to hermetically seal the cavity 160 disposed within the cavity of the packaged electronic device. According to a further aspect, the inner seal ring 120a may form the “walls” of the cavity 160, as shown in FIGS. 1A and 1B. According to the embodiment shown in FIGS. 3E-3N, the outer seal ring120b circumscribes both the cavity and the inner seal ring 120a (i.e., thereby providing a “nesting” effect) to protect the electronic devices disposed in the cavity (such as the IDT electrodes shown in FIGS. 1A and 1B) from external environmental effects by providing a hermetic seal. The inner seal ring 120a may thus circumscribe the cavity and provide the electrical contact to the electronic devices disposed in the cavity as well as provide a hermetic seal. Thus, according to some embodiments the inner seal ring 120a may also be deposited on at least a portion of the temporary adhesive material 110 through the via opening 137 etched in the layer of dielectric material 115, as shown in FIG. 3E. It is to be appreciated that although FIGS. 3E-3N illustrate two separate seal ring structures 120a

and 120b, other configurations using multiple seal rings are also within the scope of this disclosure, such as three or four seal ring structures.

According to some embodiments, one or both of the inner and outer seal rings 120a and 120b may comprise gold. In accordance with some embodiments, the inner and outer seal rings 120a and 120b may comprise multiple materials and/or multiple layers of materials. For example, seal rings 120a and 120b may comprise a layer of gold and a layer of indium (In). In accordance with at least one embodiment, the inner and outer seal rings 120a and 120b may each comprise a transient liquid phase (TLP) bonding structure such as those described in commonly owned co-pending U.S. Provisional Application Serial No. 62/264,422 titled "IMPROVED SEAL RING," filed December 9, 2015, which is incorporated herein by reference in its entirety. For example, two metals having different melting points that are also capable of forming a binary alloy, such as such as gold and indium, may each be deposited in different ratios, such that the ratio of gold to indium in the inner seal ring 120a may be different than the ratio of gold to indium in the outer seal ring 120b. According to other embodiments, the inner seal ring 120a is gold, and the outer seal ring 120b comprises gold and indium. The sealing material(s) used to form inner and outer seal rings 120a and 120b may be deposited using any one or more techniques, such as e-beam evaporation or plating methods. According to some embodiments, the inner and outer seal rings 120a and 120b may have a thickness, for example, between about 5 microns and about 20 microns.

In step 225, and as illustrated in FIG. 3F, the device substrate 125 is attached to the carrier substrate 105. According to various aspects, bonding structures 130a and 130b, disposed on the device substrate 125 are aligned and attached to the corresponding seal rings 120a and 120b disposed on the carrier substrate 105. In some embodiments, the bonding structures 130a and 130b comprise metal material. For instance, the bonding structures 130a and 130b may comprise gold (Au) and/or indium (In), and/or a composite eutectic mixture of other suitable metals. In some embodiments, the device substrate is attached to the carrier substrate using an AuIn eutectic bonding technique performed at low process temperatures (e.g., ~190 °C). For example, indium may be evaporated onto gold contacts (thereby forming the bonding structures 130a and 130b) using an e-beam evaporation device. The structures forming seal rings 120a and 120b may each comprise gold and indium (in different ratios) that are aligned with the

corresponding bonding structures (such that 130a aligns with 120a and 130b aligns with 120b) and subjected to a heat treatment, thereby forming a eutectic bond. Thus, according to certain aspects, the low melting point of indium allows for a low temperature eutectic bonding process for joining the device substrate and the carrier substrate and forming a hermetic seal.

5 In step 230, the carrier substrate 105 may be removed from the device substrate 125 by removing the temporary adhesive material 110, as illustrated in FIG. 3G. For example, the temporary adhesive material 110 may be thermally decomposed or dissolved in a solvent to allow for the carrier substrate 105 to be removed and for the packages 100a and 100b shown in FIGS. 1A and 1B to be further processed and/or completed. Once removed, the carrier substrate 10 105 may be reused in another packaging process, as indicated at 231 in FIG. 2A. In certain instances, the carrier substrate 105 may undergo further processing, such as cleaning etc., before being used again in a separate packaging process. According to some embodiments, the carrier substrate 105 may be reused multiple times for forming multiple packaged devices.

Once the layer of temporary adhesive material 110 has been removed, a layer of polymer 15 material 135 may be deposited on at least a portion of the layer of dielectric material 115 in step 235 (FIG. 3H). According to various aspects, the layer of polymer material 135 may also be disposed on at least a portion of the seal rings 120a and 120b, such as the inner seal ring120a, through the via 137 formed in the layer of dielectric material in step 215, as shown in FIG. 3H. Step 235 may also include curing the layer of polymer material 135 through a heating process. 20 In accordance with at least one embodiment, the layer of polymer material 135 may provide mechanical stability for the packaged device. The polymer material 135 may comprise one or more polymers, non-limiting examples of which include epoxy materials, including photoresist materials such as SU-8, polyimide, and other organic materials, such as benzocyclobutene (BCB), etc. The layer of polymer material 135 may be deposited using any one of a number of 25 different processes, such as spin coating and chemical vapor deposition (CVD) techniques.

In step 240, and as shown in FIG. 3I, a via opening 142 may be formed in the layer of polymer material 135 using wet etch or dry etch processes. According to various aspects, conductive material and/or conductive structures may be formed within via opening 142 to allow for electrical current to pass through to the electronic devices disposed on the device substrate 30 125. For example, via opening 142 formed in the layer of polymer material 135 may also align

with the via opening 137 formed in the layer of dielectric material 115, so that conductive material can be deposited into the opening for the purposes of forming an electric contact with the inner seal ring 120a (and the electronic devices disposed on the device substrate).

Steps 242, 244, and 246 of FIG. 2A are associated with FIGS. 3J-3L, and represent one option for packaging an electronic device in accordance with one embodiment. For example, in step 242 (FIG. 3J) a pad 140 formed from conductive material may be formed within via opening 142 of the polymer material 135, and as shown in FIG. 3J, may also be formed on at least a portion of an outer surface of the polymer material 135. The material forming the pad 140 may extend through the entire depth of the polymer material 135, and also contact at least a portion of the outer surface of the dielectric material 115 and an outer surface of the portion of the inner seal ring 120a surrounding the cavity 160. According to various aspects, the pad 140 may be a bond pad, as readily understood by those of skill in the art. The pad 140 may be formed using typical lithography techniques, for example by depositing a layer of metal, such as copper, onto the polymer layer 135 and then coating the metal with a thick layer of photoresist, which is then exposed and developed to protect the areas that form the final pad structure. An etch process, such as a wet etch process, may then remove the metal outside the desired areas that form the pad 140. Once the pad 140 has been formed, solder material 145 may be deposited in step 244 (FIG. 3K) onto the surface of the pad, and in step 246 solder reflow is performed to melt the solder bumps (FIG. 3L).

Steps 243 and 245 of FIG. 2A are associated with FIGS. 3M and 3N and represent another option for packaging the electronic device in accordance with another embodiment. For example, in step 243, a metal seed layer 150 is deposited on at least a portion of the outer surface of the layer of polymer material 135 and within the via opening 142 formed within the polymer material 135 (FIG. 3M). As shown in FIG. 3M, the metal seed layer 150 may also be formed on at least a portion of the outer surface of both the dielectric layer 115 and the inner seal ring 120a. The metal seed layer 150 may be deposited using PVD methods, such as sputtering or evaporative techniques. According to at least one embodiment, the metal seed layer 150 may comprise copper (Cu) or gold (Au), which are deposited as a seed layer using a sputter technique. According to some embodiments, a barrier layer of titanium tungsten (TiW), nickel vanadium (NiV), or titanium (Ti) may be used to protect diffusion of the metal seed layer 150 into one or

more underlying layers. For instance, a layer of TiW may be deposited on the polymer layer 135 and within via opening 142 prior to depositing the metal seed layer 150. In step 245, portions of the metal seed layer 150 are removed (FIG. 3N) to form bond pads that allow for electrical contact between elements of the package, (e.g., electrodes) and the outside of the package. The
5 metal seed layer 150 may be removed using an etch method, such as a wet etch processing technique using peroxide, potassium iodide (KI), or acid based solutions, as recognized by those skilled in the art.

Referring back to FIG. 3L, a conductive via or path is thus formed between the reflowed solder material 145 through the conductive pad 140 and through vias 142 and 137 formed in the
10 polymer material 135 and dielectric material 115 respectively, to the inner seal ring 120a and finally to the bonding structure 130a disposed on the device substrate 125. Likewise, referring to FIG. 3N, a similar conductive via or path is formed between the metal seed layer 150 through the inner seal ring 120a to the bonding structure 130a. This allows for electrical contact between elements of the package, such as IDT electrodes 155 of FIGS. 1A and 1B, and the outside of the
15 package.

In step 260, the packaged devices are mounted to an adhesive-coated tape and singulated using a die cutting process. For example, an outer portion of the device substrate 125 (opposite the cavity 160 where no components are fabricated) may be attached to the adhesive-coated tape and cut to the size of the individual packages.

20 FIG. 2B is a flow chart illustrating alternative embodiments of the method described previously in FIG. 2A. For example, according to one embodiment, after the device substrate 125 is attached to the carrier substrate 105 in act 225, the device substrate 125 may be thinned (step 227). For example, a SAW filter device substrate can be thinned from a starting thickness of greater than 250 microns to a thickness in a range of about 150 to about 200 microns. Having
25 the carrier substrate attached to the device structure improves the mechanical stability of the device substrate, which can be very fragile and susceptible to damage during the thinning process. In certain instances, this allows the entire thickness of the finished packaged device to be less than 250 microns. In accordance with one embodiment, the device substrate may be thinned after attaching it to the carrier substrate (step 227), after which the carrier substrate 105
30 may be removed (step 230) as discussed above. According to other embodiments, the carrier

substrate is first removed (step 230) and the device substrate may be further processed (step 231). For example, the device substrate may undergo additional thermal processing while the carrier substrate is removed. The carrier substrate may be re-attached (step 232) and the device substrate may be thinned (step 233). According to some embodiments, a different carrier
5 substrate material may be used in the re-attachment process at step 232 than was used in steps 205-220. For example, a GaAs carrier substrate may be used for steps 205-230, and then a sapphire carrier substrate may be attached at step 232 and used during the device substrate thinning process of step 233. Similar examples using other materials are also within the scope of this disclosure.

10 The processes depicted in FIGS. 2A and 2B include examples of particular sequences of acts according to particular embodiments. The acts included in these processes may be performed by, or using, one or more semiconductor manufacturing devices as will be understood by those skilled in the art. Some acts may be optional and, as such, may be omitted in accord with one or more embodiments. Additionally, the order of acts can be altered, or other acts can
15 be added, without departing from the scope of the embodiments described herein.

In accordance with one or more embodiments, the packaged electronic device illustrated in FIGS. 1A and 1B may be an acoustic wave device, such as a SAW filter. It will be appreciated by those skilled in the art, given the benefit of this disclosure, that components or devices, such as an acoustic wave filter, an antenna duplexer, a module, or a communications
20 device, for example, may be configured to use embodiments of the packaging process according to this disclosure, and that such components or devices may have enhanced or improved features through the benefits provided by the packaging process.

According to one embodiment, a packaged electronic device including an acoustic wave device may be used to provide an antenna duplexer having improved characteristics. FIG. 4
25 illustrates a block diagram of one example of an antenna duplexer which can incorporate embodiments of the packaged electronic device disclosed herein. The antenna duplexer 300 includes a transmission filter 302 and a reception filter 304 that are connected to a shared antenna terminal 306. The transmission filter 302 includes a transmit terminal 303 for connecting the transmission filter to transmitter circuitry (not shown), and the reception filter
30 includes a reception terminal 305 for connecting the reception filter to receiver circuitry (not

shown). Either or both of the transmission filter 302 and the reception filter 304 can include one or more of the packaged electronic devices, such as the acoustic wave devices as disclosed herein. By configuring the antenna duplexer 300 to use the packaged acoustic wave devices, an antenna duplexer having improved characteristics and enhanced performance (resulting from the improved characteristics of the packaged acoustic wave devices discussed above such as the reduced thickness of the package) can be realized.

Further, embodiments of the packaged acoustic wave devices may be incorporated, optionally as part of the antenna duplexer 300, into a module that may ultimately be used in a device, such as a wireless communications device, for example, so as to provide a module having enhanced performance. FIG. 5 is a block diagram illustrating one example of a module 400 including an embodiment of a packaged acoustic wave device 100. The module 400 further includes connectivity 402 to provide signal interconnections, packaging 404, such as for example, a package substrate, for packaging of the circuitry, and other circuitry die 406, such as, for example amplifiers, pre-filters, modulators, demodulators, down converters, and the like, as would be known to one of skill in the art of semiconductor fabrication in view of the disclosure herein. In certain embodiments, the packaged acoustic wave device 100 in module 400 may be replaced with the antenna duplexer 300, so as to provide an RF module, for example.

Furthermore, configuring an acoustic wave filter and/or antenna duplexer to use embodiments of the packaged acoustic wave device can achieve the effect of realizing a communication device having enhanced performance using the same. FIG. 6 is a schematic block diagram of one example of a communication device 500 (e.g., a wireless or mobile device) that can include the antenna duplexer 300 incorporating one or more packaged acoustic wave devices, as discussed above. The communication device 500 can represent a multi-band and/or multi-mode device such as a multi-band/multi-mode mobile phone, for example. In certain embodiments, the communication device 500 can include the antenna duplexer 300, a transmission circuit 502 connected to the antenna duplexer via the transmit terminal 303, a reception or receive circuit 504 connected to the antenna duplexer 300 via the reception terminal 305, and an antenna 506 connected to the antenna duplexer via the antenna terminal 306. The transmission circuit 502 and reception circuit 504 may be part of a transceiver that can generate RF signals for transmission via the antenna 506 and can receive incoming RF signals from the

antenna 506. The communication device 500 can further include a controller 508, a computer readable medium 510, a processor 512, and a battery 514.

It will be understood that various functionalities associated with the transmission and receiving of RF signals can be achieved by one or more components that are represented in FIG. 6 as the transmission circuit 502 and the reception circuit 504. For example, a single component can be configured to provide both transmitting and receiving functionalities. In another example, transmitting and receiving functionalities can be provided by separate components.

Similarly, it will be understood that various antenna functionalities associated with the transmission and receiving of RF signals can be achieved by one or more components that are collectively represented in FIG. 6 as the antenna 506. For example, a single antenna can be configured to provide both transmitting and receiving functionalities. In another example, transmitting and receiving functionalities can be provided by separate antennas. In yet another example in which the communication device is a multi-band device, different bands associated with the communication device 500 can be provided with different antennas.

To facilitate switching between receive and transmit paths, the antenna duplexer 300 can be configured to electrically connect the antenna 506 to a selected transmit or receive path. Thus, the antenna duplexer 300 can provide a number of switching functionalities associated with an operation of the communication device 500. In addition, as discussed above, the antenna duplexer 300 may include the transmission filter 302 and reception filter 304, which are configured to provide filtering of the RF signals. As discussed above, either or both of the transmission filter 302 and reception filter 304 can include embodiments of the packaged acoustic wave device, and thereby provide enhanced features and/or performance through the benefits of the ability to downsize and improved connection reliability achieved using embodiments of the packaged acoustic wave device. In certain examples, the antenna duplexer 300 in the communication device 500 can be replaced with a module 400, which includes the antenna duplexer, as discussed above.

As shown in FIG. 6, in certain embodiments, a controller 508 can be provided for controlling various functionalities associated with operations of the antenna duplexer 300 and/or other operating component(s). In certain embodiments, a processor 512 can be configured to facilitate implementation of various processes for operation of the communication device 500.

The processes performed by the processor 512 may be implemented by computer program instructions. These computer program instructions may be provided to a processor of a general purpose computer, special purpose computer, or other programmable data processing apparatus to produce a machine, such that the instructions, which execute via the processor of the computer
5 or other programmable data processing apparatus, create a mechanism for operating the communication device 500. In certain embodiments, these computer program instructions may also be stored in the computer-readable medium 510. The battery 514 can be any suitable battery for use in the communication device 500, including, for example, a lithium-ion battery.

Unless the context clearly requires otherwise, throughout the description and the claims,
10 the words “comprise,” “comprising,” and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of “including, but not limited to.” The word “coupled,” as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words “herein,” “above,” “below,” and words of similar import, when used in
15 this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word “or” in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any
20 combination of the items in the list.

The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled
25 in the relevant art will recognize. For example, while acts of the disclosed processes are presented in a given order, alternative embodiments may perform routines having acts performed in a different order, and some processes or acts may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or acts may be implemented in a variety of different ways. Also, while processes or acts are at times shown as being performed in series,

these processes or acts may instead be performed in parallel, or may be performed at different times.

The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments
5 described above can be combined to provide further embodiments.

Having thus described several aspects of at least one embodiment of this invention, it is to be appreciated various alterations, modifications, and improvements will readily occur to those skilled in the art. Any feature described in any embodiment may be included in or substituted for any feature of any other embodiment. Such alterations, modifications, and
10 improvements are intended to be part of this disclosure, and are intended to be within the scope of the invention. Accordingly, the foregoing description and drawings are by way of example only.

What is claimed is:

CLAIMS

1. A method of forming a packaged electronic device comprising:

depositing a layer of temporary adhesive material on at least a portion of a surface of a
5 first substrate having a coefficient of thermal expansion;

depositing a layer of dielectric material on at least a portion of the layer of temporary adhesive material;

forming at least one seal ring on at least a portion of the layer of dielectric material;

providing a second substrate having a coefficient of thermal expansion that is
10 substantially the same as the coefficient of thermal expansion of the first substrate, the second substrate having at least one bonding structure attached to a surface of the second substrate; and

aligning the at least one seal ring to the at least one bonding structure and bonding the first substrate to the second substrate.

15 2. The method of claim 1 further comprising thinning the second substrate.

3. The method of claim 2 wherein the second substrate has a thickness in a range of about 150 to 200 microns.

20 4. The method of claim 1 further comprising removing the first substrate from the second substrate by removing the layer of temporary adhesive material.

5. The method of claim 4 further comprising forming at least one via opening in the layer of dielectric material before forming the at least one seal ring.

25

6. The method of claim 4 further comprising reusing the first substrate for forming multiple packaged electronic devices.

7. The method of claim 4 further comprising depositing a layer of polymer material on at least a portion of the layer of dielectric material.

8. The method of claim 7 further comprising forming at least one via opening in the layer of
5 polymer material.

9. The method of claim 8 further comprising forming at least one conductive pad, including portions disposed in the at least one via opening of the layer of polymer material.

10 10. The method of claim 9 further comprising depositing solder material onto the at least one conductive pad and reflowing the solder material.

11. The method of claim 8 further comprising depositing a metal seed layer including portions disposed in the at least one via opening of the layer of polymer material.
15

12. The method of claim 8 further comprising mounting the packaged electronic device in electronic device modules.

13. The method of claim 12 further comprising mounting the electronic device modules in
20 electronic devices.

14. A recyclable carrier substrate for use in forming a packaged electronic device comprising:

a substrate having a coefficient of thermal expansion that is substantially the same as a
25 coefficient of thermal expansion of a substrate of the electronic device used in forming the packaged electronic device;

a layer of temporary adhesive material disposed on at least a portion of a surface of the substrate;

a layer of dielectric material disposed on at least a portion of the layer of temporary
30 adhesive material; and

at least one seal ring formed on at least a portion of the layer of dielectric material.

15. The recyclable carrier substrate of claim 14 wherein the at least one seal ring is further formed on at least a portion of the temporary adhesive material.

5

16. The recyclable carrier substrate of claim 15 wherein the at least one seal ring is formed on portions of the temporary adhesive material through one or more openings formed in the layer of dielectric material.

10 17. The recyclable carrier substrate of claim 14 wherein the at least one seal ring comprises an inner seal ring and an outer seal ring.

18. The recyclable carrier substrate of claim 17 wherein the inner seal ring includes a binary alloy of two metal materials having a first ratio, and the outer seal ring includes the binary alloy
15 of two metal materials having a second ratio that is different than the first ratio.

19. A packaged electronic device comprising:

a substrate;

at least one bonding structure disposed on a surface of the substrate;

20 at least one seal ring formed on the at least one bonding structure;

a layer of dielectric material disposed on at least a portion of the at least one seal ring;

a layer of polymer material disposed on at least a portion of the dielectric layer and at least a portion of the at least one seal ring;

at least one conductive via formed on at least a portion of the polymer material and
25 extending through openings formed in the polymer material and the layer of dielectric material to the at least one seal ring; and

at least one electronic device disposed on the substrate and within a cavity that is at least partially defined by the at least one seal ring.

20. The packaged electronic device of claim 19 wherein the thickness of the packaged electronic device is less than 250 microns.

21. The packaged electronic device of claim 20 wherein the substrate is sapphire, lithium
5 tantalite, lithium niobate, zirconium dioxide, zinc oxide, or quartz.

22. The packaged electronic device of claim 21 wherein the cavity is further defined by a portion of the layer of dielectric material and the surface of the substrate.

10 23. The packaged electronic device of claim 22 further comprising interdigital (IDT) electrodes of an acoustic wave filter disposed on a surface of the substrate within the cavity.

24. The packaged electronic device of claim 19 included in an electronic device module.

15 25. The packaged electronic device of claim 24 wherein the electronic device module is a radio frequency (RF) device module.

26. The packaged electronic device of claim 25 wherein the electronic device module is included in a duplexer.

20

27. The packaged electronic device of claim 25 included in an RF device.

28. A method for using a recyclable carrier substrate comprising:

depositing a layer of temporary adhesive material on at least a portion of a surface of a
25 recyclable carrier substrate having a first coefficient of thermal expansion;

depositing a layer of dielectric material on at least a portion of the layer of temporary adhesive material;

forming at least one seal ring on at least a portion of the layer of dielectric material;

aligning and bonding the at least one seal ring to at least one bonding structure attached
30 to a surface of a first device substrate having a second coefficient of thermal expansion that is

substantially the same as the first coefficient of thermal expansion of the recyclable carrier substrate; and

removing the recyclable carrier substrate by removing the layer of temporary adhesive material.

5

29. The method of claim 28 further comprising:

repeating the depositing of the layer of temporary adhesive material, the depositing of the layer of dielectric material, and the forming of the at least one seal ring using the removed recyclable carrier substrate; and

10 aligning and bonding the at least one seal ring to at least one bonding structure attached to a surface of a second device substrate having a third coefficient of thermal expansion that is substantially the same as the first coefficient of thermal expansion of the removed recyclable carrier substrate.

15 30. The method of claim 28 further comprising thinning the first device substrate prior to removing the recyclable carrier substrate.

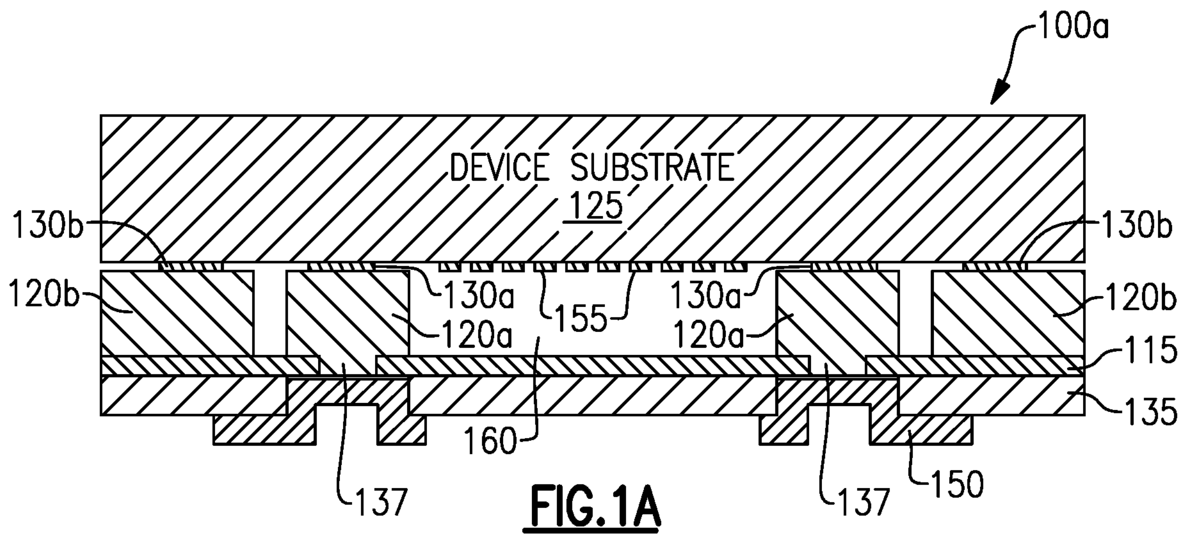

FIG.1A

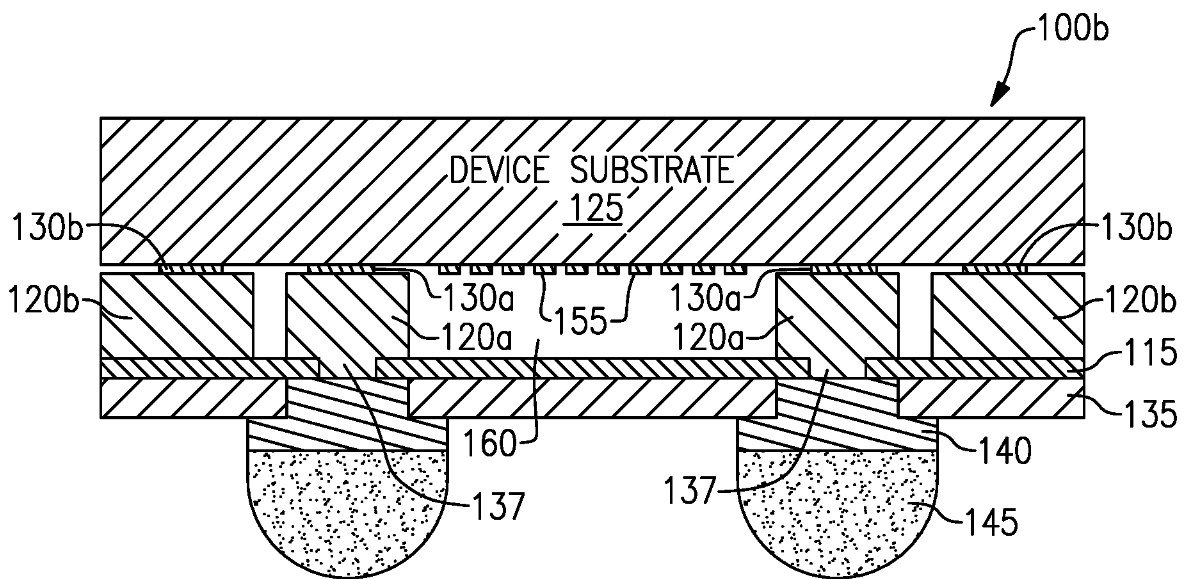

FIG.1B

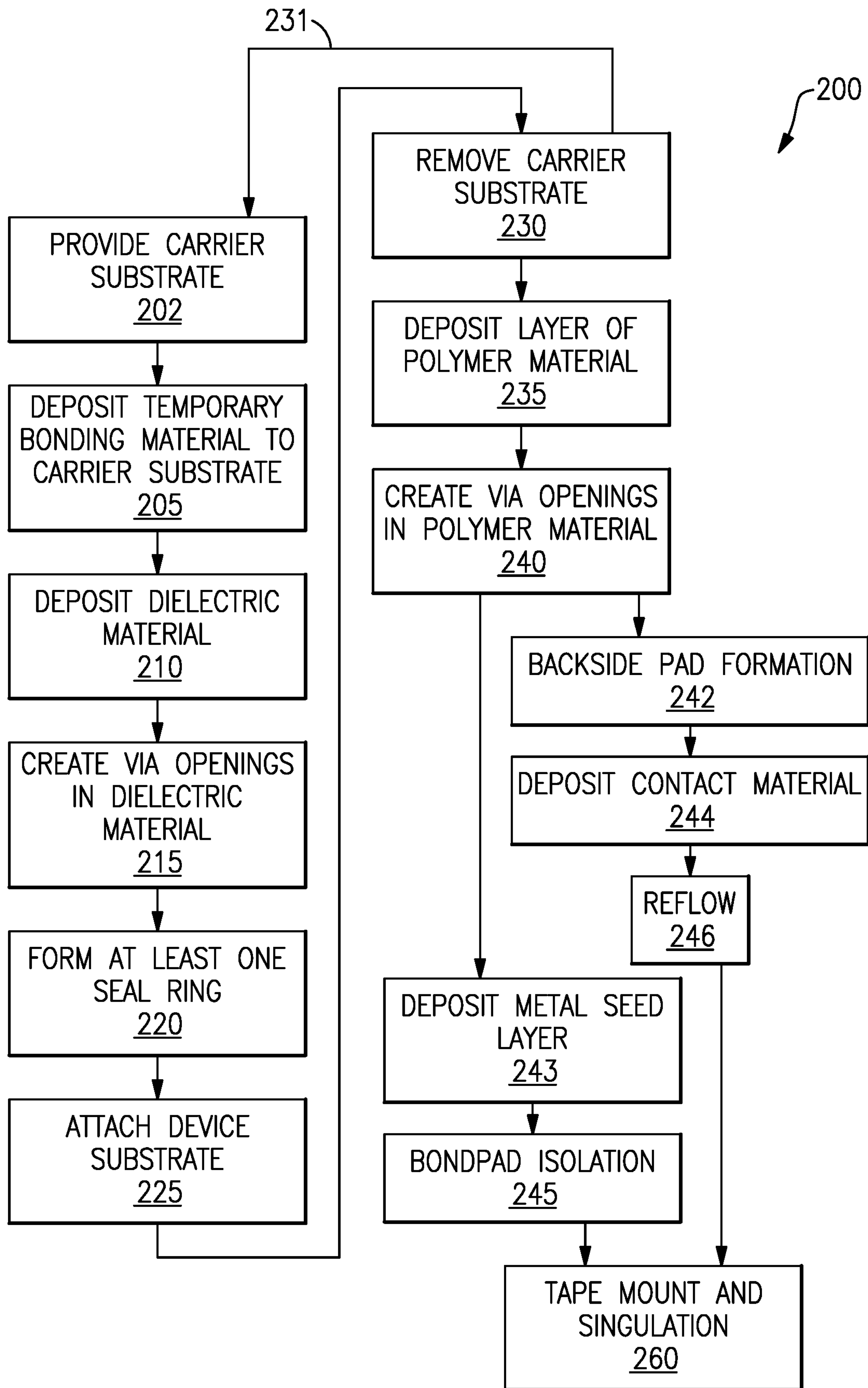

FIG.2A

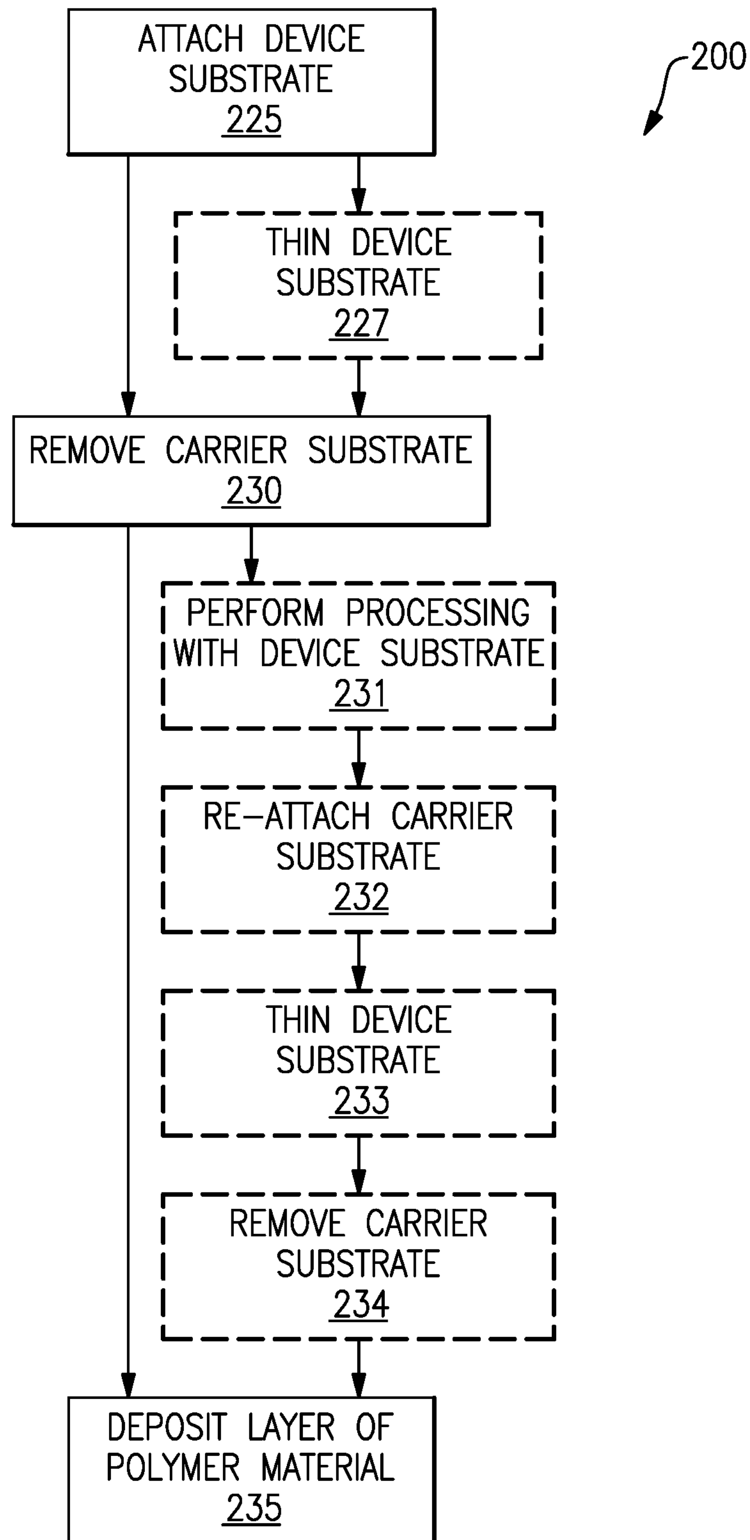

FIG.2B

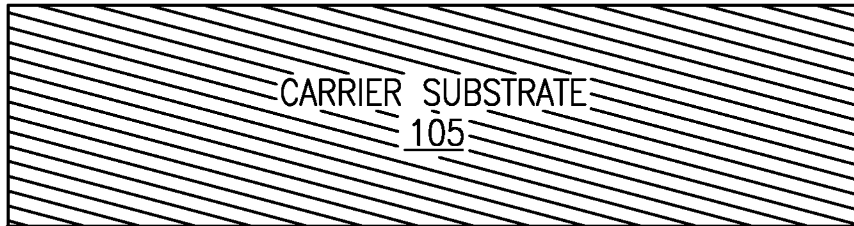

FIG.3A

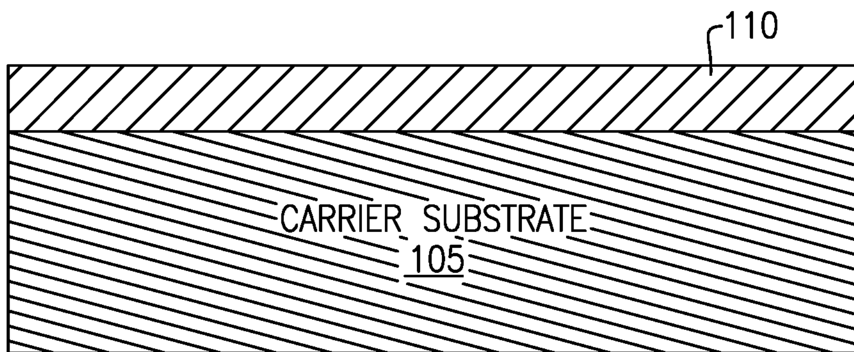

FIG.3B

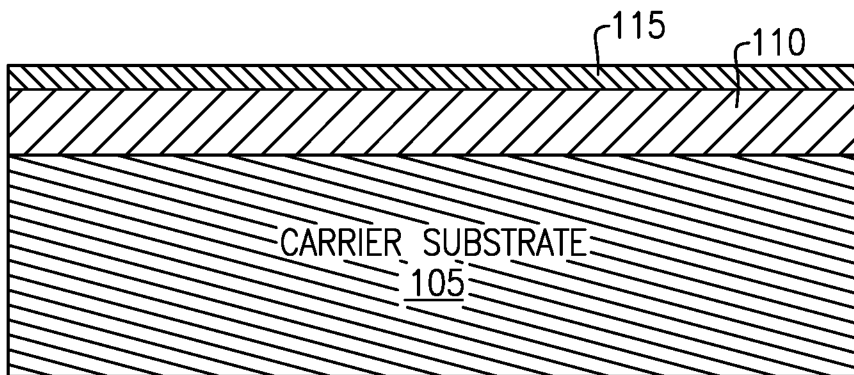

FIG.3C

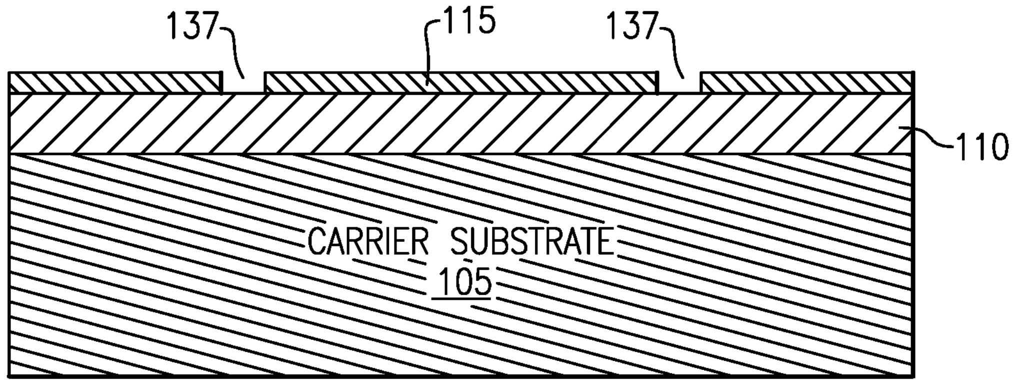

FIG.3D

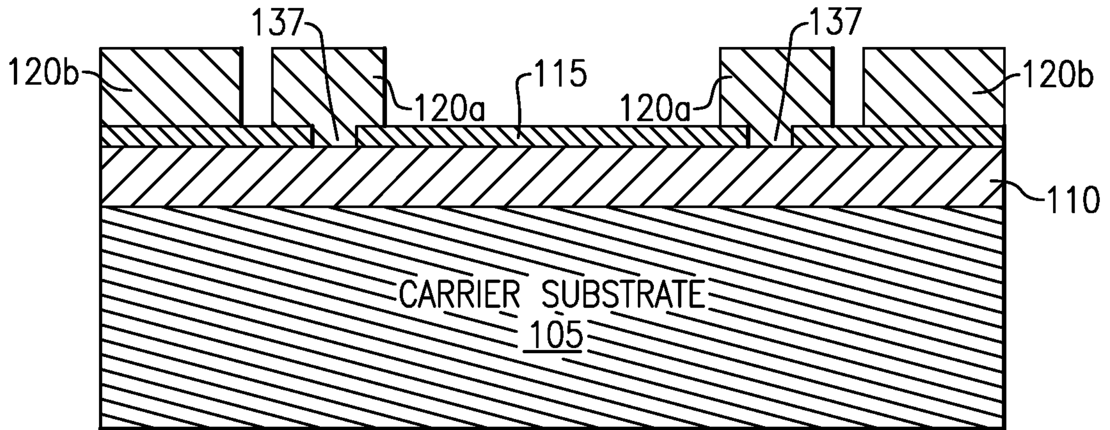

FIG.3E

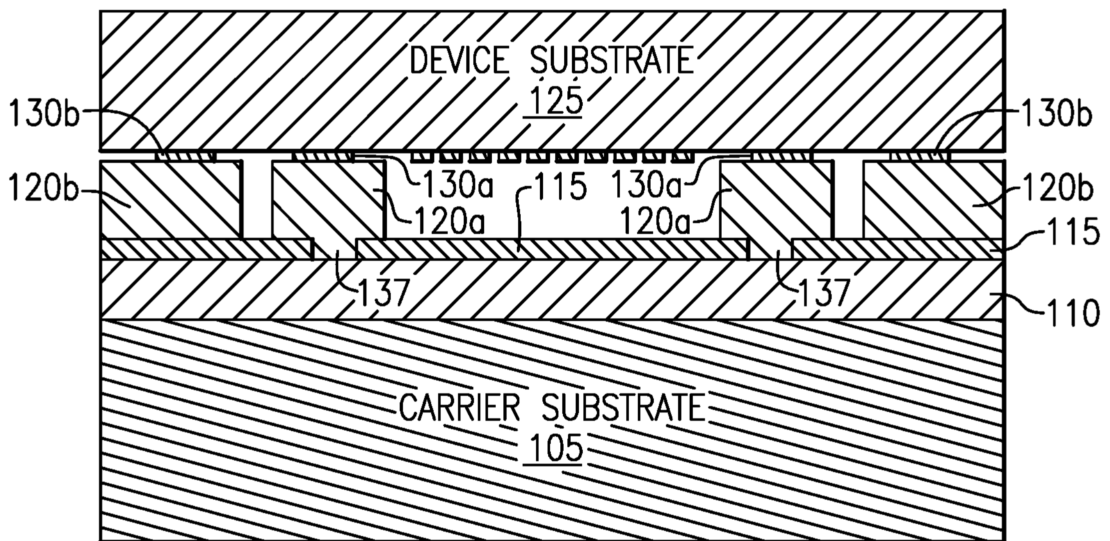

FIG.3F

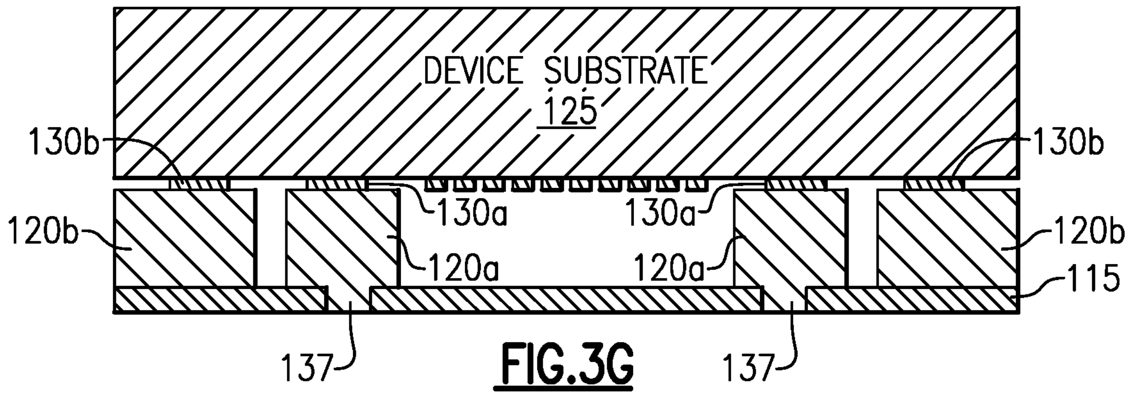

FIG.3G

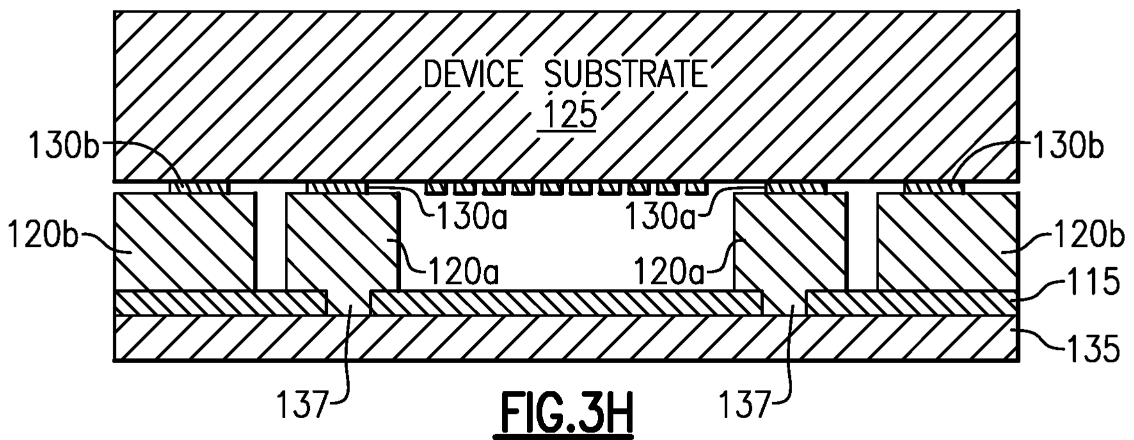

FIG.3H

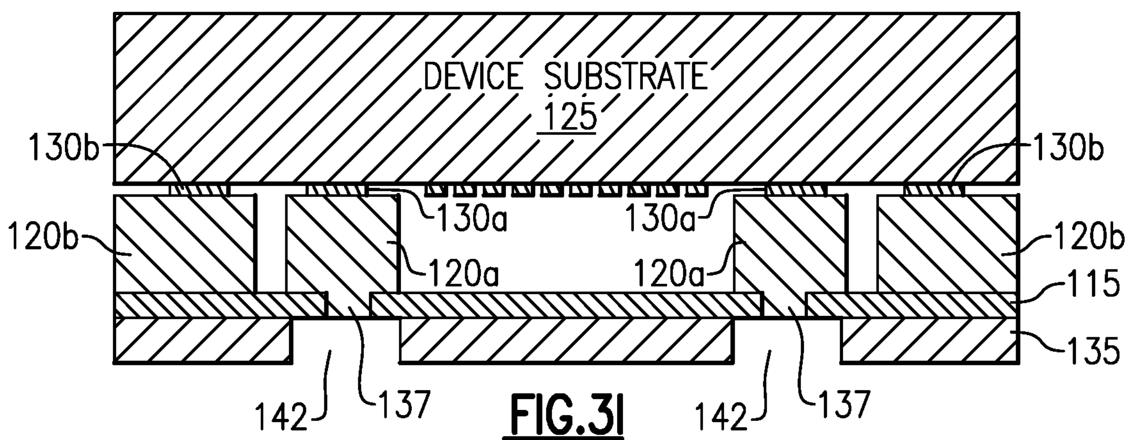

FIG.3I

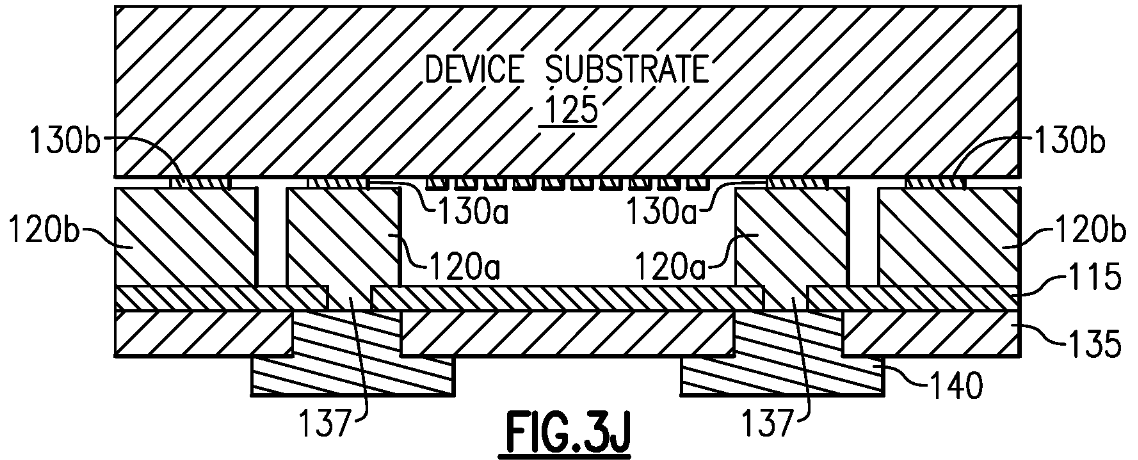

FIG.3J

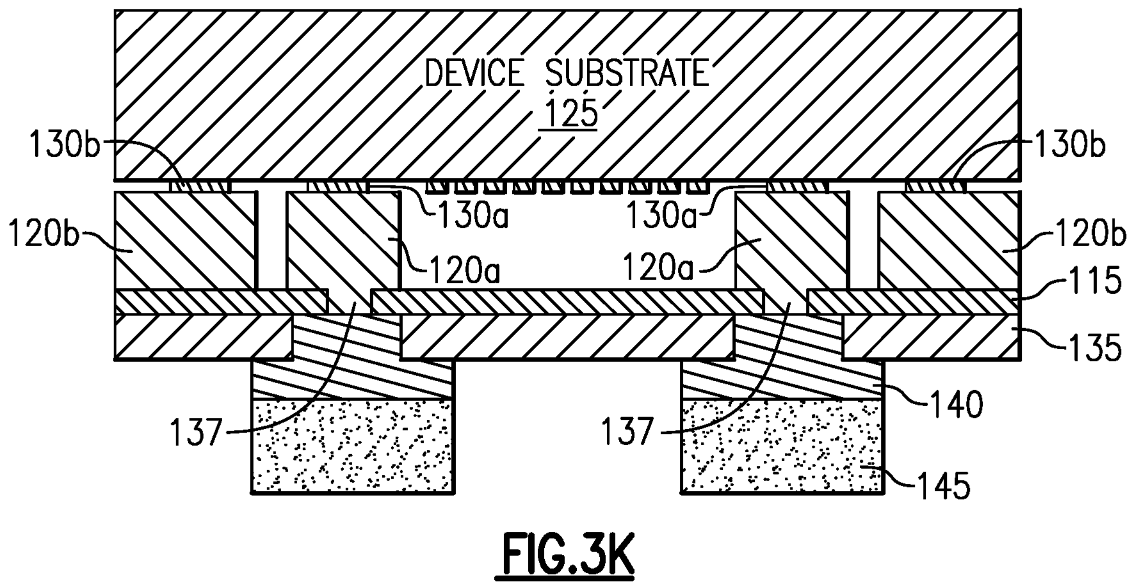

FIG.3K

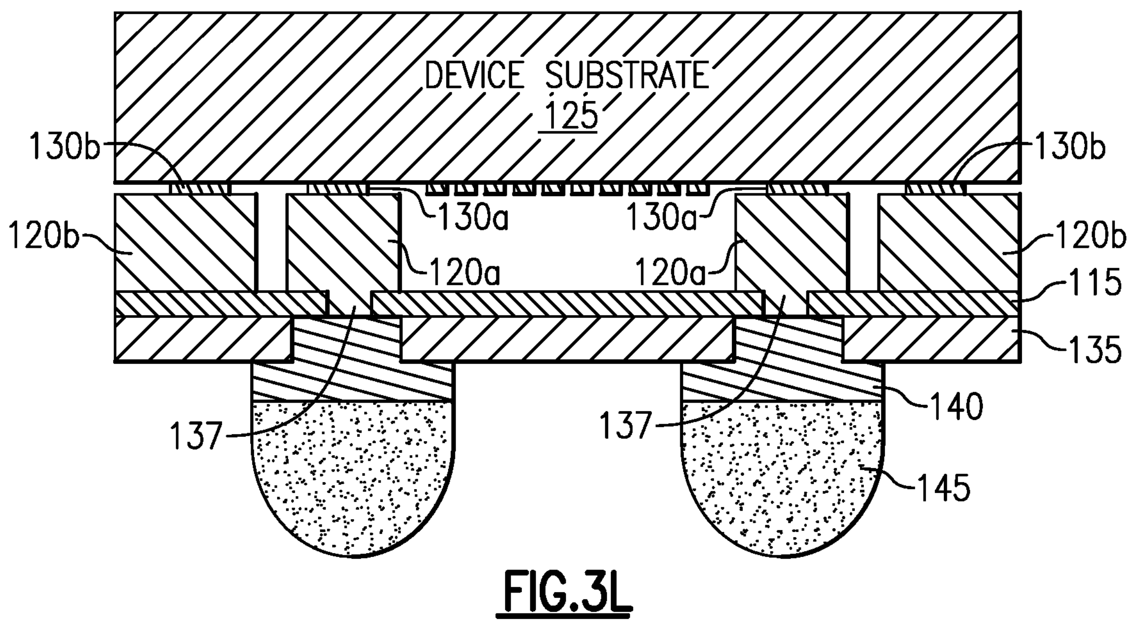

FIG.3L

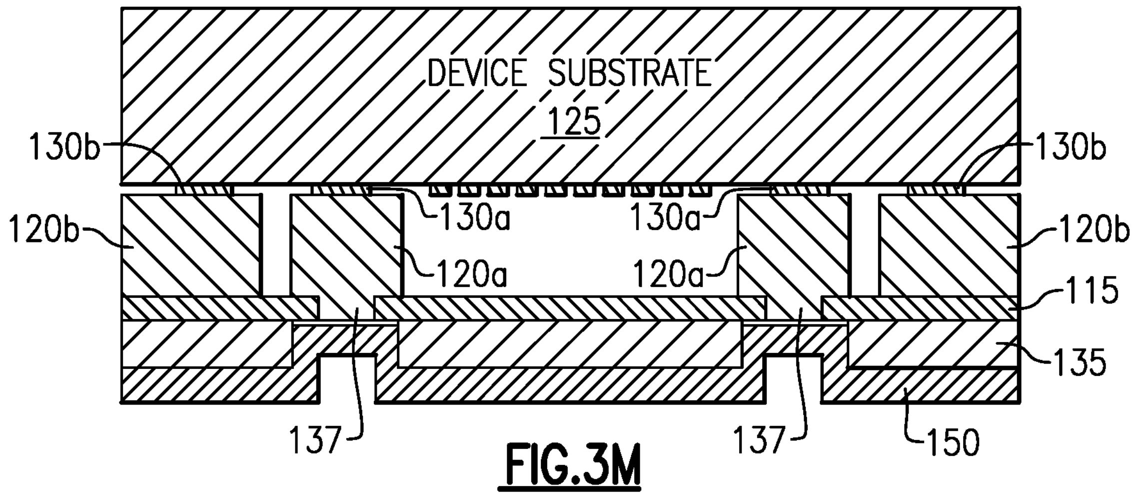

FIG.3M

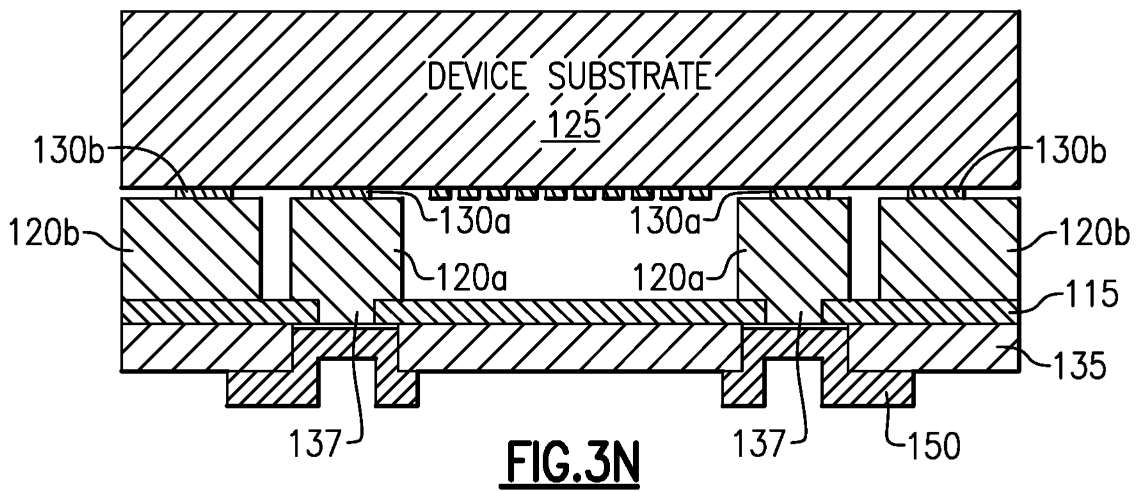

FIG.3N

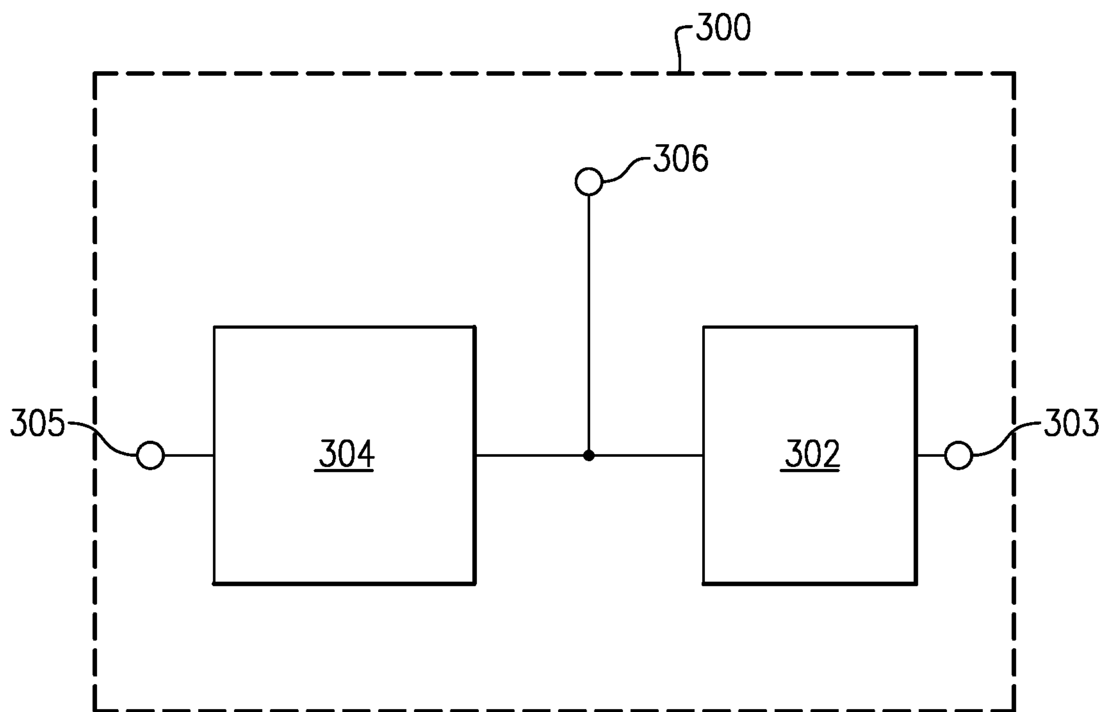

FIG.4

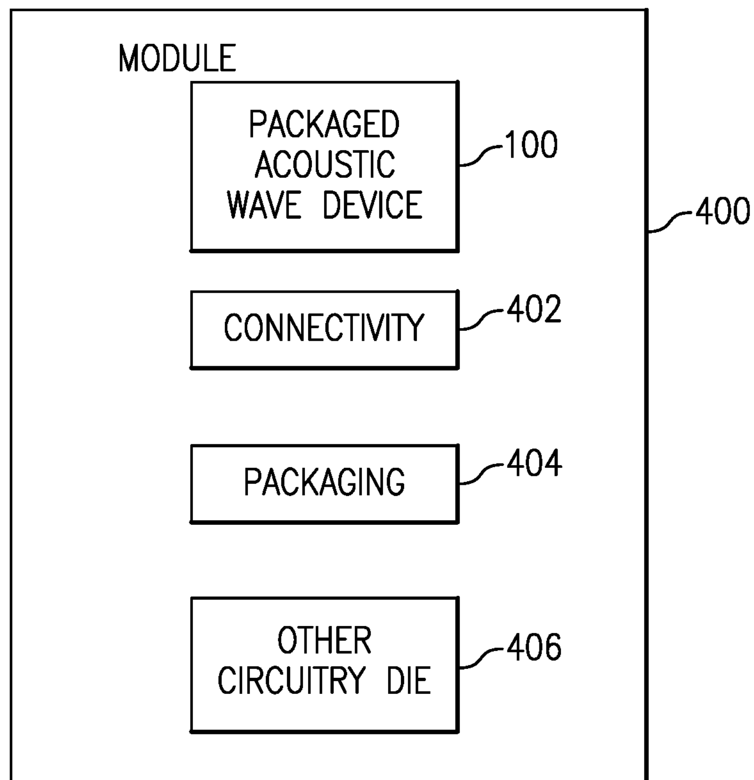

FIG.5

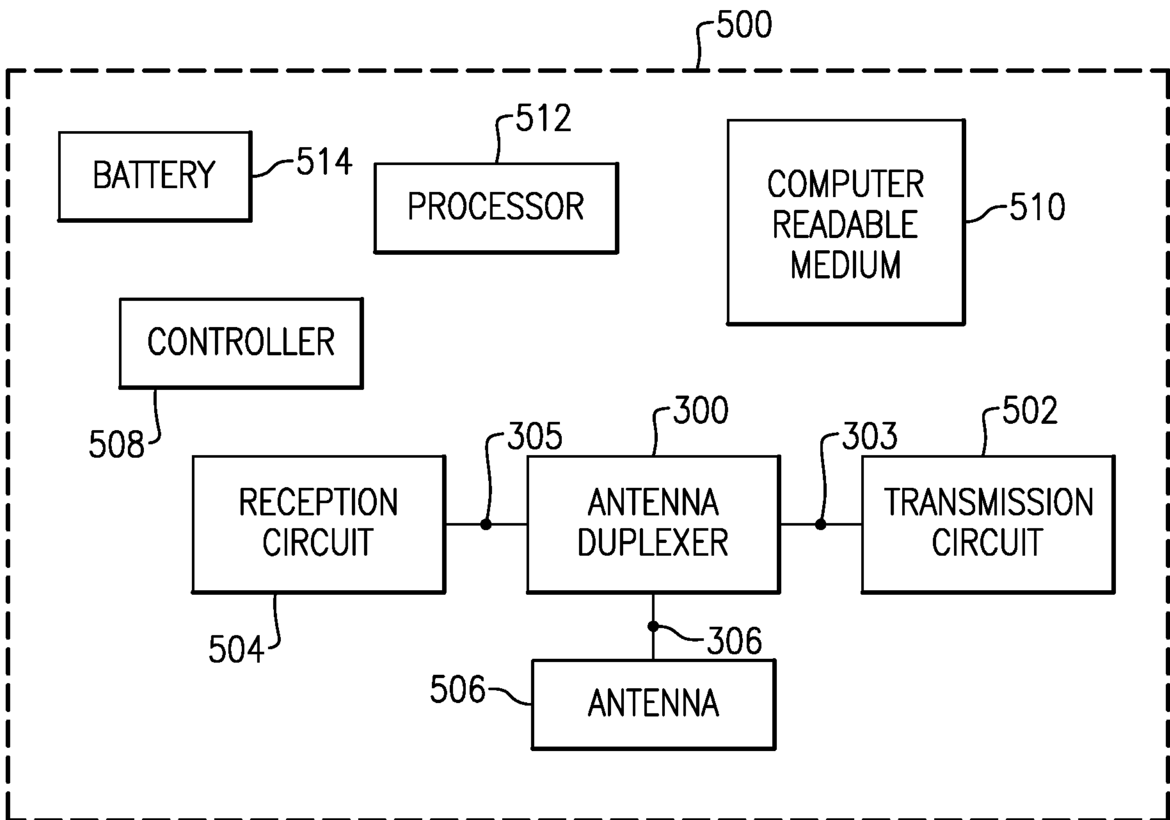

FIG.6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/017323

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/538(2006.01)i, H01L 23/525(2006.01)i, H01L 23/00(2006.01)i, H01L 23/34(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 23/538; H01L 21/60; H01L 21/768; H01L 21/56; H01L 29/84; H01L 23/48; H01L 23/498; H01L 23/525; H01L 23/00; H01L 23/34

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: carrier substrate, package, adhesive layer, dielectric layer, seal ring, recyclable

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5561085 A (BERNARD GOROWITZ et al.) 01 October 1996 See columns 6-10 and figures 3(a)-3(d).	1-30
Y	US 2007-0176250 A1 (MOON-CHUL LEE et al.) 02 August 2007 See paragraphs [0042]-[0045], [0051], [0069], claim 9 and figure 2.	1-30
Y	US 2014-0015122 A1 (MENG-WEI CHOU et al.) 16 January 2014 See paragraphs [0030]-[0047] and figures 1, 8-12.	7-13,19-27
A	US 2013-0069241 A1 (YAOJIAN LIN et al.) 21 March 2013 See paragraph [0054] and figures 4g-4i.	1-30
A	US 2008-0067664 A1 (JI-HYUK LIM et al.) 20 March 2008 See claim 1 and figure 1.	1-30

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
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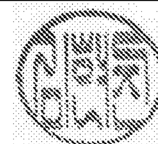

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