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(54) **DEUTERATED STRUCTURES FOR IMAGE SENSORS AND METHODS FOR FORMING THE SAME**

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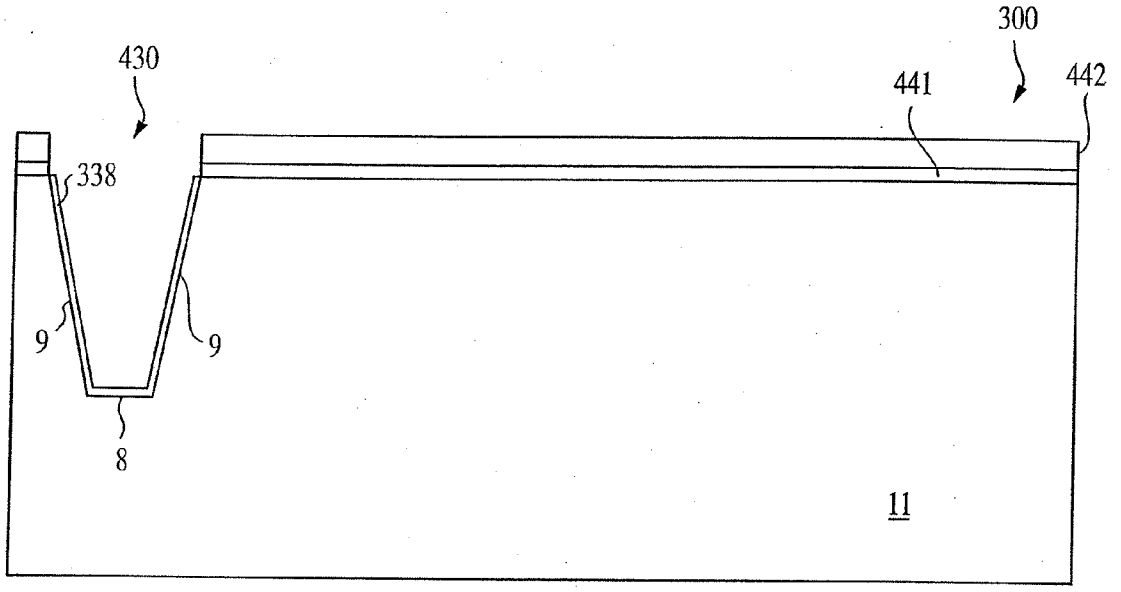
(57) **ABSTRACT**

A pixel cell with a photo-conversion device and at least one structure includes a deuterated material adjacent the photo-conversion device.



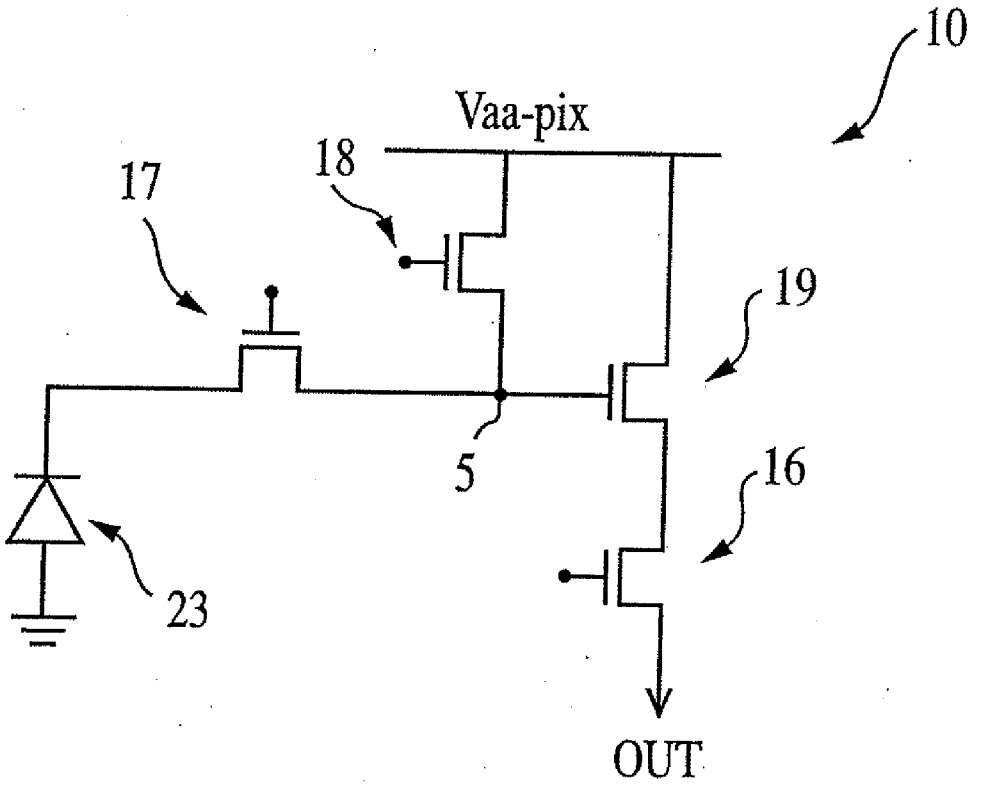


FIG. 1
(PRIOR ART)

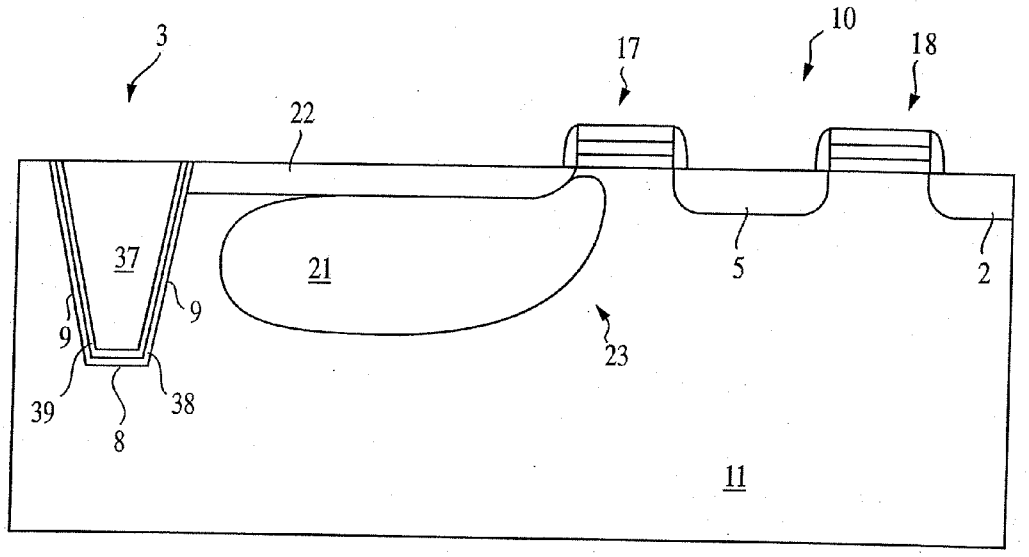


FIG. 2
(PRIOR ART)

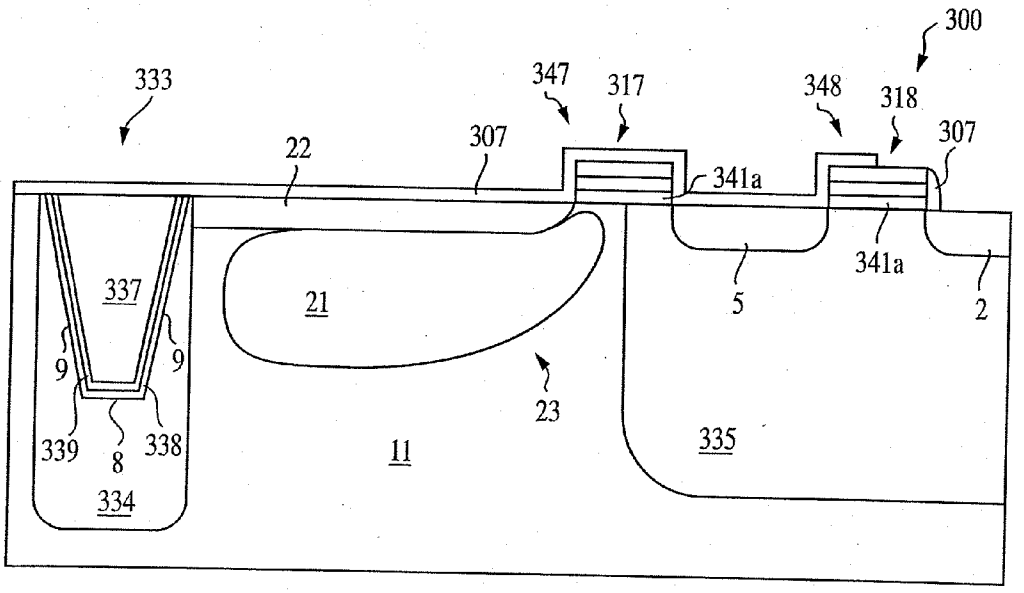


FIG. 3

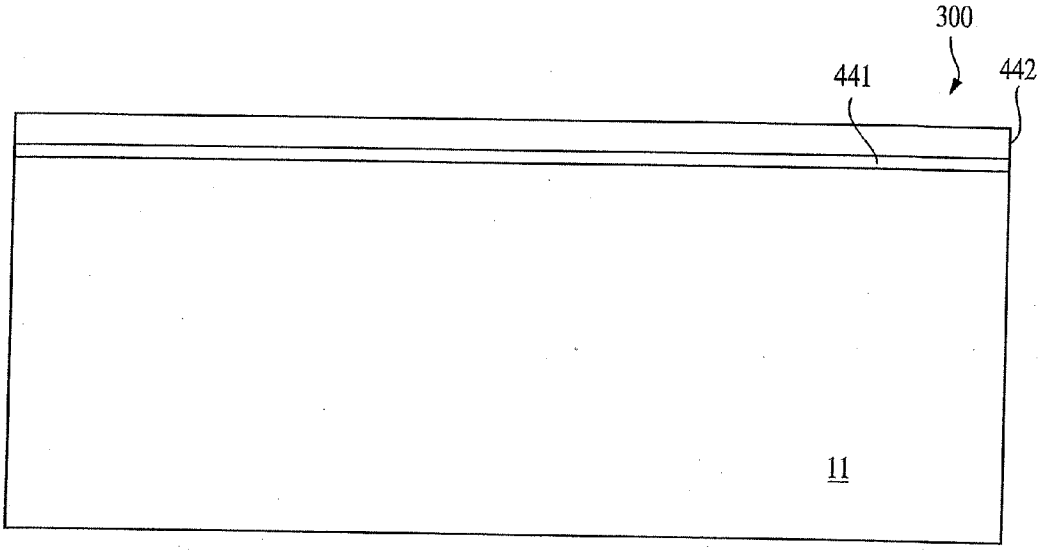


FIG. 4A

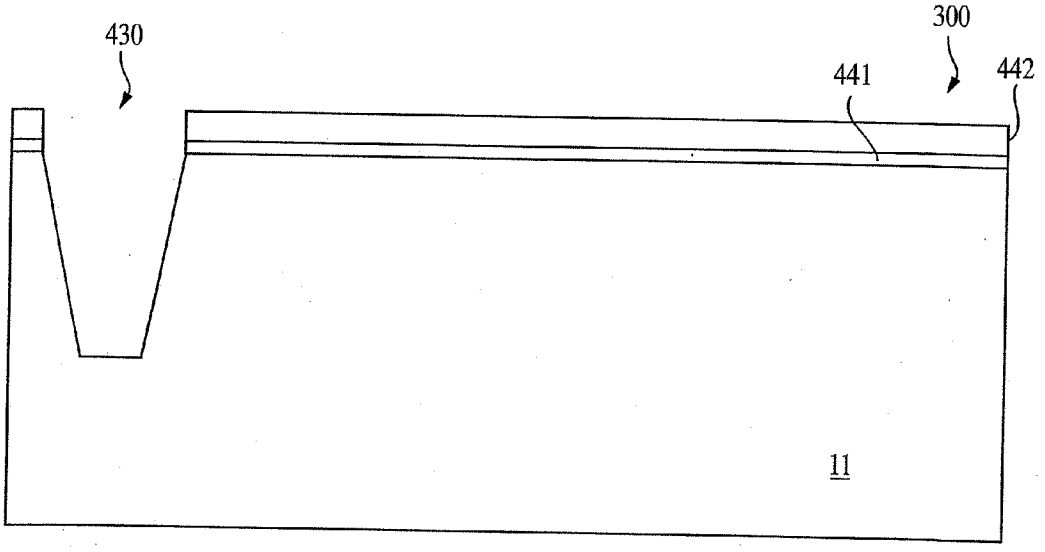


FIG. 4B

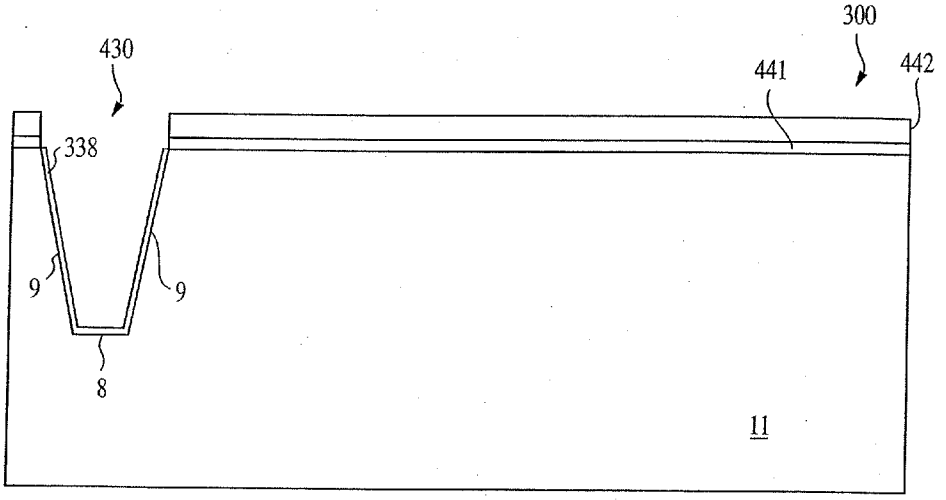


FIG. 4C

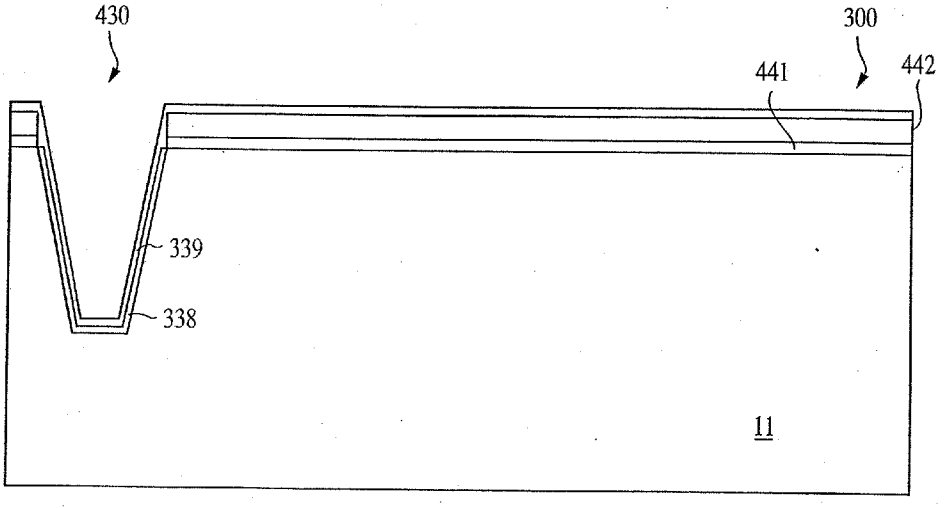


FIG. 4D

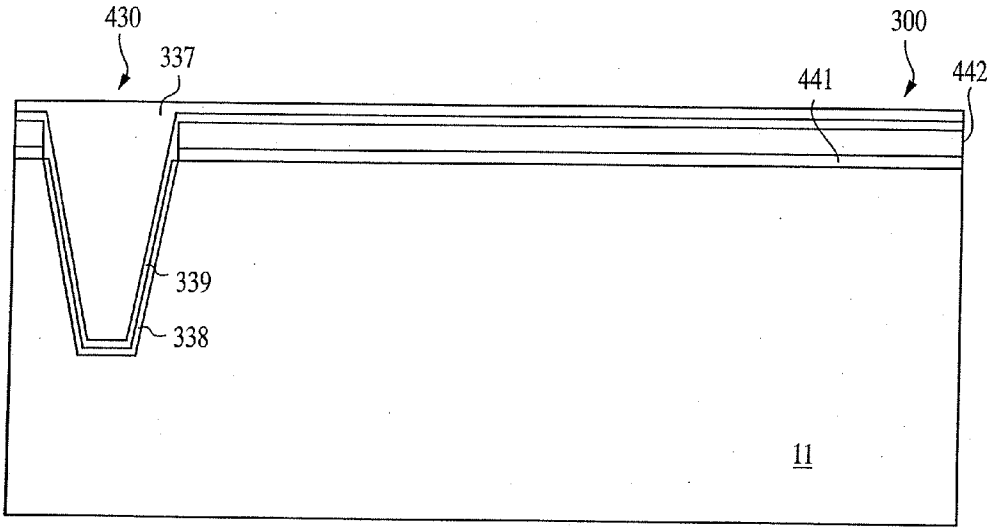


FIG. 4E

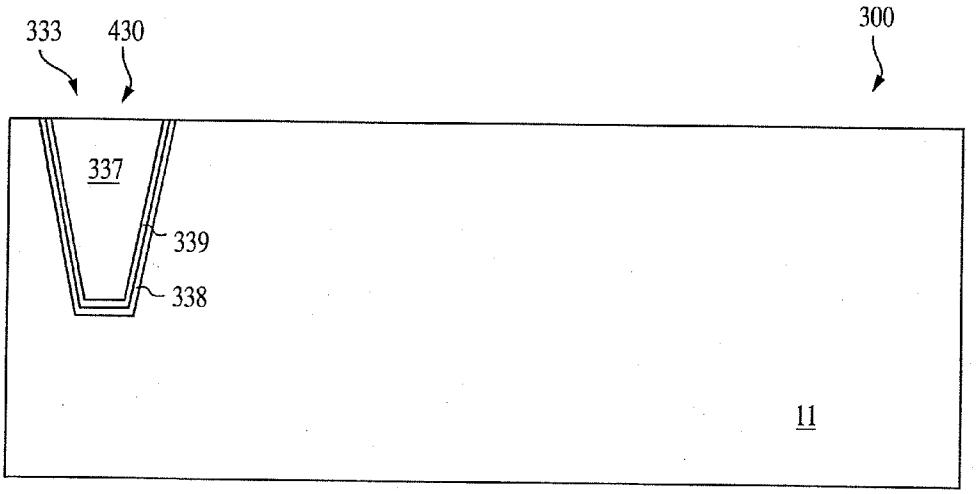


FIG. 4F

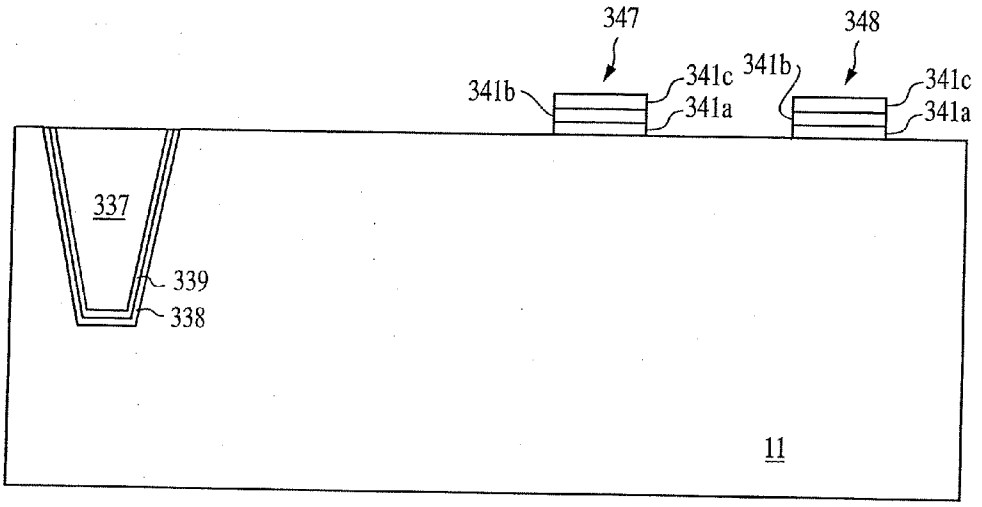

347
348
341b
341c
341a
341b
341c
341a
337
339
338
11

FIG. 4G

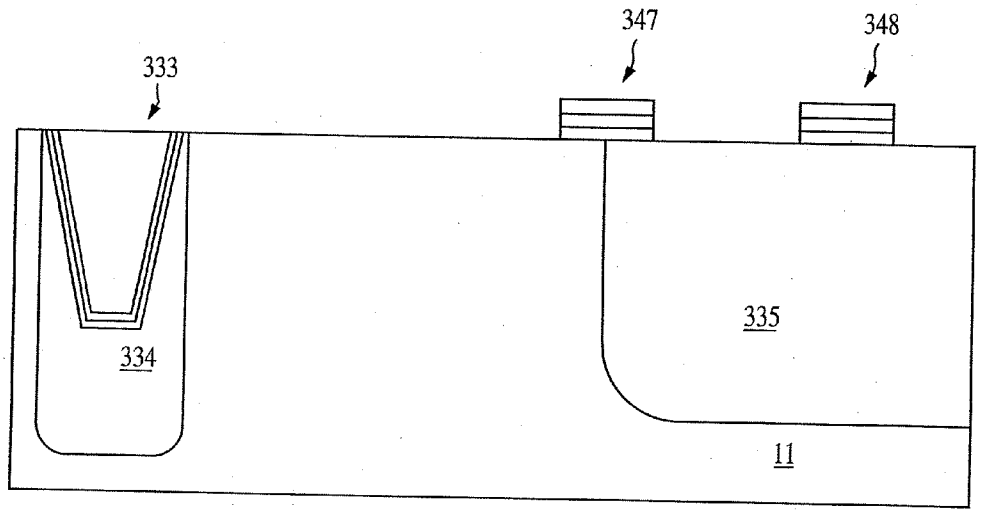

347
348
333
335
334
11

FIG. 4H

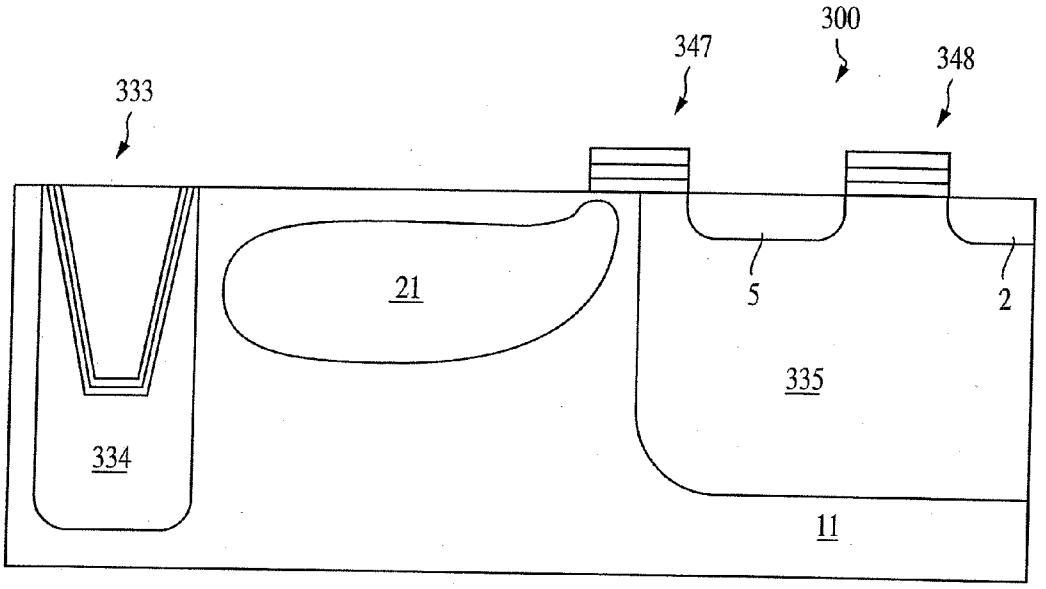


FIG. 4I

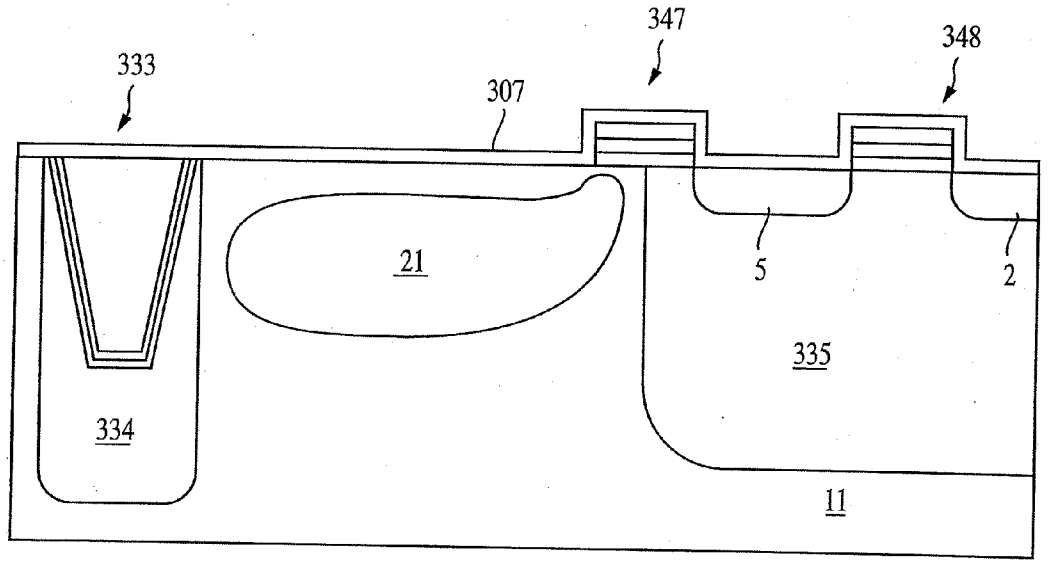


FIG. 4J

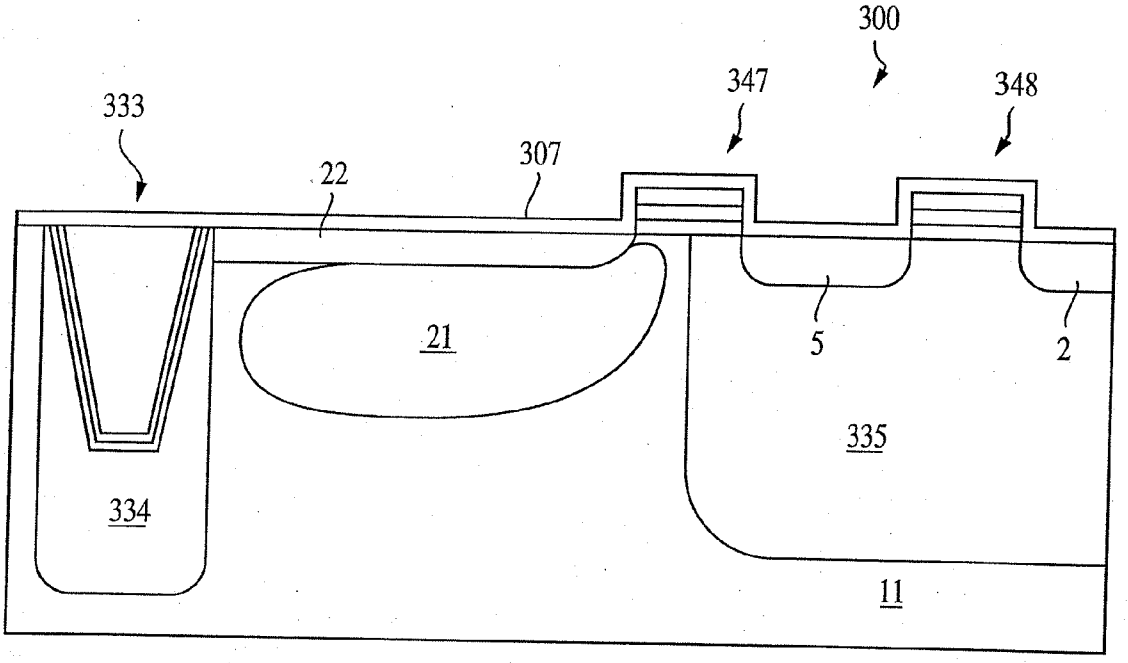


FIG. 4K

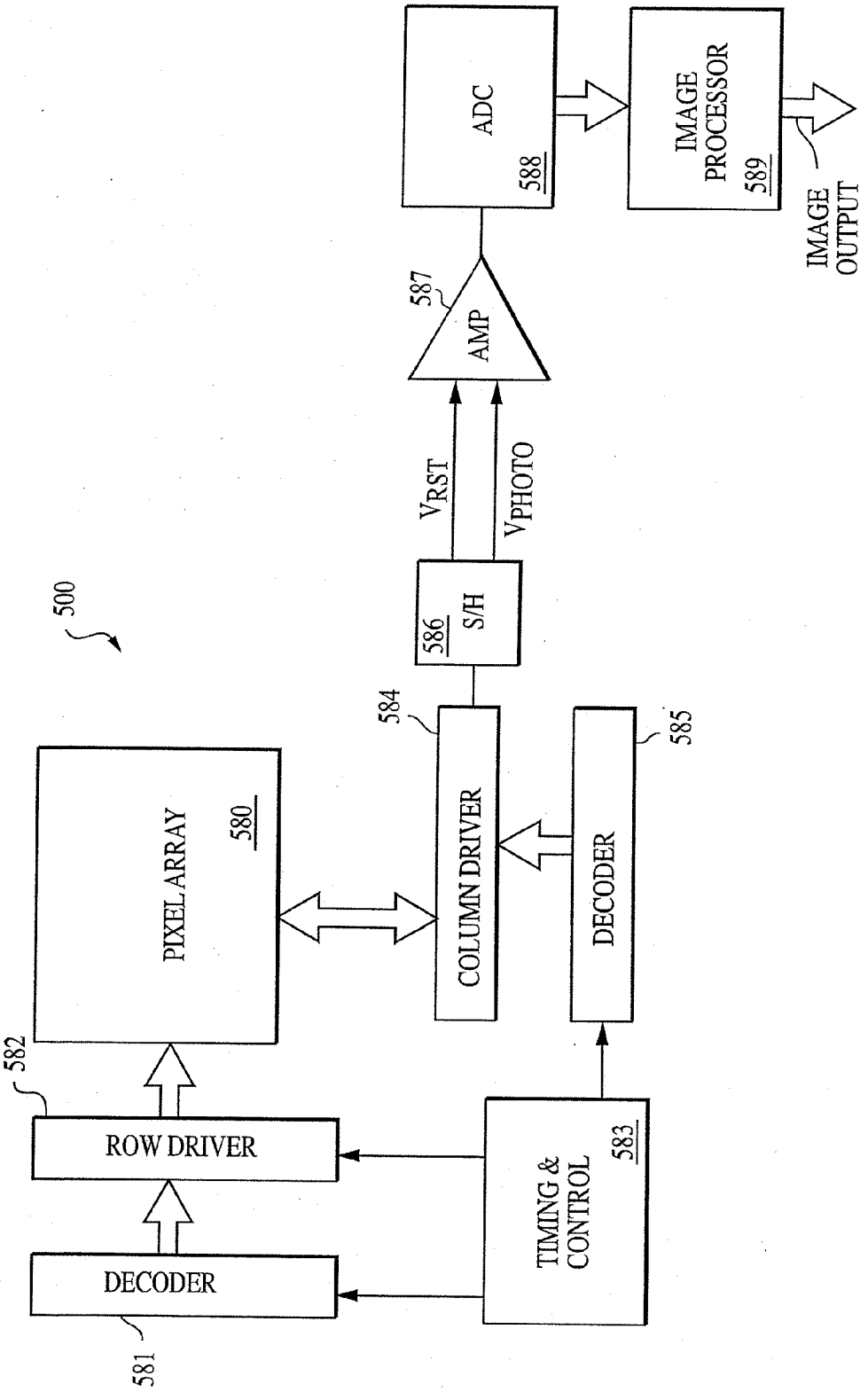

500
PIXEL ARRAY
580
582
ROW DRIVER
DECODER
581
584
COLUMN DRIVER
585
DECODER
586
S/H
V_{RST}
V_{PHOTO}
587
AMP
ADC
588
IMAGE PROCESSOR
589
IMAGE OUTPUT
TIMING & CONTROL
583

FIG. 5

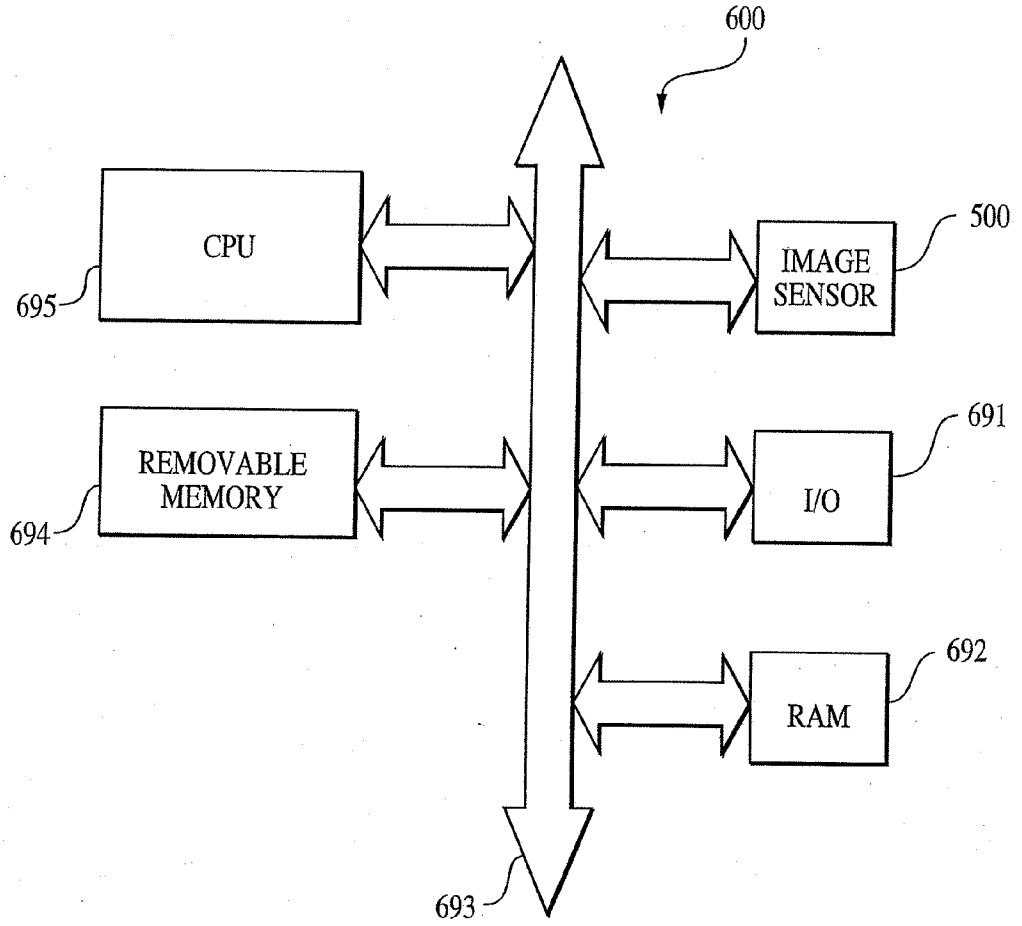

600
CPU
695
IMAGE SENSOR
500
REMOVABLE MEMORY
694
I/O
691
RAM
692
693

FIG. 6

DEUTERATED STRUCTURES FOR IMAGE SENSORS AND METHODS FOR FORMING THE SAME

FIELD OF THE INVENTION

[0001] The present invention relates generally to the field of semiconductor devices and more particularly to trench isolation technology for use in semiconductor devices, including CMOS image sensors.

BACKGROUND OF THE INVENTION

[0002] CMOS image sensors are increasingly being used as low cost imaging devices. A CMOS image sensor circuit includes a focal plane array of pixel cells, each one of the cells includes a photogate, photoconductor, or photodiode having an associated charge accumulation region within a substrate for accumulating photo-generated charge. Each pixel cell may include a transistor for transferring charge from the charge accumulation region to a sensing node, and a transistor, for resetting the sensing node to a predetermined charge level prior to charge transference. The pixel cell may also include a source follower transistor for receiving and amplifying charge from the sensing node and an access transistor for controlling the readout of the cell contents from the source follower transistor.

[0003] In a CMOS image sensor, the active elements of a pixel cell perform the necessary functions of: (1) photon to charge conversion; (2) accumulation of image charge; (3) transfer of charge to the sensing node accompanied by charge amplification; (4) resetting the sensing node to a known state before the transfer of charge to it; (5) selection of a pixel for readout; and (6) output and amplification of a signal representing pixel charge from the sensing node.

[0004] CMOS image sensors of the type discussed above are generally known as discussed, for example, in Nixon et al., "256×256 CMOS Active Pixel Sensor Camera-on-a-Chip," IEEE Journal of Solid-State Circuits, Vol. 31(12), pp. 2046-2050 (1996); and Mendis et al., "CMOS Active Pixel Image Sensors," IEEE Transactions on Electron Devices, Vol. 41(3), pp. 452-453 (1994). See also U.S. Pat. Nos. 6,177,333 and 6,204,524, which describe the operation of conventional CMOS image sensors and are assigned to Micron Technology, Inc., the contents of which are incorporated herein by reference.

[0005] A schematic diagram of a conventional CMOS pixel cell **10** is shown in FIG. **1**. The illustrated CMOS pixel cell **10** is a four transistor (4T) cell. The CMOS pixel cell **10** generally comprises a photo-conversion device **23** for generating and collecting charge generated by light incident on the pixel cell **10**, and a transfer transistor **17** for transferring photoelectric charges from the photo-conversion device **23** to a sensing node, typically a floating diffusion region **5**. The floating diffusion region **5** is electrically connected to the gate of an output source follower transistor **19**. The pixel cell **10** also includes a reset transistor **18** for resetting the floating diffusion region **5** to a predetermined voltage; and a row select transistor **16** for outputting a signal from the source follower transistor **19** to an output terminal in response to an address signal.

[0006] FIG. **2** is a cross-sectional view of the pixel cell **10** of FIG. **1** depicting the photo-conversion device **23**. The exemplary CMOS pixel cell **10** has a photo-conversion device **23**, which may be formed as a pinned photodiode. The photodiode **23** has a p-n-p construction comprising a p-type surface layer **22** and an n-type photodiode region **21** within a p-type active layer **11**. The photodiode **23** is adjacent to and partially underneath the transfer transistor **17**. The reset transistor **18** is on a side of the transfer transistor **17** opposite the photodiode **23**. As shown in FIG. **2**, the reset transistor **18** includes a source/drain region **2**. The floating diffusion region **5** is between the transfer and reset transistors **17**, **18**.

[0007] In the CMOS pixel cell **10** depicted in FIGS. **1** and **2**, electrons are generated by light incident on the photo-conversion device **23** and are stored in the n-type photodiode region **21**. These charges are transferred to the floating diffusion region **5** by the transfer transistor **17** when the transfer transistor **17** is activated. The source follower transistor **19** produces an output signal from the transferred charges. A maximum output signal is proportional to the number of electrons extracted from the n-type photodiode region **21**.

[0008] Conventionally, a shallow trench isolation (STI) region **3** adjacent to the charge collection region **21** is used to isolate the pixel cell **10** from other pixel cells and devices of the image sensor. The STI region **3** is typically formed using a conventional STI process. The STI region **3** is typically lined with an oxide liner **38** and filled with a dielectric material **37**. Also, the STI region **3** can include a nitride liner **39** between the oxide liner **38** and the dielectric material **37**.

[0009] The nitride liner **39** provides several benefits, including improved corner rounding near the STI region **3** corners. The nitride liner **39** typically has tensile stress. Since the dielectric material **37** typically introduces compressive stress, the presence of the nitride liner **39** results in an overall decrease in stress levels. Reduced stress levels provide decreased leakage currents in the photo-conversion device **23**. Particularly, leakage from trap-assisted tunneling and trap-to-trap tunneling mechanisms is decreased.

[0010] A common problem associated with the above described STI region **3** is dangling bonds (e.g., dangling Si—bonds) at the surface of the substrate **11** along the trench bottom **8** and sidewalls **9**. The dangling bonds create a high density of trap sites along the trench bottom **8** and sidewalls **9**. These trap sites are normally uncharged but become charged when electrons and holes become trapped in the sites. As a result of these trap sites formed along the bottom **8** and sidewalls **9** of the STI region **3**, current generation near and along the trench bottom **8** and sidewalls **9** can be significant. Current generated from trap sites inside or near the photodiode **23** depletion region causes undesired dark current and an increase in fixed pattern noise.

[0011] Conventionally, hydrogen passivation is used to reduce the dangling bonds. However, the nitride liner **39** acts as a diffusion barrier for hydrogen (H_2) during passivation and reduces passivation of the dangling bonds. Therefore, when the nitride liner **39** is used dark current may increase.

[0012] It is desirable to have an isolation region with a nitride liner and reduced dangling bonds.

BRIEF SUMMARY OF THE INVENTION

[0013] Exemplary embodiments of the invention provide a pixel cell having a photo-conversion device and at least one structure including a deuterated material adjacent the photo-conversion device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The foregoing and other aspects of the invention will be better understood from the following detailed descrip-

tion of the invention, which is provided in connection with the accompanying drawings, in which:

[0015] FIG. **1** is a schematic diagram of a conventional pixel cell;

[0016] FIG. **2** is a cross sectional side view of a conventional pixel cell;

[0017] FIG. **3** is a cross sectional side view of a pixel cell according to an exemplary embodiment of the invention;

[0018] FIG. **4**A depicts the pixel cell of FIG. **3** at an initial stage of processing;

[0019] FIGS. **4**B-**4**K depict the pixel cell of FIG. **3** at intermediate stages of processing;

[0020] FIG. **5** is a block diagram of a CMOS image sensor according to an exemplary embodiment of the invention; and

[0021] FIG. **6** is a schematic diagram of a computer processor system incorporating the CMOS image sensor of FIG. **5**.

DETAILED DESCRIPTION OF THE INVENTION

[0022] In the following detailed description, reference is made to the accompanying drawings, which form a part hereof and illustrate specific embodiments in which the invention may be practiced. In the drawings, like reference numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and that structural, logical and electrical changes may be made without departing from the spirit and scope of the present invention.

[0023] The terms "wafer" and "substrate" are to be understood as including silicon, silicon-on-insulator (SOI), silicon-on-sapphire (SOS), and silicon-on-nothing (SON) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a "wafer" or "substrate" in the following description, previous process steps may have been utilized to form regions or junctions in the base semiconductor structure or foundation. In addition, the semiconductor need not be silicon-based, but could be based on silicon-germanium, germanium, or gallium-arsenide.

[0024] The term "pixel" or "pixel cell" refers to a picture element unit cell containing a photo-conversion device and transistors for converting electromagnetic radiation to an electrical signal. For purposes of illustration, a representative pixel cell is illustrated in the figures and description herein, and typically fabrication of all pixel cells in an image sensor will proceed concurrently and in a similar fashion.

[0025] FIG. **3** is a cross-sectional view of a pixel cell **300** according to an exemplary embodiment of the invention. The pixel cell **300** is similar to the pixel cell **10** depicted in FIGS. **1** and **2**, except that one or more of the pixel cell **300** structures includes a material containing deuterium, rather than the conventional structures that contain hydrogen. In particular, the pixel cell **300** includes an improved isolation region **333**, which has a deuterated nitride liner **339** and a deuterated oxide liner **338**, and an improved transfer transistor **317** gate stack **347**, which has a deuterated gate oxide layer **341***a*. The pixel cell **300** also includes as deuterated oxide layer **307** over the transfer gate stack **347**, the photodiode **23**, the floating diffusion region **5**, and portions of the reset gate stack **348**.

[0026] Further, the pixel cell **300** may include a first conductivity type doped well, e.g., a p-type well **334** surrounding the isolation region **333** and a p-type well **335** below the floating diffusion region **5**, the reset transistor **318**, and a portion of the transfer transistor **317**. Although not shown in FIG. **3**, the pixel cell **300** also includes source follower and row select transistors **19**, **16**, respectively (as shown in FIG. **1**).

[0027] Recently, deuterium has been shown to be a far superior passivating species than hydrogen by a factor of 30. See e.g., Cheng et al., *Improved Hot-Carrier Reliability of SOI Transistors by Deuterium Passivation of Defects at Oxide/Silicon Interfaces,* IEEE Transactions on Electron Devices, Vol. 49., No. 3, March 2002, pgs. 529-531. See also, Tseng et al., *ALD HfO_2 Heavy Water (D_2O) for improved MOSFET Stability,* Electron Devices Meeting, 2003. IEDM '03 Technical Digest, IEEE International, December 2003, pp. 4.1.1-4.1.4, which is incorporated herein by reference. In essence, deuterium is an isotope of hydrogen and possesses a larger molecular size and is less susceptible than hydrogen to being displaced by hot carriers. The deuterated structures **338**, **339**, **341***a*, **307** serve as a solid source of deuterium, which improves the passivation of dangling bonds. The deuterated liners **338**, **339**, in particular, improve the passivation of dangling bonds along the isolation region sidewalls **9** and bottom **8**, thereby reducing dark current.

[0028] The passivation of a silicon dangling bond by hydrogen (H) requires an activation energy of 1.51 eV (Si^{-}+H_2=Si—H+H). Passivation of a silicon dangling bond by deuterium (D) requires an analogous activation energy of 1.51 eV (Si^{-}+D_2=Si–D+D). Whereas, replacing a hydrogen-passivated bond by deuterium (Si—H+D_2=Si–D+HD) requires an activation energy of 1.84 eV. As a result, deuterium incorporation at the substrate **11**/oxide liner **338** interface is largely limited by the replacement of pre-existing hydrogen with deuterium.

[0029] FIGS. **4**A-**4**K depict the formation of pixel cell **300** according to an exemplary embodiment of the invention. No particular order is required for any of the actions described herein, except for those logically requiring the results of prior actions. Accordingly, while the actions below are described as being performed in a general order, the order is exemplary only and can be altered if desired.

[0030] As illustrated in FIG. **4**A, a pad oxide layer **441** is formed on the substrate **11**. Preferably, the pad oxide layer **441** is formed as a deuterated pad oxide layer. The deuterated pad oxide layer **441** can be formed, for example, by thermal oxidation in the presence of heavy water (D_2O). If desired, the pad oxide layer **441** can instead be formed as a conventional (non-deuterated) pad oxide layer **441**.

[0031] A sacrificial layer **442** is formed on the deuterated pad oxide layer **441**. In the illustrated embodiment, the sacrificial layer **442** is a deuterated silicon nitride layer. As is know in the art, a deuterium containing nitride material can be formed by using deuterium-containing compound (e.g., ammonia (ND_3) and silane (SiD_4)) instead of a hydrogen-containing compound (e.g., ammonia (NH_3) and silane (SiH_4)). In this manner the deuterated silicon nitride layer **442** can be formed. If desired, the sacrificial layer **442** can instead be a conventional nitride layer or a dielectric anti-reflective coating (DARC) layer formed by known methods.

[0032] FIG. **4**B depicts the formation of a trench **430** in the substrate **11** and through the layers **441**, **442** on the substrate **11**. The trench **430** can be formed by any known technique. For example, a photoresist mask (not shown), either positive or negative resist (preferably positive) as known in the art, is

applied over the sacrificial layer **442** and patterned using standard photolithographic patterning techniques. The sacrificial layer **442** and the pad oxide layer **441** are etched by a dry etch process. The etch process is allowed to continue into the substrate **11** to form the trench **430**. In one implementation, the trench **430** extends into the substrate **11** to a depth of approximately 1000 Å to approximately 8000 Å. An anisotropic etch such as a plasma or reactive ion etch (RIE) process can be used as the dry etch. The photoresist mask (not shown) is removed using standard photoresist stripping techniques, preferably by a plasma etch.

[0033] A thin layer of oxide **338**, between approximately 50 Å and approximately 150 Å thick, is formed on the trench **430** sidewalls **9** and bottom **8**, as shown in FIG. **4**C. Preferably, the oxide layer **338** is a deuterated oxide layer. The deuterated oxide layer **338** is formed similarly to the deuterated pad oxide layer **441**, as described above in connection with FIG. **4**A. Alternatively, the trench **430** can be lined with a conventional oxide layer.

[0034] Optionally, before or after the oxide layer **338** is formed, deuterium can be implanted into the oxide layer **338** and trench **430** sidewalls **9** and bottom **8**. The deuterium implant increases the deuterium concentration at the oxide **338**/substrate **11** interface. The deuterium implant can be conducted by methods known in the art. For example, a mask (e.g., photoresist) (not shown) can formed over the substrate **11** and patterned to provide an opening to the trench **430**. According to an embodiment of the invention, the implant dose is within the range of approximately 1×10^{13} atoms/cm^2 to approximately 1×10^{15} atoms/cm^2 at an energy within the range of approximately 10 keV to approximately 100 keV. Preferably, the implant dose is approximately 2×10^{14} atoms/cm^2 at an energy of approximately 40 keV. After the implant, an inert anneal step is conducted at a temperature within the range of approximately 800 degrees Celsius (° C.) to approximately 1000° C. for approximately 10 minutes to approximately 30 minutes. Preferably the inert anneal step is conducted at approximately 850° C. for approximately 20 minutes.

[0035] Alternatively, the deuterium implant and inert anneal steps can instead be conducted after the formation of the nitride liner **339** described below in connection with FIG. **4**D.

[0036] As depicted in FIG. **4**D, the trench **430** is lined with a nitride liner **339**. Preferably, the nitride liner **339** is a deuterated nitride liner, e.g., deuterated silicon nitride. The deuterated nitride liner **339** is formed by any suitable technique, to a thickness within the range of approximately 50 Å to approximately 150 Å. For example, the deuterated nitride liner **339** can be deposited using deuterium-containing compound (e.g., ammonia (ND_3) and silane (SiD_4)). Alternatively, the trench **430** can be lined a conventional nitride liner, or can lack a nitride liner.

[0037] Optionally, once the nitride liner **339** is formed, a high pressure deuterium anneal can be conducted, which serves to increase the incorporation of deuterium at the oxide **338**/substrate **11** interface. The high pressure anneal is conducted at a pressure within the range of approximately 1 atmosphere (atm) to approximately 5 atm at a temperature within the range of approximately 300° C. to approximately 500° C. The anneal time is within the range of approximately 30 minutes to approximately 120 minutes. Preferably the high pressure anneal is conducted at a pressure of approximately 5 atm at a temperature of approximately 400° C. for approximately 30 minutes.

[0038] The trench **430** is then filled with a dielectric material **337** as shown in FIG. **4**E. The dielectric material **337** may be an oxide material, for example a silicon oxide, such as SiO or SiO_2; oxynitride; a nitride material, such as silicon nitride; silicon carbide; a high temperature polymer; or other suitable dielectric material. In the illustrated embodiment, the dielectric material **337** is a high density plasma (HDP) oxide.

[0039] A chemical mechanical polish (CMP) step is conducted to remove the nitride layer **442** over the surface of the substrate **11** outside the trench **430**, as shown in FIG. **4**F. Also, the pad oxide layer **441** is removed, for example, using a field wet buffered-oxide etch step and a clean step.

[0040] FIG. **4**G depicts the formation of the transfer transistor **317** (FIG. **3**) gate stack **347** and the reset transistor **318** (FIG. **3**) gate stack **348**. A first insulating layer **341***a* is formed on the substrate **11**. Preferably, the first insulating layer is a deuterated oxide layer, for example, deuterated silicon oxide. The deuterated oxide layer **341***a* serves as the gate oxide layer **341***a* for the subsequently formed transistor gate **341***b*. Alternatively, the gate oxide layer **341***a* in one or more of the gate stacks **347**, **348** can be formed without deuterium.

[0041] Next, a layer of conductive material **341***b* is deposited over the deuterated oxide layer **341***a*. The conductive layer **341***b* serves as the gate electrode for the transistors **317**, **318** (FIG. **3**). The conductive layer **341***b* may be a layer of polysilicon, which may be doped to a second conductivity type, e.g., n-type. A second insulating layer **341***c* is deposited over the conductive layer **341***b*. The insulating layer **341***c* may be formed of, for example, an oxide (SiO_2), a nitride (silicon nitride), an oxynitride (silicon oxynitride), ON (oxide-nitride), NO (nitride-oxide), or ONO (oxide-nitride-oxide).

[0042] The conductive layer **341***b* and the second insulating layer **341***c* may be formed by conventional deposition methods, such as chemical vapor deposition (CVD) or plasma enhanced chemical vapor deposition (PECVD), among others. The layers **341***a*, **341***b*, **341***c* are then patterned and etched to form the multilayer gate stacks **347**, **348** shown in FIG. **4**G.

[0043] The invention is not limited to the structure of the gate stacks **347**, **348** described above. Additional layers may be added or the gate stacks **347**, **348** may be altered as is desired and known in the art. For example, a silicide layer (not shown) may be formed between the gate electrodes **341***b* and the second insulating layers **341***c*. The silicide layer may be included in the gate stacks **347**, **348**, or in all of the transistor gate stack structures in an image sensor circuit, and may be titanium silicide, tungsten silicide, cobalt silicide, molybdenum silicide, or tantalum silicide. This additional conductive layer may also be a barrier layer/refractor metal, such as titanium nitride/tungsten (TiN/W) or tungsten nitride/tungsten (WN_x/W), or it could be formed entirely of tungsten nitride (WN_x).

[0044] Although not shown, the source follower and row select transistors **19**, **16** (FIG. **1**), respectively, can be formed concurrently with and in the same manner as the transfer and reset transistors **317**, **318** as described below. Accordingly, the source follower and row select transistors **19**, **16** may or may not have deuterated gate oxide layers **341***a*.

[0045] Doped p-type wells **334**, **335** are implanted into the substrate **11**, as shown in FIG. **4**H. The first p-well **334** is formed in the substrate **11** surrounding the isolation region

333 and extending below the isolation region 333. The second p-well 335 is formed in the substrate 11 from a point below the transfer gate stack 347 extending in a direction in the substrate 11 away from where the photodiode 23 (FIG. 3) is to be formed. The p-wells 334, 335 are formed by known methods. For example, a layer of photoresist (not shown) can be patterned over the substrate 11 having an opening over the area where the p-wells, 334, 335 are to be formed. A p-type dopant, such as boron, can be implanted into the substrate 11 through the opening in the photoresist. The p-wells 334, 335 are formed having a p-type dopant concentration that is higher than adjacent portions of the substrate 11. Alternatively, the p-wells 334, 335 can be formed prior to the formation of the trench 430.

[0046] As depicted in FIG. 4I, a doped n-type region 21 is implanted in the substrate 11 (for the photodiode 23 of FIG. 3). For example, a layer of photoresist (not shown) may be patterned over the substrate 11 having an opening over the surface of the substrate 11 where photodiode 23 (FIG. 3) is to be formed. An n-type dopant, such as phosphorus, arsenic, or antimony, may be implanted through the opening and into the substrate 11. Multiple implants may be used to tailor the profile of region 21. If desired, an angled implantation may be conducted to form the doped region 21, such that implantation is carried out at angles other than 90 degrees relative to the surface of the substrate 11.

[0047] As shown in FIG. 4I, the n-type region 21 is formed from a point adjacent the transfer gate stack 347 and extending in the substrate 11 between the gate stack 347 and the isolation region 333. The region 21 forms a photosensitive charge accumulating region for collecting photo-generated charge.

[0048] The floating diffusion region 5 and source/drain region 2 are implanted by known methods to achieve the structure shown in FIG. 4I. The floating diffusion region 5 and source/drain region 2 are formed as n-type regions. Any suitable n-type dopant, such as phosphorus, arsenic, or antimony, may be used. The floating diffusion region 5 is formed on the side of the transfer gate stack 347 opposite the n-type photodiode region 21. The source/drain region 2 is formed on a side of the reset gate stack 348 opposite the floating diffusion region 5.

[0049] FIG. 4J depicts the formation of a dielectric layer 307. Illustratively, layer 307 is a deuterated oxide layer, but layer 307 may be any appropriate deuterated dielectric material, such as a deuterated nitride, among others, formed by methods known in the art. Alternatively, the dielectric layer 307 can be formed without deuterium.

[0050] The doped surface layer 22 for the photodiode 23 is implanted, as illustrated in FIG. 4K. Doped surface layer 22 is formed as a highly doped p-type surface layer and is formed to a depth of approximately 0.1 μm. A p-type dopant, such as boron, indium, or any other suitable p-type dopant, may be used to form the p-type surface layer 22.

[0051] The p-type surface layer 22 may be formed by known techniques. For example, layer 22 may be formed by implanting p-type ions through openings in a layer of photoresist. Alternatively, layer 22 may be formed by a gas source plasma doping process, or by diffusing a p-type dopant into the substrate 11 from an in-situ doped layer or a doped oxide layer deposited over the area where layer 22 is to be formed.

[0052] The deuterated oxide layer 307 is etched such that remaining portions form a sidewall spacer on a sidewall of the reset gate stack 348. The layer 307 remains over the transfer gate stack 347, the photodiode 23, the floating diffusion region 5, and a portion of the reset gate stack 348 to achieve the structure shown in FIG. 3. Alternatively, a dry etch step can be conducted to etch portions of the deuterated oxide layer 307 such that only sidewall spacers (not shown) remain on the transfer gate stack 347 and the reset gate stack 348.

[0053] Conventional processing methods can be used to form other structures of the pixel 300. For example, insulating, shielding, and metallization layers to connect gate lines, and other connections to the pixel 300 may be formed. Also, the entire surface may be covered with a passivation layer (not shown) of, for example, silicon dioxide, borosilicate glass (BSG), phosphosilicate glass (PSG), or borophosphosilicate glass (BPSG), which is CMP planarized and etched to provide contact holes, which are then metallized to provide contacts. Conventional layers of conductors and insulators may also be used to interconnect the structures and to connect pixel 300 to peripheral circuitry.

[0054] While the pixel cell 300 is described including multiple deuterated structures, embodiments of the invention include a pixel cell having only one of the deuterated structures and a pixel cell having fewer deuterated structures than are described above in connection with the embodiment of FIG. 3.

[0055] While the above embodiments are described in connection with the formation of p-n-p-type photodiodes the invention is not limited to these embodiments. The invention also has applicability to other types of photo-conversion devices, such as a photodiode formed from n-p or n-p-n regions in a substrate, a photogate, or a photoconductor. If an n-p-n-type photodiode is formed the dopant and conductivity types of all structures would change accordingly.

[0056] Although the above embodiments are described in connection with 4T pixel cell 300, the configuration of pixel cell 300 is only exemplary and the invention may also be incorporated into other pixel circuits having different numbers of transistors. Without being limiting, such a circuit may include a three-transistor (3T) pixel cell, a five-transistor (5T) pixel cell, a six-transistor (6T) pixel cell, and a seven-transistor pixel cell (7T). A 3T cell omits the transfer transistor, but may have a reset transistor adjacent to a photodiode. The 5T, 6T, and 7T pixel cells differ from the 4T pixel cell by the addition of one, two, or three transistors, respectively, such as a shutter transistor, a CMOS photogate transistor, and an anti-blooming transistor.

[0057] A typical single chip CMOS image sensor 500 is illustrated by the block diagram of FIG. 5. The image sensor 500 includes a pixel cell array 580 having one or more pixel cells 300 (FIG. 3) described above. The pixel cells 300 of array 580 are arranged in a predetermined number of columns and rows.

[0058] Referring to FIGS. 3 and 5, in operation, the rows of pixel cells 300 in array 580 are read out one by one. Accordingly, pixel cells 300 in a row of array 580 are all selected for readout at the same time by a row select line, and each pixel cell 300 in a selected row provides a signal representative of received light to a readout line for its column. In the array 580, each column also has a select line, and the pixel cells 300 of each column are selectively read out in response to the column select lines.

[0059] The row lines in the array 580 are selectively activated by a row driver 582 in response to row address decoder 581. The column select lines are selectively activated by a column driver 584 in response to column address decoder

585. The array 580 is operated by the timing and control circuit 583, which controls address decoders 581, 585 for selecting the appropriate row and column lines for pixel signal readout.

[0060] The signals on the column readout lines typically include a pixel reset signal (V_{rst}) and a pixel image signal (V_{photo}) for each pixel cell. Both signals are read into a sample and hold circuit (S/H) 586 in response to the column driver 584. A differential signal (V_{rst}-V_{photo}) is produced by differential amplifier (AMP) 587 for each pixel cell, and each pixel cell's differential signal is digitized by analog-to-digital converter (ADC) 588. The analog-to-digital converter 588 supplies the digitized pixel signals to an image processor 589, which performs appropriate image processing before providing digital signals defining an image output.

[0061] FIG. 6 illustrates a processor-based system 600 including an image sensor 500 of FIG. 5. The processor-based system 600 is exemplary of a system having digital circuits that could include image sensor devices. Without being limiting, such a system could include a computer system, camera system, scanner, machine vision, vehicle navigation, video phone, surveillance system, auto focus system, star tracker system, motion detection system, image stabilization system, and data compression system.

[0062] The processor-based system 600, for example a camera system, generally comprises a central processing unit (CPU) 695, such as a microprocessor, that communicates with an input/output (I/O) device 691 over a bus 693. Image sensor 500 also communicates with the CPU 695 over bus 693. The processor-based system 600 also includes random access memory (RAM) 692, and can include removable memory 694, such as flash memory, which also communicate with CPU 695 over the bus 693. Image sensor 500 may be combined with a processor, such as a CPU, digital signal processor, or microprocessor, with or without memory storage on a single integrated circuit or on a different chip than the processor.

[0063] It is again noted that the above description and drawings are exemplary and illustrate preferred embodiments that achieve the objects, features and advantages of the present invention. It is not intended that the present invention be limited to the illustrated embodiments. Any modification of the present invention which comes within the spirit and scope of the following claims should be considered part of the present invention.

1-44. (canceled)

45. A method of forming a pixel cell, the method comprising the acts of:

forming a photo-conversion device; and

forming at least one structure comprising a deuterated material adjacent the photo-conversion device.

46. The method of claim 45, wherein the act of forming the at least one structure comprises forming an isolation region by forming a trench within the substrate and partially filling the trench with a deuterated material.

47. The method of claim 46, wherein the act of at least partially filling the trench comprises lining the trench with deuterated nitride.

48. The method of claim 47, wherein the deuterated nitride liner is formed having a thickness within the range of approximately 50 Å to approximately 150 Å.

49. The method of claim 47, further comprising the act of forming an oxide liner in the trench.

50. The method of claim 46, wherein the act of at least partially filling the trench comprises lining the trench with deuterated oxide.

51. The method of claim 50, wherein the oxide liner is formed having a thickness within the range of approximately 50 Å to approximately 150 Å.

52. The method of claim 46, further comprising the act of forming a doped well of a first conductivity type in the substrate surrounding the trench.

53. The method of claim 46, further comprising the act of filling the trench with a dielectric material selected from the group consisting of high density plasma, high density plasma, silicon oxide, oxynitride, nitride, and high temperature polymer.

54. The method of claim 46, further comprising implanting deuterium into the substrate at a surface of the substrate within the trench.

55. The method of claim 54, wherein the act of implanting is conducted before the act of at least partially filling the trench.

56. The method of claim 54, wherein the act of implanting deuterium comprises using an implant dose within the range of approximately 1×10^{13} atoms/cm^2 to approximately 1×10^{15} atoms/cm^2.

57. The method of claim 56, wherein the act of implanting deuterium comprises using an implant dose is approximately 2×10^{14} atoms/cm^2.

58. The method of claim 54, wherein he act of implanting deuterium comprises implanting at an energy within the range of approximately 10 keV to approximately 100 keV.

59. The method of claim 58, wherein he act of implanting deuterium comprises implanting at an energy of approximately 40 keV.

60. The method of claim 54, further comprising conducting and an inert anneal after the act of implanting.

61. The method of claim 60, wherein the act of conducting an inert anneal comprises annealing at a temperature within the range of approximately 800° C. to approximately 1000° C.

62. The method of claim 61, wherein the act of conducting an inert anneal comprises annealing at a temperature of approximately 850° C.

63. The method of claim 60, wherein the act of conducting an inert anneal comprises annealing for a time within the range of approximately 10 minutes to approximately 30 minutes.

64. The method of claim 63, wherein the act of conducting an inert anneal comprises annealing for approximately 20 minutes.

65. The method of claim 46, further comprising the act of annealing at a pressure within the range of approximately 1 atm to approximately 5 atm.

66. The method of claim 65, wherein the act of annealing is conducted subsequently to the act of at least partially filling the trench.

67. The method of claim 66, wherein the act of annealing comprises annealing at a pressure of approximately 5 atm.

68. The method of claim 65, wherein the act of annealing comprises annealing at a temperature within the range of approximately 300° C. to approximately 500° C.

69. The method of claim 68, wherein the act of annealing comprises annealing at a temperature of approximately 400° C.

70. The method of claim **65**, wherein the act of annealing comprises annealing for a time within the range of approximately 30 minutes to approximately 120 minutes.

71. The method of claim **70**, wherein the act of annealing comprises annealing for 30 minutes.

72. The method of claim **45**, wherein the act of forming the at least one structure comprises forming a transistor coupled to the photo-conversion device by forming the transistor comprising a deuterated gate oxide layer.

73. The method of claim **45**, wherein the act of forming the at least one structure comprises forming a deuterated dielectric layer over the photo-conversion device.

74. The method of claim **73**, wherein the act of forming deuterated dielectric layer comprises forming the deuterated dielectric layer extending over at least one transistor gate and a floating diffusion region.

75. A method of forming an isolation region, the method comprising:

etching a trench in a substrate; and

partially filling the trench with a deuterated material.

76. The method of claim **75**, wherein the act of partially filling the trench comprises lining the trench with deuterated nitride.

77. The method of claim **76**, wherein the deuterated nitride liner is formed having a thickness within the range of approximately 50 Å to approximately 150 Å.

78. The method of claim **76**, further comprising the act of forming an oxide liner between the deuterated nitride liner and the substrate.

79. The method of claim **75**, wherein the act of partially filling the trench comprises lining the trench with deuterated oxide.

80. The method of claim **79**, wherein the oxide liner is formed having a thickness within the range of approximately 50 Å to approximately 150 Å.

81. The method of claim **75**, further comprising forming a deuterated oxide layer over the substrate prior to etching the trench.

82. The method of claim **81**, further comprising forming a deuterated dielectric layer over the deuterated oxide layer prior to etching the trench.

83. The method of claim **82**, wherein the act of forming the deuterated dielectric layer comprises forming a deuterated nitride layer.

84. The method of claim **75**, further comprising implanting deuterium into the substrate at a surface of the substrate within the trench.

85. The method of claim **84**, wherein the act of implanting is conducted before partially filling the trench.

86. The method of claim **84**, wherein the act of implanting deuterium comprises using an implant dose within the range of approximately 1×10^{13} atoms/cm^2 to approximately 1×10^{15} atoms/cm^2.

87. The method of claim **86**, wherein the act of implanting deuterium comprises using an implant dose is approximately 2×10^{14} atoms/cm^2.

88. The method of claim **84**, wherein he act of implanting deuterium comprises implanting at an energy within the range of approximately 10 keV to approximately 100 keV.

89. The method of claim **88**, wherein he act of implanting deuterium comprises implanting at an energy of approximately 40 keV.

90. The method of claim **84**, further comprising conducting and an inert anneal after the act of implanting.

91. The method of claim **90**, wherein the act of conducting an inert anneal comprises annealing at a temperature within the range of approximately 800° C. to approximately 1000° C.

92. The method of claim **91**, wherein the act of conducting an inert anneal comprises annealing at a temperature of approximately 850° C.

93. The method of claim **90**, wherein the act of conducting an inert anneal comprises annealing for approximately 10 minutes to approximately 30 minutes.

94. The method of claim **93**, wherein the act of conducting an inert anneal comprises annealing for approximately 20 minutes.

95. The method of claim **75**, further comprising the act of annealing at a pressure within the range of approximately 1 atm to approximately 5 atm.

96. The method of claim **95**, wherein the act of annealing is conducted subsequently to the act of at least partially filling the trench.

97. The method of claim **95**, wherein the act of annealing comprises annealing at a pressure of approximately 5 atm.

98. The method of claim **97**, wherein the act of annealing comprises annealing at a temperature within the range of approximately 300° C. to approximately 500° C.

99. The method of claim **98**, wherein the act of annealing comprises annealing at a temperature of approximately 400° C.

100. The method of claim **95**, wherein the act of annealing comprises annealing for a time within the range of approximately 30 minutes to approximately 120 minutes.

101. The method of claim **100**, wherein the act of annealing comprises annealing for 30 minutes.

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