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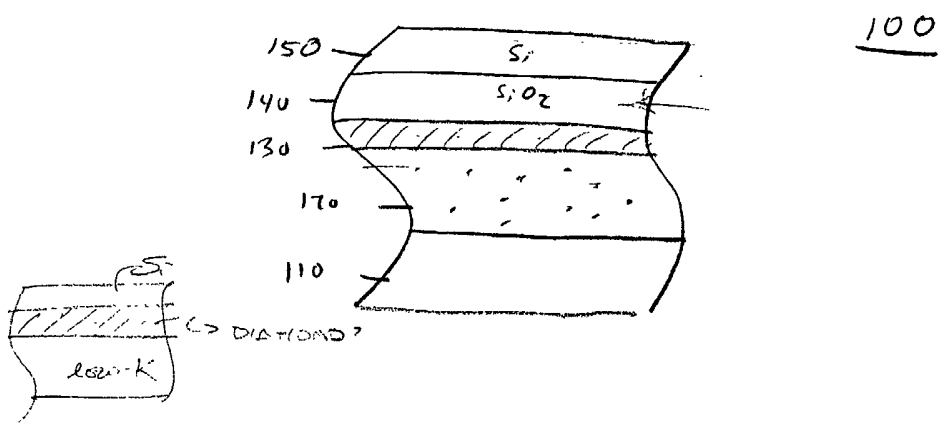
(54) Title: SPECIALIZED SUBSTRATES FOR USE IN SEQUENTIAL LATERAL SOLIDIFICATION PROCESSING



(57) Abstract: Substrates having modified effective thermal conductivity for use in the sequential lateral solidification process are disclosed. In one arrangement, a substrate includes a glass base layer, a low conductivity layer formed adjacent to a surface of the base layer, a high conductivity layer formed adjacent to the low conductivity layer, a silicon compound layer formed adjacent to the high conductivity layer, and a silicon layer formed on the silicon compound layer. In an alternative arrangement, the substrate includes an internal subsurface melting layer which will act as a heat reservoir during subsequent sequential lateral solidification processing.

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SPECIALIZED SUBSTRATES FOR USE IN SEQUENTIAL LATERAL SOLIDIFICATION PROCESSING

SPECIFICATION

BACKGROUND OF THE INVENTION

I. Field of the invention.

The present invention relates to techniques for processing of semiconductor films, and more particularly to techniques for processing semiconductor films on glass or other substrates.

II. Description of the related art.

Techniques for fabricating large grained single crystal or polycrystalline silicon thin films using sequential lateral solidification are known in the art. For example, in U.S. Patent Application Serial No. 09/390,537, the contents of which are incorporated by reference herein and which application is assigned to the common assignee of the present application, particularly advantageous apparatus and methods for growing large grained polycrystalline or single crystal silicon structures using energy-controllable laser pulses and small-scale translation of a silicon sample to implement sequential lateral solidification are disclosed. Using the sequential lateral solidification technique, low defect density crystalline silicon films can be produced on those substrates that do not permit epitaxial regrowth, upon which high performance microelectronic devices can be fabricated.

The effectiveness with which sequential lateral solidification can be implemented depends on several factors, the most important of which corresponds to the length of lateral crystal growth achieved per laser pulse. Such lateral crystal growth depends on several parameters, including the duration of the laser pulses, film thickness, substrate temperature at the point of laser pulse irradiation, the energy density of the laser pulse incident on the substrate, and the effective thermal conductivity of the substrate.

In particular, if all other factors are kept constant, reducing the thermal conductivity of the substrate will have the effect of increasing lateral crystal growth.

While there have been attempts to utilize low thermal conductivity materials, such as porous glass, in connection with sequential lateral solidification for the purpose of enhancing lateral crystal growth, such attempts have not achieved commercially viable results. For example, when a porous glass layer is used under a silicon film in the sequential lateral solidification process densification, and subsequent physical distortion, of such glass has been observed. Accordingly, there exists a need in the art for a technique for fabricating substrates having a modified effective thermal conductivity in order to optimize the sequential lateral solidification process.

SUMMARY OF THE INVENTION

An object of the present invention is to provide substrates having modified effective thermal conductivity which can be later used in an optimized sequential lateral solidification process.

A further object of the present invention is to provide substrates having modified effective thermal conductivity.

Still a further object of the present invention is to provide substrates having a directionally optimized effective thermal conductivity.

Yet a further object of the present invention is to provide multi layer substrates where one or more of the subsurface layers act as a heat reservoir in order to optimize the effective thermal characteristics of the substrate.

In order to achieve these objectives as well as others that will become apparent with reference to the following specification, the present invention provides a substrate having modified effective thermal conductivity for use in the sequential lateral solidification process. The substrate includes a base layer, e.g., glass, a low conductivity layer formed adjacent to a surface of the base layer, a high conductivity layer formed adjacent to the low conductivity layer, and a silicon layer formed on the high conductivity layer.

In a preferred arrangement, the low conductivity layer is porous glass, and is in the range of 5,000 Angstroms to 2 microns thick. The high conductivity layer may

be a metal, and should be sufficiently thin so as to not increase the overall vertical conductivity of the substrate, preferably in the range of 50 to 5,000 Angstroms thick.

An intermediate silicon compound layer is preferably formed between the silicon layer and the high conductivity layer. The silicon compound may be silicon dioxide, and should be sufficiently thick to prevent diffusion of impurities from the high conductivity layer. It is preferred that the silicon compound layer is in the range of 200 to 2,000 Angstroms thick.

In an alternative arrangement, the present invention provides a substrate having modified effective thermal conductivity for use in the sequential lateral solidification process, wherein the high conductivity layer is replaced by an internal subsurface melting layer. In this arrangement, the substrate includes a base layer, a low conductivity layer formed adjacent to the base layer, a subsurface melting layer having a melting point which is less than that of silicon and formed adjacent to the low conductivity layer, a silicon compound layer formed adjacent to the subsurface melting layer, and silicon layer formed on the silicon compound layer.

The accompanying drawings, which are incorporated and constitute part of this disclosure, illustrate a preferred embodiment of the invention and serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram of a substrate in accordance with a preferred embodiment of the present invention;

Fig. 2 is an illustrative diagram showing lateral solidification of silicon;

Figs. 3a and b are graphs showing the relationship between the temperature of solidifying silicon and the position of such silicon around a liquid to solid interface; and

Fig. 4 is a schematic diagram of a substrate in accordance with a second preferred embodiment of the present invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to Fig. 1, a preferred embodiment of the present invention will be described. As shown in Fig. 1, the substrate 100 includes a bulk glass plate layer 110, a low conductivity layer 120, a high conductivity layer 130, a silicon dioxide layer 130 and a semiconducting film layer 150. The multilayer structure of substrate 100 may be fabricated by any combination of thin film formation techniques, such as physical or chemical vapor deposition, electrochemical deposition, or spin coating.

The low conductivity layer 120 may be porous glass or a polymer film layer. In addition, the layer 120 must have a conductivity which is less than the glass plate 110 and sufficiently thick so that the glass plate layer 110 will not participate when the substrate 100 is used in later processing. Layer 120 will be in the order of 5,000 Angstroms to 2 microns thick.

The high conductivity layer 130 may be a metallic layer such as copper or aluminum. The high conductivity layer must have a conductivity which is greater than that of the glass plate 110, and sufficiently thin so as to not increase the overall vertical conductivity of the substrate 100, i.e., conductivity in the direction which crosses layers 110, 120, 130, 140, 150. Typically, layer 130 will be in the order of 50 to 5,000 Angstroms thick.

The silicon dioxide layer 140 should be sufficiently thick to prevent potential diffusion of unwanted impurities from the underlying layer 130 to the silicon cap 150. The Layer 140 will be in the order of 200 to 2,000 Angstroms thick. Alternatively, the layer 140 may be fabricated from silicon nitride or a mixture of silicon dioxide and silicon nitride.

Alternatively, the high conductivity layer 130 may be formed from a material which is electrically and chemically compatible with the semiconducting film layer 150, such as diamond. In this case, the silicon dioxide layer 140 may be omitted, with the semiconducting film layer 150 formed directly on the high conductivity layer 130.

Finally, the top semiconducting film layer may be either be amorphous, microcrystalline or polycrystalline silicon, or a mixture thereof. Typically, layer 150 will be in the order of 200 to 2,000 Angstroms thick.

When fabricated as described above, the substrate 100 will exhibit either a reduced overall effective thermal conductivity, or a reduced effective thermal conductivity in the vertical direction. Having such a modified thermal conductivity, the substrate 100 is highly useful in order to improve lateral crystal growth in the lateral solidification process, as will be now described.

Referring next to Fig. 2, the lateral solidification of silicon in accordance with the above-noted sequential lateral solidification technique is illustrated. Fig. 2 represents a cross sectional view of the silicon film 150 as it may appear during lateral solidification, with liquid silicon 210 solidifying into crystalline silicon 220 at a velocity Vg. As the liquid silicon solidifies through the motion of the interface 230, latent heat is released at the interface 230 due to reduction in enthalpy associated with the liquid to solid transition. The lateral solidification will continue along moving boundary 230 until either impingement of the interface with another similar interface, or until nucleation.

Referring next to Fig. 3a, a graphs showing the relationship between the temperature of solidifying silicon and the position of such silicon around a liquid to solid interface is shown, where T_{bulk} represents the temperature of the bulk liquid silicon as it cools, T_{int} represents the temperature of the silicon as the interface 230, and T_{mp} represents the melting temperature of silicon. As those skilled in the art will appreciate, the temperature of T_{int} will impact the growth rate of the forming crystal, with a lower temperature leading to a faster growth rate. Likewise, when T_{bulk} reaches a certain temperature range, random nucleation will commence, ceasing the crystal growth process.

Referring to Fig. 3b, two possible temperature profiles for solidifying silicon are shown, at a time t after laser irradiation. The temperature profile 310 represents a poor temperature profile, as the high interface temperature will cause slow lateral solidification, and the low temperature in the region away from the interface 230 will cause the temperature of those regions of liquid silicon to drop below the nucleation temperature range, ΔT_N. In contrast the temperature profile 320 represents a optimal temperature profile, with a lower interface temperature causing more rapid lateral solidification, and a less cooling in the liquid silicon away from the interface 230 such

that the temperature remains above the nucleation temperature range for a loner time.

Referring next to Fig. 4, a substrate in accordance with a second preferred embodiment of the present invention is now described. As shown in Fig. 4, the substrate 400 includes a bulk glass plate layer 410, a low conductivity layer 420, a subsurface melting layer 430, a silicon dioxide layer 430 and a semiconductor layer 450 made from a predetermined semiconductor material. The low conductivity layer 420, a silicon dioxide layer 430 and semiconductor layer 450 may be fabricated as described above in connection with substrate 100 by any combination of thin film formation techniques, such as physical or chemical vapor deposition, electrochemical deposition, or spin coating.

The subsurface melting layer 430 must have a melting point which is less than or equal to that of the predetermined semiconductor material, and preferably should exhibit an increased conductivity after melting. In addition, it is highly preferable to use a material having a high latent heat for the melting layer 430, such as a Silicon Germanium alloy. A 1000 Angstrom thick layer of Silicon Germanium alloy would be suitable for melting layer 430. Alternatively, an approximately 1000 Angstrom thick layer of certain metals such as Aluminum or Copper could be used for melting layer 430.

When fabricated as described above, the substrate 400 will exhibit either a reduced overall effective thermal conductivity, or a reduced effective thermal conductivity in the vertical direction. When used in the sequential lateral solidification process, the melting layer 430 will partially or completely melt, thereby storing heat. Later, as the melting layer solidifies, heat will be released through the phase transformation from liquid to solid, thereby preventing rapid cooling of the overlying silicon layer 450, and delaying nucleation. Thus, as shown in Fig. 3b, the solidification of the melting layer 430 will have the effect of moving the temperature profile of the solidifying silicon layer up from profile 310 to profile 320 in the regions away from the boundary 230. With such a modified thermal conductivity, the substrate 400 is likewise highly useful in order to improve lateral crystal growth in the lateral solidification process.

The foregoing merely illustrates the principles of the invention. Various modifications and alterations to the described embodiments will be apparent to those

skilled in the art in view of the teachings herein. For example, the silicon layer 150, 450 may be replaced by other semiconductors such Germanium, Silicon Germanium, Gallium Arsenide, or Gallium Nitride, with, in the case of the second embodiment, suitable modifications to the melting layer 430. Likewise, other metals may be used for the high conductivity layer 130. Moreover, the high and low conductivity layers may be either a single unitary layer, or consist of multiple sub-layers. It will thus be appreciated that those skilled in the art will be able to devise numerous systems and methods which, although not explicitly shown or described herein, embody the principles of the invention and are thus within the spirit and scope of the invention.

CLAIMS

1. A substrate having modified effective thermal conductivity for use in the sequential lateral solidification process, comprising:

(a) a base layer having a base layer conductivity and at least a top surface;

(b) a low conductivity layer having a conductivity which is less than said base layer conductivity, a first side and a second side, said low conductivity layer first side formed adjacent to said top surface of said base layer;

(c) a high conductivity layer having a conductivity which is greater than said base layer conductivity, a first side and a second side, said high conductivity layer first side formed adjacent to said second side of said low conductivity layer; and

(d) a semiconductor layer formed on said second side of said high conductivity layer.

2. The substrate of claim 1, wherein said low conductivity layer comprises porous glass.

3. The substrate of claim 2, wherein said low conductivity layer is in the range of 5,000 Angstroms to 2 microns thick.

4. The substrate of claim 1, wherein said high conductivity layer comprises a metal.

5. The substrate of claim 4, wherein said high conductivity layer is sufficiently thin so as to not increase the overall vertical conductivity of said substrate.

6. The substrate of claim 4, wherein said high conductivity layer is in the range of 50 to 5,000 Angstroms thick.

7. The substrate of claim 1, further comprising a silicon compound layer having said predetermined silicon compound conductivity, a first side and a second side, wherein said silicon compound layer first side is formed adjacent to said second side of said high conductivity layer and said semiconductor layer is formed on said second side of said silicon compound layer.

8. The substrate of claim 7, wherein said silicon compound comprises silicon dioxide, and said silicon compound layer is sufficiently thick to prevent diffusion of impurities from said high conductivity layer.

9. The substrate of claim 8, wherein said silicon compound layer is in the range of 200 to 2,000 Angstroms thick.

10. The substrate of claim 1, wherein said base layer comprises glass.

11. A substrate having modified effective thermal conductivity for use in the sequential lateral solidification process, comprising:

(a) a base layer having a base layer conductivity and at least a top surface;

(b) a low conductivity layer having a conductivity which is less than said base layer conductivity, a first side and a second side, said low conductivity layer first side formed adjacent to said top surface of said base layer;

(c) a subsurface melting layer having a melting point which is less than or equal to that of a predetermined semiconductor material, a first side and a second side, said subsurface melting layer first side formed adjacent to said second side of said low conductivity layer;

(d) a silicon compound layer having a first side and a second side, said silicon compound layer first side formed adjacent to said second side of said subsurface melting layer; and

(e) a semiconductor layer comprising said predetermined semiconductor material and formed on said second side of said silicon compound layer.

12. The substrate of claim 11, wherein said low conductivity layer comprises porous glass.

13. The substrate of claim 12, wherein said low conductivity layer is in the range of 5,000 Angstroms to 2 microns thick.

14. The substrate of claim 11, wherein said melting layer exhibits an increased conductivity after melting.

15. The substrate of claim 11, wherein said melting layer comprises a material having a high latent heat.

16. The substrate of claim 15, wherein said melting layer comprises Silicon Germanium.

17. The substrate of claim 16, wherein said melting layer is approximately 1000 Angstroms thick.

18. The substrate of claim 11, wherein said silicon compound comprises silicon dioxide, and said silicon compound layer is sufficiently thick to prevent diffusion of impurities from said melting layer.

19. The substrate of claim 18, wherein said silicon compound layer is in the range of 200 to 2,000 Angstroms thick.

20. The substrate of claim 11, wherein said base layer comprises glass.

Fig 1

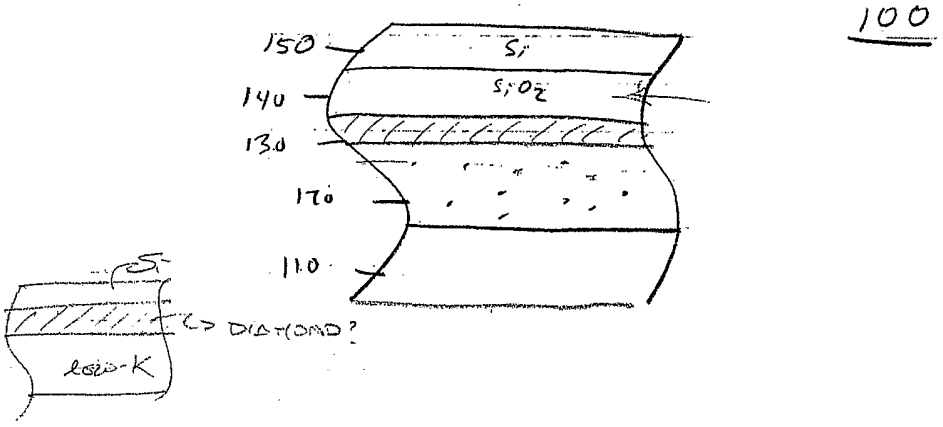


Fig 2

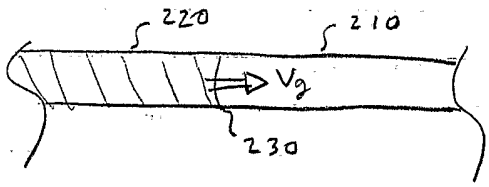


Fig. 3a

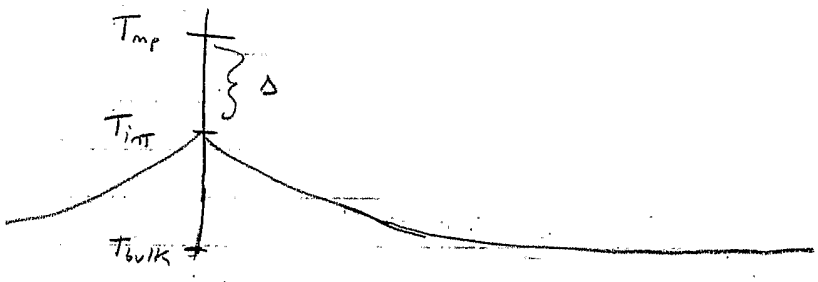


Fig 3b

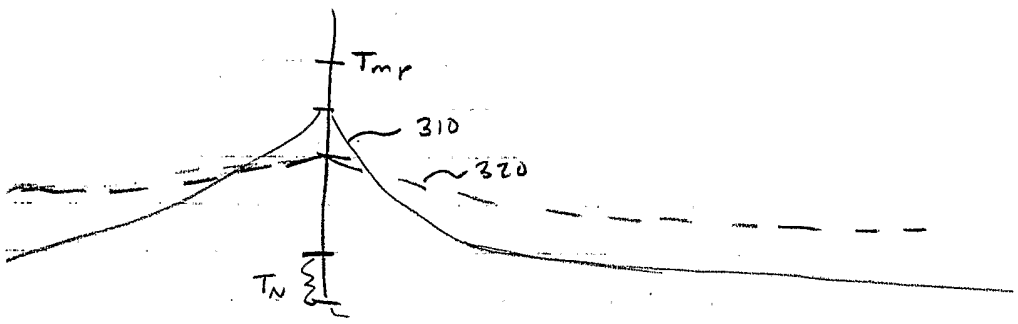
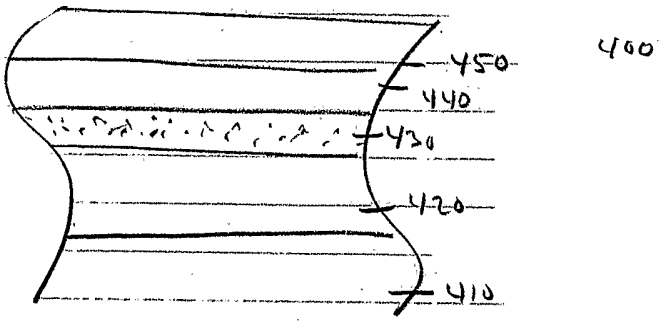


Fig 4



INTERNATIONAL SEARCH REPORT

Inte tional Application No
PCT/US 01/44563

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L C30B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 639 277 A (HAWKINS GILBERT A) 27 January 1987 (1987-01-27) the whole document	1,4,5,7, 8,11,15, 18
A		2,3,6,9, 12
X	PATENT ABSTRACTS OF JAPAN vol. 012, no. 024 (E-576), 23 January 1988 (1988-01-23) & JP 62 181419 A (NEC CORP), 8 August 1987 (1987-08-08) abstract	1,4,5,7, 8,10,11, 15,18,20
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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
19 August 2002	05/09/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Le Meur, M-A

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INTERNATIONAL SEARCH REPORT

Inte tional Application No
PCT/US 01/44563

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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Form PCT/ISA/210 (continuation of second sheet) (July 1992)

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Information on patent family members

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