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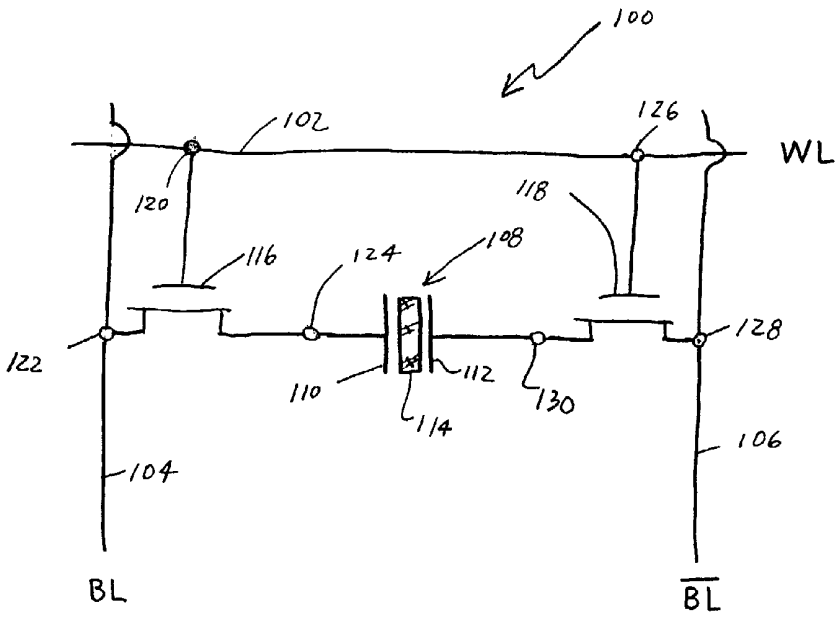
(54) Title: STATIC 2T-1C FERROELECTRIC MEMORY



(57) Abstract: The ferroelectric memory cell (100, 300) includes first and second switches (116, 316, 118, 318), typically transistors, which are electrically configured to interconnect the ferroelectric capacitor (108, 308) to a bit line (104, 304) and a complimentary bit line (106, 306). The switches conduct when an associated word line (102, 302) is energized, and isolate when the word line is not energized. When the word line is energized, the bit line and complimentary bit line share charge from the capacitor. A memory structure (200) using a plurality of the inventive memory cells is also disclosed, as is one specific example of a memory structure fabricated using integrated circuit technology. The inventive cell can improve memory density while exhibiting the property of non-volatility.

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CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of United States Provisional application serial number 60/258,391 filed December 27, 2000.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to the electrical and electronic arts, and more particularly relates to a nonvolatile ferroelectric memory cell and memory structure.

Brief Description of the Prior Art

Static memories are used both for data storage within microprocessors, as well as stand-alone storage devices. A single memory cell of such a device, shown in figure 1, and designated generally as 10, is typically formed with 6 CMOS transistors 12, 14, 16, 18, 20, 22. Transistors 14, 16, 18, 20 form a pair of cross-coupled inverters, while transistors 12 and 22 serve as access transistors which become conductive when the word line 24 is raised in voltage. They then serve to connect the flip-flop formed by the cross-coupled inverters to the bit line 26 and complimentary bit line 28. Devices using this type of cell are well-known in the prior art, for example, they are discussed at pages 960-962 of the book Microelectronic Circuits by Sedra and Smith (3rd Edition 1991, Oxford University Press).

While devices utilizing such memory cells have the advantage that read operations are nondestructive, and refreshing is not required as it is with DRAM, it is still necessary that the memory cells be constantly connected to a voltage supply in order to preserve the data. Further, the density is low due to the fact that 6 transistors

are required to store a single bit of data. The SRAM does, however, have the advantages of low power and stability (low noise).

One alternative to SRAM is to take advantage of ferroelectric materials. As shown in figure 2, this can be done by forming a memory cell 30 similar to a DRAM cell, having a FET 32 and a capacitor 34. The capacitor 34 includes a ferroelectric material 36 as the dielectric between its plates. The gate of the transistor 32 is connected to a word line 38, while one of the (interchangeable) source and drain terminals is connected to the bit line 40. Unlike DRAM, FRAM is non-volatile and will therefore retain data when power is turned off. It is also capable of achieving high density. However, it suffers from high power consumption and is noisy, due to interference from adjacent cells.

There is, therefore, a need in the prior art for a non-volatile RAM cell which can improve memory density.

SUMMARY OF THE INVENTION

The present invention, which addresses the needs identified in the prior art, provides a memory cell which is configured for interconnection with a word line, a bit line, and a complementary bit line. The cell includes a capacitor, a first switch, and a second switch. The capacitor has first and second plates with a ferroelectric material located between them. The first and second switches are electrically interconnected with the word line, the bit lines, and the plates of the capacitor, and are configured such that they cause the bit lines to share charge from the capacitor when the switches are activated by a control signal on the word line.

The present invention also provides a non-volatile memory structure, which includes a plurality of word lines, a plurality of bit lines, and a plurality of complimentary bit lines. The non-volatile memory structure further includes a plurality of memory cells

of the type just described which are located at a plurality of cell locations. Each of the complimentary bit lines is associated with a corresponding one of the bit lines to form a plurality of bit line pairs, and the bit line pairs are positioned so as to intersect the word lines at the plurality of cell locations.

Another aspect of the present invention includes a specific structure for the non-volatile memory. The structure includes a semiconductor substrate, a plurality of word lines, a plurality of bit lines and a plurality of complimentary bit lines. The word lines are formed outward of the substrate, the bit lines are formed outward of the word lines, and the complimentary bit lines are also formed outward of the word lines. Each of the complimentary bit lines is associated with a corresponding one of the bit lines to form a plurality of bit line pairs, which are positioned so as to intersect the word lines at a plurality of cell locations.

The structure further includes a plurality of capacitors and a plurality of field effect transistors. The capacitors each include a first conductive plate spaced outward of the substrate, a second conductive plate spaced outward of the first conductive plate, and a ferroelectric material located between the first and second plates. Each of the field effect transistors includes a first drain/source region formed in the substrate and a second, shared drain/source region formed in the substrate. The first and second drain/source regions are separated by a region of the substrate which is adjacent to a portion of a corresponding one of the word lines, and the portion functions as a gate electrode.

The structure yet further includes a plurality of bit line contacts, a plurality of electrodes, and a plurality of counter electrodes. The bit line contacts extend between the second, shared drain/source regions of the plurality of field effect transistors and corresponding ones of the bit lines and the complementary bit lines. The electrodes extend between the first plates of the plurality of capacitors and corresponding ones of

the first drain/source regions of the plurality of field effect transistors. The plurality of counter electrodes in turn each include a transverse strap and a counter electrode contact. The transverse strap runs from one of the second conductive plates of the plurality of capacitors, substantially parallel to the substrate, in a direction substantially parallel to the word lines. The counter electrode contact extends outwardly from another corresponding one of the first drain/source regions of the plurality of field effect transistors, and is electrically interconnected with the transverse strap.

Each of the plurality of capacitors, together with that pair of the field effect transistors which are connected to the first and second plates of that capacitor, forms a memory cell at a corresponding one of the cell locations of the structure. The second shared drain/source regions of the plurality of field effect transistors are shared between adjacent ones of the field effect transistors which are associated with the same one of the bit lines. The adjacent field effect transistors are in different ones of the memory cells.

For a better understanding of the present invention, together with other and further features and advantages, reference should now be had to the following description, taken in conjunction with the accompanying drawings, and the scope of the invention will be pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a view of a 6 - transistor CMOS SRAM memory cell in accordance with the prior art;

Figure 2 is a view of a DRAM - type FeRAM cell in accordance with the prior art;

Figure 3 is a schematic view of a 2 transistor, 1 capacitor FeRAM cell in accordance with the present invention;

Figure 4 is a top plan view of one form of memory structure in accordance with the present invention, wherein certain hidden lines have been rendered as solid lines for purposes of illustrative convenience;

Figure 5 is a cross-sectional view of the memory structure of figure 4 taken along line V - V thereof;

Figure 6 is a cross-sectional view of the memory structure of figure 4 taken along line VI - VI thereof;

Figure 7 is a schematic view of a memory structure in accordance with the present invention including appropriate control and sensing circuitry;

Figure 8 is a view of the wave fronts for various signals associated with the memory cell of figure 3; and

Figure 9 is a depiction of a memory cell in accordance with the present invention which is similar to that shown in figure 3, but which employs BJTs as the switching elements.

DETAILED DESCRIPTION OF THE INVENTION

Reference should now be had to figure 3, which depicts a memory cell 100 in accordance with the present invention, which is configured for interconnection with a word line 102, a bit line 104 and a complimentary bit line 106. The cell includes a capacitor 108 having a first plate 110, a second plate 112, and a ferroelectric material 114 located between the first and second plates. The memory cell further includes a first switch 116 and a second switch 118. The first and second switches 116, 118 are electrically interconnected with the word line 102, the bit lines 104, 106, and the plates 110, 112 of the capacitor 108, and are configured so as to cause the bit lines 104, 106 to share charge from the capacitor 108 when the switches 116, 118 are activated by a control signal on the word line 102.

As shown in figure 3, the switches are field effect transistors (FETs). However, as will be discussed below, the switches can also be binary junction transistors (BJTs). Indeed, any kind of appropriate switching device can be used to construct the memory cell in accordance with the present invention. It is, however, believed that field effect transistors are preferable.

Still with reference to figure 3, the first switch 116 can have a control terminal 120 which is electrically interconnected with the word line 102, and a first conduction terminal 122 which is electrically interconnected with the bit line 104. First switch 116 can still further have a second conduction terminal 124. The second switch 118 can have a control terminal 126 which is electrically interconnected with the word line 102, a first conduction terminal 128 which is electrically interconnected with the complimentary bit line 106 and a second conduction terminal 130. The first plate 110 of the capacitor 108 can be electrically interconnected with the second conduction terminal 124 of the first switch 116. The second plate 112 of the capacitor 108 can be electrically interconnected with the second conduction terminal 130 of the second switch 118.

As noted, the switches 116, 118 can be formed from FETs. In this case, the control terminals 120, 126 can be gate terminals, and the conduction terminals 122, 124, 128, 130 can be drain/source terminals. The terminals are referred to as drain/source terminals since the FETs can be configured to conduct in either direction in the memory cell 100 depicted in figure 3.

Preferably, the ferroelectric material 114 can be selected, and the capacitor 108 can be sized, such that sufficient charge can be shared with the bit line 104 and the complimentary bit line 106 during a READ operation without requiring a refresh operation. The ferroelectric material can have a dielectric constant which ranges approximately from a lower value to an upper value. Preferably, the lower value can be about 150. Further, preferably, the upper value can be about 3000. Preferably,

capacitor 108 can have a capacitance which ranges approximately from a lower value to an upper value. The lower value can preferably be about 30 femtofarrads. Further, the upper value can preferably be about 50 femtofarrads.

Any appropriate material which exhibits ferroelectric properties can be used for the ferroelectric material 114. At present, three different compounds are believed to be preferable; these include: $BaTiO_3$, $SrTiO_3$, and $Pb(Zr,Ti)O_3$.

Reference should now be had to figure 7. Figure 7 depicts a non-volatile memory structure, designated generally as 200, formed in accordance with the present invention. Structure 200 includes a memory array 202. The array includes a plurality of word lines 102 and a plurality of bit lines 104. A plurality of complimentary bit lines 106 are also included. Each complimentary bit line 106 is associated with a corresponding one of the bit lines 104 to form a plurality of bit line pairs. The bit line pairs intersect the word lines 102 at a plurality of cell locations 204. It will be appreciated that, for purposes of illustrative convenience, 8 bit line pairs and 5 word lines have been depicted in figure 7. Further, 40 cell locations have been depicted in figure 7, of which 8 have been labeled. It should be appreciated that any desired number of word lines and bit line pairs can be provided, to form any desired number of cell locations. A plurality of memory cells of the type described above are located at the plurality of cell locations 204.

Still referring to figure 7, memory structure 200 can include a word decoder/word line driver 206 which is electrically interconnected with the plurality of word lines 102 and which is electrically configured to provide a signal to a given one of the word lines 102 which is sufficient to activate those of the switches 116, 118 which are electrically interconnected to that one of the word lines 102. Structure 200 can further include a bit line controller 208 which is electrically interconnected with the plurality of bit line pairs formed by bit lines 104 and complimentary bit lines 106. The bit line controller 208 can,

in turn, include a bit line selector assembly 210 which is configured to select a given one of the bit line pairs, and a plurality of sense amplifiers 212 which are configured to sense voltage differential between the bit line pairs formed by bit lines 104 and complimentary bit lines 106, in a READ operation, and further to apply a voltage differential greater than the coercive voltage of the dielectric material 114 to the bit line pairs during a WRITE operation. The bit line controller 208 can further include a voltage generator 214 which is associated with the plurality of sense amplifiers 212. The voltage generator 214 can further include a charge pump 216 which is suitable for providing the aforementioned voltage which is greater than the coercive voltage.

Still referring to figure 7, the bit line selector assembly 210 can, if desired, include a plurality of individual bit line selectors 218, which can be in the form of multiplexers. In one exemplary configuration, each multiplexer can be connected on one side to four bit line pairs and on the other side to one of the sense amplifiers 212. It should be appreciated that only two sense amplifiers 212 and two bit line selectors 218 are shown in figure 7 for illustrative convenience, but as many as desired can be included. An appropriate data output device 220 can also be provided if desired. Most of the control circuitry for the array 202 depicted in figure 7 is conventional in nature, and is described, for example, in the aforementioned reference by Sedra and Smith in section 13.9 at pages 956-965, and in other well known reference materials. The purpose of charge pump 216 of voltage generator 214 is twofold. First, it provides a relatively high write voltage for the ferroelectric capacitors 108; essentially, a step function voltage to overcome the critical voltage of the ferroelectric material 114. Further, it will be appreciated that it would normally be wasteful of power to have the sense amplifiers 212 turned on at all times. Accordingly, the sense amplifiers 212 can be pre-charged before a sensing operation, that is, they can preferably be turned on only at such time as they are going to be connected to a given bit line pair through one

of the multiplexer bit line selectors 218. In contrast to a conventional DRAM, no restore of the data is needed after the READ operation, because of the use of the ferroelectric capacitors 108. The charge in the capacitor 108 will remain at the remnant polarization, and thus, each memory cell 100 is non-volatile.

Reference should now be had to figure 9 which depicts a form of memory cell similar to that depicted in figure 3, but employing BJTs instead of FETs. Elements in figure 9 similar to those in figure 3 have received the same reference character, incremented by 200. In the cell depicted in figure 9, the switches 316, 318 are BJTs, the control terminals 320, 326 are base terminals of the BJTs, and the conduction terminals 322, 324, 328, 330 are emitter/collector terminals. As depicted in figure 9, conduction terminals 322, 328 coupled to bit line 304 and complimentary bit line 306 are shown as collector terminals, while conduction terminals 324, 330 coupled to plates 310, 312 of capacitor 308 respectively are shown as emitter terminals. It will be appreciated that it is necessary to have current flow in both directions through BJT switches 316, 318, and accordingly, it will be necessary for the switches 316, 318 to operate in an inverse mode where the emitter and collector functions are reversed. It should be appreciated that while npn transistors are shown in figure 9, pnp transistors can also be used. It should be noted that the use of BJTs in the inverse or reverse mode is well known in digital logic circuits, as discussed, for example, in the aforementioned reference by Sedra and Smith at pages 995-996.

It should be appreciated that a BJT cell of the type shown in figure 9 could also be incorporated into a memory structure of the type shown in figure 7, by locating a suitable BJT cell at every one of the cell locations 204. Any required modifications to the control circuitry would be clear to those of skill in the electronics art.

Reference should now be had to figure 8, which depicts the wave fronts for various signals during read and write operations on the inventive memory structure.

Reference should also be had to figures 3 and 7. The top waveform in figure 8 shows the clock signal. Next, labeled BL, BLB are the bit line and complimentary bit line voltages. After that, labeled BLS, is the bit line select voltage, which is used to control connection of the bit line pair to the sense amplifier 212 through an appropriate multiplexer 218. Next, labeled SAEQ, is the voltage to equalize the bit lines for the sense amplifier. Following that, labeled SAEN, is the voltage for enabling the sense amplifier 212. Finally, labeled D, DB are the output data and complimentary output data. For BL, BLB and D, DB, it will be appreciated that the true data appears on the top and the complimentary data appears on the bottom.

First, during the READ operation, a voltage is applied to the word line 102 at the first vertical dash-dot line, causing the switches 116, 118 to become conductive. As this happens, the bit line and complimentary bit line experience a gradually increasing voltage differential (or differential voltage) due to charge sharing from the plates of the capacitor 110, 112. When the BLS voltage is high, the given bit line pair is connected to the appropriate sense amplifier 212 through the multiplexer 218. Prior to this, the given sense amplifier 212 is equalized and ready for the sensing operation. During the sensing operation, the sense amplifier will sense and amplify the differential signal to provide a rail to rail signal level. When the SAEN voltage is high, the sense amplifier is turned off, and the data and complimentary data simply track the bit line data. After the second vertical dash-dot line, the sense amplifier is enabled by the sense amplifier voltage going low, which causes the voltage initially present on the bit line and complimentary bit line to be amplified and output on the data and complimentary data lines. The BL and BLB differential returns to zero under the influence of the SAEQ signal as the bit line pair is deselected when the BLS signal goes low. The word line is also de-energized and the desired data is read as the D, DB signal in data output module 220. At the third vertical dash-dot line, the equalization signal is turned off, as

is the sense amplifier, and the differential between the data and complimentary data signals returns to zero. Then, at the fourth vertical dash-dot line, the write operation commences. As the word line voltage is again increased, charge sharing from the capacitor causes the bit line and complimentary bit line voltage differential to rise. During the WRITE (between the fourth and fifth dash-dot lines), the sense amplifier is first equalized by SAEQ and then the outside signal charges up the bit lines. Between the fifth and sixth dash-dot lines, a large voltage differential is applied between the bit line and complimentary bit line to overcome the remanence of the ferroelectric material 114 between the plates of the capacitor. The BLS signal goes high so that this voltage can be applied to the bit line pair through the sense amplifier from the charge pump 216. The SAEN signal goes low so that the sense amplifier 212 can function to apply the high voltage differential. Between the fifth and sixth vertical dash-dot lines, the sense amplifier is powered by the SAEN at a boosted voltage and writes to the cell. Finally, after the sixth vertical dash-dot line, the word line voltage goes low, isolating the bit line and complimentary bit line from the capacitor 108. The bit line is no longer connected to the sense amplifier and the internal nodes of the sense amplifier are equalized when the SAEN signal goes high.

Reference should now be had to figures 4, 5 and 6 which depict one exemplary form of non-volatile memory structure in accordance with the present invention. The structure includes a semiconductor substrate 150, and a plurality of word lines 102 are formed outwardly of the substrate 150. Also included are a plurality of bit lines 104 formed outwardly of the word lines 102, and a plurality of complimentary bit lines 106 also formed outwardly of the word lines 102. Each of the complimentary bit lines 106 is associated with a corresponding one of the bit lines 104 to form a plurality of bit line pairs. The bit line pairs are positioned so as to intersect the word lines 102 at a plurality of cell locations. Also included in the non-volatile memory structure are a

plurality of capacitors 108. Each capacitor in turn includes a first conductive plate 110 spaced outward of the substrate 150, a second conductive plate 112 spaced outward of the first conductive plate 110, and a ferroelectric material 114 located between the first and second plates 110, 112.

The memory structure further includes a plurality of field effect transistors, designated as 152 in figure 4, which are formed in the substrate 150. Each of the field effect transistors 152 further includes a first drain/source region 154 formed in the substrate 150 and a second, shared drain/source region 156 also formed in the substrate 150. The first and second drain/source regions 154, 156 are separated by regions 158 of the substrate 150 which are adjacent a portion of a corresponding one of the word lines 102. This portion of the word lines 102 functions as a gate electrode.

Also included are a plurality of bit line contacts 160 which extend between the second, shared drain/source regions 156 of the plurality of field effect transistors 152 and corresponding ones of the bit lines 104 and complimentary bit lines 106. Still further included in the non-volatile memory structure are a plurality of electrodes 162 which extend between the first plates 110 of the plurality of capacitors 108 and corresponding ones of the first drain/source regions 154 of the plurality of field effect transistors 152. The memory structure further includes a plurality of counter electrodes 164, each of which in turn includes a transverse strap 166 running from one of the second conductive plates 112 of the plurality of capacitors 108, substantially parallel to the substrate 150 in a direction substantially parallel to the word lines 102, and a counterelectrode contact 168. The counterelectrode contact extends outwardly from another corresponding one of the first drain/source regions 154 of the plurality of field effect transistors 152 and is electrically interconnected with the transverse strap 166. Each of the plurality of capacitors 108, together with that pair of the field effect transistors 152 which are connected to the first and second plates of that particular

capacitor 108 forms a memory cell at a corresponding one of the cell locations of the structure. The second, shared drain/source regions 156 of the plurality of field effect transistors 152 are shared between adjacent ones of the field effect transistors 152 which are associated with the same one of the bit lines 104. However, the adjacent field effect transistors 152 are in different ones of the memory cells.

Well-known integrated circuit fabrication techniques can be used to form the memory structure depicted in figures 4-6. The substrate 150 can be made, for example, from a suitable p-type silicon substrate. The source/drain regions 154, 156 can be made, for example, from suitably doped n^+ regions. The electrodes 162 and counterelectrodes 164, including the portions 166 and 168, can be made, for example, from Tungsten. The ferroelectric material 114 can be any of the materials discussed hereinabove. The plates 110, 112 of the capacitors 108 can be, for example, a high melting point noble metal which is stable and does not react with the ferroelectric material during annealing. This material should also have a low resistivity, ρ. Suitable materials are, for example, platinum or copper. The bit lines 104 and complimentary bit lines 106 can be made from a suitable metal such as copper or aluminum, for example, or any other suitable desirable conducting material. The word lines can be made, for example, from polysilicon. Other suitable materials can also be employed.

The aforementioned n^+ regions can be formed, for example, by diffusion. An appropriate isolation oxide, such as SiO_2, can be employed to form isolation regions 170. Additional insulating material, such as SiO_2 or another appropriate oxide, can be included around the remainder of the components as shown at 172. This insulation 172 can form the insulation inward of the gates of the field effect transistors formed by the word lines 102.

Again, it should be emphasized that the memory structure in figures 4-6 can be made using conventional manufacturing techniques, except that the ferroelectric

material must be deposited between the plates of the capacitors. Those of skill in the art will appreciate how this may be accomplished by studying the specification and drawings of the present patent application.

The approximate footprint of a single cell is outlined at 174 in figure 4. The cell footprint is approximately the size of the two transistors which form the cell, since the capacitor is overlaid outwardly of the transistors. For two transistors at 0.18 μm ground rules, the cell area is approximately 0.35 μm^2. The physical dimensions of the capacitor 108 can be fairly small. This is due to the fact that the known ferroelectric materials available today typically have a large dielectric constant ranging from 150 to 3000. The composition of the materials is similar to that which is used for high dielectric constant materials in DRAM. Approximately 30 - 50 femtofarrads of capacitance would typically provide sufficient signal for the bit line pairs formed by bit lines 104 and complimentary bit lines 106 to sense. Any operable value for capacitance is considered to be within the scope of the present invention.

As noted, any appropriate ferroelectric material may be used for ferroelectric material 114. Typically, such materials have the chemical structure ABO_3, such as $BaTiO_3$, $SrTiO_3$, or PZT, that is, Pb(Zr,Ti) O_3. PZT is the oldest of the materials, while $BaTiO_3$ and $SrTiO_3$ are currently the most popular forms. At present $SrTiO_3$ is believed to be the best ferroelectric material.

As noted above, the word lines 102 can be formed from polysilicon, and in turn can form the gate regions of the transistors. It is believed preferable, although not necessary, that the word lines be stitched with a second level of metal in order to provide reduced resistance, inasmuch as the polysilicon has fairly high resistive properties. Based on the foregoing description, those of skill in the art will be able to select appropriate materials and dimensions to construct the inventive memory array described herein.

It will be appreciated that, in operation, the data is stored between the plates 110, 112 of the capacitor 108, in each cell, after the write process causes the polarization of the ferroelectric material 114. As noted, the high dielectric constant of the ferroelectric materials permits a relatively small capacitor area, compared to capacitors made of silicon oxide or nitride materials. Further, the high dielectric constant of the material in the capacitor enables provision of sufficient charge stored in the capacitor to share to the bit line 104 and complimentary bit line 106 during a read operation. As long as no critical electric field is applied in the reverse direction to the ferroelectric material 114, the remnant polarization is maintained without the need of an external applied voltage, thus permitting non-volatile low power storage of information. The switching devices 116, 118 permit the transfer of data to the bit line and complimentary bit line when the particular bit address is selected, and also prevent the data in the particular cell from being degraded or lost when the address has not been selected.

Further, as noted, the write process will require an initial higher voltage short pulse through the supply of the sensing circuitry, when flipping of the cell polarity is required, as the critical voltage (critical polarization) will be needed to reverse the polarization of the ferroelectric material 114 in capacitor 108. Unlike DRAM, no restore of the data is needed after the read process, due to the use of the ferroelectric capacitor. As noted, a charge pump 216 can be provided in the voltage generator 214 to generate the high voltage write data pulse.

While there have been described what are presently believed to be the preferred embodiments of the invention, those skilled in the art will realize that various changes and modifications may be made to the invention without departing from the spirit of the invention, and it is intended to claim all such changes and modifications as fall within the scope of the invention.

What is Claimed is:

1. A memory cell configured for interconnection with a word line, a bit line, and a complementary bit line, said cell comprising:

(a) a capacitor having a first plate, a second plate, and a ferroelectric material located between said first and second plates;

(b) a first switch; and

(c) a second switch;

wherein:

said first and second switches are electrically interconnected with the word line, the bit lines, and said plates of said capacitor and are configured so as to cause the bit lines to share charge from said capacitor when said switches are activated by a control signal on the word line.

2. The cell of Claim 1, wherein:

said first switch has a control terminal electrically interconnected with the word line, a first conduction terminal electrically interconnected with the bit line, and a second conduction terminal;

said second switch has a control terminal electrically interconnected with the word line, a first conduction terminal electrically interconnected with the complementary bit line, and a second conduction terminal;

said first plate of said capacitor is electrically interconnected with said second conduction terminal of said first switch; and

said second plate of said capacitor is electrically interconnected with said second conduction terminal of said second switch.

3. The cell of Claim 2, wherein said switches comprise FETs, said control terminals comprise gate terminals, and said conduction terminals comprise drain/source terminals.

4. The cell of Claim 2, wherein said switches comprise BJTs, said control terminals comprise base terminals, and said conduction terminals comprise emitter/collector terminals.

5. The cell of Claim 1, wherein said ferroelectric material is selected and said capacitor is sized such that sufficient charge can be shared with the bit line and complementary bit line during a READ operation without necessity for a refresh.

6. The cell of Claim 1, wherein:

said ferroelectric material has a dielectric constant ranging approximately from a lower value to an upper value;

said lower value is about 150; and

said upper value is about 3000.

7. The cell of Claim 1, wherein:

said capacitor has a capacitance ranging approximately from a lower value to an upper value;

said lower value is about 30 femtofarrads; and

said upper value is about 50 femtofarrads.

8. The cell of Claim 1, wherein said ferroelectric material comprises at least one of: $BaTiO_3$, $SrTiO_3$, and $Pb(Zr,Ti)O_3$.

9. The cell of Claim 1, wherein said cell has a footprint area of about 0.35 μm^2.

10. A non-volatile memory structure comprising:

(a) a plurality of word lines;

(b) a plurality of bit lines;

(c) a plurality of complementary bit lines, each of said complementary bit lines being associated with a corresponding one of said bit lines to form a plurality of bit line pairs, said bit line pairs being positioned so as to intersect said word lines at a plurality of cell locations; and

(d) a plurality of memory cells located at said plurality of cell locations, each of said memory cells in turn comprising:

(d-1) a capacitor having a first plate, a second plate, and a ferroelectric material located between said first and second plates;

(d-2) a first switch; and

(d-3) a second switch;

wherein:

said first and second switches are electrically interconnected with an adjacent one of the word lines, an adjacent one of the bit line pairs, and said plates of said capacitor and are configured so as to cause the adjacent one of the bit line pairs to share charge from said capacitor when said switches are activated by a control signal on the word line.

11. The memory structure of Claim 10, wherein:

said first switch has a control terminal electrically interconnected with the adjacent one of word lines, a first conduction terminal electrically interconnected with the bit line of the adjacent one of the bit line pairs, and a second conduction terminal;

said second switch has a control terminal electrically interconnected with the adjacent one of the word lines, a first conduction terminal electrically interconnected with the complementary bit line of the adjacent one of the bit line pairs, and a second conduction terminal;

said first plate of said capacitor is electrically interconnected with said second conduction terminal of said first switch; and

said second plate of said capacitor is electrically interconnected with said second conduction terminal of said second switch.

12. The memory structure of Claim 11, wherein said switches comprise FETs, said control terminals comprise gate terminals, and said conduction terminals comprise drain/source terminals.

13. The memory structure of Claim 11, wherein said switches comprise BJTs, said control terminals comprise base terminals, and said conduction terminals comprise emitter/collector terminals.

14. The memory structure of Claim 10, wherein said ferroelectric material is selected and said capacitor of each of said memory cells is sized such that sufficient charge can be shared with the adjacent bit line pair during a READ operation without necessity for a refresh.

15. The memory structure of Claim 10, wherein:

said ferroelectric material has a dielectric constant ranging approximately from a lower value to an upper value;

said lower value is about 150; and

said upper value is about 3000.

16. The memory structure of Claim 10, wherein:

said capacitor of each of said memory cells has a capacitance ranging approximately from a lower value to an upper value;

said lower value is about 30 femtofarrads; and

said upper value is about 50 femtofarrads.

17. The memory structure of Claim 10, wherein said ferroelectric material comprises at least one of:

$BaTiO_3$, $SrTiO_3$, and $Pb(Zr,Ti)O_3$.

18. The memory structure of Claim 10, wherein each of said cells has a footprint area of about 0.35 μm^2.

19. The memory structure of Claim 10, further comprising:

(e) a word decoder/word line driver which is electrically interconnected with said plurality of word lines and which is electrically configured to provide a signal to a given one of said word lines sufficient to activate those of said switches electrically interconnected thereto; and

(f) a bit line controller which is electrically interconnected with said plurality of bit line pairs, said bit line controller in turn comprising:

(f-1) a bit line selector assembly which is configured to select a given one of said bit line pairs; and

(f-2) a plurality of sense amplifiers configured to sense voltage differential between said bit line pairs in a READ operation and to apply a voltage differential greater than a coercive voltage of said dielectric material to said bit line pairs during a WRITE operation.

20. The memory structure of Claim 19, wherein said bit line controller further comprises a voltage generator associated with the plurality of sense amplifiers, said voltage generator having a charge pump suitable for providing said voltage greater than said coercive voltage.

21. A non-volatile memory structure comprising:

a semiconductor substrate;

a plurality of word lines formed outward of said substrate;

a plurality of bit lines formed outward of said word lines;

a plurality of complementary bit lines formed outward of said word lines, each of said complementary bit lines being associated with a corresponding one of said bit lines to form a plurality of bit line pairs, said bit line pairs being positioned so as to intersect said word lines at a plurality of cell locations;

a plurality of capacitors, each of said capacitors in turn comprising:

a first conductive plate spaced outward of said substrate;

a second conductive plate spaced outward of said first conductive plate; and

a ferroelectric material located between said first and second plates;

a plurality of field effect transistors formed in said substrate, each of said field effect transistors in turn comprising:

a first drain/source region formed in said substrate; and

a second, shared, drain/source region formed in said substrate, said first and second drain/source regions being separated by a region of said substrate adjacent a portion of a corresponding one of said word lines, said portion functioning as a gate electrode;

a plurality of bit line contacts, said plurality of bit line contacts extending between said second, shared drain/source regions of said plurality of field effect transistors and corresponding ones of said bit lines and said complementary bit lines;

a plurality of electrodes, said plurality of electrodes extending between said first plates of said plurality of capacitors and corresponding ones of said first drain/source regions of said plurality of field effect transistors; and

a plurality of counter electrodes, each of said plurality of counter electrodes in turn comprising:

a transverse strap running from one of said second conductive plates of said plurality of capacitors, said transverse strap running substantially parallel to said substrate in a direction substantially parallel to said word lines; and

a counter electrode contact extending outwardly from another corresponding one of said first drain/source regions of said plurality of field effect transistors and being electrically interconnected with said transverse strap;

wherein:

each of said plurality of capacitors, together with that pair of said field effect transistors which are connected to said first and second plates of said capacitor, forms a memory cell at a corresponding one of said cell locations of said structure; and

said second, shared drain/source regions of said plurality of field effect transistors are shared between adjacent ones of said field effect transistors which are associated with a same one of said bit lines, said adjacent field effect transistors being in different ones of said memory cells.

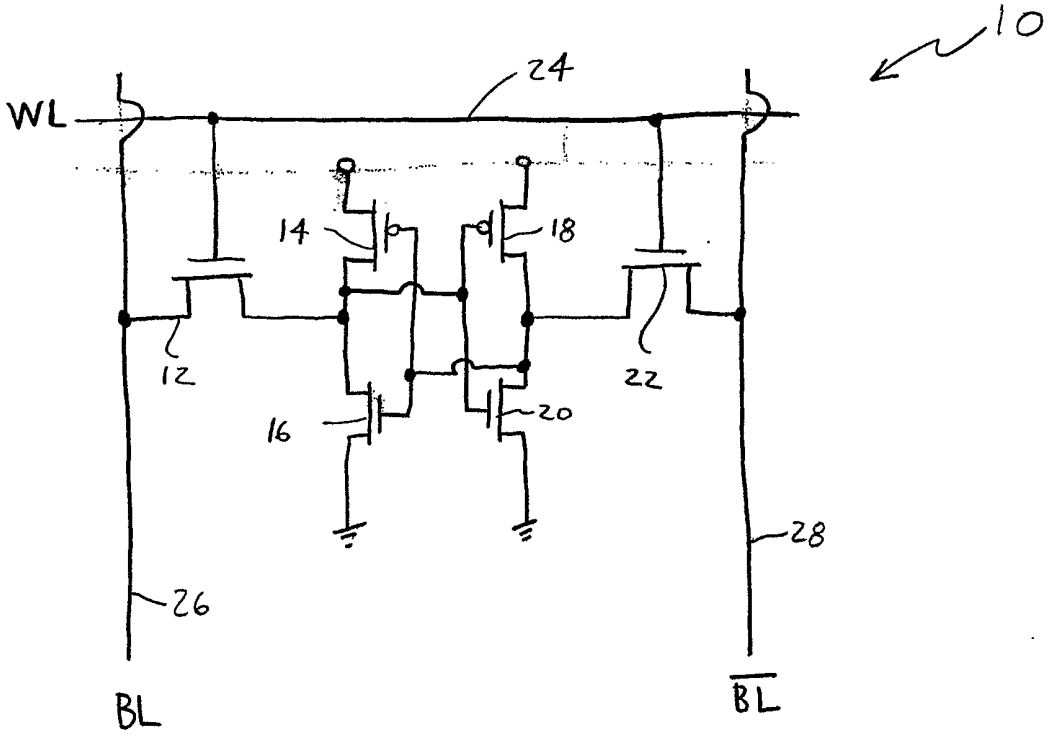

FIG. 1 (PRIOR ART)

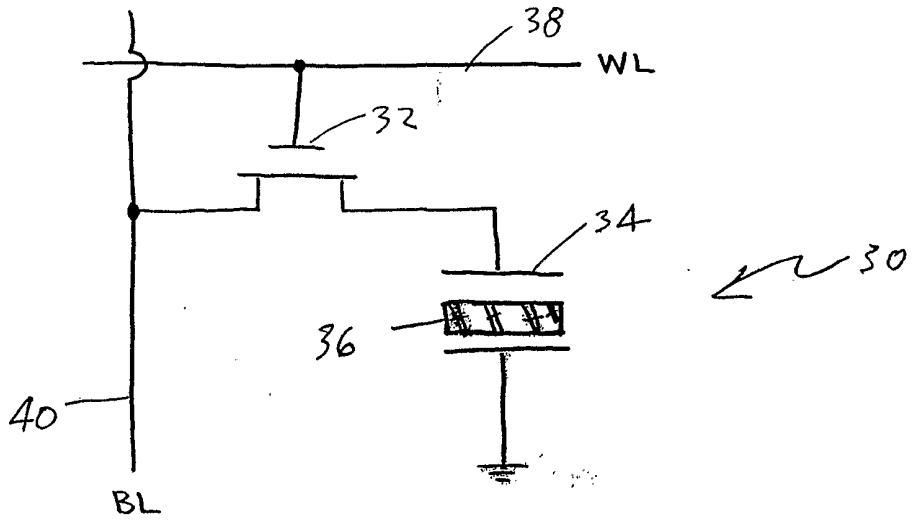

FIG. 2 (PRIOR ART)

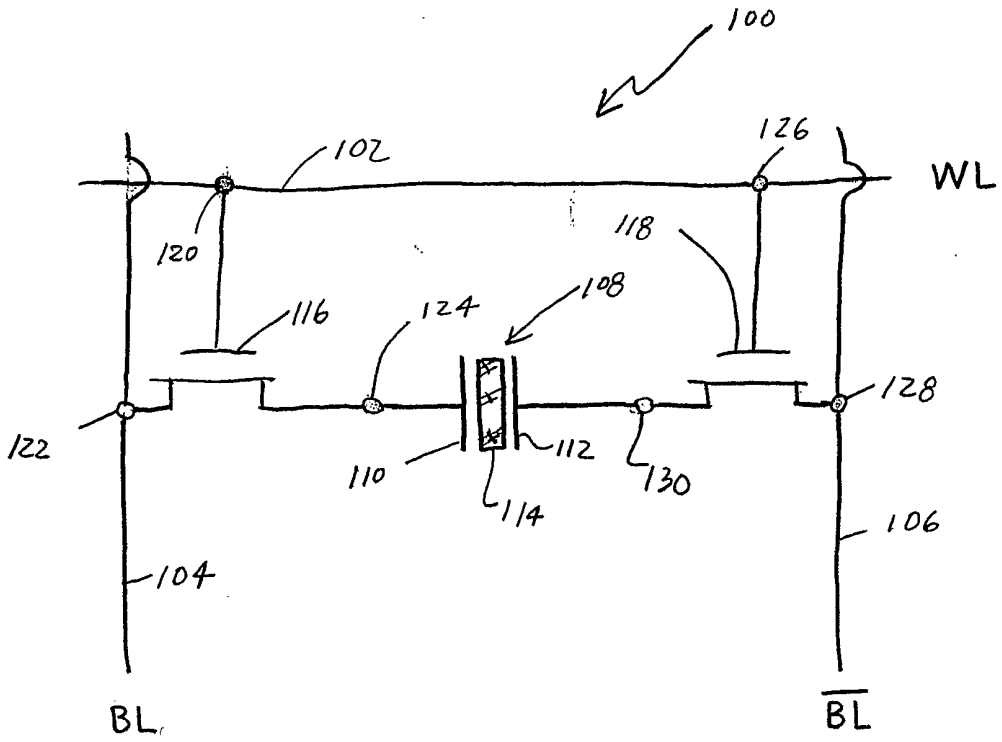
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FIG. 3

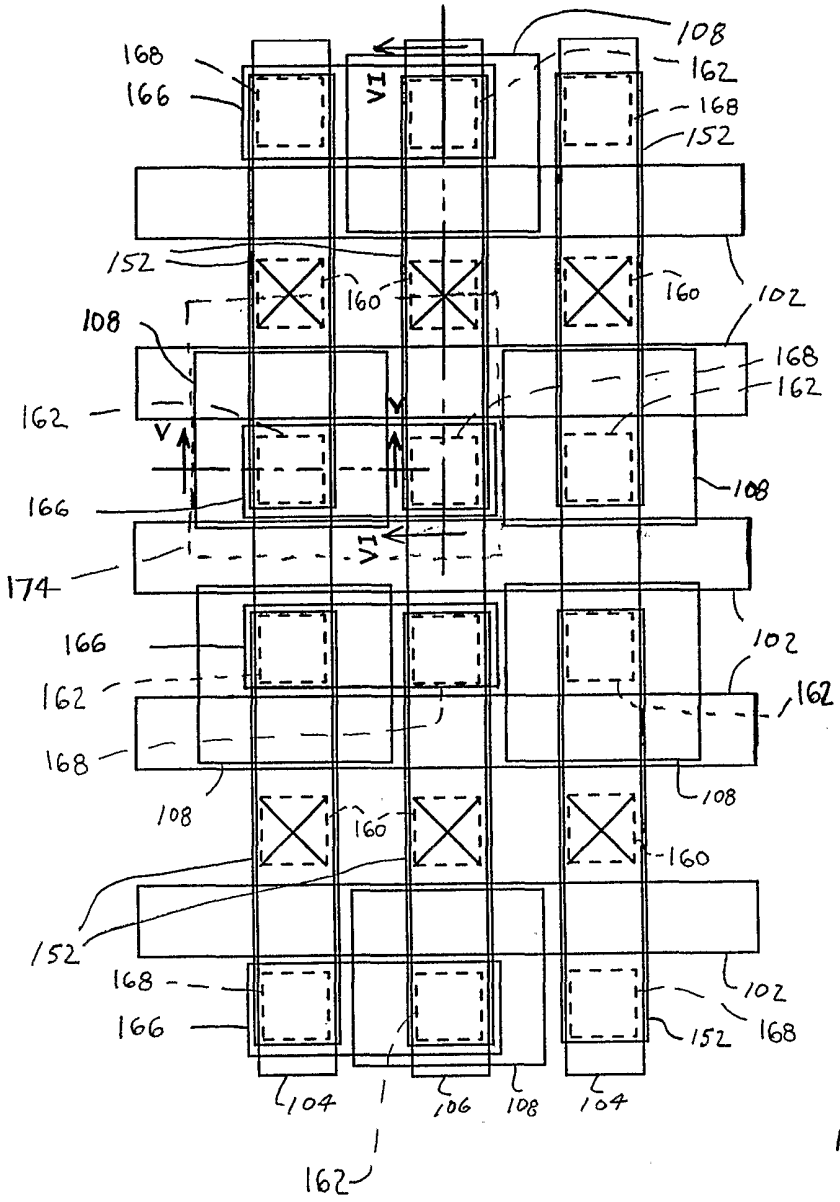
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FIG. 4

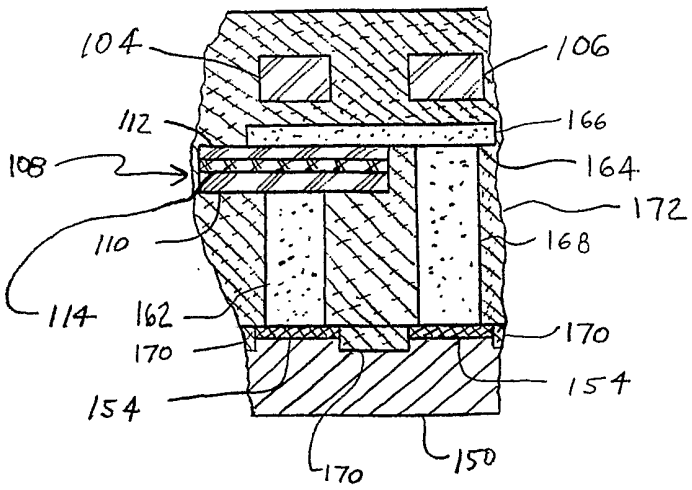
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FIG. 5

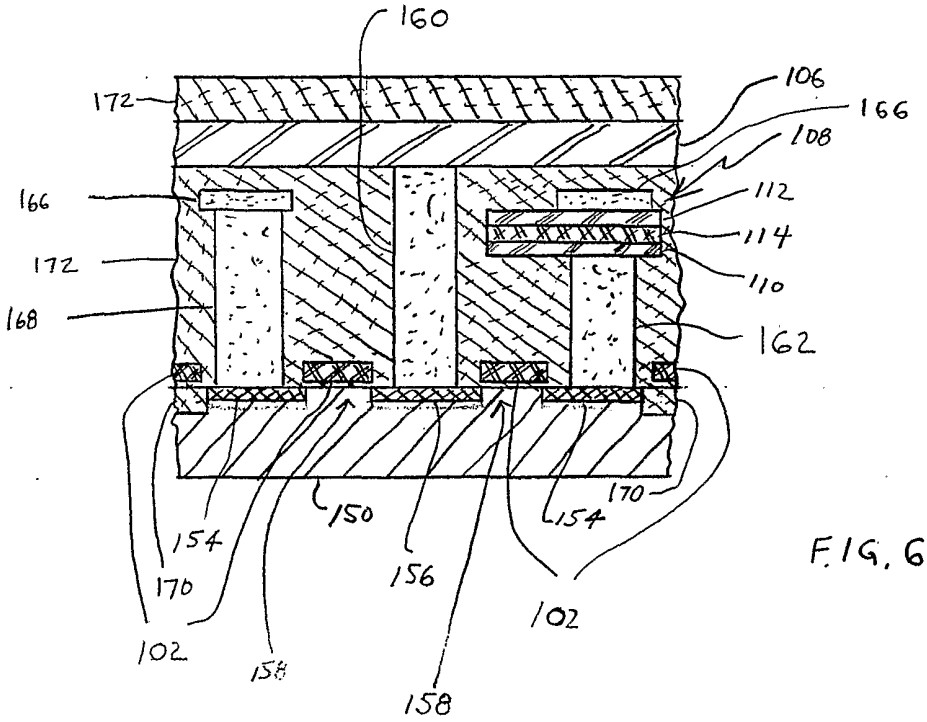
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FIG. 6

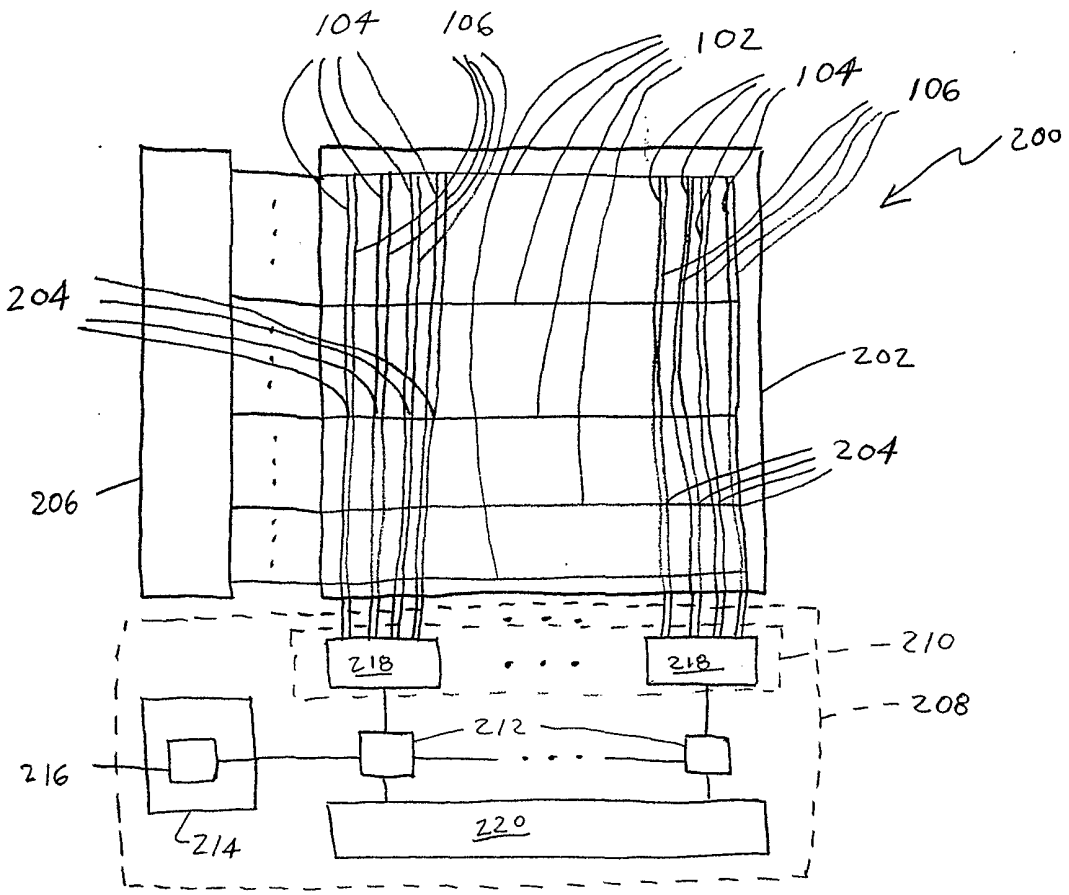
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FIG. 7

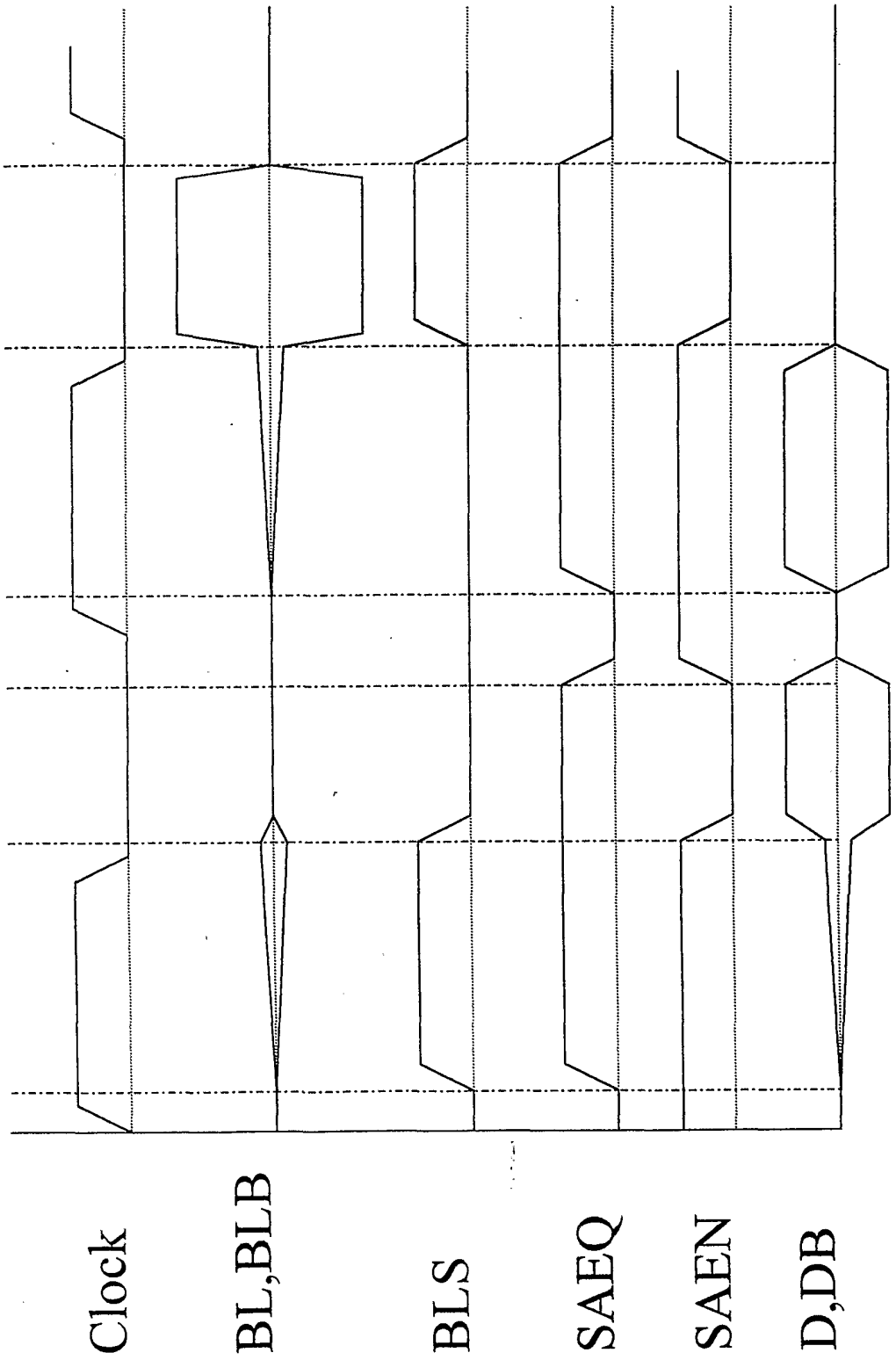
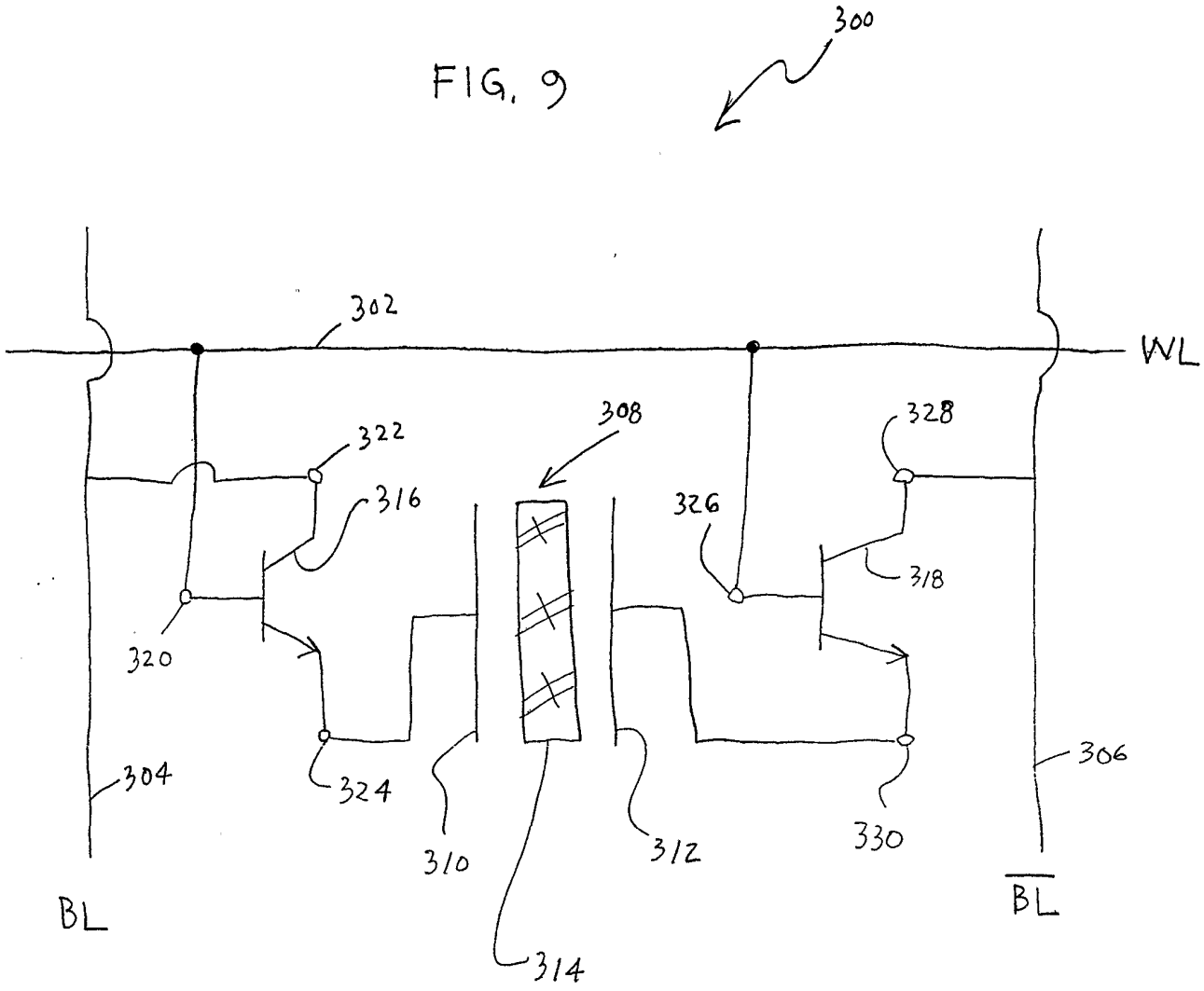


FIG. 8

FIG. 9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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/49809

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :G11C 11/22 7/00
US CL : 365/145, 149, 154
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 365/145, 149, 154

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4,888,733 A (MOBLEY) 19 DECEMBER 1989 (19/12/89) all	1-20
A,P	US 6,229,728 B1 (ONO ET AL) 08 MAY 2001 (08/05/01) a;;	1-21

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
01 MAY 2002	17 MAY 2002
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer SON THANH DINH Telephone No. (703) 308-4120

Form PCT/ISA/210 (second sheet) (July 1998)★