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(54) SYSTEM AND METHOD FOR PROVIDING AN ARBITRATED MEMORY BUS IN A HYBRID COMPUTING SYSTEM

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**Publication Classification**

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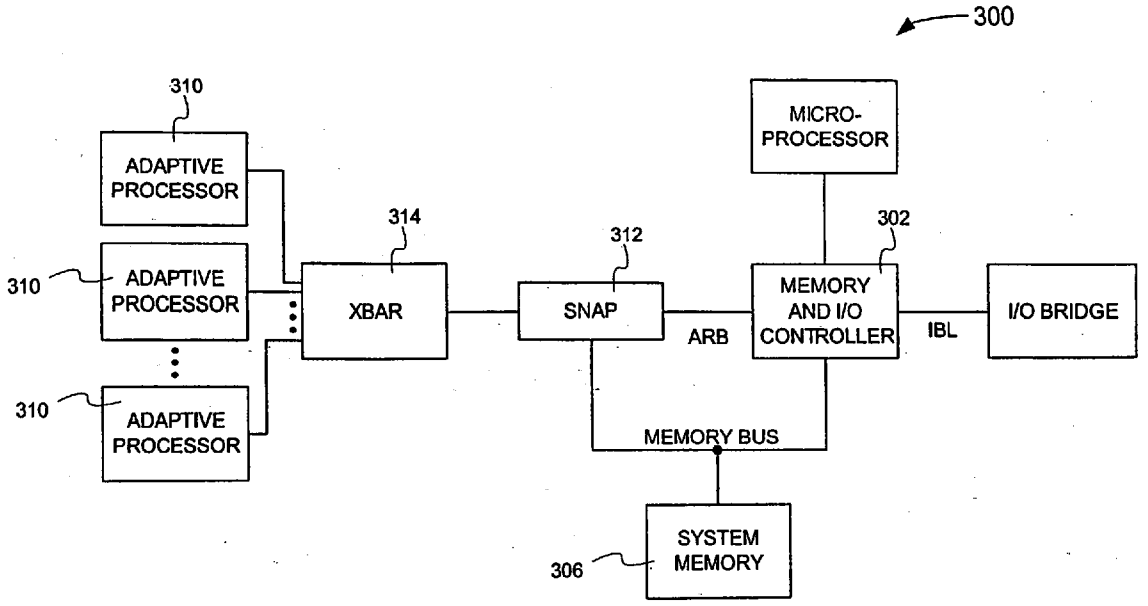
(52) **U.S. Cl.** ..... **710/309**

(57) **ABSTRACT**

A computing system having at least one microprocessor and a memory subsystem coupled to the at least one microprocessor. A memory controller is coupled to manage memory transactions between the memory subsystem and the at least one microprocessor. At least one arbitration port is coupled to the memory controller and configured to receive an external arbitration signal.



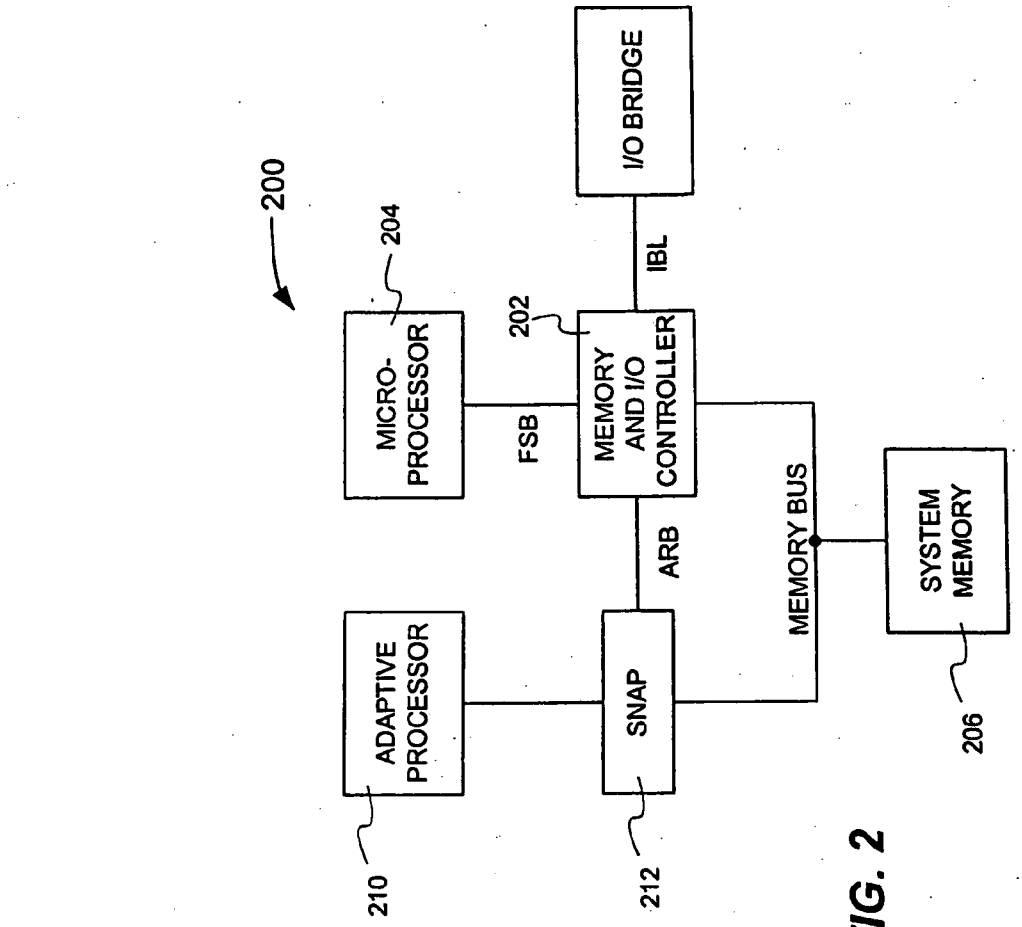



FIG. 2

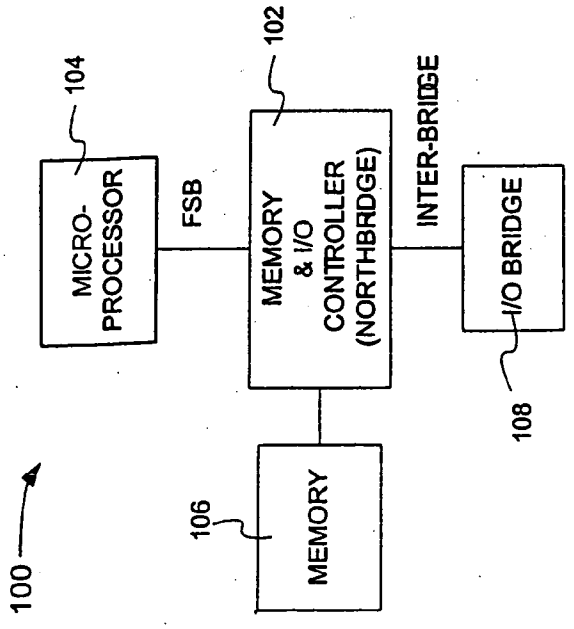



FIG. 1
(Prior Art)

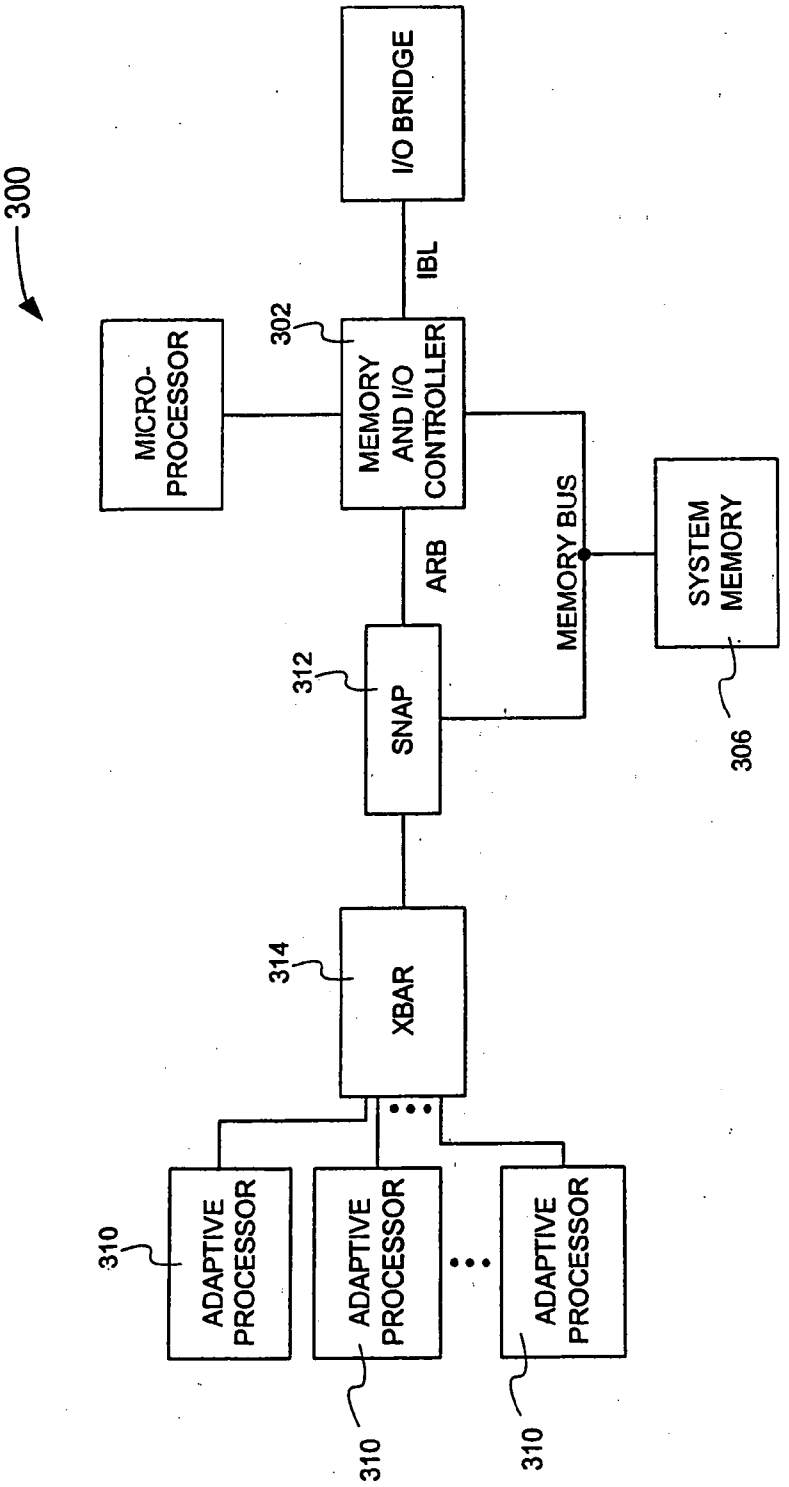

300
I/O BRIDGE
IBL
302
MICRO-PROCESSOR
MEMORY AND I/O CONTROLLER
ARB
MEMORY BUS
SYSTEM MEMORY
306
312
SNAP
314
XBAR
310
ADAPTIVE PROCESSOR
ADAPTIVE PROCESSOR
ADAPTIVE PROCESSOR
310
310

FIG. 3

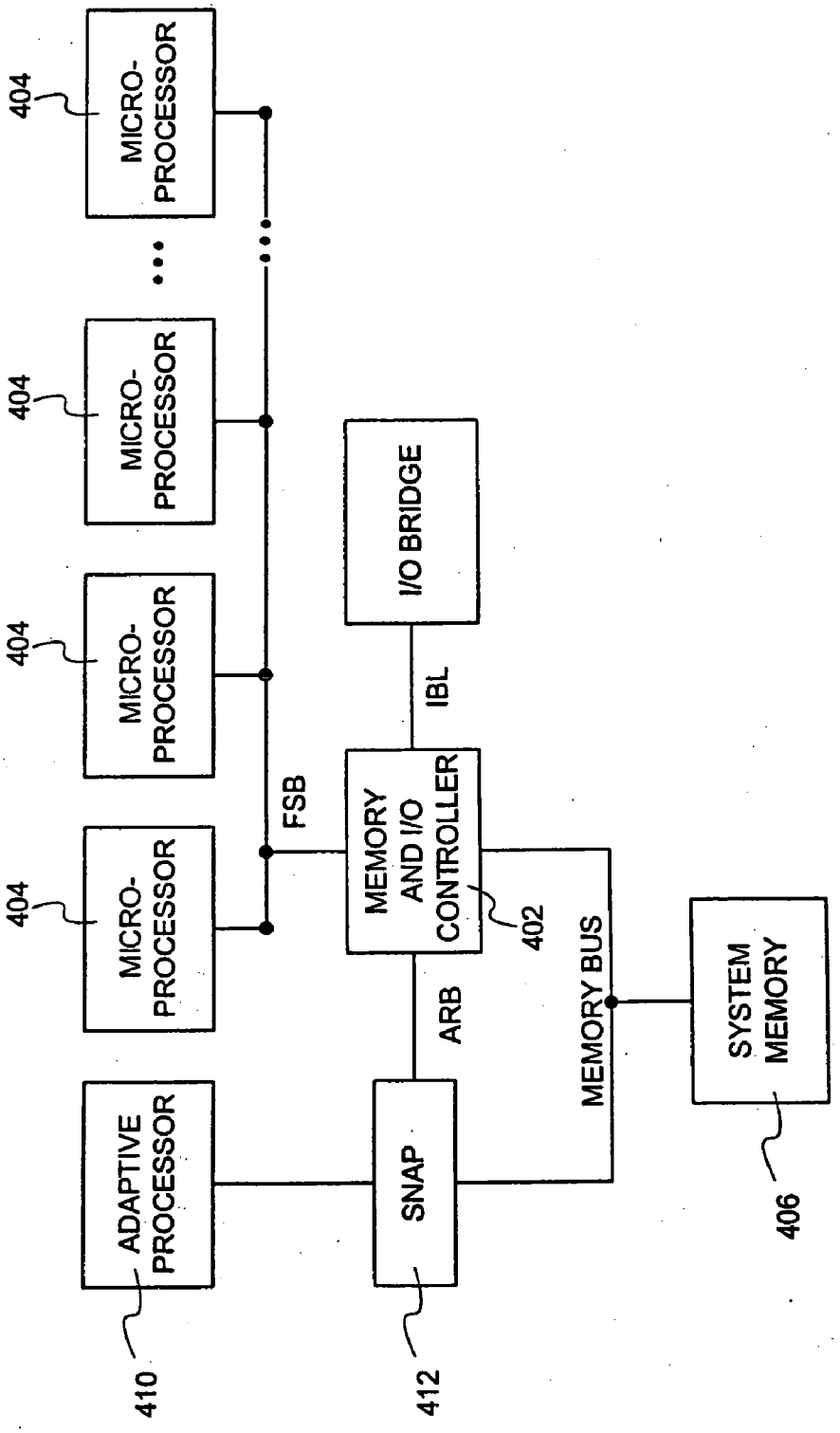

404
MICRO-PROCESSOR
404
MICRO-PROCESSOR
404
MICRO-PROCESSOR
404
MICRO-PROCESSOR
FSB
I/O BRIDGE
IBL
MEMORY AND I/O CONTROLLER
402
ARB
MEMORY BUS
SYSTEM MEMORY
406
ADAPTIVE PROCESSOR
410
SNAP
412

FIG. 4

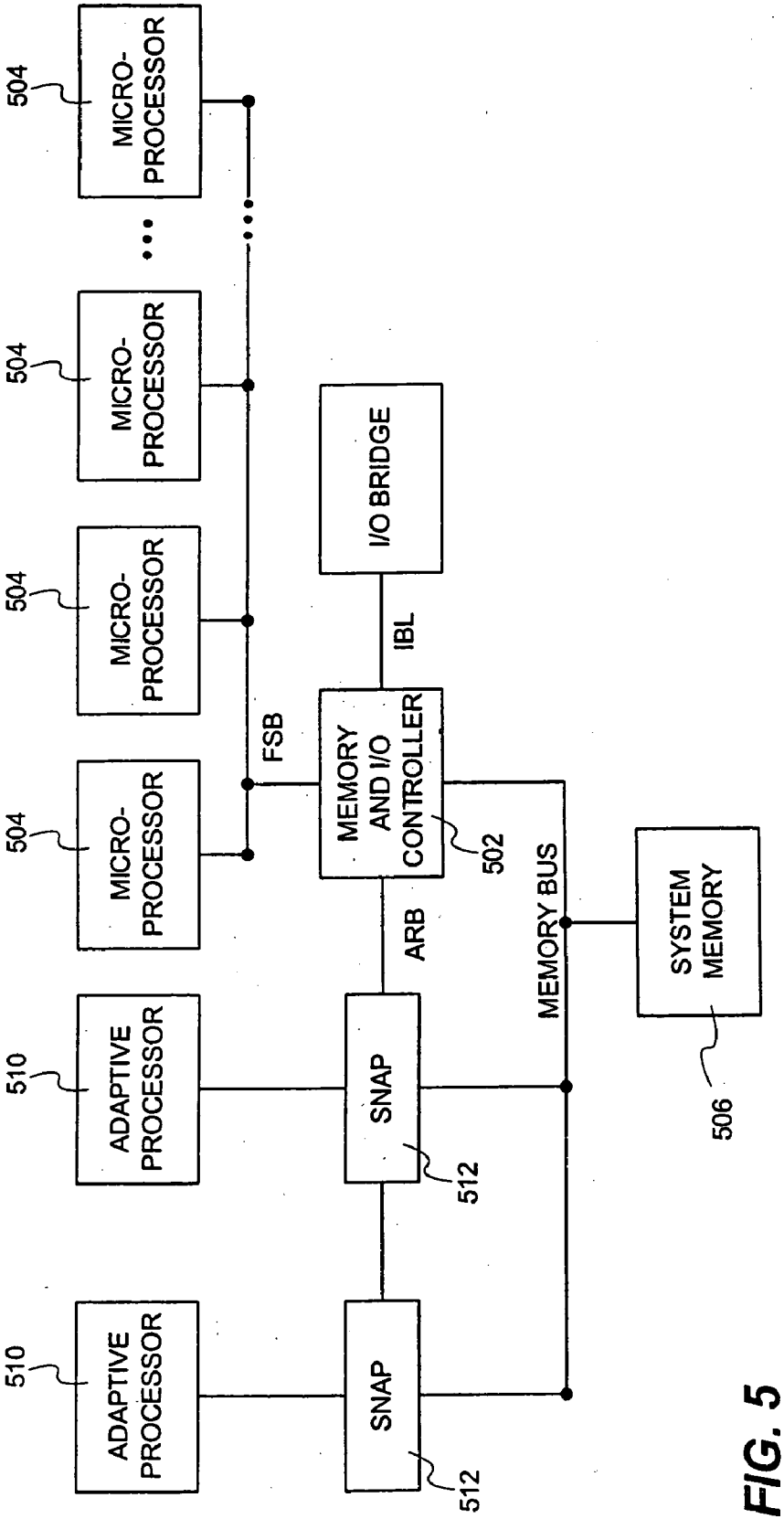

504
MICRO-PROCESSOR
504
MICRO-PROCESSOR
504
MICRO-PROCESSOR
504
MICRO-PROCESSOR
FSB
I/O BRIDGE
IBL
MEMORY AND I/O CONTROLLER
502
ARB
MEMORY BUS
SYSTEM MEMORY
506
510
ADAPTIVE PROCESSOR
SNAP
512
510
ADAPTIVE PROCESSOR
SNAP
512

FIG. 5

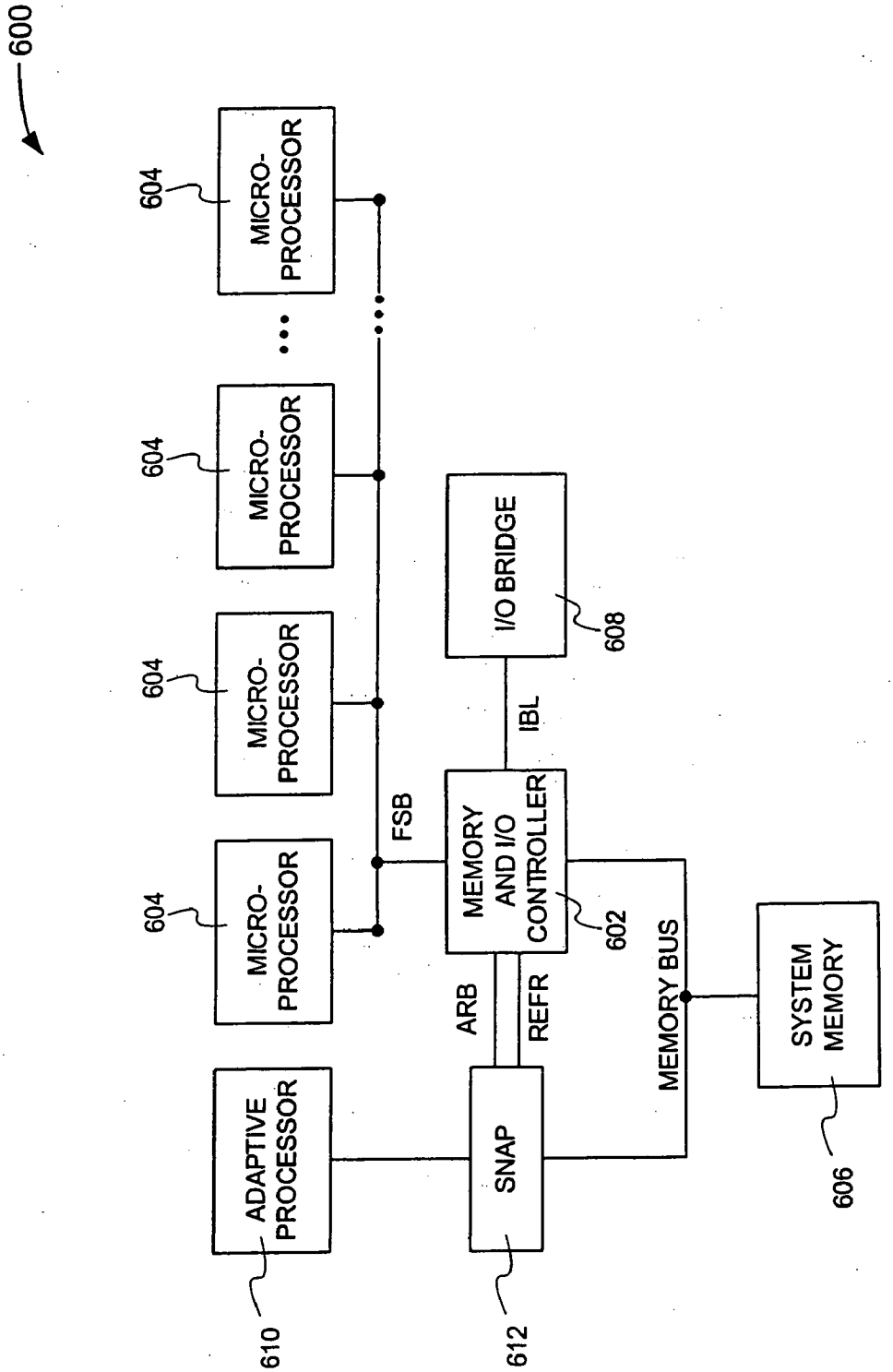

600
604
MICRO-PROCESSOR
604
MICRO-PROCESSOR
604
MICRO-PROCESSOR
604
MICRO-PROCESSOR
FSB
I/O BRIDGE
608
IBL
MEMORY AND I/O CONTROLLER
602
ARB
REFR
MEMORY BUS
SYSTEM MEMORY
606
ADAPTIVE PROCESSOR
610
SNAP
612

FIG. 6

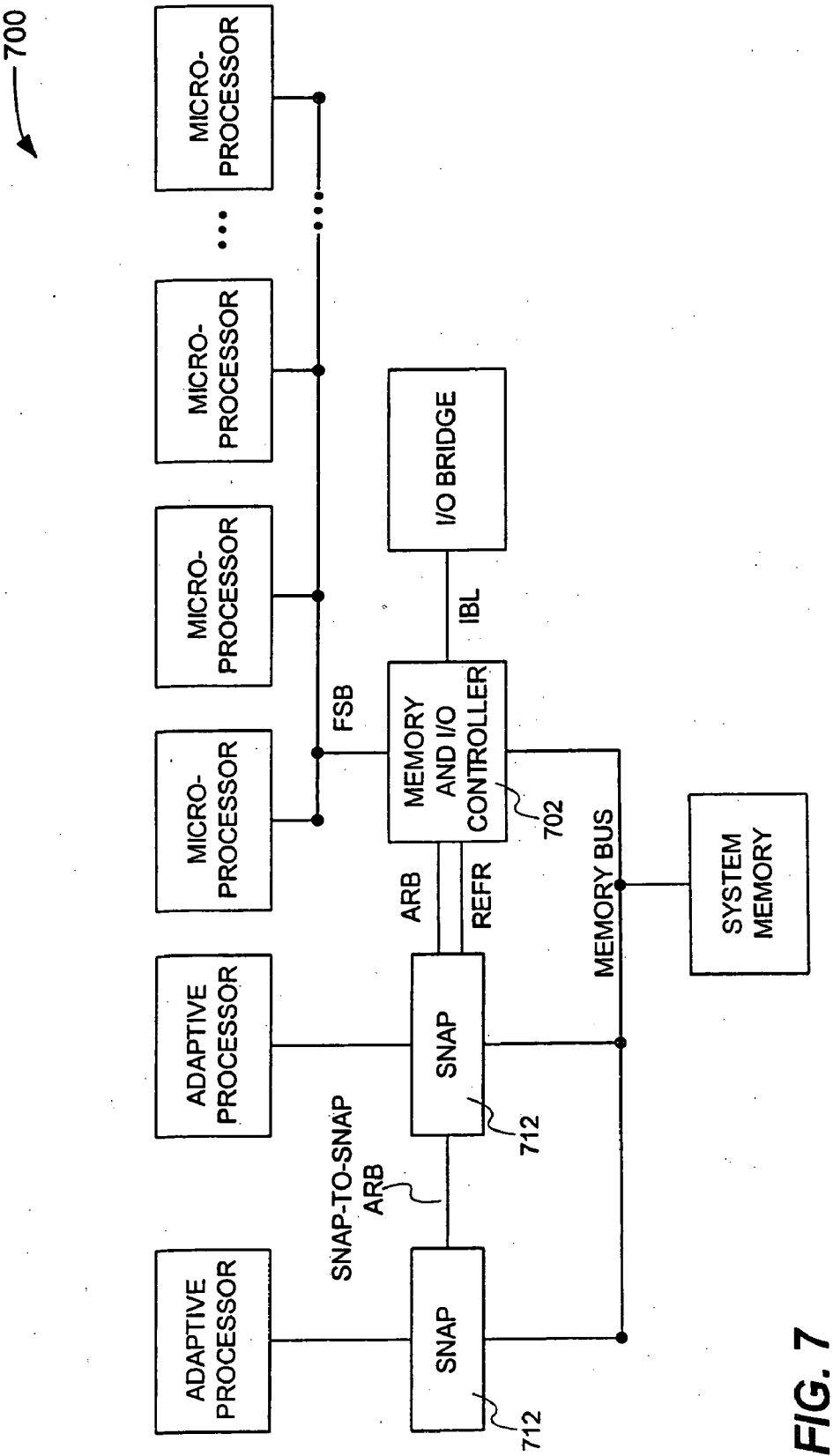

700
MICRO-PROCESSOR
MICRO-PROCESSOR
MICRO-PROCESSOR
MICRO-PROCESSOR
FSB
I/O BRIDGE
IBL
MEMORY AND I/O CONTROLLER
702
ARB
REFR
MEMORY BUS
SYSTEM MEMORY
ADAPTIVE PROCESSOR
SNAP
712
SNAP-TO-SNAP ARB
ADAPTIVE PROCESSOR
SNAP
712

FIG. 7

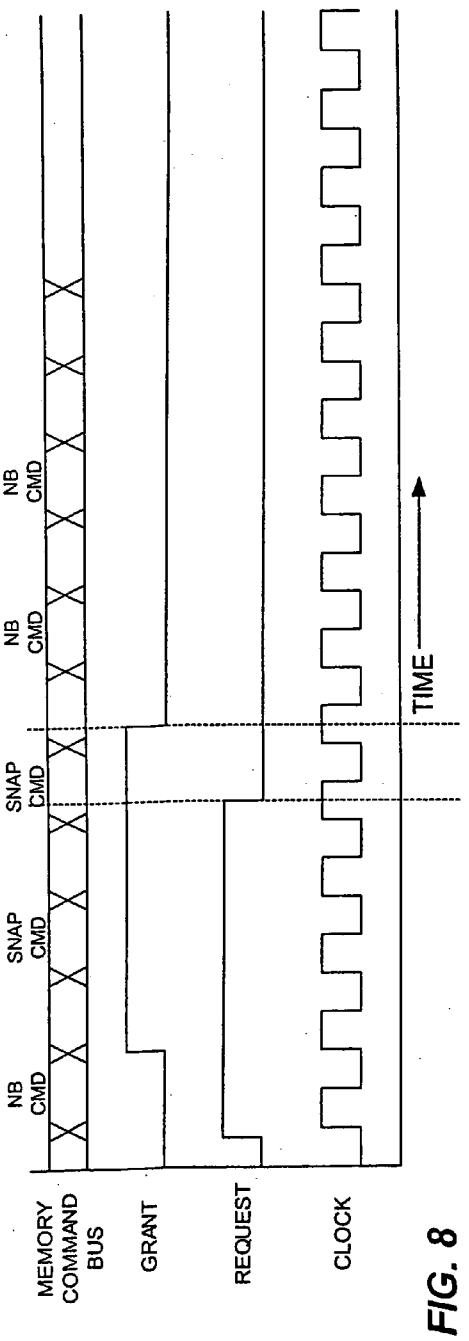

NB CMD
SNAP CMD
SNAP CMD
NB CMD
NB CMD
TIME
MEMORY COMMAND BUS
GRANT
REQUEST
CLOCK

FIG. 8

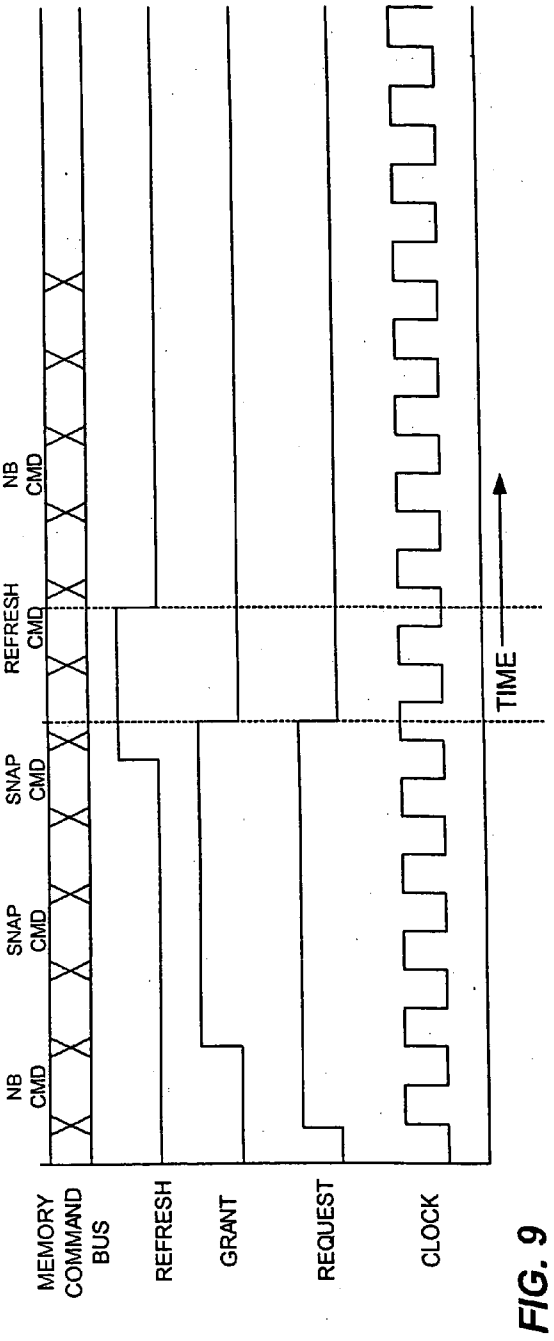

NB CMD
SNAP CMD
SNAP CMD
REFRESH CMD
NB CMD
TIME
MEMORY COMMAND BUS
REFRESH
GRANT
REQUEST
CLOCK

FIG. 9

# SYSTEM AND METHOD FOR PROVIDING AN ARBITRATED MEMORY BUS IN A HYBRID COMPUTING SYSTEM

## CROSS REFERENCE TO RELATED PATENT APPLICATIONS

[0001] The present invention is a continuation of U.S. patent application Ser. No. 10/284,994 filed Oct. 31, 2002 for: "System and Method For Providing An Arbitrated Memory Bus In A Hybrid Computing System", U.S. patent application Ser. No. 09/755,744 filed Jan. 5, 2001 for: "Multiprocessor Computer Architecture Incorporating a Plurality of Memory Algorithm Processors in the Memory Subsystem" which is a divisional application of U.S. patent application Ser. No. 09/481,902 filed Jan. 12, 2000 (now U.S. Pat. No. 6,247,110) which is a continuation application of U.S. patent application Ser. No. 08/992,763 filed Dec. 17, 1997 (now U.S. Patent No. 6,076,152). The present invention is also related to the subject matter of U.S. Pat. No. 6,339,819 issued Jan. 15, 1992 for: "Multiprocessor with Each Processor Element Accessing Operands in Loaded Input Buffer and Forwarding Results to FIFO Output Buffer". The foregoing patent application and issued patents are assigned to SRC Computers, Inc., assignee of the present invention, the disclosures of which are herein specifically incorporated in their entirety by this reference.

## BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention.

[0003] The present invention relates, in general, to the field of computer systems and techniques for interconnecting various processing or computing elements. More particularly, the present invention relates to a computer system architecture and memory controller having an arbitration interface enabling external devices to access system memory resources cooperatively.

[0004] 2. Relevant Background.

[0005] Conventional computer system architecture for single-processor systems include a microprocessor that communicates with other devices through a "system chipset". The system chipset implements various input/output and controller functions that enable the microprocessor to communicate with external devices such as memory, mass storage, display devices, network interfaces, printers, and the like. A typical system chipset will implement an interface to the microprocessor often referred to as a "front side bus" or "FSB" that couples to high-speed, low-latency, or bandwidth intensive components such as memory. The chipset implements a secondary interface, often referred to as a "peripheral bus" that operates at a lower speed couples to lower speed devices such as mass storage controllers, printers, network interfaces, and the like.

[0006] The system chipset is often produced as multiple specialized components. In a typical configuration, a "north bridge" component implements the microprocessor interface and an interface to the memory subsystem. A "south bridge" component implements the peripheral interface. The north bridge and south bridge components are coupled to bridge the peripheral interface with the microprocessor interface. The interface between the microprocessor and memory is a particularly constrained interface for most applications. In most personal computer architectures, it is assumed that one device will have exclusive access to the FSB (e.g., the single microprocessor being coupled to the FSB). Because of this, all memory transactions must be implemented through a port to the north bridge chip. This increases the system memory access time for the external devices. In the case of hybrid computing systems in which the external device is an adaptive processor, this increase in access time reduces the performance benefits of the hybrid system.

[0007] In many cases, a direct memory access (DMA) controller is implemented on the peripheral bus, within the north bridge device, or through a DMA port on the north bridge component to manage memory transactions between the peripheral bus and the memory subsystem. DMA controllers are typically designed to support memory transactions with lower speed peripherals coupled through the south bridge device, as opposed to devices that require significant memory bandwidth such as external processors. In other words, the DMA controller supports peripheral memory activity, and so operates at the slower peripheral interface speeds. While DMA controllers relieve the microprocessor from handling all memory operations, the slower speed interface limits the ability to access the memory subsystem at speeds similar to those available to the microprocessor.

[0008] The north bridge of a traditional computer system internally arbitrates between the processor, the graphics port, and peripheral devices and DMA controller for access to the system memory bus. Currently, system chipsets do not provide external access to the arbitration logic. Hence, external devices that desire to access the memory subsystem are constrained to use the arbitration mechanisms implemented by the north bridge component.

[0009] SMP (symmetric multiprocessing) refers to systems that execute programs using multiple processors that share a common operating system and memory. In symmetric multiprocessing, the processors share memory and the I/O bus or data path. A single copy of the operating system is in charge of all the processors. Because conventional computing system architectures do not enable multiple devices to access the memory bus, implementing systems in which multiple processors share memory is difficult. As a result, SMP systems based on mass-produced components that are designed for conventional architectures have used lower-speed access granted at peripheral bus speeds, or implemented processing components within the memory subsystem. An example of the later implementation is the multi-adaptive processor (MAP™) described in commonly assigned U.S. Pat. No. 6,247,110 (MAP is a trademark or registered trademark of SRC Computers, Inc.).

[0010] In view of the above, it is apparent that a need exists for a computing system that exposes the arbitration mechanisms to enable access to a memory subsystem at high speed. Moreover, there is a particular need for system chipset architectures that utilize an externally provided arbitration signal such that a memory subsystem bus can be accessed by multiple agents such as multiple processors and other components that couple to the memory subsystem bus.

## SUMMARY OF THE INVENTION

[0011] Briefly stated, the present invention involves a computing system having at least one microprocessor and a memory subsystem coupled to the at least one microproces-

sor. A memory controller is coupled to manage memory transactions between the memory subsystem and the at least one microprocessor. At least one arbitration port is coupled to the memory controller and configured to receive an external arbitration signal.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0012] **FIG. 1** shows a functional block diagram of a typical computing system implemented with a microprocessor, memory and a system chipset including a ("North Bridge") and a peripheral bus controller ("South Bridge");

[0013] **FIG. 2** illustrates a functional block diagram of a memory-connected hybrid computing system including a microprocessor and an adaptive processor coupled to system memory in accordance with the present invention;

[0014] **FIG. 3** is a functional block diagram of an alternative embodiment hybrid computing system in accordance with the present invention having one or more adaptive processors coupled to shared system memory with a microprocessor;

[0015] **FIG. 4** shows a functional block diagram of a hybrid symmetrical multiprocessing (SMP) computing system in accordance with the present invention in which a memory system arbiter mechanism and port is implemented in the north bridge component of the system chipset;

[0016] **FIG. 5** illustrates a functional block diagram of an alternative configuration hybrid SMP computing system having multiple adaptive processors coupled to an arbitrated-access shared memory subsystem in accordance with the present invention;

[0017] **FIG. 6** shows a functional block diagram of an alternative embodiment hybrid SMP computing system having memory system access arbitration mechanisms implemented in a switch/network adapter port (SNAP) implemented in a in accordance with the present invention;

[0018] **FIG. 7** is a functional block diagram of another alternative embodiment hybrid SMP computing system having multiple adaptive processors with memory system access arbitration mechanisms implemented in a switch/network adapter port (SNAP) implemented in a in accordance with the present invention;

[0019] **FIG. 8** shows a timing diagram of a first embodiment arbitration sequence useful in a two-wire implementation of an arbitration signal bus/port in accordance with the present invention; and

[0020] **FIG. 9** shows a timing diagram of a first embodiment arbitration sequence useful in a three-wire implementation of an arbitration signal bus/port in accordance with the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0021] The present invention involves multiprocessor and hybrid computer systems, including symmetric multiprocessing (SMP) computing systems that enable shared access to system memory from the various processes. In exemplary implementations of the present invention, substantially conventional system chipsets are modified to expose internal arbitration logic to external devices. In this manner, one or more external devices, such as adaptive processors, have a direct link to the system memory without need to access system memory through the system chipset. In other implementations, arbitration logic is implemented in devices external to the system chipset, in which case the system chipset is modified to arbitrate for memory system access rather than assume it has exclusive access. In either case, modifications to the system chipset are minimal, and an arbitration signal bus or port may be implemented with as few as two or three connections to the system chipset.

[0022] **FIG. 1** shows a high-level functional block diagram of a typical computing system **100** is shown. The computing system **100** may be, for example, a personal computer ("PC") architecture that incorporates a commercially available integrated circuit ("IC") memory controller ("north bridge") **102** such as the P4X333/P4X400 devices available from VIA Technologies, Inc.; the M1647 device available from Acer Labs, Inc. and the 824430X device available from Intel Corporation. North bridge **102** is coupled by means of a front side bus ("FSB") to a processor **104** such as one of the Intel® Pentium® series or Xeon™ series of processors also available from Intel Corporation. North bridge **102** is coupled via a memory bus to system memory **106**, which comprises, for example, an arrangement of synchronous dynamic random access ("SDRAM") memory modules. Other memory configurations and devices such as double data rate (DDR) SDRAM, RDRAM and DRDRAM by Rambus Corporation, Enhanced SDRAM (ESDRAM) produced by Ramtron International Corporation, and the like. As noted hereinbefore, conventional north bridge components are configured to support a single processor **104** over the FSB, which makes adding additional processors difficult. Even where the system chipset support multiple processors coupled to the FSB, as described in alternative embodiments, the FSB architecture is very specific to a particular processor type. Hence, coupling advanced or special-purpose processing devices such as an adaptive processor in a manner that gives the adaptive processor suitable access to the memory subsystem **106** has been difficult or impossible.

[0023] In some implementations, a dedicated accelerated graphics port ("AGP"), not shown, is provided for interfacing system **100** to external graphics processing components while an inter-bridge bus couples north bridge IC **102** to a "south bridge"**108**. The north bridge **102** and south bridge **108** are together referred to as a system chipset as they are typically designed to work together to provide desired system I/O functionality. The allocation of functionality between the components of a chipset may be altered between implementations, and some or all of the I/O functionality may be integrated into a microprocessor **104** as in the case of a microcontroller. For purposes of the present invention, it is sufficient to note that the north bridge component **102** handles the high-speed I/O functions typically associated with accessing a memory subsystem.

[0024] South bridge **108** may be implemented by, for example, an SLC90E66 device available from Standard Microsystems, Corporation or the VT8235 device available from VIA Technologies. South bridge **108** implements a variety of I/O interfaces and ports that couple system **100** to, for example, a peripheral component interconnect ("PCI") bus, universal serial bus (USB), IEEE 1394 port, system management ("SM") bus, general purpose ("GP") I/O as

well as industry standard architecture/extended I/O ("ISA/EIO") bus and the like. South bridge **108** may also implement special purpose ports to graphics devices, audio devices, local area network devices, disk drives, flash memory, and the like depending on the needs of a particular application. In general, the interfaces of south bridge **108** handle slower, narrow bandwidth I/O as compared to north bridge **102**.

[**0025**] In contrast with the architecture shown in **FIG. 1**, the hybrid computing systems shown in **FIG. 2-FIG. 7** illustrate various implementation that enable a external processing devices to share access to a memory subsystem. Hybrid computer systems are those that incorporate both standard microprocessors and adaptive processors. These are typically large multiprocessor server-type systems that reside on a shared network. The overall performance and flexibility of such systems is directly proportional to the level of coupling between the microprocessors and the adaptive processors and system memory. When the disparate processor types are treated as peers and have balanced (e.g., substantially equal) bandwidths and latencies to a shared memory, the system performance will usually be maximized. In general, the implementations shown in **FIG. 2-FIG. 7** provide an arbitration port and arbitration mechanism that enables an external processor to cooperatively share access to a memory subsystem to achieve such balanced access.

[**0026**] For example, in **FIG. 2**, system **200** expands on the typical computer system **100** by adding an adaptive processor **210** coupled to the system memory bus through a system/network adapter port (SNAP) **212**. An adaptive processor such as a multi-adaptive processor (MAP) introduced by SRC Computers, Inc, provide users the capability of having hardware logic-implemented functions, which can greatly accelerate application algorithms over what is otherwise implemented in software within a conventional microprocessor **204**. Details of an exemplary SNAP implementation and functionality are described in U.S. patent application Ser. No. 09/932,330 filed Aug. 17, 2001 for: "Switch/Network Adapter Port for Clustered Computers Employing a Chain of Multi-Adaptive Processors in a Dual In-Line Memory Module Format" assigned to SRC Computers, Inc., Colorado Springs, Colo., assignee of the present invention, the disclosure of which is herein specifically incorporated in its entirety by this reference. SNAP **212** is typically placed in a DIMM slot of a computer system, and is thereby coupled to the memory bus. While SNAP **202** is implemented on the memory subsystem and occupies memory address space, it is a configurable device that can be configured to perform processing and I/O functions. Although a SNAP **212** is closely coupled to the memory system **206**, it exhibits some overhead in conducting memory transactions as a result of its "slave" with respect to the memory bus. However, this overhead minimally impacts overall performance because as the overhead incurred when setting up the arbitration signal port is spread out over all the memory transactions that are processed by adaptive processor **210**.

[**0027**] In hybrid system **200**, memory and I/O controller **202**, implemented as a north bridge chip in the example, can no longer assume that microprocessor **204** will be the only agent that will have control of system memory **206**. Adaptive processor **210** requires shared access to system memory **206** to begin memory transactions (i.e., read, write, modify, lock, unlock, and the like). In accordance with this implementation of the present invention, arbitration logic within memory and I/O controller **202** is provided with an external arbitration port to communicate arbitration signals between SNAP **212** and memory and I/O controller **202**. The arbitration signals comprise, in a particular example, a relatively simple request/grant scheme in which a request signal is asserted by an agent that seeks memory system access, and a grant signal is asserted by the arbitration logic to the agent that currently has access to the memory subsystem. As the arbitration logic within a conventional north bridge chip already includes logic for such decision making, it is a relatively straightforward effort to provide a port (e.g., I/O pins, driver mechanisms, and perhaps buffers) for external arbitration signals called for by the present invention.

[**0028**] In operation, for an adaptive processor to become an arbitrating agent on the system memory bus of hybrid system, some motherboard layout changes would be needed. A Switch Network Adapter Port (SNAP) would be placed in one of the DIMM slots in the system. An additional header is added to the motherboard to provide connections to the chip selects of the other DIMM modules in the system. SNAP connects into this header are provided though a ribbon cable. This header would be 18 to 20 pins in size, for example. In a conventional computer system **100**, this header is unused and not populated on the motherboard. From this slot, SNAP **212** drives the address and command information to the other DIMM's in the system. Data is transferred to and from SNAP **212** across the data lines common to all DIMMs. The standard SSTL2 interface used in SDRAM's allows for multiple drivers to be present on the bus, thus the present invention may be implemented without requiring additional tri-state capability. As a result, the present invention contemplates minor modifications of the system chipset and motherboard and no modifications of conventional DIMM memory components.

[**0029**] In particular implementations of the present invention, the north bridge **202** is designed to be compatible with conventional systems such a system **100** in **FIG. 1**. Such compatibility enables the manufacture of a single IC that meets the demands of both conventional system **100** and hybrid system **200**, typically resulting in more efficient manufacturing. In such an implementation, the request line can be tied to an inactive state for conventional systems **100**, which would make the memory and I/O controller the sole agent arbitrating for memory system access.

[**0030**] With an ability to access memory subsystem **206** directly, the additional agents such as adaptive processor **210** see a low latency, and higher bandwidth memory accesses. In addition, microprocessor **204** is not needed in the data movement to adaptive processor **210**, thus freeing microprocessor **204** to perform other non-memory related tasks.

[**0031**] **FIG. 3** illustrates another embodiment of a hybrid system **300** in which the present invention is implemented. In the embodiment of **FIG. 3**, multiple adaptive processors **310** are provided using a crossbar **314** to couple to SNAP **312**. Although not shown, more than one SNAP **312** and microprocessor system can be connected into the crossbar switch **314**. Adaptive processors **310** are substantially equivalent to processor **210** in the description of **FIG. 2**, and SNAP device **312** is substantially equivalent to SNAP **212** in

**FIG. 2**. In the implementation of **FIG. 3**, crossbar **314** selectively couples one adaptive processor **310** to SNAP **312** such that from the perspective of SNAP **312**, a single adaptive processor **310** is connected. In this manner, SNAP **312** can be programmed to couple adaptive processors **310** to the memory bus and memory subsystem **306** is a manner substantially equivalent to that described in the implementation of **FIG. 2**. Crossbar **314** will require some form of arbitration/control to select a specific processor **310** to couple to SNAP **312**. In a particular example, this control function is implemented in the SNAP **312** interface and leverages control functions defined for communication with adaptive processors **310**, hence, no additional wiring or resources are required to implemented control of crossbar **314**. This can be implemented, for example, by logic configured within one or more of adaptive processors **310**, or by an external management agent (not shown). Alternatively, crossbar **314** may implement a round-robin selection of adaptive processors **310** to implement a time-sharing like algorithm for access to system memory **306**.

[**0032**] **FIG. 4** illustrates a hybrid system that differs from that shown in **FIG. 2** in that a plurality of processors **404** are coupled to the FSB in combination with external access to the memory bus. Adaptive processors **410** are substantially equivalent to processor **210** in the description of **FIG. 2**, and SNAP device **412** is substantially equivalent to SNAP **212** in **FIG. 2**. Some system chipsets include a memory and I/O controller **402** that can interface with multiple microprocessors **402** on the FSB. The memory transactions generated by microprocessors **404** are arbitrated with transaction requests from adaptive processor **410** to enable shared access to system memory **406**. Memory and I/O controller **402** may implement equal access to all processors **404** and **410**, or may offer preferred access to some. For example, all of the microprocessors **404** together may bet 50% access, while the remaining 50% is allocated to adaptive processor **410**. Enabling variable access bandwidth may require some modifications to the arbitration logic within memory and I/O controller **402**. It is contemplated that the programming within SNAP **412** may also be modified to account for more demanding access by processors **404**, for example, by regulating or governing the frequency with which adaptive processor **410** is allowed to access system memory **406**.

[**0033**] **FIG. 5** illustrates an implementation in which multiple processors **504** share FSB access to memory and I/O controller **502** while multiple adaptive processors **510** access memory and I/O controller **502** through SNAPs **512**. Because SNAP devices **512** are configurable, they can be configured to operate in parallel. SNAP-to-SNAP connection **512** may be a physical connection, or a virtual connection implemented through memory commands. Each adaptive processor **510** has access to the memory bus and therefore arbitrated access to system memory **506**. The implementation of **FIG. 5** leverages the arbitration mechanisms within memory and I/O controller **502** which include the ability to arbitrate amongst multiple requesting agents. SNAPs **512** include mechanisms to coordinate memory bus access amongst themselves, and may include mechanisms to self-govern the frequency with which memory bus accesses are asserted to account for increased access by multiple microprocessors **504**.

[**0034**] **FIG. 6** and **FIG. 7** illustrate exemplary embodiments in which arbitration control logic is implemented within a SNAP **612** or SNAP **712** rather than relying entirely on arbitration logic within a memory and I/O controller **602** or **702**. In some cases, the manufacturer of memory and I/O controller **602**/**702** may provide external access to the memory bus without direct access to the arbitration mechanisms. In this case, arbitration logic within SNAPs **612** and **712** will monitor the memory refresh signal on the memory bus. In a particular implementation, the memory refresh control is retained in the north bridge component **602**/**702** so that it remains compatible with conventional computer systems.

[**0035**] **FIG. 6** is a SMP computer system **600** that is similar to that shown in **FIG. 4**, but differs in that SNAP **612** implements arbitration logic external to memory and I/O controller **602**. This external arbitration logic enables adaptive processor **610** to access memory subsystem **606**. The memory and I/O component **602** asserts a request signal when an access to system memory is pending from one of microprocessors **604** or I/O bridge **608**. Memory refresh is implemented by causing memory and I/O component **602** to assert a refresh signal to SNAP **612** before a refresh cycle. On the next command cycle following the refresh signal, the memory refresh mechanisms within memory and I/O component **606** controls the memory bus to perform refresh of system memory **606**.

[**0036**] **FIG. 7** shows a SMP computer system **700** that is similar to that shown in **FIG. 5**, but differs in that SNAP **712** implements arbitration logic external to memory and I/O controller **702**. Like the implementation of **FIG. 6**, the use of external arbitration logic is implemented by providing a refresh signal from memory and I/O controller **702** to at least one SNAP **712** so that refresh functionality is retained by memory and I/O controller **702**. To use memory and I/O controller **702** in a conventional computer system **100**, the grant line is tied to a signal level indicating that the memory and I/O controller **702** is in control of the memory bus.

[**0037**] **FIG. 8** and **FIG. 9** illustrate exemplary timing diagrams for operating a computer system in accordance with the present invention. In **FIG. 8** and **FIG. 9**, the horizontal access represents increasing time, divided into cycles indicated by the clock signal. The vertical access represents signal level (e.g., voltage, current, or the like) indicating signal events over time. The request and grant signals in **FIG. 8** indicate the state of the arbitration bus labeled "ARB" in **FIG. 2**-**FIG. 5**. The request and grant signals in **FIG. 8** indicate the state of the arbitration bus labeled "ARB" in **FIG. 6** and **FIG. 7**, while the refresh signal line in **FIG. 9** indicates the state of the refresh line shown in **FIG. 6** and **FIG. 7**. In the upper region of each timing diagram clock cycles are designated "NB CMD" to indicate a time period when a north bridge command is asserted. (i.e. a command asserted by memory and I/O controller). In cycles labeled "SNAP CMD", a SNAP device controls the arbitrated memory bus, and in cycles labeled "REFRESH CMD" in **FIG. 9**, the refresh mechanisms (in the north bridge component in the particular examples) control the arbitrated memory bus. For convenience, the discussion of **FIG. 8** and **FIG. 9** will refer to a SNAP signal as a signal generated by any of SNAP devices **212**, **312**, **412**, **512**, **612**, or **712**. Likewise, memory and I/O controllers **202**, **302**, **402**, **30502**, **602**, and **702** will be referred to as the north bridge component.

[0038] In **FIG. 8**, the north bridge is initially in control of the memory bus. A SNAP device asserts a REQUEST signal, which is held in a request state until a GRANT is received one or more clock cycles later. The GRANT will be generated by the arbitration logic within the north bridge component according to arbitration algorithms implemented by the particular north bridge component. Upon assertion of a GRANT signal, the SNAP device has control of the memory bus until it releases the memory bus by dropping the REQUEST line. It is contemplated that some mechanism may be provided to force the SNAP device to relinquish control of the memory bus to avoid deadlock/live-lock situations. However, in the normal operation shown in **FIG. 8**, the arbitration logic within the north bridge component recognizes the de-assertion of the REQUEST signal and places the GRANT line low in a subsequent clock cycle, after which, the north bridge component retains control of the memory bus until a subsequent SNAP request is handled. For conventional operation, the GRANT line is tied permanently to a signal state indicating north bridge control (e.g., low in **FIG. 8**) so that north bridge component retains continuous control.

[0039] In **FIG. 9**, the north bridge is initially in control of the memory bus. The REQUEST/GRANT protocol is largely similar to that shown in **FIG. 8**, however, because arbitration logic is implemented in the SNAP devices, the SNAP device must be made aware of the REFRESH state of the memory system. As shown in **FIG. 9**, upon detection of a REFRESH signal indicating that the north bridge component is about to perform a refresh operation, the SNAP device relinquishes control by de-asserting the REQUEST and GRANT signals. Upon completion of the refresh cycle, the SNAP can once again arbitrate for control of the memory bus by asserting a REQUEST, and awaiting a GRANT that will be generated by the north bridge component's internal arbitration mechanisms. For conventional operation, the GRANT line is tied permanently to a signal state indicating north bridge control (e.g., low in **FIG. 8**), and the REQUEST/REFRESH lines are unused so that north bridge component retains continuous control.

[0040] While there have been described above the principles of the present invention in conjunction with specific computing system architectures and components, it is to be clearly understood that the foregoing description is made only by way of example and not as a limitation to the scope of the invention. Particularly, it is recognized that the teachings of the foregoing disclosure will suggest other modifications to those persons skilled in the relevant art. Such modifications may involve other features which are already known per se and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure herein also includes any novel feature or any novel combination of features disclosed either explicitly or implicitly or any generalization or modification thereof which would be apparent to persons skilled in the relevant art, whether or not such relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as confronted by the present invention. The applicants hereby reserve the right to formulate new claims to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

[0041] Although the invention has been described and illustrated with a certain degree of particularity, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the combination and arrangement of parts can be resorted to by those skilled in the art without departing from the spirit and scope of the invention, as hereinafter claimed.

We claim:

**1**. A computing system comprising:

at least one microprocessor;

a memory subsystem coupled to the at least one microprocessor;

a memory controller in a chipset of the computing system for issuing read and write commands to the memory subsystem and receiving data that results from the read and write commands coupled to manage memory transactions between the memory subsystem and the at least one microprocessor;

one or more external devices including an independent memory controller for issuing read and write commands to the memory subsystem and receiving data that results from the read and write commands coupled to the memory subsystem so as to have access to the memory subsystem without going through the memory controller; and

at least one arbitration port coupled to the memory controller and configured to receive an external arbitration signal from the one or more external devices, wherein the one or more external devices utilize the external arbitration signal to access the memory subsystem.

**2**. The computing system of claim 1 wherein the arbitration port is implemented in a north bridge component of a system chipset.

**3**. The computing system of claim 2 further comprising:

a plurality of interface ports implemented by the north bridge component, each of the plurality of interface ports supporting memory transactions from external systems; and

an arbitration mechanism within the north bridge component for arbitrating amongst the plurality of interface ports for access to the memory subsystem,

wherein the at least one arbitration port couples to the arbitration mechanism.

**4**. The computing system of claim 2 further comprising:

a plurality of interface ports implemented by the north bridge component, each of the plurality of interface ports supporting memory transactions from external systems;

an internal arbitration mechanism within the north bridge component for arbitrating amongst the plurality of interface ports for access to the memory subsystem; and

an external arbitration mechanism coupled to provide the arbitration signal over the arbitration port to the internal arbitration mechanism.

**5**. The computing system of claim 1 wherein the arbitration port is implemented in a memory controller.

**6**. The computing system of claim 1 wherein the memory controller is integrated with the at least one microprocessor and the arbitration port is implemented in the memory controller of the microprocessor.

**7**. The computing system of claim 1 wherein one or more external devices access the at least one arbitration port to conduct transactions with the memory subsystem.

**8**. A symmetric multiprocessor (SMP) computer system comprising:

at least two microprocessors;

a shared system memory;

a memory controller coupled to the shared system memory and the at least two microprocessors for issuing read and write commands to the shared system memory and receiving data that results from the read and write commands wherein the memory controller is implemented in a north bridge component of a system chipset;

one or more external devices including an independent memory controller for issuing read and write commands to the shared system memory and receiving data that results from the read and write commands coupled to the shared system memory such that a data path from the shared system memory to the at least one external device does not pass through the memory controller implemented in the north bridge component; and

a memory arbitration port within the memory controller and configured to receive an external arbitration signal from the one or more external devices to control the data flow of the data path.

**9**. The SMP computer system of claim 8 wherein an arbitration mechanism includes resources for preventing access to specified memory locations by a first of the at least two microprocessors when the specified memory locations are in use by a second of the at least two microprocessors.

**10**. The SMP computer system of claim 8 wherein an arbitration mechanism includes resources for reserving specified memory locations for exclusive access by a subset of the at least two microprocessors.

**11**. A computing system comprising:

at least one microprocessor;

a memory subsystem;

an IO subsystem;

a memory/IO controller in a chipset of the computing system coupled to manage transactions between the memory subsystem and the I/O subsystem and the at least one microprocessor;

one or more external devices containing independent memory controllers to couple the external devices to the memory subsystem so as to have access to the memory subsystem without utilizing the memory IO controller of the chipset, wherein one of the external devices includes a memory request arbiter; and

at least one arbitration port coupled to the memory/IO controller of the chipset and configured to receive an external arbitration signal from the external device including the request arbiter,

wherein the one or more external devices utilize the external arbitration signal to gain direct access to perform autonomous transactions to the memory subsystem.

**12**. The computing system of claim 11 wherein the arbitration mechanism is implemented in a memory/IO component of a system chipset.

**13**. The computing system of claim 12 further comprising:

a plurality of interface ports implemented by the north bridge component, each of the plurality of interface ports supporting memory transactions from external systems; and

an arbitration mechanism within the north bridge component for arbitrating amongst the plurality of interface ports for access to the memory subsystem,

wherein the at least one arbitration port couples to the arbitration mechanism.

**14**. The computing system of claim 12 further comprising:

a plurality of interface ports implemented by the north bridge component, each of the plurality of interface ports supporting memory transactions from external systems;

an internal arbitration mechanism within the north bridge component for arbitrating amongst the plurality of interface ports for access to the memory subsystem; and

an external arbitration mechanism coupled to provide the arbitration signal over the arbitration port to the internal arbitration mechanism.

**15**. The computing system of claim 11 wherein the memory controller is integrated with the at least one microprocessor and the request arbiter is implemented in the memory controller of the microprocessor.

**16**. A symmetric multiprocessor (SMP) computer system comprising:

at least two microprocessors;

a memory subsystem;

a memory/IO controller coupled to the memory subsystem and the at least two microprocessors wherein the memory/IO controller is implemented in a system chipset;

one or more external devices containing memory controllers coupled to the memory subsystem such that the external devices have an independent transaction path to and from the memory;

a memory arbitration port within the memory/IO controller of the chipset and configured to receive an external arbitration signal from the one or more external devices; and

a transaction arbiter in one of the external devices to provide the arbitration control signal to the memory/IO controller in the chipset.

**17**. The SMP computer system of claim 16 wherein an arbitration mechanism includes resources for preventing access to specified memory locations by a first of the at least two microprocessors when the specified memory locations are in use by a second of the at least two microprocessors.

**18**. The SMP computer system of claim 16 wherein an arbitration mechanism includes resources for reserving specified memory locations for exclusive access by a subset of the at least two microprocessors.

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