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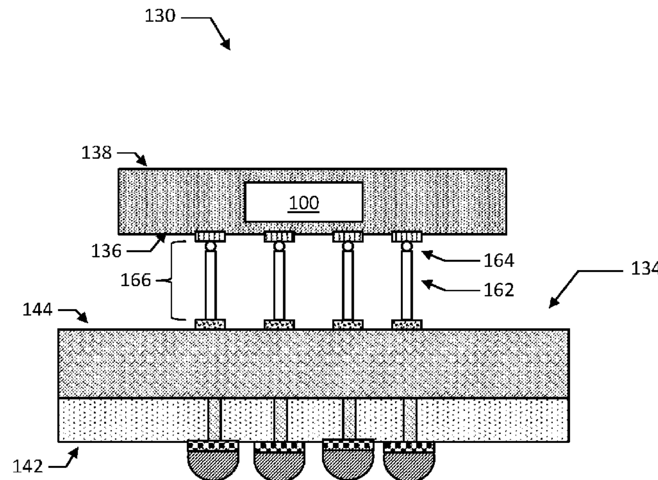

FIG. 3

132 140 146 148 150 152 154 158

(57) Abstract: Disclosed herein are qubit device packages, as well as related computing devices and methods. An exemplary qubit device package includes a quantum die and a package substrate. The face of the quantum die that houses one or more quantum circuit components is electrically connected to the package substrate by first level interconnects in the form of conductive pillars. Implementing the first level interconnects as conductive pillars allows providing sufficient distance between the quantum die and the package substrate to reduce TLS losses caused by the package substrate while, at the same time, keeping the overall footprint of the interconnects relatively small, thus providing a scalable approach to reducing quantum losses. In addition, the relatively small footprint of the conductive pillars allows providing them sufficiently close to one another to ensure improved isolation/shielding between different signal lines.

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LOW LOSS HIGH ISOLATION FIRST LEVEL INTERCONNECTS FOR QUBIT DEVICE PACKAGES

Background

[0001] Quantum computing refers to the field of research related to computation systems that use quantum mechanical phenomena to manipulate data. These quantum mechanical phenomena, such as superposition (in which a quantum variable can simultaneously exist in multiple different states) and entanglement (in which multiple quantum variables have related states irrespective of the distance between them in space or time), do not have analogs in the world of classical computing, and thus cannot be implemented with classical computing devices. For example, classical computers encode data into binary values, commonly referred to as bits, where, at any given time, a bit is always in only one of two states – it is either 0 or 1. Quantum computers use so-called quantum bits, referred to as qubits (both terms “bits” and “qubits” often interchangeably refer to the values that they hold as well as to the actual devices that store the values). Similar to a bit of a classical computer, at any given time, a qubit can be either 0 or 1. However, in contrast to a bit of a classical computer, a qubit can also be 0 and 1 at the same time, which is a result of superposition of quantum states. Entanglement also contributes to the unique nature of qubits in that input data to a quantum processor can be spread out among entangled qubits, allowing manipulation of that data to be spread out as well: providing input data to one qubit results in that data being shared to other qubits with which the first qubit is entangled.

[0002] “Qubit devices” refer to devices that include one or more dies which host one or more quantum circuit components (i.e. circuit components comprising qubits). A die hosting one or more quantum circuit components may be referred to in the following as a “quantum die.” Packaging of qubit devices also requires considerations not found in the world of classical computing. For example, presence of a package substrate in the vicinity of a quantum die causes significant losses for certain types of qubits, the losses thought to be attributed to the undesirable presence of two-level systems (TLS) in a typical package substrate – a uniquely quantum phenomenon. Indirectly, TLS losses also present challenges for providing sufficient isolation/shielding in terms of electromagnetic interference between different signal line interconnects between a package substrate and a qubit device package in a way that would allow providing a large number of quantum circuit components in a single qubit device package (i.e. in a way that is scalable). Thus, providing electrical interconnects between a package substrate and a qubit device package (such interconnects commonly referred to as “first level interconnects”) remains a challenge in terms of enabling low losses and high isolation while, at the same time, keeping the overall footprint of the interconnects small enough to be scalable.

Brief Description of the Drawings

[0003] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0004] FIG. 1 provides a schematic illustration of an exemplary device implementing superconducting qubits, according to some embodiments of the present disclosure.

[0005] FIG. 2 provides a schematic illustration of an exemplary physical layout of a device implementing superconducting qubits, according to some embodiments of the present disclosure.

[0006] FIG. 3 provides a schematic illustration of an exemplary qubit device package coupling a die with a qubit device to a package substrate with a front metallization stack using conductive pillars as first level interconnects, according to some embodiments of the present disclosure.

[0007] FIG. 4 is a flow diagram of a first illustrative method of manufacturing a qubit device package with first level interconnects in the form of conductive pillars, according to some embodiments of the present disclosure.

[0008] FIGS. 5A-5D provide schematic illustrations of a device package at different stages of manufacturing when the method shown in FIG. 4 is used, according to some embodiments of the present disclosure.

[0009] FIG. 6 is a flow diagram of a second illustrative method of manufacturing a qubit device package with first level interconnects in the form of conductive pillars, according to some embodiments of the present disclosure.

[0010] FIGS. 7A-7D provide schematic illustrations of a device package at different stages of manufacturing when the method shown in FIG. 6 is used, according to some embodiments of the present disclosure.

[0011] FIG. 8 is a flow diagram of a third illustrative method of manufacturing a qubit device package with first level interconnects in the form of conductive pillars, according to some embodiments of the present disclosure.

[0012] FIGS. 9A-9D provide schematic illustrations of a device package at different stages of manufacturing when the method shown in FIG. 8 is used, according to some embodiments of the present disclosure.

[0013] FIG. 10 provides a schematic illustration of ground shields formed using the conductive pillars, according to some embodiments of the present disclosure.

[0014] FIG. 11 provides a schematic illustration of partially hexagonal ground shields formed using the conductive pillars, according to some embodiments of the present disclosure.

[0015] FIG. 12 provides a schematic illustration of open coaxial ground shields formed using the conductive pillars, according to some embodiments of the present disclosure.

[0016] FIGS. 13A and 13B are top views of a wafer and dies that may include one or more of conductive pillar first level interconnects disclosed herein, according to some embodiments of the present disclosure.

[0017] FIG. 14 is a cross-sectional side view of a device assembly that may include one or more of conductive pillar first level interconnects disclosed herein, according to some embodiments of the present disclosure.

[0018] FIG. 15 is a block diagram of an example quantum computing device that may include one or more of conductive pillar first level interconnects disclosed herein, in accordance with various embodiments.

Detailed Description

Overview

[0019] Disclosed herein are qubit device packages, as well as related computing devices and methods. An exemplary qubit device package may include a die and a package substrate. One or more quantum circuit components are disposed on one face of the die (hence, the die is a "quantum die"), and that face of the die is electrically connected to the package substrate by first level interconnects in the form of electrically conductive (e.g. metal) pillars. Implementing the first level interconnects as conductive pillars which may have a relatively high aspect ratio (i.e. a ratio between a height and a width of a pillar) allows providing sufficient distance between the quantum die and the package substrate to reduce TLS losses caused by the package substrate while, at the same time, keeping the overall footprint of the interconnects relatively small. Reducing the footprint allows providing fine pitch, high density first level interconnects, thus providing a scalable approach to reducing quantum losses. In addition, the relatively small footprint of the conductive pillars allows providing them sufficiently close to one another to ensure improved isolation in terms of electromagnetic interference (i.e. improved shielding) between different signal lines.

[0020] While some embodiments are explained herein with reference to transmons, one class of superconducting qubits, subject matter disclosed herein is not limited in this regard and may include other embodiments of quantum circuits implementing other classes of superconducting qubits, or quantum circuits implementing qubits other than superconducting qubits, all of which are within the scope of the present disclosure.

[0021] In order to provide substantially lossless connectivity to, from, and between the qubits, some or all of the electrically conductive portions of qubit devices/assemblies proposed herein, i.e. signal lines, ground planes, resonators, electrodes, etc., may be made from one or more

superconducting/superconductive materials. However, some or all of these electrically conductive portions could be made from electrically conductive materials which are not superconducting. In the following, unless specified otherwise, reference to an electrically conductive material implies that a superconducting material can be used. Furthermore, materials described herein as "superconducting materials" may refer to materials, including alloys of materials, which exhibit superconducting behavior at typical qubit operating conditions (e.g. materials which exhibit superconducting behavior at very low temperatures at which qubits typically operate, which materials may, or may not, exhibit such behavior at e.g. room temperatures).

[0022] In the following detailed description, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present disclosure may be practiced without the specific details or/and that the present disclosure may be practiced with only some of the described aspects. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0023] For purposes of explanation, reference is made to the accompanying drawings that form a part hereof, and in which are shown, by way of illustration, embodiments that may be practiced. The accompanying drawings are not necessarily drawn to scale. For example, to clarify various layers, structures, and regions, the thickness of some layers may be enlarged. Furthermore, while drawings illustrating various structures/assemblies of exemplary devices may be drawn with precise right angles and straight lines, real world process limitations may prevent implementations of devices exactly as shown. Therefore, it is understood that such drawings revised to reflect example real world process limitations, in that the features may not have precise right angles and straight lines, are within the scope of the present disclosure. Drawings revised in this manner may be more representative of real world structure/assemblies as may be seen on images using various characterization tools, such as e.g. scanning electron microscopy (SEM) or transmission electron microscopy (TEM). In addition, the various structures/assemblies of the present drawings may further include possible processing defects, such as e.g. the rounding of corners, the drooping of the layers/lines, unintentional gaps and/or discontinuities, unintentionally uneven surfaces and volumes, etc., although these possible processing defects may not be specifically shown in the drawings. It is to be understood that other embodiments may be utilized and structural or logical changes to the drawings and descriptions may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0024] Various operations may be described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of

description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0025] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges. The meaning of "a," "an," and "the" include plural references. The meaning of "in" includes "in" and "on."

[0026] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. Furthermore, stating in the present disclosure that any part (e.g. a layer, film, area, or plate) is in any way positioned on or over (e.g. positioned on/over, provided on/over, located on/over, disposed on/over, formed on/over, etc.) another part means that the referenced part is either in contact with the other part, or that the referenced part is above the other part with one or more intermediate part(s) located therebetween. On the other hand, stating that any part is in contact with another part means that there is no intermediate part between the two parts.

[0027] The terms “substantially,” “close,” “approximately,” “near,” and “about,” generally refer to being within +/- 20% of a target value. Unless otherwise specified, the use of the ordinal adjectives “first,” “second,” and “third,” etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0028] In the following detailed description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. In some examples, as used herein, the terms “oxide,” “carbide,” “nitride,” etc. refer to compounds containing, respectively, oxygen, carbon, nitrogen, etc. In another example, the term "connected" means a direct electrical or magnetic connection between the things that are connected, without any intermediary devices, while the term "coupled"

means either a direct electrical or magnetic connection between the things that are connected or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means one or more passive and/or active components that are arranged to cooperate with one another to provide a desired function.

[0029] In yet other examples, as used herein, terms indicating what may be considered an idealized behavior, such as e.g. "superconducting" or "lossless", are intended to cover functionality that may not be exactly ideal but is within acceptable margins for a given application. For example, a certain level of loss, either in terms of non-zero electrical resistance or non-zero amount of spurious TLS may be acceptable such that the resulting materials and structures may still be referred to by these "idealized" terms. Specific values associated with an acceptable level of loss are expected to change over time as fabrication precision will improve and as fault-tolerant schemes may become more tolerant of higher losses, all of which are within the scope of the present disclosure.

[0030] Furthermore, while the present disclosure may include references to microwave signals, this is done only because current qubits are designed to work with such signals because the energy in the microwave range is higher than thermal excitations at the temperature that qubits are operated at. In addition, techniques for the control and measurement of microwaves are well known. For these reasons, typical frequencies of qubits are in 2-10 gigahertz (GHz) range, in order to be higher than thermal excitations, but low enough for ease of microwave engineering. However, advantageously, because excitation energy of qubits is controlled by the circuit elements, qubits can be designed to have any frequency. Therefore, in general, qubits could be designed to operate with signals in other ranges of electromagnetic spectrum and embodiments of the present disclosure could be modified accordingly. All of these alternative implementations are within the scope of the present disclosure.

Quantum computing and superconducting qubits

[0031] As previously described herein, quantum computing, or quantum information processing, refers to the field of research related to computation systems that use quantum-mechanical phenomena to manipulate data. One example of quantum-mechanical phenomena is the principle of quantum superposition, which asserts that any two or more quantum states can be added together, i.e. superposed, to produce another valid quantum state, and that any quantum state can be represented as a sum of two or more other distinct states. Quantum entanglement is another example of quantum-mechanical phenomena. Entanglement refers to groups of particles being generated or interacting in such a way that the state of one particle becomes intertwined with that of the others. Furthermore, the quantum state of each particle cannot be described independently. Instead, the quantum state is given for the group of entangled particles as a whole. Yet another example of quantum-mechanical phenomena is sometimes described as a "collapse" because it

asserts that when we observe (measure) particles, we unavoidably change their properties in that, once observed, the particles cease to be in a state of superposition or entanglement (i.e. by trying to ascertain anything about the particles, we collapse their state).

[0032] Put simply, superposition postulates that a given particle can be simultaneously in two states, entanglement postulates that two particles can be related in that they are able to instantly coordinate their states irrespective of the distance between them in space and time, and collapse postulates that when one observes a particle, one unavoidably changes the state of the particle and its' entanglement with other particles. These unique phenomena make manipulation of data in quantum computers significantly different from that of classical computers (i.e. computers that use phenomena of classical physics). As previously described herein, quantum computers use qubits where, similar to a bit of a classical computer, at any given time, a qubit can be either 0 or 1, but, in contrast to a bit of a classical computer, a qubit can also be 0 and 1 at the same time, which is a result of superposition of quantum states. Furthermore, entanglement also contributes to the unique nature of qubits in that input data to a quantum processor can be spread out among entangled qubits, allowing manipulation of that data to be spread out as well: providing input data to one qubit results in that data being shared to other qubits with which the first qubit is entangled.

[0033] Compared to well-established and thoroughly researched classical computers, quantum computing is still in its infancy, with the highest number of qubits in a solid-state quantum processor currently being about 10. One of the main challenges resides in protecting qubits from decoherence so that they can stay in their information-holding states long enough to perform the necessary calculations and read out the results.

[0034] As the foregoing illustrates, ability to manipulate and read out quantum states, making quantum-mechanical phenomena visible and traceable, and ability to deal with and improve on the fragility of quantum states of a qubit present unique challenges not found in classical computers. These challenges explain why so many current efforts of the industry and the academics continue to focus on a search for new and improved physical systems whose functionality could approach that expected of theoretically designed qubits. Physical systems for implementing qubits that have been explored until now include e.g. superconducting (SC) qubits, single trapped ion qubits, Silicon (Si) quantum dot qubits, photon polarization qubits, etc.

[0035] Out of the various physical implementations of qubits listed above, superconducting qubits are promising candidates for building a quantum computer.

[0036] All of superconducting qubits operate based on the Josephson effect, which refers to a macroscopic quantum phenomenon of supercurrent, i.e. a current that, due to zero electrical resistance, flows indefinitely long without any voltage applied, across a device known as a Josephson

Junction. Josephson Junctions are integral building blocks in superconducting quantum circuits where they form the basis of quantum circuit elements that can approximate functionality of theoretically designed qubits.

[0037] Within superconducting qubit implementations, three classes are typically distinguished: charge qubits, flux qubits, and phase qubits. Transmons, a type of charge qubits with the name being an abbreviation of “transmission line shunted plasma oscillation qubits”, are particularly encouraging because they exhibit reduced sensitivity to charge noise.

[0038] In implementations when superconducting qubits are implemented as transmon qubits, two basic elements of superconducting quantum circuits are inductors and capacitors. However, circuits made using only these two elements cannot make a system with two energy levels because, due to the even spacing between the system’s energy levels, such circuits will produce harmonic oscillators with a ladder of equivalent states. A nonlinear element is needed to have an effective two-level quantum state system, or qubit. Josephson Junction is an example of such non-linear, non-dissipative circuit element. Thus, Josephson Junctions may be viewed as the central circuit elements of a quantum computer based on superconducting qubits.

[0039] A Josephson Junction includes two superconductors connected by a weak link. For example, a Josephson Junction may be implemented as a thin layer of an insulating material, referred to as a barrier or a tunnel barrier and serving as the “weak link” of the junction, sandwiched between two layers of superconductor, where a Josephson Junction acts as a superconducting tunnel junction.

[0040] In transmons, LC circuits formed using Josephson Junctions as inductors have uneven spacing between their energy states, thus providing an effective two-level quantum state system. In other classes of superconducting qubits, Josephson Junctions combined with other circuit elements have similar functionality of providing the non-linearity necessary for forming effective two-level quantum states, or qubits. In other words, when implemented in combination with other circuit elements (e.g. capacitors in transmons or superconducting loops in flux qubits), one or more Josephson Junctions allow realizing a quantum circuit element which has uneven spacing between its energy levels resulting in a unique ground and excited state system for the qubit. This is illustrated in FIG. 1, providing a schematic illustration of a superconducting quantum circuit 100, according to some embodiments of the present disclosure.

[0041] As shown in FIG. 1, an exemplary superconducting quantum circuit 100 may include two or more qubits: 102-1 and 102-2. Qubits 102-1 and 102-2 may be identical and thus the discussion of FIG. 1 refers generally to the “qubit 102,” and the same applies to referring to Josephson Junctions 104-1 and 104-2 generally as “Josephson Junctions 104” and referring to circuit elements 106-1 and 106-2 generally as “circuit elements 106.” As shown in FIG. 1, each of the superconducting qubits

102 may include one or more Josephson Junctions 104 connected to one or more other circuit elements 106, which, in combination with the Josephson Junction(s) 104, form a non-linear circuit providing a unique two-level quantum state for the qubit. The circuit elements 106 could be e.g. capacitors in transmons or superconducting loops in flux qubits.

[0042] FIG. 1 further illustrates that the exemplary superconducting quantum circuit 100 may also include interconnects 107, which interconnects may include first level interconnects in the form of electrically conductive (e.g. metal) pillars as described herein.

[0043] Further, as also shown in FIG. 1, an exemplary superconducting quantum circuit 100 may include means 108 for providing external control of qubits 102 and means 110 for providing internal control of qubits 102. In this context, "external control" refers to controlling the qubits 102 from outside of, e.g., an integrated circuit (IC) chip comprising the qubits, including control by a user of a quantum computer, while "internal control" refers to controlling the qubits 102 within the IC chip. For example, if qubits 102 are transmon qubits, external control may be implemented by means of flux bias lines (also known as "flux lines" and "flux coil lines") and by means of readout and drive lines (also known as "microwave lines" since qubits are typically designed to operate with microwave signals), described in greater detail below. On the other hand, internal control lines for such qubits may be implemented by means of resonators, e.g., coupling and readout resonators, also described in greater detail below.

[0044] Any one of the qubits 102, the external control means 108, and the external control means 110 of the quantum circuit 100 may be provided on, over, or at least partially embedded in a substrate (not shown in FIG. 1).

[0045] FIG. 2 provides a schematic illustration of an exemplary physical layout 111 of a superconducting quantum circuit where qubits are implemented as transmons, according to some embodiments of the present disclosure.

[0046] Similar to FIG. 1, FIG. 2 illustrates two qubits 102. In addition, FIG. 2 illustrates flux bias lines 112, microwave lines 114, a coupling resonator 116, a readout resonator 118, and conductive contacts 120 and 122. The flux bias lines 112 and the microwave lines 114 may be viewed as examples of the external control means 108 shown in FIG. 1. The coupling resonator 116 and the readout resonator 118 may be viewed as examples of the internal control means 110 shown in FIG.1.

[0047] Running a current through the flux bias lines 112, provided from the conductive contacts 120, allows tuning (i.e. changing) the frequency of the corresponding qubits 102 to which each line 112 is connected. In general, it operates in the following manner. As a result of running the current in a particular flux bias line 112, magnetic field is created around the line. If such a magnetic field is in sufficient proximity to the qubit 102, e.g. by a portion of the flux bias line 112 being provided next

to the qubit 102, the magnetic field couples to the qubit, thereby changing the spacing between the energy levels of the qubit. This, in turn, changes the frequency of the qubit since the frequency is directly related to the spacing between the energy levels via Planck's equation. The Planck's equation is $E=h\nu$, where E is the energy (in this case the energy difference between energy levels of a qubit), h is the Planck's constant and ν is the frequency (in this case the frequency of the qubit). As this equation illustrates, if E changes, then ν changes. Provided there is sufficient multiplexing, different currents can be sent down each of the flux lines allowing for independent tuning of the various qubits.

[0048] Typically, the qubit frequency may be controlled in order to bring the frequency either closer to or further away from another resonant item, for example a coupling resonator such as 116 shown in FIG. 2 that connects two or more qubits together, as may be desired in a particular setting.

[0049] For example, if it is desirable that a first qubit 102 (e.g. the qubit 102 shown on the left side of FIG. 2) and a second qubit 102 (e.g. the qubit 102 shown on the right side of FIG. 2) interact, via the coupling resonator 116 connecting these qubits, then both qubits 102 may need to be tuned to be at nearly the same frequency. One way in which such two qubits could interact is that, if the frequency of the first qubit 102 is tuned very close to the resonant frequency of the coupling resonator 116, the first qubit can, when in the excited state, relax back down to the ground state by emitting a photon (similar to how an excited atom would relax) that would resonate within the coupling resonator 116. If the second qubit 102 is also at this energy (i.e. if the frequency of the second qubit is also tuned very close to the resonant frequency of the coupling resonator 116), then it can absorb the photon emitted from the first qubit, via the coupling resonator 116, and be excited from its ground state to an excited state. Thus, the two qubits interact in that a state of one qubit is controlled by the state of another qubit. In other scenarios, two qubits could interact via a coupling resonator at specific frequencies, but these three elements do not have to be tuned to be at nearly the same frequency with one another. In general, two or more qubits could be configured to interact with one another by tuning their frequencies to specific values or ranges.

[0050] On the other hand, it may sometimes be desirable that two qubits coupled by a coupling resonator do not interact, i.e. the qubits are independent. In this case, by applying magnetic flux, by means of controlling the current in the appropriate flux bias line, to one qubit it is possible to cause the frequency of the qubit to change enough so that the photon it could emit no longer has the right frequency to resonate on the coupling resonator. If there is nowhere for such a frequency-detuned photon to go, the qubit will be better isolated from its surroundings and will live longer in its current state. Thus, in general, two or more qubits could be configured to avoid or eliminate interactions with one another by tuning their frequencies to specific values or ranges.

[0051] The state(s) of each qubit 102 may be read by way of its corresponding readout resonator 118. As explained below, the qubit 102 induces a resonant frequency in the readout resonator 118. This resonant frequency is then passed to the microwave lines 114 and communicated to the pads 122.

[0052] To that end, a readout resonator 118 may be provided for each qubit. The readout resonator 118 may be a transmission line that includes a capacitive connection to ground on one side and is either shorted to the ground on the other side (for a quarter wavelength resonator) or has a capacitive connection to ground (for a half wavelength resonator), which results in oscillations within the transmission line (resonance), with the resonant frequency of the oscillations being close to the frequency of the qubit. The readout resonator 118 is coupled to the qubit by being in sufficient proximity to the qubit 102, more specifically in sufficient proximity to the capacitor of the qubit 102, when the qubit is implemented as a transmon, either through capacitive or inductive coupling. Due to a coupling between the readout resonator 118 and the qubit 102, changes in the state of the qubit 102 result in changes of the resonant frequency of the readout resonator 118. In turn, because the readout resonator 118 is in sufficient proximity to the microwave line 114, changes in the resonant frequency of the readout resonator 118 induce changes in the current in the microwave line 114, and that current can be read externally via the wire bonding pads 122.

[0053] The coupling resonator 116 allows coupling different qubits together, e.g. as described above, in order to realize quantum logic gates. The coupling resonator 116 is similar to the readout resonator 118 in that it is a transmission line that includes capacitive connections to ground on both sides (i.e. a half wavelength resonator), which also results in oscillations within the coupling resonator 116. Each side of the coupling resonator 116 is coupled (again, either capacitively or inductively) to a respective qubit by being in sufficient proximity to the qubit, namely in sufficient proximity to the capacitor of the qubit, when the qubit is implemented as a transmon. Because each side of the coupling resonator 116 has coupling with a respective different qubit, the two qubits are coupled together through the coupling resonator 116. In this manner, state of one qubit depends on the state of the other qubit, and the other way around. Thus, coupling resonators may be employed in order to use a state of one qubit to control a state of another qubit.

[0054] In some implementations, the microwave line 114 may be used to not only readout the state of the qubits as described above, but also to control the state of the qubits. When a single microwave line is used for this purpose, the line operates in a half-duplex mode where, at some times, it is configured to readout the state of the qubits, and, at other times, it is configured to control the state of the qubits. In other implementations, microwave lines such as the line 114 shown in FIG. 2 may be used to only readout the state of the qubits as described above, while

separate drive lines such as e.g. drive lines 124 shown in FIG. 2, may be used to control the state of the qubits. In such implementations, the microwave lines used for readout may be referred to as readout lines (e.g. readout line 114), while microwave lines used for controlling the state of the qubits may be referred to as drive lines (e.g. drive lines 124). The drive lines 124 may control the state of their respective qubits 102 by providing, using e.g. conductive contacts 126 as shown in FIG. 2, a microwave pulse at the qubit frequency, which in turn stimulates (i.e. triggers) a transition between the states of the qubit. By varying the length of this pulse, a partial transition can be stimulated, giving a superposition of the states of the qubit.

[0055] Flux bias lines, microwave lines, coupling resonators, drive lines, and readout resonators, such as e.g. those described above, together form interconnects for supporting propagation of microwave signals. Further, any other connections for providing direct electrical interconnection between different quantum circuit elements and components, such as e.g. connections from electrodes of Josephson Junctions to plates of the capacitors or to superconducting loops of superconducting quantum interference devices (SQUIDS) or connections between two ground lines of a particular transmission line for equalizing electrostatic potential on the two ground lines, are also referred to herein as interconnects. Still further, the term "interconnect" may also be used to refer to elements providing electrical interconnections between quantum circuit elements and components and non-quantum circuit elements, which may also be provided in a quantum circuit, as well as to electrical interconnections between various non-quantum circuit elements provided in a quantum circuit. Examples of non-quantum circuit elements which may be provided in a quantum circuit may include various analog and/or digital systems, e.g. analog to digital converters, mixers, multiplexers, amplifiers, etc.

[0056] Coupling resonators and readout resonators may be configured for capacitive coupling to other circuit elements at one or both ends in order to have resonant oscillations, whereas flux bias lines and microwave lines may be similar to conventional microwave transmission lines because there is no resonance in these lines. Each one of these interconnects may be implemented as any suitable architecture of a microwave transmission line, such as e.g. a coplanar waveguide, a stripline, a microstrip line, or an inverted microstrip line. Typical materials to make the interconnects include aluminum (Al), niobium (Nb), niobium nitride (NbN), titanium nitride (TiN), molybdenum rhenium (MoRe), and niobium titanium nitride (NbTiN), all of which are particular types of superconductors. However, in various embodiments, other suitable superconductors and alloys of superconductors may be used as well.

[0057] In various embodiments, the interconnects as shown in FIG. 2 could have different shapes and layouts. For example, some interconnects may comprise more curves and turns while other

interconnects may comprise less curves and turns, and some interconnects may comprise substantially straight lines. In some embodiments, various interconnects may intersect one another, in such a manner that they don't make an electrical connection, which can be done by using e.g. a bridge, bridging one interconnect over the other. As long as these interconnects operate in accordance with use of these interconnects as known in the art for which some exemplary principles were described above, quantum circuits with different shapes and layouts of the interconnects than those illustrated in FIG. 2 are all within the scope of the present disclosure.

[0058] In addition, FIG. 2 further illustrates ground conductive contacts (i.e. contacts connecting to the ground plane) 128. As is known in the art, such ground contacts are typically used when a die supports propagation of microwave signals in order to e.g. suppress microwave parallel plate modes, cross-coupling between circuital blocks, and substrate resonant modes. In general, providing ground pathways may improve signal quality, enable fast pulse excitation and improve the isolation between the different lines.

[0059] Only two ground contacts are labeled in FIG. 2 with the reference numeral 128, but all white circle shown throughout the die housing the quantum circuit 111 are intended to illustrate exemplary locations of ground conductive contacts, e.g. conductive bumps, to be connected to the interposer substrate. The illustration of the location and the number of the ground contacts 128 in FIG. 2 is purely illustrative and, in various embodiments, ground contacts 128 may be provided at different places, as known in microwave engineering. The signal conductive contacts 120, 122, and 126 are used for programming, tuning and readout of the qubits. The die on which these conductive contacts and the rest of the quantum circuit are provided may consist of multiple conductive layers that may be electrically isolated from each other by an insulating material, which could include any suitable material, such as an interlayer dielectric (ILD). Examples of insulating materials may include silicon oxide, silicon nitride, aluminum oxide, carbon-doped oxide, and/or silicon oxynitride.

[0060] Any one of the conductive contacts as shown in FIG. 2 may be coupled to corresponding conductive contacts of a package substrate using first level interconnects in the form of electrically conductive (e.g. metal) pillars as described herein.

[0061] While FIGs. 1 and 2 illustrate examples of quantum circuits comprising only two qubits 102, embodiments with any larger number of qubits are possible and are within the scope of the present disclosure. Furthermore, while FIGs. 1 and 2 illustrate embodiments specific to transmons, subject matter disclosed herein is not limited in this regard and may include other embodiments of quantum circuits implementing other types of superconducting qubits, or quantum circuits implementing qubits other than superconducting qubits, all of which are within the scope of the present disclosure.

Flip-chip packaging assembly for superconducting qubits

[0062] In some embodiments, the quantum circuit 100, e.g. as illustrated with the physical layout 111, may be included in/on a die and coupled to a package substrate to form a SC qubit device package. For example, FIG. 3 illustrates some embodiments of the present disclosure showing a SC qubit device package 130 in which a SC quantum circuit 100 is included in a die 132, and the die 132 is coupled to a package substrate 134.

[0063] Some of the elements referred in the description of FIG. 3 with reference numerals are indicated in FIG. 3 with different patterns, with a legend showing the correspondence between the reference numerals and patterns being provided at the bottom of FIG. 3, and are not labeled in FIG. 3 with arrows pointing to them in order to not clutter the drawing. For example, the legend illustrates that FIG. 3 uses different patterns to show the die 132, conductive contacts 140, 148, and 150, etc.

[0064] The die 132 may include a first face 136 and an opposing second face 138. Various quantum circuit components in the form of e.g. the qubits 102 and the resonators 116/118 may be proximate to or provided on the first face 136, and conductive pathways may extend over/in the die 132 and be coupled between these elements and the conductive contacts 120, 122, 126, and 128, also disposed at the first face 136. A plurality of the conductive contacts 120, 122, 126, and 128 which may be disposed at the first face 136 of the SC qubit die 132 are schematically illustrated in FIG. 3 as conductive contacts 140. The conductive pathways between the various quantum circuit components and the conductive contacts 140 are not specifically shown in FIG. 3 because the details of the SC quantum circuit 100 are not specifically shown in FIG. 3, but could be in the form of e.g. one or more of flux bias lines 112, microwave lines 114, and drive lines 124, and may be implemented as conductive vias, conductive lines, and/or any combination of conductive vias and lines. In some embodiments, such conductive pathways are also disposed on the first face 136 of the die 132.

[0065] The package substrate 134 may include a first face 142 and an opposing second face 144. As shown in FIG. 3, conductive contacts 150 may be disposed at the second face 144. Furthermore, in some optional embodiments, conductive contacts 148 may be disposed at the first face 142. In such optional embodiments, conductive pathways 152 may extend through an insulating material 154 of the package substrate 134 between the first face 142 and the second face 144 of the package substrate 134, electrically coupling various ones of the conductive contacts 148 to various ones of the conductive contacts 150, in any desired manner. The conductive pathways 152 may include one or more conductive vias, one or more conductive lines, or a combination of conductive vias and conductive lines, for example. The conductive pathways 152 may e.g. provide electrical connectivity

to second level interconnects 158 (also optional), in case the package substrate 134 is coupled to further components, such as e.g. a circuit board, not specifically shown in FIG. 3 because connectivity to further components via the second level interconnects 158 is optional. In case the second level interconnects 158 are used, the conductive contacts 148 at the first face 142 of the package substrate 134 may be used to connect the conductive pathways with the second level interconnects 158, as shown in FIG. 3.

[0066] FIG. 3 further illustrates first level interconnects implemented in the form of, at least, conductive pillars 162 coupling the conductive contacts 140 at the first face 136 of the quantum die 132 and the conductive contacts 150 at the opposing face of the package substrate 134 (i.e. at the second face 144). As shown in FIG. 3, optionally, the first level interconnects 166 may further include solder bumps 164, e.g. for improving electrical connectivity between the conductive contacts 140 at the first face 136 of the die 132 and the conductive pillars 162. The solder bumps 164 are shown in FIG. 3 as while circles associated with the conductive contacts 140 (i.e. between the conductive contacts 140 and the conductive pillars 162).

[0067] How electrical connections are made for the signal and ground conductive contacts on a die and on a package substrate is well-known in the art of packaging and, therefore, in the interests of brevity, not described here in detail. In general, connections are made by providing a metallization stack on, or as a part of, the second face 144 of the package substrate 134, schematically shown as a metallization stack 146 in FIG. 3.

[0068] Having first level interconnects 166 disposed between the first face 136 of the die 132 and the second face 144 of the package substrate 134 (e.g., using such interconnects as a part of flip chip packaging techniques) may enable the SC qubit device package 130 to achieve a smaller footprint and higher die-to-package-substrate connection density than could be achieved using conventional wirebond techniques (in which conductive contacts between the die 132 and the package substrate 134 are constrained to be located on the periphery of the die 132). For example, a die 132 having a square first face 136 with side length N may be able to form 4N wirebond interconnects to the package substrate 134, versus N2 flip chip interconnects (utilizing the entire "full field" surface area of the first face 136). Additionally, in some applications, wirebond interconnects may generate unacceptable amounts of heat that may damage or otherwise interfere with the performance of the SC quantum circuit 100. Using flip chip first level interconnects 166 may enable the SC qubit device package 130 to have much lower parasitic inductance relative to using wirebonds to couple the die 132 and the package substrate 134, which may result in an improvement in signal integrity for high speed signals communicated between the die 132 and the package substrate 134.

[0069] In some prior implementations of flip chip first level interconnects, solder bumps were used instead of conductive pillars as described herein. While using solder bumps provides advantages over conventional wirebonding techniques, it may not always be the most optimal approach, as described below.

[0070] One reason is that, in some implementations, solder bumps may not allow reducing TLS losses with sufficiently small overall footprint of the interconnects (e.g. area on the die 132 devoted to implementation of conductive contacts to be coupled to the interconnects) required for scaling to larger number of quantum circuit components. This may be explained as follows. As previously described herein, materials typically used in a package substrate such as the package substrate 134 may be lossy in terms of the presence of spurious TLS. When such materials are at a close distance to certain quantum circuit components of the quantum circuit 100, e.g. resonators of superconducting qubits, as is the case with flip chip packaging described herein, they cause losses which lead to decoherence of the qubits. In order to reduce such losses, it is desirable to provide the quantum die 132 at a certain minimum distance from the package substrate 134, the distance sometimes referred to as a “standoff height,” referring to the distance between the first face 136 of the die 132 and the second face 144 of the package substrate 134. Solder bumps typically have an aspect ratio of about 1 or less, i.e. their height is typically equal to their width or smaller. Therefore, in order to achieve sufficient standoff height, e.g. on the order of 100 micrometers (microns) or more, each of the solder bumps may be about 100 microns wide. When scaling the quantum die 132 to implement larger numbers of quantum circuit components, larger number of first level interconnects are needed, which, if implemented as solder bumps, may occupy substantial area on the die 132 because each solder bump must be wide enough to ensure adequate standoff height from the package substrate 134 (i.e. the footprint of the solder bumps may be unacceptably large).

[0071] In some implementations, the challenges of using solder bumps as first level interconnects may further be exacerbated by the need to provide sufficient isolation between different signal conductive contacts. As known in microwave engineering and described above, a single microwave connection is typically implemented by having a signal line and one or more ground lines/planes, using any suitable microwave transmission line architecture, such as e.g. coplanar waveguide (CPW). Different signal conductive contacts are typically separated from one another by the minimum number of the ground conductive contacts. Since, as described above, each of the conductive contacts implemented as a solder bump may be relatively wide, providing this minimal separation between the signal lines allows minimizing the overall footprint of the conductive contacts 140 and, hence, the first level interconnects. However, such an arrangement may have poor isolation between the neighboring signal conductive contacts, compromising qubit device performance. On

the other hand, providing larger number of ground conductive contacts between the signal conductive contacts may improve isolation but at the cost of the larger footprint for implementing a given number of signal contacts.

[0072] Embodiments of the present disclosure are based on recognition that at least some of the challenges, in certain implementations, of the flip-chip packaging for qubit devices using solder bumps can be improved on by implementing first level interconnects in the form of conductive pillars 162 instead of the solder bumps.

[0073] In various embodiments, the conductive pillars 162 can take on any suitable shape and dimensions in order to satisfy design requirements. For example, in some embodiments, each of the conductive pillars 162 can have a height between about 100 and 300 microns, including all values and ranges therein, e.g. between about 100 and 200 microns, or between about 120 and 180 microns. In some embodiments, the conductive pillars 162 can be substantially perpendicular to the first face 136 of the die 132 as well as to the second face 144 of the package substrate 134.

[0074] In some embodiments, each of the conductive pillars 162 can have a width (i.e. a transverse cross-sectional dimension, e.g. a diameter, in case the conductive pillars are circular in their cross-section) between about 5 and 2000 microns, including all values and ranges therein.

[0075] In some embodiments, the conductive pillars 162 may have different ranges depending on whether they are designated to server as signal or ground pillars, e.g. signal pillars may have a width between about 5 and 50 micrometers, including all values and ranges therein, while ground pillars may have a width between about 50 and 2000 micrometers, including all values and ranges therein.

[0076] In some embodiments, each of the conductive pillars 162 can have an aspect ratio (i.e. a ratio of a height of the conductive pillar to a width of the conductive pillar) between about 0.5 and 10 , e.g. between about 2 and 8, or between about 4 and 8.

[0077] In some embodiments, the conductive pillars 162 can be made of one or more superconductive materials in their entirety, or may be coated with a layer of one or more superconductive materials over a core of a non-superconductive material. For example, the core of at least some of the conductive pillars 162 could be made from a non-superconductive material such as e.g. copper, silver or gold, which core coated with a layer of one or more superconductive material, this outer layer having a thickness of at least about 10 nanometers (nm). Some examples of suitable superconductive materials may include aluminum (Al), niobium (Nb), tin (In), titanium (Ti), osmium, zinc (Z), molybdenum (Mo), tantalum (Ta), vanadium, or composites of such materials (e.g., niobium nitride (NbN), titanium nitride (TiN), molybdenum rhenium (MoRe), or niobium titanium nitride (NbTiN)), as well as any other materials which act as superconductors at typical qubit operating temperatures. Any of these superconductive materials can also be used for the

conductive contacts 140 and 150, as well as for the conductive contacts 148 in case the qubit device package 130 implements the optional second level interconnects 158.

[0078] In some embodiments, the first level interconnects 166 may include not only the conductive pillars 162 but also include further conductive material elements, e.g. solder bumps or other solder elements, or elements made of conductive epoxy, between the conductive pillars 162 and the conductive contacts 140 at the first face 136 of the die 132. An example of such further conductive material elements is shown in FIG. 3 as solder bumps 164 provided over each of the conductive pillars 162. In various embodiments, the solder may include one or more of indium, bismuth, or gallium. In general, the first level interconnects 166 may include a solder having a melting point that is less than 180 degrees Celsius.

[0079] In some embodiments, the structures and materials in the quantum circuit 100 may be damaged if the quantum circuit 100 is exposed to the high temperatures that are common in conventional integrated circuit processing (e.g., greater than about 100 degrees Celsius, or greater than about 180-200 degrees Celsius). In particular, on embodiments in which the first level interconnects include solder bumps 164 over the conductive pillars 162, the solder may be a low-temperature solder (e.g., a solder having a melting point below 100 degrees Celsius) so that it can be melted to couple the conductive contacts 140 and respective conductive pillars 162 without having to expose the die 132 to higher temperatures and risk damaging the quantum circuit 100. Examples of solders that may be suitable include indium-based solders (e.g., solders including indium alloys). When low-temperature solders are used, however, these solders may not be fully solid during handling of the qubit device package 130 (e.g., at room temperature or temperatures between room temperature and 100 degrees Celsius), and thus the solder of the first level interconnects 166 alone may not reliably mechanically couple the die 132 and the package substrate 134 (and thus may not reliably electrically couple the die 132 and the package substrate 134). In some such embodiments, the qubit device package 130 may further include a mechanical stabilizer to maintain mechanical coupling between the die 132 and the package substrate 134, even when solder of the first level interconnects 166 is not solid. Since presence of any material that is lossy in terms of spurious TLSs may cause decoherence of the SC qubits 102, if used, such a mechanical stabilizer should be a material having relatively low losses in terms of TLSs. Alternatively, the stabilizer can be in the form of a metallic or non-metallic cover that is attached to the die or the package to prevent the die movement.

[0080] In the embodiments where the solder bumps 164 are used, the surface of the die around the contacts 140 may be coated with a material which is not wetted by the solder material of the solder bumps 164. This material is generally known as a solder mask and can take any appropriate form,

such as silicon nitride, aluminum oxide, and silicon oxide. The presence of this solder mask material enables solder mask defined contacts.

[0081] In some embodiments, a solder resist material may be disposed around at least some of the conductive contacts 140 and/or 150 (not specifically shown in FIG. 3). The solder resist material may be a polyimide or similar material, or may be any appropriate type of packaging solder resist material. In some embodiments, the solder resist material may be a liquid or dry film material including photoimageable polymers. In some embodiments, the solder resist material may be non-photoimageable.

[0082] In some embodiments, the particular quantum circuit 100 illustrated in the qubit device package 130 of FIG. 3 may be implemented with the physical layout 111 illustrated in FIG. 2, but any of the quantum circuits 100 disclosed herein or as known in the art may be included in a die (e.g., the die 132), and coupled to a package substrate (e.g., the package substrate 134) via the first level interconnects 166 as described herein. In particular, any number of qubits 102, flux bias lines 112, microwave lines 114, coupling resonators 116, readout resonators 118, drive lines 124, conductive contacts 120, 122, 126, and 128, and other components discussed herein with reference to the SC quantum circuit 100 may be included in the die 132.

[0083] In some embodiments, the package substrate 134 may be or may otherwise include a silicon interposer, and the conductive pathways 152 may be through-silicon vias and conductive patterned traces on the silicon substrate. Silicon may have a desirably low coefficient of thermal expansion compared with other dielectric materials that may be used for the insulating material 154, and thus may limit the degree to which the package substrate 134 expands and contracts during temperature changes relative to such other materials (e.g., polymers having higher coefficients of thermal expansion). A silicon interposer may also help the package substrate 134 achieve a desirably small line width and maintain high connection density to the die 132.

[0084] Limiting differential expansion and contraction may help preserve the mechanical and electrical integrity of the qubit device package 130 as the qubit device package 130 is fabricated (and exposed to higher temperatures) and used in a cooled environment (and exposed to lower, e.g. cryogenic, temperatures). In some embodiments, thermal expansion and contraction in the package substrate 134 may be managed by maintaining an approximately uniform density of the conductive material in the package substrate 134 (so that different portions of the package substrate 134 expand and contract uniformly), using reinforced dielectric materials as the insulating material 154 (e.g., dielectric materials with silicon dioxide fillers, referred to as prepreg), or utilizing stiffer materials as the insulating material 154 (e.g., material including glass cloth fibers).

[0085] In some embodiments, at least portions of the insulating material 154 may be a dielectric material (e.g., a dielectric laminate or an ILD in the case of silicon substrate), and may take the form of any of the embodiments of the insulating materials disclosed herein, for example.

[0086] In some embodiments, the insulating material 154 of the package substrate 134 may be selected to be the same as an insulating material which may be used in the qubit die 132. In one implementation, the die 132 and/or the package substrate 134 may be made of a highly crystalline material such as, but not limited to, highly crystalline silicon or sapphire, and may be provided as a wafer or a portion thereof. In other implementations, the package substrate 134 and the foundation of the die 132 may be non-crystalline. In general, any material that may provide sufficient advantages (e.g. sufficiently good electrical isolation and/or ability to apply known fabrication and processing techniques) to outweigh the possible disadvantages (e.g. negative effects of various defects), and that may serve as a foundation upon which a quantum circuit may be built, falls within the spirit and scope of the present disclosure for being used as the package substrate 132 and the substrate of the die 132. Additional examples of substrates include silicon-on-insulator (SOI) substrates, III-V substrates, and quartz substrates.

[0087] In some embodiments, conductive lines of the die 132 and the package substrate 134 may extend into and out of the plane of the drawing, providing conductive pathways to route electrical signals to and/or from various elements in the die 132.

[0088] The conductive vias and/or lines that provide the conductive pathways in/on the die 132 or/and in/on the package substrate 134 (e.g. conductive pathways 152) may be formed using any suitable techniques. Examples of such techniques may include subtractive fabrication techniques, additive or semi-additive fabrication techniques, single Damascene fabrication techniques, dual Damascene fabrication techniques, or any other suitable technique. In some embodiments, layers of insulator material, such as e.g. oxide material or nitride material, may insulate various structures in the conductive pathways from proximate structures, and/or may serve as etch stops during fabrication. In some embodiments, additional layers, such as e.g. diffusion barrier layers or/and adhesion layers may be disposed between conductive material and proximate insulating material. Diffusion barrier layers may reduce diffusion of the conductive material into the insulating material. Adhesion layers may improve mechanical adhesion between the conductive material and the insulating material.

[0089] In some embodiments, the conductive contacts 140 and/or 150 may take form of solder bond pads, but, in other embodiments, other conductive contact structures may be used (e.g., conductive epoxies, anisotropic conductive films, copper to copper bonding posts, etc.) to route electrical signals to/from the die 132.

[0090] In some embodiments, the conductive contacts 140 and/or 150 may include multiple layers of material that may be selected to serve different purposes. In some embodiments, the conductive contacts 140 and/or 150 may be formed of aluminum, and may include a layer of gold (e.g., with a thickness of less than 1 micron) between the aluminum and the adjacent first level interconnect to limit the oxidation of the surface of the contacts and improve the wetting and adhesion with adjacent solder, in case solder bumps are used. Alternate materials for the surface finish include palladium, platinum, silver and tin. In some embodiments, the conductive contacts 140 and/or 150 may be formed of aluminum, and may include a layer of a barrier metal such as nickel, as well as a layer of gold, or other appropriate material, wherein the layer of barrier metal is disposed between the aluminum and the layer of gold, and the layer of gold is disposed between the barrier metal and the adjacent interconnect. In such embodiments, the gold, or other surface finish, may protect the barrier metal surface from oxidation before assembly, and the barrier metal may limit the diffusion of solder from the adjacent interconnects into the aluminum.

[0091] As discussed above, in some embodiments, the conductive contacts 140 may provide the contacts from the quantum circuit 100 on the die 132 to couple to the package substrate 134 via the first level interconnects 166, as discussed above. Additionally or alternatively, some or all of the conductive contacts 140 may provide the contacts from the quantum circuit 100 on the die 132 to couple other components, e.g. to another die, e.g. a control die (not specifically shown in the FIGS).

[0092] The metallization stack 146 may include a plurality of alternating dielectric layers and conductive (e.g. superconductive) layers (not specifically shown in FIG. 3), e.g. where each conductive layer is electrically isolated from other conductive layers by one or more dielectric layers. In various embodiments, the dielectric layers of the metallization stack 146 may include one or more dielectric materials as described herein, e.g. with reference to the ILD or the insulating material 154, while the conductive layers may include one or more electrically conductive, e.g. superconductive, materials as described herein, e.g. with reference to the conductive material of the conductive pathways and/or conductive contacts of the qubit device package 130.

[0093] In various embodiments, more or fewer structures may be included in the conductive pathways, conductive contacts, and first level interconnects described with reference to FIG. 3. Various interconnect structures may be arranged within the quantum circuit 100 and in the package substrate 134 of the qubit device package 130 to route electrical signals according to a wide variety of designs (in particular, the arrangement is not limited to the particular configuration of the structure depicted in FIG. 3 or any of the other accompanying figures, and may include more or fewer components/elements). During operation of the quantum circuit 100 of a qubit device package with the first level interconnects 166 as described herein, electrical signals (such as e.g.

power, input/output (I/O) signals, including various control signals for external and internal control of the qubits 102) may be routed to and/or from the qubits 102 of the quantum circuit 100 through the first level interconnects 166, the conductive contacts 140 and 150, and conductive pathways of the die 132 and the package substrate 134. Examples of arrangements of electronics packages that may include any embodiment of the qubit device package 130 are discussed below with reference to FIGS. 13A-15.

[0094] Qubit device packages using conductive pillars as first level interconnects as disclosed herein may be manufactured using any suitable techniques. For example, FIG. 4 is a flow diagram of a first exemplary method 200 of manufacturing a qubit device package with first level interconnects in the form of conductive pillars, according to some embodiments of the present disclosure. FIGS. 5A-5D provide schematic illustrations of a device package at different stages of manufacturing when the method shown in FIG. 4 is used, according to some embodiments of the present disclosure. Similarly, FIG. 6 is a flow diagram of a second exemplary method 220 of manufacturing a qubit device package with first level interconnects in the form of conductive pillars and FIGS. 7A-7D provide schematic illustrations of a device package at different stages of manufacturing when the method shown in FIG. 6 is used, according to some embodiments of the present disclosure. Finally, FIG. 8 is a flow diagram of a third exemplary method 240 of manufacturing a qubit device package with first level interconnects in the form of conductive pillars and FIGS. 9A-9D provide schematic illustrations of a device package at different stages of manufacturing when the method shown in FIG. 8 is used, according to some embodiments of the present disclosure. Each of these methods can be used to manufacture the qubit device package 130 as described herein. Although the operations of each of these methods are illustrated once each and in a particular order, the operations may be performed in any suitable order and repeated as desired. For example, one or more operations may be performed in parallel to manufacture multiple qubit device packages using conductive pillars as first level interconnects substantially simultaneously. In another example, the operations may be performed in a different order to reflect the structure of a particular qubit device package in which conductive pillars will be included.

[0095] Referring to FIG. 4, the first method 200 may begin with providing a dielectic layer over a package substrate (process 201, a result of which is shown with a structure 211 shown in FIG. 5A). The dielectric layer provided at 201 may take the form of any of the embodiments of dielectric materials disclosed herein, such as e.g. ILD materials described herein, and may be provided over a package substrate, such as e.g. the package substrate 134, using any suitable technique such as e.g. lamination, spin-coating, or spray coating.

[0096] FIG. 5A, as well as subsequent FIGS. showing device packages at different stages of manufacturing of any of the methods illustrates only portions of the package substrate 134, without necessarily showing all of the details of the package substrate 134 as shown in FIG. 3, in order to not clutter the drawings. In particular, FIG. 5A illustrates the metallization stack 146 of the package substrate 134 and a dielectric layer 215 provided over the metallization stack 146. In other embodiments, the dielectric layer 215 may be considered to be a part of the metallization stack 146. A thickness of the dielectric layer 215, a dimension measured in the vertical direction of FIG. 5A, may be substantially equal to the desired height of the final conductive pillars to be formed.

[0097] In various embodiments, the conductive pillars 162 of the first level interconnects 166 as described herein may be viewed as part of the package substrate 134. In general, a package substrate 134 for any of the qubit device packages described herein may be manufactured using any suitable technique, e.g. using any of the subtractive manufacturing process or/and semi-additive manufacturing processes as known in the art. The package substrate 134 may be provided on a carrier that may provide mechanical support during manufacture, and may be formed of any suitable material (e.g., a metal sheet, a dielectric material, or a reinforced dielectric material). During manufacturing of the package substrate 134, conductive materials as described herein may be deposited on the carrier to any desired thickness using any suitable technique (e.g., sputtering, electroplating, electroless plating, lamination, etc.) and patterned using any suitable technique, e.g. as a part of forming the conductive contacts 150. For example, the conductive materials of the package substrate 134 may be patterned by providing a mask material (e.g., by lamination, spin coating, or slit coating), patterning the mask material (e.g., by photolithography, laser direct imaging, electron beam lithography, etc.), and etching the conductive material in accordance with the patterned mask material (e.g., using wet or dry etching), and removing the remaining mask material). The insulating material of the package substrate 134, e.g. the dielectric material 215 described below, may also be provided using any suitable technique (e.g., lamination or spin coating), and may cover or surround the conductive materials, e.g. cover or surround the conductive pathways and conductive contacts of the package substrate 134, as described herein. The insulating material may be, for example, an ILD material, as discussed above. Furthermore, during the manufacturing of the package substrate 134, cavities/openings may be formed in the insulating material, e.g. as a part of forming the vias filled with conductive materials, as described below. The cavities/openings may be formed using any suitable technique (e.g., laser or mechanical drilling, or using photolithography for photoimageable insulating materials). In some embodiments, the cavities may be drill holes. The cavities may be filled with a same or different conductive material than the one described above for forming the conductive contacts 150. In some embodiments, the

conductive material filling the cavities may be a superconducting material. Additional conductive contacts may be provided on the package substrate, e.g. the conductive contacts 148 on the first face of the package substrate 134, e.g. by repeating at least some of the operations discussed above, as appropriate, and may be insulated by additional insulating material. Manufacturing of the package substrate 134 may further include providing the solder resist material on one or both faces of the substrate using any suitable technique (e.g., lamination or spin coating), patterning the solder resist material using any suitable technique (e.g., photolithography), and removing the carrier from the assembly of the package substrate.

[0098] The method 200 may then proceed with providing, in the dielectric layer 215, tall vias 216 filled with a conductive material, as well as conductive contacts at the bottom of the vias (process 202, a result of which is shown with a structure 212 shown in FIG. 5B). The tall vias 216 provided at 201, including the conductive material(s) filling the vias may take the form of any of the embodiments of the conductive pillars disclosed herein, and may be provided using any suitable technique for forming and filling vias, as known in the art. In particular, each of the vias 216 may have the dimensions as described herein with reference to the conductive pillars 162, and the conductive materials filling the vias 216 may include any of the materials described herein with reference to the conductive pillars 162. The conductive contacts at the bottom of the vias provided at 202 may include any of the conductive contacts 150 described herein. The vias provided at 202 are referred to as “tall” because, compared to other methods described herein, these vias originaly extend substantially through the entire height of the final conductive pillars being formed.

[0099] At process 203, the dielectric material around at least some of the vias 216 filled with conductive material is etched to leave substantially only the conductive material of the vias 216, thus forming the conductive pillars, e.g. the conductive pillars 162 as described herein (a result of 203 is shown with a structure 213 shown in FIG. 5C). In some embodiments, the dielectric layer 215 may be etched at 203 using dry reactive ion etch (dry RIE, or DRIE) as known in the art. Particularly advantageous for superconducting qubits, the dielectric material 215 may be etched in process 203 around the vias which will be provided in the vicinity, e.g. opposite to, some quantum circuit components, such as e.g. resonators. For example, the dielectric material may be removed in some or all of an area of the package substrate 134 which will be facing an area surrounded in FIG. 2 with a dashed line, thus reducing TLS losses due to the presence of the lossy dielectric material around the resonators 116 and/or 118.

[0100] At an optional process 204, solder bumps may be provided between the conductive pillars formed at 203 and the quantum die. FIG. 5D illustrates one embodiment of a result of the process 204, where solder bumps 217 are provided over the conductive pillars of FIG. 5C. The solder bumps

217 provided at 204 may take the form of any of the embodiments of the solder bumps 164 described herein, and may be provided over the conductive pillars using any suitable technique as known in the art such as e.g. plating, stencil printing or solder preform placement. FIG. 5D does not show a quantum die on the other side of the solder bumps 217 in order to not clutter the drawing, but such a quantum die could take the form of any of the embodiments of the quantum die 132 described herein, brought into contact with the package substrate 134 with the conductive pillars provided thereon to form the qubit device package 130. In some embodiments, the die 132 may be brought in contact with the package substrate 134 using a pick-and-place apparatus, for example, and a reflow or thermal compression bonding operation may be used to couple the die 132 to the package substrate 134 via the solder bumps 164. Attaching the die 132 to the package substrate 134 may include electrically connecting some of the conductive contacts, e.g. the contacts 140 described herein, at the first face 136 of the die 132 with some of the (i.e. with the associated) plurality of conductive pillars 162 now formed at the second face 144 of the package substrate 134, as e.g. shown in FIG. 3.

[0101] In an embodiment alternative to that shown in FIG. 5D, the method 200 may be modified so that the solder bumps 217 are provided at process 204 on the quantum die 132 instead of being provided on the package substrate 134, and then the quantum die 132 with the solder bumps can be brought into contact with the structure 213 of FIG. 5C to form the qubit device package 130.

[0102] In an embodiment alternative to that shown in FIGS. 5C and 5D, the method 200 may be modified so that solder bump placement may precede the etching. In such an embodiment, the solder bumps 217 may be placed over the vias 216 of the structure 212 and after that etching as described with reference to process 203 may be performed.

[0103] Because of the order and nature of the processes employed in the method 200 (as shown in FIG. 4 as well as various modifications thereof, described above), this method may be referred to as a “via-in-pad plus RIE” method because vias with conductive materials are formed in a “pad” of a package substrate with the dielectric layer, and because an etch such as e.g. a RIE is performed to remove the dielectric material around some of the vias, thus forming conductive pillars. In some implementations, it may be not desirable, or not possible, to form vias which are tall enough for the desired height of the conductive pillars to be used as first level interconnects described herein, or to form vias of the desired aspect ratio. For example, there may be manufacturing limitations to the height or/and the aspect ratio that may be achieved for the vias formed in the process 203 described above. In such scenarios, methods according to FIGS. 8 or 10 may be used, in which methods electroplating is employed to extend the height of the conductive pillars formed otherwise by the “via-in-pad plus RIE” method. Thus, the methods 220 and 240 of FIGS. 8 and 10 may be referred to

as “via-in-pad plus RIE plus electroplating” and “via-in-pad plus electroplating plus RIE,” indicating that in both of these two methods via-in-pad and RIE (or, in general, any kind of isotropic etching) is used similar to the first method shown in FIG. 4, as well as further employing electroplating. Such names for the methods of FIGS. 8 and 10 also indicate that these two FIGS. use RIE and electroplating processes in different order.

[0104] Turning to the method 220 shown in FIG. 6, the method 220 may begin with providing the layer 215 of a dielectric material over a package substrate (process 221, a result of which is shown with a structure 231 shown in FIG. 7A), in a manner analogous to that described above for the process 201, except that now the thickness of the dielectric layer 215 may be smaller than that provided in the process 201. For example, in some embodiments, the thickness of the dielectric layer 215 may be between about 20% and 80% of the desired final height of the conductive pillars being formed, e.g. between about 30% and 70%, or between about 40% and 60%. Descriptions provided above with reference to the process 201 are applicable to the process 221 and, therefore, in the interests of brevity, are not repeated.

[0105] The method 220 may then proceed with providing, in the dielectric layer 215 provided at process 221, tall vias 216 filled with a conductive material, as well as conductive contacts at the bottom of the vias (process 222, a result of which is shown with a structure 232 shown in FIG. 7B), in a manner analogous to that described above for the process 202. Descriptions provided above with reference to the process 202 are applicable to the process 222 and, therefore, in the interests of brevity, are not repeated. Since the thickness of the layer 215 provided at 221 is smaller than that provided at 201, the height of the vias 216 provided at 222 is respectively smaller. Hence, the vias provided at 222 are referred to herein as “medium” vias.

[0106] At 223, the dielectric material around at least some of the vias 216 filled with conductive material is etched to leave substantially only the conductive material of the vias 216, thus forming elements 235 which may be referred to as “intermediate conductive pillars” because they are not yet the final conductive pillars 162 to be used as interconnects, in a manner analogous to that described above for the process 203. Descriptions provided above with reference to the process 203 are applicable to the process 223 and, therefore, in the interests of brevity, are not repeated. A result of 223 is shown with a structure 233 shown in FIG. 7C.

[0107] Once the intermediate conductive pillars 235 are provided, they may be extended in height by electroplating/electrodeposition of a metal 217 over the materials of the vias 216 (process 224, a result of which is shown with a structure 234 shown in FIG. 7D). All techniques for electroplating/electrodeposition known in the art applicable for use in the electroplating process 224. As a result of performing electroplating, metal elements 236 are grown over the intermediate

conductive pillars 235, as shown in FIG. 7D. Together, the electroplated metal elements 236 and the intermediate conductive pillars 2356 may form the final conductive pillars for use as first level interconnects, e.g. the conductive pillars 162. In various embodiments, the top pillar diameters may be the same as the lower pillar diameter, or may be different, depending on the mechanical requirements and the aspect ratios desired. For example, to avoid via delamination or "tip over" from the lower dielectric layer, it might be desired to have wider diameter lower pillars while having narrower diameter upper pillars to reduce the electrical impact.

[0108] In various embodiments, materials used to form the intermediate conductive pillars 235 and materials used to form the electroplated elements 236 may be the same or different. Materials used for electroplating may include, but are not limited to, one or more of e.g. copper, silver or gold.

[0109] In various embodiments, the height of the intermediate conductive pillars 235 may be between about 20 and 400 micrometers (micron), including all ranges and values therein, e.g. between about 50 and 300 micron, or between about 80 and 120 micron, while the height of the electroplated metal elements 236 may be between about 20 and 400 micron, including all ranges and values therein, e.g. between about 50 and 300 micron, or between about 80 and 120 micron. In various embodiments, a height of each of the plurality of conductive pillars after the electroplating may be between about 2 and 4 times greater than a height of each of the plurality of the intermediate conductive pillars (i.e. the conductive pillars before the electroplating), e.g. between about 2 and 3 times, or between about 2.5 and 3.8 times.

[0110] In various embodiments, an aspect ratio of each of the conductive pillars 162 formed of an intermediate conductive pillar 235 and an electroplated metal element 236 on top may be as described above with reference to the conductive pillars 162 shown in FIG. 3.

[0111] Similar to the process 200, at an optional process 225, solder bumps may be provided between the conductive pillars formed at 224 and the quantum die, in a manner analogous to that described above for the process 204. A result of the process 225 is not shown in FIGS. 7A-7D, but may be envisioned as similar to that shown in FIG. 5D except that now each final conductive pillar 162 includes the via-in-pad conductive portion 235 and the electroplated portion 236, as described above. Descriptions provided above with reference to the process 204 are applicable to the process 225 and, therefore, in the interests of brevity, are not repeated.

[0112] Turning to the method 240 shown in FIG. 8, the method 240 may begin with processes 241 and 242, similar to the processes 221 and 222 described above, which descriptions, therefore, are not repeated here. Results of the processes 241 and 242 are shown with structures 251 and 252 shown in FIGS. 9A and 9B, respectively (which results are the same as sown in FIGS. 7A and 7B).

[0113] After that, electroplating and etching processes are reversed in the method 240 compared to the method 220. Namely, as shown in FIG. 8, first, electroplating to extend the medium vias 216 with the electroplated portions 236 is performed (process 243, a result of which is shown with a structure 253 shown in FIG. 9C), in a manner analogous to that described above for the process 224, and, after that, the dielectric material is etched around at least some of the vias 216 to form the intermediate conductive pillars 235 (process 244, a result of which is shown with a structure 254 shown in FIG. 9D), in a manner analogous to that described above for the process 223. In the interests of brevity, descriptions of these electroplating and etching processes are not repeated here.

[0114] One difference with the electroplating process of the method 240 compared to that of the method 220, in the method 220, the fact that the vias 216 have already been etched around to form the intermediate conductive pillars helps acting as a guide for selective deposition of the electroplated metal only on the intermediate conductive pillars 235 of FIG. 7C (a mask may also be used to guide metal deposition by electroplating, both in methods 220 and 240). With the method 240, depending on the electroplating process used and depending on the type of the dielectric layer 215, it may be advantageous to, optionally, provide conductive pads 218 above at least some (or all) of the vias 216 of FIG. 9B, prior to performing the electroplating, in order to account for potential misalignment in the electroplating process 243. Such optional conductive pads 218 are shown in FIG. 9C for the two vias 216 shown on the left. In some embodiments, the conductive pads 218 may be provided by performing lithography using a mask opening that is larger than a mask opening used for the electroplating. If used, such conductive pads could also remain after the etching process 244 even though they are not specifically shown in FIG. 9D. Of course, the shape and locations of the conductive pads 218 shown in FIG. 9C is purely illustrative and, in various embodiments, any number of conductive pads 218, having any suitable shape, may be used.

[0115] As a result of performing electroplating and etching in the method 240, metal elements 236 are grown over the intermediate conductive pillars 235, as shown in FIG. 9D. Together, the electroplated metal elements 236 and the intermediate conductive pillars 235 may form the final conductive pillars for use as first level interconnects, e.g. the conductive pillars 162. Considerations provided above for the intermediate conductive pillars 235, the electroplated elements 236, and the conductive pillars 162 that they form in the method 220 are applicable to the method 240 and, therefore, in the interests of brevity, are not repeated here.

[0116] Similar to the process 200, at an optional process 245, solder bumps may be provided between the conductive pillars formed at 244 and the quantum die, in a manner analogous to that described above for the process 225. A result of the process 245 is not shown in FIGS. 9A-9D, but

may be envisioned as similar to that shown in FIG. 5D except that now each final conductive pillar 162 includes the via-in-pad conductive portion 235 and the electroplated portion 236, as described above. Descriptions provided above with reference to the process 225 are applicable to the process 245 and, therefore, in the interests of brevity, are not repeated.

[0117] The first level interconnects 166 with the conductive pillars 162 as described herein, may be arranged in any suitable configuration between the conductive contacts 150 at the second face of the package substrate 134 and the conductive contacts 140 at the first face of the die 132, with each of the first level interconnects serving either as a signal or a ground interconnect. As described above, first level interconnects serving as ground interconnects by being connected to a ground potential act as ground shields, shielding/protecting signal interconnects from unwanted electromagnetic interference. Advantageously, the conductive pillars 162 as described herein may be arranged in any suitable configuration to optimize the shielding effect, with FIGS. 10-12 illustrating some of such exemplary configurations. Each of FIGS. 10-12 provide a cross-sectional top view similar to that shown in FIG. 2. FIG. 10 illustrates conductive contacts connecting to signal lines as black circles and conductive contacts connecting to ground lines/planes as white circles, while FIGS. 11-12 differ from the illustration of FIG. 10 in that they illustrate a plurality of conductive contacts connecting to ground lines/planes as black lines, instead of individual ground contacts. Positions and locations of the signal and ground conductive contacts as shown in FIGS. 10-12 correspond to positions and locations of the first level interconnects 166 as described herein, since, as described above, the first level interconnects 166 extend, substantially perpendicularly to the die 132 and the package substrate 134, between the die 132 and the package substrate 134.

[0118] FIG. 10 illustrates an exemplary arrangement 300 of the conductive pillars 162 of the first level interconnects 166 described herein (or, correspondingly, of the conductive contacts 140 or the conductive contacts 150) where two or more ground conductive pillars/ conductive contacts may be considered to form a sub-group, with a plurality of such sub-groups at least partially surrounding a signal conductive pillar. Each one of dashed closed lines 301-305 shown in FIG. 10 illustrate such a sub-group of ground conductive pillars, partially surrounding a signal conductive pillar 306. In particular, the exemplary arrangement of FIG. 10 illustrates that the five ground conductive pillar sub-groups 301-305 form a partial polygon (a partial hexagon in this example) around the signal conductive pillar 306. As can be seen in FIG. 10, although not specifically labeled with reference numerals in order to not clutter the drawing, at least some of the other signal lines are similarly surrounded by five sub-groups of ground lines as described above.

[0119] In various embodiments, an area enclosed by the partial polygon, e.g. the area indicated in FIG. 10 with dotted background, may be between about 0.0001 and 3 square millimeters (mm2), e.g.

between about 0.01 and 2 mm2, or between about 0.25 and 0.5 mm2. The polygon is partial so that a contact can be made to the signal line associated with the signal conductive pillar 306, as illustrated in FIG. 10 with a die trace 307 in the form of a thick black line (in other embodiments, the die traces may take any other arbitrary shapes). Having partially open ground polygon allows some of the vapors produced during certain manufacturing/assembly processes to escape without significantly reducing the isolation between the signals. It also helps with the different wash steps after assembly to ensure clean surfaces for both the die and the package. Additionally, since assembly is typically done under atmospheric pressure but actual quantum computing operation is done in vacuum, the openings allows the air to escape during the vacuum pumping step before cooling down the chip to perform quantum computations.

[0120] In some embodiments, it is the area of the partial polygon where the dielectric material 215 is etched away, leaving substantially free-standing conductive pillars as described herein, as e.g. shown in FIGS. 5D, 7D, or 9D where some of the dielectric material 215 is removed, leaving the conductive pillars 162. Thus, the conductive pillars of and enclosed by the partial polygon (e.g. the ground and signal conductive pillars shown over the dotted background in FIG. 10) may be viewed as forming a group such that a space between the first face 136 of the die 132 and the second face 144 of the package substrate 134 outside of a contour of the group (e.g. the contour being defined as an outline of the dotted area shown in FIG. 10) may include the dielectric material 215, while the dielectric material 215 may be substantially absent in a space between the first face 136 of the die 132 and the second face 144 of the package substrate 134 inside of said contour. In this manner, the conductive pillars may form ground shields with hollow (i.e. no dielectric material inside) shapes. If a contour of one group is immediately adjacent to a contour of another group, then an area where the dielectric material 215 is substantially absent may extend continuously from one group to the next.

[0121] As described above, removing the dielectric layer 215 under quantum circuit components of the SC quantum circuit 100 disposed on the first face 136 of the die 132, such as e.g. under the resonators of the die 132, results in the electromagnetic fields from the resonators not traversing any, or at least traversing less of the lossy dielectric material, especially if the dielectric layer 215 is removed so that the top metal layer of the metallization stack 146, which top layer may be made of one or more superconductive materials, is exposed. This, in turn, reduces losses in the quantum die 132 and improves quality factor of the resonators. In addition, the top metal layer of the metallization stack 146 may be made from non-superconductive materials without substantial sacrifice in the performance of the SC quantum circuit 100 disposed on the first face 136 of the die 132. Thus, the group of conductive pillars around which the dielectric material 215 is removed may

be provided opposite one or more resonators, or other quantum circuit components of the quantum circuit 100 disposed on the first face 136 of the die 132.

[0122] In various embodiments, an average distance between two adjacent conductive pillars of the many conductive pillars of such a group may be between about 10 and 2000 micron, e.g. between about 100 and 1000 micron, or between about 200 and 400 micron. In conventional implementations using solder bumps as first level interconnects, the minimum feasible spacing between two bumps is equal to about double of the height of a solder bump (e.g. about 400 micron for a 200 micron tall bumps). Because of the isolation requirement, two signal bumps will require at least one grounding bump between them, so the spacing becomes about 800 micron. In contrast, when using conductive pillars as described herein, this spacing may be reduced because the aspect ratio of the pillars can be much higher than that of the solder bumps. Furthermore, the non-bump shaped ground shields which can be made using conductive pillars allows providing better isolation.

[0123] In other embodiments, the ground shields similar to that formed by the sub-groups 301-305 and described above may take on other shapes, as is illustrated with the examples of FIGS. 11 and 12. FIG. 11 provides a schematic representation of the hexagonal ground shields (thick black lines) substantially as shown in FIG. 10 (but a schematic representation of the structure 300 is shown this time), while FIG. 12 provides an analogous schematic representation of a structure 310 with ground shields (again, thick black lines) forming substantially coaxial structures.

[0124] Having the different sub-groups of ground shields only partially enclose each signal line, i.e. using voids in between the different sub-groups as shown in FIGS. 11 and 12, advantageously allows flux/assembly vapors produced during the manufacturing process to escape from the center signal lines. At the same time, having the different sub-groups of ground shields partially overlap, as e.g. shown in FIG. 12 with sub-groups 311-314 of ground conductive pillars around each signal conductive pillar 315 partially overlapping (e.g. the sub-groups 311 and 312 partially overlap with an opening in between them, similar to the sub-groups 311 and 314, the sub-groups 312 and 313, or the sub-groups 313 and 314), enables higher electrical isolation. The ground shields 311-314 around the signal conductive pillar 315 together form a coaxial vertical interconnect for the quantum circuit 100, extending between the first face 136 of the quantum die 132 and the package substrate 134. While FIG. 12 illustrates the ground shields 311-314 as arcs, in general, they may be of any arbitrary shape surrounding the signal line 315, preferably with overlapping opens as shown in FIG. 12 (e.g. one overlapping open is formed between the partially overlapping sub-groups 311 and 312, similar overlapping opens are formed between the sub-groups 311 and 314, between the sub-groups 312 and 313, or between the sub-groups 313 and 314). When, as described above, the dielectric material is removed within the contours/polygons defined by each collection of ground shields

around a given signal line, the conductive pillars as described herein can form ground shields with hollow (i.e. no dielectric material inside) shapes. The size of an area enclosed by each set of the ground-shields around a given signal line may be substantially as described above with reference to FIG. 10 for the area shown with the dotted background.

[0125] Some or all of the areas enclosed by the conductive pillar ground-shields of arbitrary shapes enclosing signal conductive pillars may overlap or be included within an area enclosed within a dashed contour in FIG. 2 (i.e. an area where the resonators of a quantum circuit are provided). Of course, in other embodiments, the shape of the area shown in FIG. 2 with the dashed line may be different than a rectangle shown in FIG. 2, as long as the shape is such that electromagnetic fields from the resonator(s) of the quantum circuit 100 are not substantially affected by the potentially lossy material of the dielectric layer under the resonator(s).

[0126] FIGS. 13A-B are top views of a wafer 1100 and dies 1102 that may be formed from the wafer 1100, where the dies 1101 may be included in any of the qubit device packages disclosed herein, e.g., the qubit device package 130, or any combinations of these packages. The wafer 1100 may include semiconductor material and may include one or more dies 1102 having conventional and qubit device elements formed on a surface of the wafer 1100. Each of the dies 1102 may be a repeating unit of a semiconductor product that includes any suitable conventional and/or qubit device. After the fabrication of the semiconductor product is complete, the wafer 1100 may undergo a singulation process in which each of the dies 1102 is separated from one another to provide discrete "chips" of the semiconductor product. A die 1102 may include one or more qubit devices 100 and/or supporting circuitry to route electrical signals to the qubit devices 100 (e.g., interconnects connected to the conductive contacts 120/122/126, and other conductive vias and lines), as well as any other IC components. In some embodiments, the wafer 1100 or the die 1102 may include a memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 1102. For example, a memory array formed by multiple memory devices may be formed on a same die 1102 as a processing device (e.g., the processing device 2002 of FIG. 15) or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array.

[0127] FIG. 14 is a cross-sectional side view of a device assembly 1300 that may include any of the embodiments of the qubit device packages disclosed herein. The device assembly 1300 includes a number of components disposed on a circuit board 1302. The device assembly 1300 may include components disposed on a first face 1340 of the circuit board 1302 and an opposing second face

1342 of the circuit board 1302; generally, components may be disposed on one or both faces 1340 and 1342.

[0128] In some embodiments, the circuit board 1302 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 1302. In other embodiments, the circuit board 1302 may be a package substrate or flexible board.

[0129] The IC device assembly 1300 illustrated in FIG. 14 includes a package-on-interposer structure 1336 coupled to the first face 1340 of the circuit board 1302 by coupling components 1316. The coupling components 1316 may electrically and mechanically couple the package-on-interposer structure 1336 to the circuit board 1302, and may include solder balls (as shown in FIG. 14), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

[0130] The package-on-interposer structure 1336 may include a package 1320 coupled to an interposer 1304 by coupling components 1318. The coupling components 1318 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 1316. In some embodiments, at least some of the coupling components 1318 may take a form of the first level interconnects as described herein, e.g. using the conductive pillars 162. Although a single package 1320 is shown in FIG. 14, multiple packages may be coupled to the interposer 1304; indeed, additional interposers may be coupled to the interposer 1304. The interposer 1304 may provide an intervening substrate used to bridge the circuit board 1302 and the package 1320. The package 1320 may be a qubit device package as described herein, e.g. one of the qubit device package 130, or a combination thereof, or may be a conventional IC package, for example. In some embodiments, the package 1320 may take the form of any of the embodiments of the qubit device packages disclosed herein, and may include a SC qubit device die 1320 coupled to a package substrate 134 (e.g., by flip chip connections comprising conductive pillars as described herein) implemented as the interposer 1304. Generally, the interposer 1304 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 1304 may couple the package 1320 (e.g., a die) to a ball grid array (BGA) of the coupling components 1316 for coupling to the circuit board 1302. In the embodiment illustrated in FIG. 14, the package 1320 and the circuit board 1302 are attached to opposing sides of the interposer 1304; in other embodiments, the package 1320 and the circuit board 1302 may be attached to a same side

of the interposer 1304. In some embodiments, three or more components may be interconnected by way of the interposer 1304.

[0131] The interposer 1304 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some embodiments, the interposer 1304 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 1304 may include metal interconnects 1308 and vias 1310, including but not limited to through-silicon vias (TSVs) 1306. The interposer 1304 may further include embedded devices 1314, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 1304. The package-on-interposer structure 1336 may take the form of any of the package-on-interposer structures known in the art.

[0132] The device assembly 1300 may include a package 1324 coupled to the first face 1340 of the circuit board 1302 by coupling components 1322. The coupling components 1322 may take the form of any of the embodiments discussed above with reference to the coupling components 1316 or 1318, and the package 1324 may take the form of any of the embodiments discussed above with reference to the package 1320. The package 1324 may be a qubit device package as described herein, e.g. the package 130, or may be a conventional IC package, for example. In some embodiments, the package 1324 may take the form of any of the embodiments of the qubit device package as described herein, e.g. one of the qubit device package 130, or a combination thereof disclosed herein, and may include a qubit device die 132 coupled to a package substrate 134 (e.g., by flip chip connections comprising conductive pillars as described herein).

[0133] The device assembly 1300 illustrated in FIG. 14 includes a package-on-package structure 1334 coupled to the second face 1342 of the circuit board 1302 by coupling components 1328. The package-on-package structure 1334 may include a package 1326 and a package 1332 coupled together by coupling components 1330 such that the package 1326 is disposed between the circuit board 1302 and the package 1332. The coupling components 1328 and 1330 may take the form of any of the embodiments of the coupling components 1316 or 1318 discussed above, and the packages 1326 and 1332 may take the form of any of the embodiments of the package 1320 discussed above. Each of the packages 1326 and 1332 may be a qubit device package as described herein or may be a conventional IC package, for example. In some embodiments, one or both of the

packages 1326 and 1332 may take the form of any of the embodiments of a qubit device package as described herein, e.g. one of the qubit device package 130, or a combination thereof, and may include a qubit device die 132 coupled to a package substrate 134 (e.g., by flip chip connections comprising conductive pillars as described herein).

[0134] FIG. 15 is a block diagram of an example quantum computing device 2000 that may include one or more of conductive pillar first level interconnects disclosed herein. A number of components are illustrated in FIG. 15 as included in the quantum computing device 2000, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the quantum computing device 2000 may be attached to one or more printed circuit boards (e.g., a motherboard), and may be included in, or include, any of the qubit device packages with one or more of conductive pillar first level interconnects described herein. In some embodiments, various ones of these components may be fabricated onto a single system-on-a-chip (SoC) die. Additionally, in various embodiments, the quantum computing device 2000 may not include one or more of the components illustrated in FIG. 15, but the quantum computing device 2000 may include interface circuitry for coupling to the one or more components. For example, the quantum computing device 2000 may not include a display device 2006, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 2006 may be coupled. In another set of examples, the quantum computing device 2000 may not include an audio input device 2018 or an audio output device 2008, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 2018 or audio output device 2008 may be coupled.

[0135] The quantum computing device 2000 may include a processing device 2002 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 2002 may include a quantum processing device 2026 (e.g., one or more quantum processing devices), and a non-quantum processing device 2028 (e.g., one or more non-quantum processing devices). The quantum processing device 2026 may include one or more of the qubit device packages with one or more of conductive pillar first level interconnects disclosed herein, and may perform data processing by performing operations on the qubits that may be generated in the quantum circuits 100, and monitoring the result of those operations. For example, as discussed above, different qubits may be allowed to interact, the quantum states of different qubits may be set or transformed, and the quantum states of different qubits may be read. The quantum processing device 2026 may be a universal quantum processor, or specialized quantum

processor configured to run one or more particular quantum algorithms. In some embodiments, the quantum processing device 2026 may execute algorithms that are particularly suitable for quantum computers, such as cryptographic algorithms that utilize prime factorization, encryption/decryption, algorithms to optimize chemical reactions, algorithms to model protein folding, etc. The quantum processing device 2026 may also include support circuitry to support the processing capability of the quantum processing device 2026, such as input/output channels, multiplexers, signal mixers, quantum amplifiers, and analog-to-digital converters.

[0136] As noted above, the processing device 2002 may include a non-quantum processing device 2028. In some embodiments, the non-quantum processing device 2028 may provide peripheral logic to support the operation of the quantum processing device 2026. For example, the non-quantum processing device 2028 may control the performance of a read operation, control the performance of a write operation, control the clearing of quantum bits, etc. The non-quantum processing device 2028 may also perform conventional computing functions to supplement the computing functions provided by the quantum processing device 2026. For example, the non-quantum processing device 2028 may interface with one or more of the other components of the quantum computing device 2000 (e.g., the communication chip 2012 discussed below, the display device 2006 discussed below, etc.) in a conventional manner, and may serve as an interface between the quantum processing device 2026 and conventional components. The non-quantum processing device 2028 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices.

[0137] The quantum computing device 2000 may include a memory 2004, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the states of qubits in the quantum processing device 2026 may be read and stored in the memory 2004. In some embodiments, the memory 2004 may include memory that shares a die with the non-quantum processing device 2028. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random-access memory (STT-MRAM).

[0138] The quantum computing device 2000 may include a cooling apparatus 2024. The cooling apparatus 2024 may maintain the quantum processing device 2026, in particular the quantum circuits 100 as described herein, at a predetermined low temperature during operation to avoid qubit decoherence and to reduce the effects of scattering in the quantum processing device 2026.

This predetermined low temperature may vary depending on the setting; in some embodiments, the temperature may be 5 degrees Kelvin or less. In some embodiments, the non-quantum processing device 2028 (and various other components of the quantum computing device 2000) may not be cooled by the cooling apparatus 2024, and may instead operate at room temperature. The cooling apparatus 2024 may be, for example, a dilution refrigerator, a helium-3 refrigerator, or a liquid helium refrigerator.

[0139] In some embodiments, the quantum computing device 2000 may include a communication chip 2012 (e.g., one or more communication chips). For example, the communication chip 2012 may be configured for managing wireless communications for the transfer of data to and from the quantum computing device 2000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0140] The communication chip 2012 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip 2012 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 2012 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 2012 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 2012 may operate in accordance with other wireless protocols in other embodiments. The quantum computing device 2000 may include an

antenna 2022 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0141] In some embodiments, the communication chip 2012 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 2012 may include multiple communication chips. For instance, a first communication chip 2012 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 2012 may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 2012 may be dedicated to wireless communications, and a second communication chip 2012 may be dedicated to wired communications.

[0142] The quantum computing device 2000 may include battery/power circuitry 2014. The battery/power circuitry 2014 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the quantum computing device 2000 to an energy source separate from the quantum computing device 2000 (e.g., AC line power).

[0143] The quantum computing device 2000 may include a display device 2006 (or corresponding interface circuitry, as discussed above). The display device 2006 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0144] The quantum computing device 2000 may include a global positioning system (GPS) device 2016 (or corresponding interface circuitry, as discussed above). The GPS device 2016 may be in communication with a satellite-based system and may receive a location of the quantum computing device 2000, as known in the art.

[0145] The quantum computing device 2000 may include an audio output device 2008 (or corresponding interface circuitry, as discussed above). The audio output device 2008 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0146] The quantum computing device 2000 may include an audio input device 2018 (or corresponding interface circuitry, as discussed above). The audio input device 2018 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0147] The quantum computing device 2000 may include an other output device 2010 (or corresponding interface circuitry, as discussed above). Examples of the other output device 2010 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0148] The quantum computing device 2000 may include an other input device 2020 (or corresponding interface circuitry, as discussed above). Examples of the other input device 2020 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0149] The quantum computing device 2000, or a subset of its components, may have any appropriate form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device.

[0150] The following paragraphs provide examples of various ones of the embodiments disclosed herein.

[0151] Example 1 provides a qubit device package that includes a quantum die and a package substrate. The die has a first face and an opposing second face, and includes a quantum device including a plurality of quantum circuit components disposed on the first face of the die. The die also has conductive contacts disposed on the first face of the die and coupled (e.g. electrically connected) to associated ones of the plurality of quantum circuit components. The package substrate has a first face and an opposing second face, and includes conductive contacts disposed on the second face of the package substrate. The qubit device package further includes first level interconnects disposed between the first face of the die and the second face of the package substrate and coupling (e.g. electrically connecting) some of the conductive contacts on the first face of the die with some of the (i.e. with the associated) conductive contacts on the second face of the package substrate, where the first level interconnects include electrically conductive (e.g. metal) pillars.

[0152] Example 2 provides the qubit device package according to Example 1, where each of the conductive pillars has a height ("stand-off height) between about 100 and 300 micrometers.

[0153] Example 3 provides the qubit device package according to Examples 1 or 2, where each of the conductive pillars has a width between about 5 and 2000 micrometers.

[0154] Example 4 provides the qubit device package according to any one of the preceding Examples, where, for each of the conductive pillars, a ratio of a height of the conductive pillar to a width of the conductive pillar (i.e. aspect ratio) is between about 0.5 and 10 , e.g. between about 0.5 and 2 , or between about 4 and 10.

[0155] Example 5 provides the qubit device package according to any one of the preceding Examples, where each of the conductive pillars include (i.e. made of in their entirety, or coated/sputtered with on the outer surface) one or more superconductive materials.

[0156] Example 6 provides the qubit device package according to Example 5, where one or more superconductive materials include one or more of aluminum (Al), niobium (Nb), niobium nitride (NbN), titanium nitride (TiN), molybdenum rhenium (MoRe), and niobium titanium nitride (NbTiN).

[0157] Example 7 provides the qubit device package according to any one of the preceding Examples, where a plurality of adjacent conductive pillars form a group such that a space between the first face of the die and the second face of the package substrate outside of a contour of the group includes a dielectric material, the dielectric material being substantially absent in a space between the first face of the die and the second face of the package substrate inside of a contour of the group.

[0158] Example 8 provides the qubit device package according to Example 7, where an average distance between two adjacent conductive pillars of the plurality of adjacent conductive pillars of the group is between about 10 and 2000 micrometers, e.g. between about 500 and 2000 micrometers, or between about 100 and 400 micrometers.

[0159] Example 9 provides the qubit device package according to Examples 7 or 8, where the plurality of quantum circuit components include one or more resonators, and the group is opposite at least one of the one or more resonators.

[0160] Example 10 provides the qubit device package according to any one of Examples 7-9, where one conductive pillar of the group is a signal conductive pillar and other conductive pillars of the group are ground conductive pillars and form one or more ground sub-groups, the one or more ground sub-groups at least partially surrounding the signal conductive pillar. In this manner, the conductive pillars may form ground shields with hollow (i.e. no dielectric material inside) shapes.

[0161] Example 11 provides the qubit device package according to Example 10, where the one or more ground sub-groups form a partial circle around the signal conductive pillar, thus providing a coaxial vertical interconnect for quantum circuits.

[0162] Example 12 provides the qubit device package according to Example 11, where an area enclosed by the partial circle is between about 0.0001 and 3 square millimeters (mm2), e.g. between about 0.5 and 2 mm2, or between about 0.01 and 0.25 mm2.

[0163] Example 13 provides the qubit device package according to Example 10, where the one or more ground sub-groups form a partial polygon (i.e. a shape with at least three straight sides) around the signal conductive pillar.

[0164] Example 14 provides the qubit device package according to Example 13, where an area enclosed by the partial polygon is between about 0.0001 and 3 square millimeters (mm2), e.g. between about 0.5 and 2 mm2, or between about 0.01 and 0.25 mm2.

[0165] Example 15 provides the qubit device package according to Examples 13 or 14, where the partial polygon is a partial hexagon.

[0166] Example 16 provides the qubit device package according to any one of the preceding Examples, where the conductive pillars are substantially perpendicular to the first face of the die and the second face of the package substrate.

[0167] Example 17 provides the qubit device package according to any one of the preceding Examples, where the first level interconnects further include conductive material elements, e.g. solder bumps or other solder elements, or elements made of conductive epoxy, between the conductive pillars and the conductive contacts at the first face of the die. In various embodiments, the solder may include one or more of indium, bismuth, or gallium. In general, the first level interconnects may include a solder having a melting point that is less than 180 degrees Celsius.

[0168] Example 18 provides the qubit device package according to any one of the preceding Examples, where the plurality of quantum circuit components include a plurality of superconducting qubits disposed on the first face of the die and a plurality of resonators disposed on the first face of the die.

[0169] Example 19 provides the qubit device package according to any one of the preceding Examples, where the conductive contacts (140) on the first face of the die are coupled (e.g. electrically connected) to the associated ones of the plurality of quantum circuit components by a plurality of conductive pathways.

[0170] Example 20 provides the qubit device package according to any one of the preceding Examples, where the conductive contacts on the second face of the package substrate are coupled to two or more conductive layers of a metallization stack provided at the second face of the package substrate.

[0171] Example 21 provides the qubit device package according to Example 20, where the metallization stack includes the two or more conductive layers separated from one another by dielectric layers.

[0172] Example 22 provides the qubit device package according to Examples 20 or 21, where the each of the two or more conductive layers includes one or more superconductive materials.

[0173] Example 23 provides the qubit device package according to any one of the preceding Examples, where the package substrate includes a silicon interposer.

[0174] Example 24 provides a method of manufacturing a qubit device package using a package substrate having a first face and an opposing second face. The method includes providing a dielectric layer over the second face of the package substrate; providing a plurality of via openings within the dielectric layer; forming a plurality of conductive pillars by filling the plurality of via openings with one or more superconductive materials; and etching a portion of the dielectric layer within a contour surrounding the plurality of conductive pillars (thus, the plurality of via openings form a group having a certain contour).

[0175] Example 25 provides the method according to Example 24, further including providing a solder bump over each of the plurality of conductive pillars.

[0176] Example 26 provides the method according to Example 25, where providing the solder bump over each of the plurality of conductive pillars includes providing the solder bump by plating, stencil printing or solder preform placement.

[0177] Example 27 provides the method according to any one of Examples 24-26, where etching the portion of the dielectric layer includes performing a dry reactive ion etch (DRIE).

[0178] Example 28 provides the method according to any one of Examples 24-27, further including performing electroplating to extend a height of the plurality of conductive pillars.

[0179] Example 29 provides the method according to Example 28, where the electroplating is performed after the etching.

[0180] Example 30 provides the method according to Example 28, where the electroplating is performed before the etching.

[0181] Example 31 provides the method according to Example 30, further including providing a conductive pad over each of the plurality of conductive pillars prior to the electroplating. Such conductive pads may account for misalignment in the electroplating step.

[0182] Example 32 provides the method according to Example 31, where providing the conductive pad over each of the plurality of conductive pillars includes performing lithography using a mask opening that is larger than a mask opening used for the electroplating.

[0183] Example 33 provides the method according to any one of Examples 28-32, where a height of each of the plurality of conductive pillars after the electroplating is between about 2 and 4 times greater than a height of each of the plurality of conductive pillars before the electroplating, e.g. between about 2 and 3 times, or between about 3 and 4 times.

[0184] Example 34 provides the method according to any one of Examples 24-33, further including attaching a die having a first face and an opposing second face to the package substrate, where the die comprises a quantum device comprising a plurality of quantum circuit components on the first face of the die and conductive contacts on the first face of the die and coupled to associated ones of

the plurality of quantum circuit components, and attaching the die to the package substrate comprises electrically connecting some of the conductive contacts at the first face of the die with some of the plurality of conductive pillars at the second face of the package substrate.

[0185] A further Example provides the method according to Example 34, further including providing a solder bump over each of the some of the conductive contacts (140) at the first face of the die prior to attaching the die to the package substrate.

[0186] Example 35 provides the method according to any one of Examples 24-34, where each of the conductive pillars has a height between about 100 and 300 micrometers.

[0187] Example 36 provides the method according to any one of Examples 24-35, where, for each of the conductive pillars, a ratio of a height of the conductive pillar to a width of the conductive pillar (i.e. aspect ratio) is between about 4 and 10.

[0188] In various further Examples, the plurality of conductive pillars in the method according to any one of Examples 24-26 may be configured as the plurality of conductive pillars in the qubit device package according to any one of Examples 1-23.

[0189] Example 37 provides a quantum computing device that includes a quantum processing device, a non-quantum processing device, and a memory device. The quantum processing device includes a die including a plurality of quantum circuit components coupled (e.g. electrically connected) to a package substrate by first level interconnects disposed between the die and the package substrate, where the first level interconnects include conductive pillars between opposing faces of the die and the package substrate, as described above. The non-quantum processing device is coupled to the quantum processing device at least partially via the package substrate to control electrical signals applied to the plurality of quantum circuit components. The memory device is configured to store data generated by the plurality of quantum circuit components during operation of the quantum processing device.

[0190] Example 38 provides the quantum computing device according to Example 37, further including a cooling apparatus configured to maintain a temperature of the die below 5 degrees Kelvin.

[0191] Example 39 provides the quantum computing device according to Examples 37 or 38, where the memory device is to store instructions for a quantum computing algorithm to be executed by the quantum processing device.

[0192] In various further Examples, the die, the package substrate, and the first level interconnects of the quantum computing device according to any one of the Examples 37-39 form a qubit device package according to any one of Examples 1-23, which may be fabricated using a method according to any one of Examples 24-36.

[0193] The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

[0194] These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

CLAIMS:

1. A qubit device package, comprising:
a die having a first face, the die comprising:
a quantum device comprising a plurality of quantum circuit components on the first face of the die, and
conductive contacts on the first face of the die and coupled to associated ones of the plurality of quantum circuit components;
a package substrate having a second face, the package substrate comprising conductive contacts on the second face of the package substrate; and
first level interconnects between the first face of the die and the second face of the package substrate and coupling some of the conductive contacts on the first face of the die with some of the conductive contacts on the second face of the package substrate,
where the first level interconnects comprise conductive pillars.

2. The qubit device package according to claim 1, wherein each of the conductive pillars has a height between 100 and 300 micrometers.

3. The qubit device package according to claim 1, wherein each of the conductive pillars has a width between 5 and 2000 micrometers.

4. The qubit device package according to claim 1, wherein, for each of the conductive pillars, a ratio of a height of the conductive pillar to a width of the conductive pillar is between 2 and 10.

5. The qubit device package according to claim 1, wherein each of the conductive pillars comprise one or more superconductive materials.

6. The qubit device package according to any one of the preceding claims, wherein a plurality of conductive pillars form a group such that a space between the first face of the die and the second face of the package substrate outside of a contour of the group includes a dielectric material, the dielectric material being substantially absent in a space between the first face of the die and the second face of the package substrate inside of a contour of the group.

7. The qubit device package according to claim 6, wherein an average distance between two adjacent conductive pillars of the plurality of adjacent conductive pillars of the group is between 10 and 2000 micrometers.

8. The qubit device package according to claim 6, wherein the plurality of quantum circuit components comprise one or more resonators, and the group is opposite at least one of the one or more resonators.

9. The qubit device package according to claim 6, wherein one conductive pillar of the group is a signal conductive pillar and other conductive pillars of the group are ground conductive pillars and form one or more ground sub-groups, the one or more ground sub-groups at least partially surrounding the signal conductive pillar.

10. The qubit device package according to claim 9, wherein the one or more ground sub-groups form a partial circle around the signal conductive pillar.

11. The qubit device package according to claim 10, wherein an area enclosed by the partial circle is between 0.0001 and 3 square millimeters.

12. The qubit device package according to claim 9, wherein the one or more ground sub-groups form a partial polygon around the signal conductive pillar.

13. The qubit device package according to any one of claims 1-5, wherein the first level interconnects further comprise conductive material elements between the conductive pillars and the conductive contacts at the first face of the die.

14. The qubit device package according to any one of claims 1-5, wherein the package substrate includes a silicon interposer.

15. A method of manufacturing a qubit device package using a package substrate having a second face, the method comprising:
providing a plurality of via openings within a dielectric layer over the second face of the package substrate;

forming a plurality of conductive pillars by filling the plurality of via openings with one or more superconductive materials; and

etching a portion of the dielectric layer within a contour surrounding the plurality of conductive pillars.

16. The method according to claim 15, further comprising providing a solder bump over each of the plurality of conductive pillars.

17. The method according to claim 16, wherein providing the solder bump over each of the plurality of conductive pillars comprises providing the solder bump by plating, stencil printing or solder preform placement.

18. The method according to claim 15, wherein etching the portion of the dielectric layer comprises performing a dry reactive ion etch (DRIE).

19. The method according to any one of claims 15-18, further comprising performing electroplating to extend a height of the plurality of conductive pillars.

20. The method according to claim 19, wherein the electroplating is performed after the etching.

21. The method according to claim 19, wherein the electroplating is performed before the etching.

22. The method according to claim 21, further comprising providing a conductive pad over each of the plurality of conductive pillars prior to the electroplating.

23. The method according to claim 22, wherein providing the conductive pad over each of the plurality of conductive pillars comprises performing lithography using a mask opening that is larger than a mask opening used for the electroplating.

24. The method according to claim 19, wherein a height of each of the plurality of conductive pillars after the electroplating is between 2 and 4 times greater than a height of each of the plurality of conductive pillars before the electroplating.

25. The method according to any one of claims 15-18, further comprising attaching a die having a first face and an opposing second face to the package substrate, wherein:

the die comprises a quantum device comprising a plurality of quantum circuit components on the first face of the die and conductive contacts on the first face of the die and coupled to associated ones of the plurality of quantum circuit components, and

attaching the die to the package substrate comprises electrically connecting some of the conductive contacts at the first face of the die with some of the plurality of conductive pillars at the second face of the package substrate.

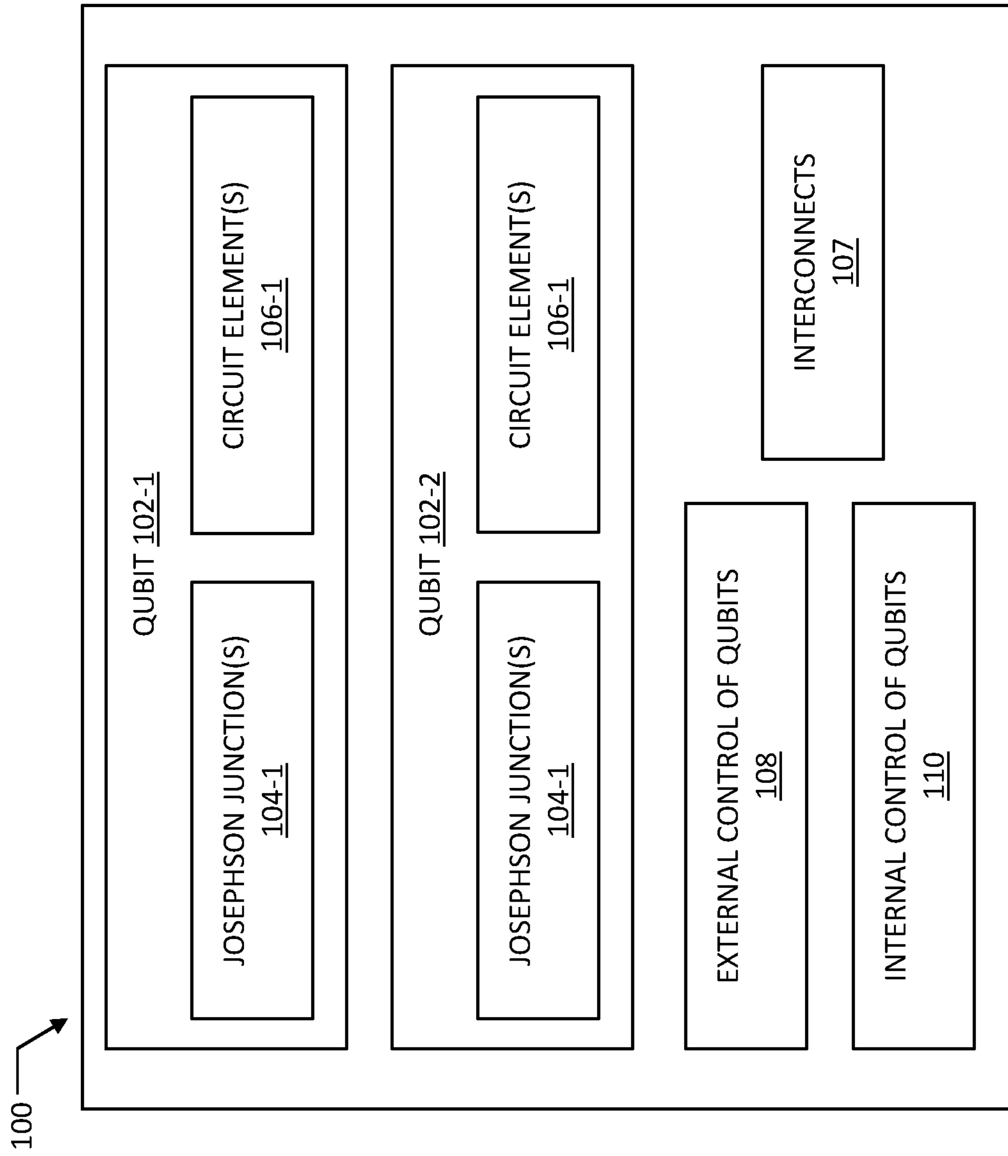


FIG. 1

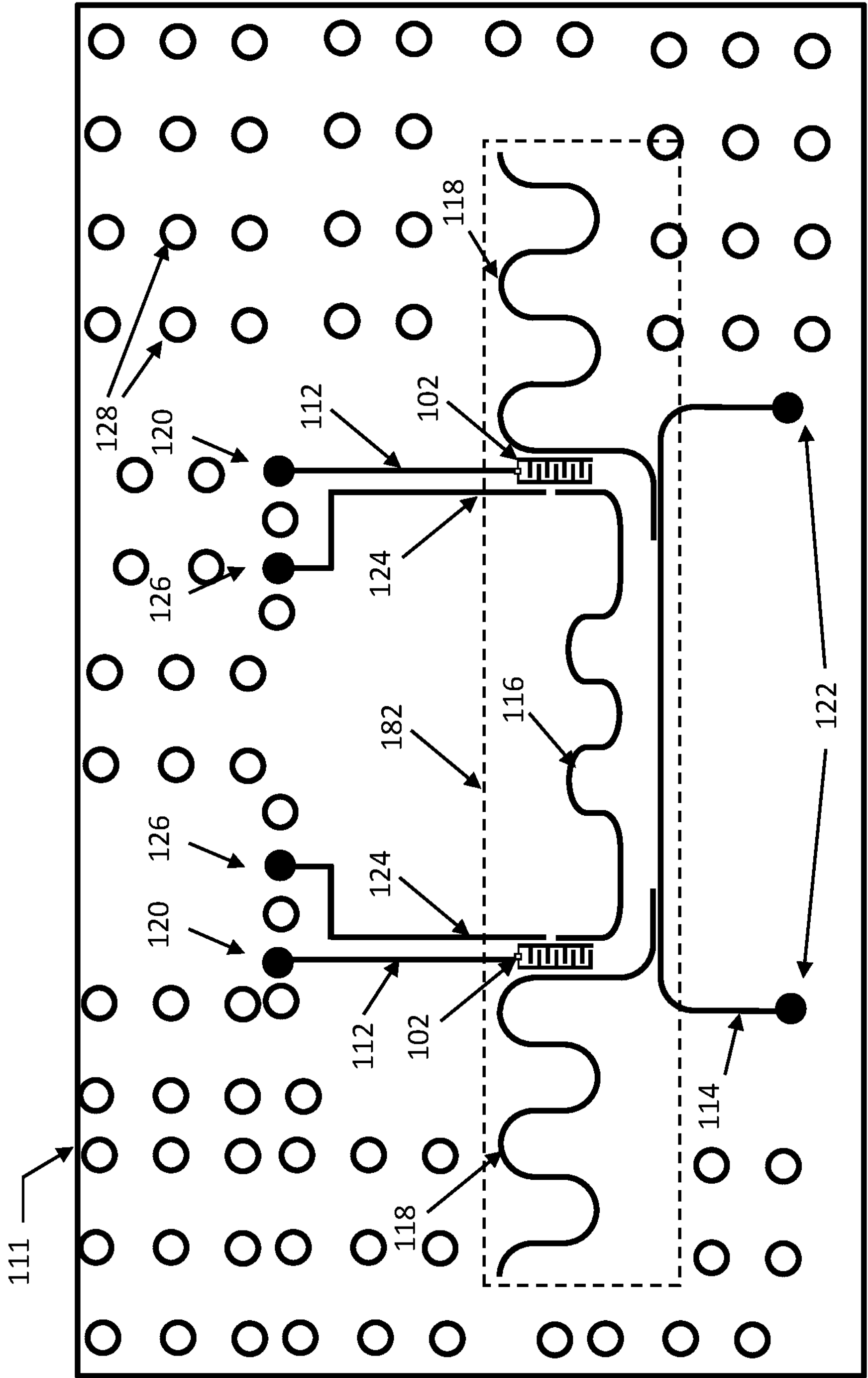


FIG. 2

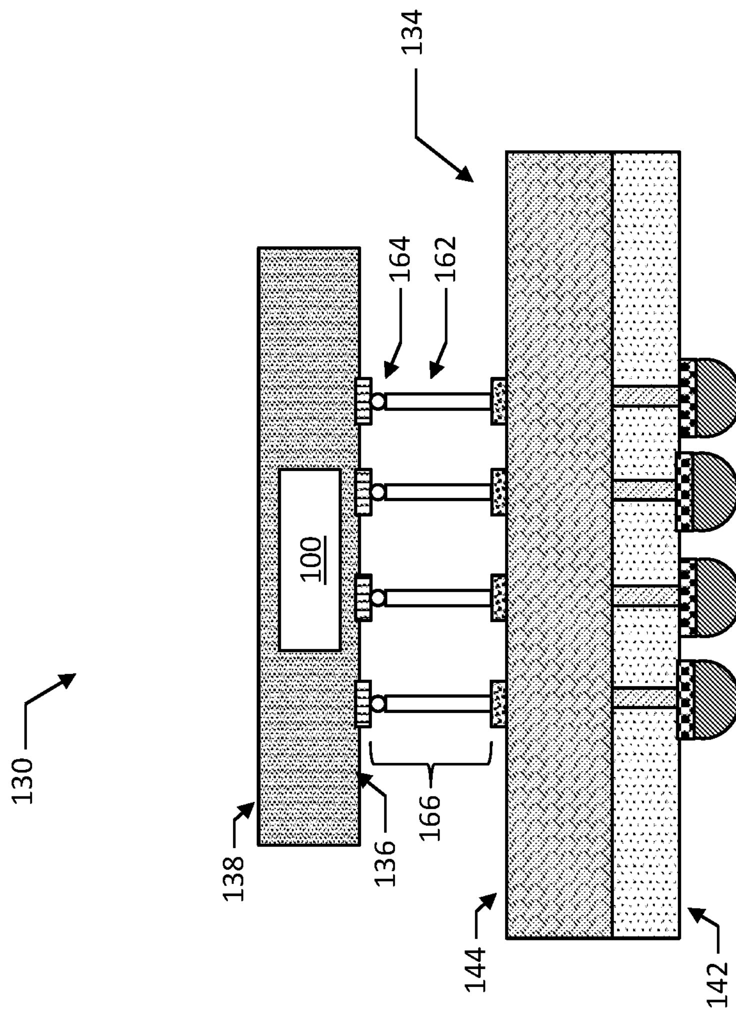
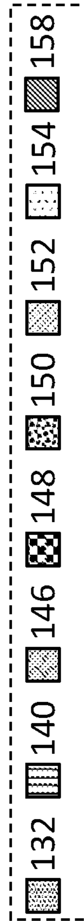


FIG. 3



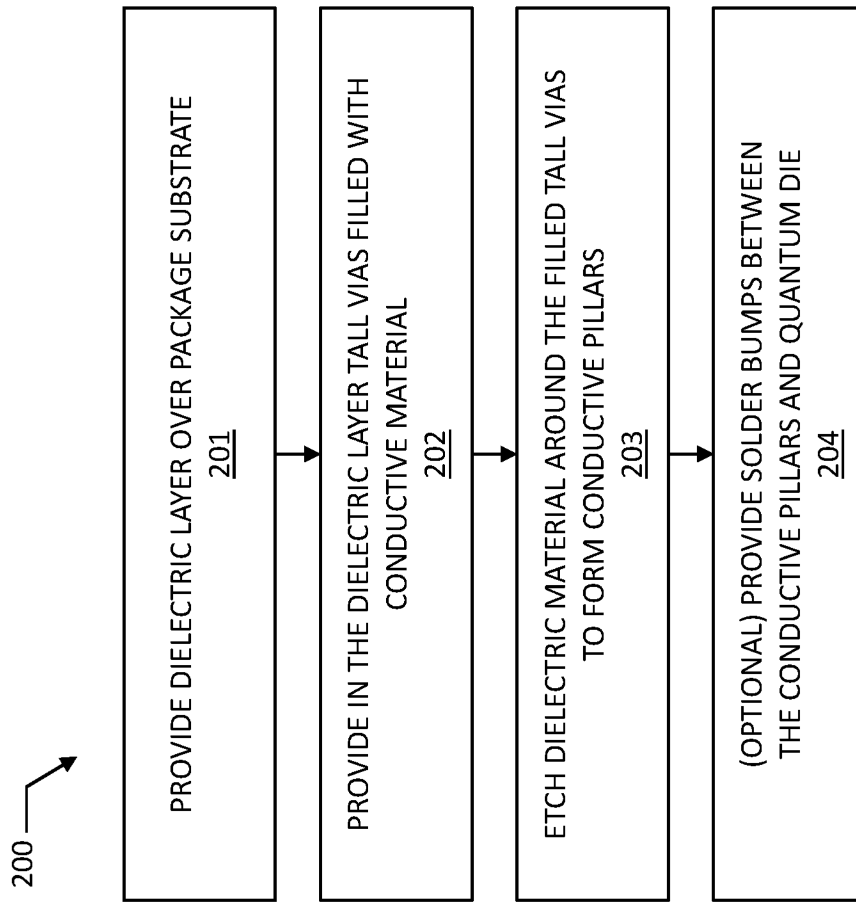


FIG. 4

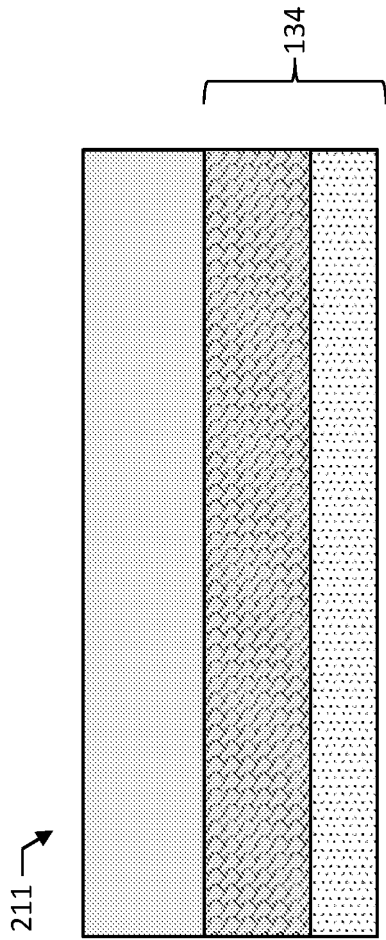


FIG. 5A

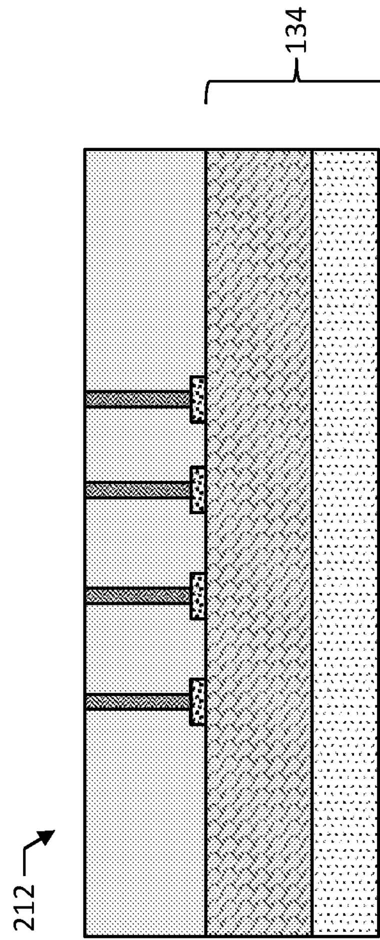
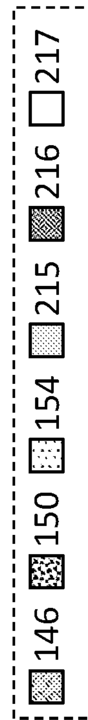


FIG. 5B



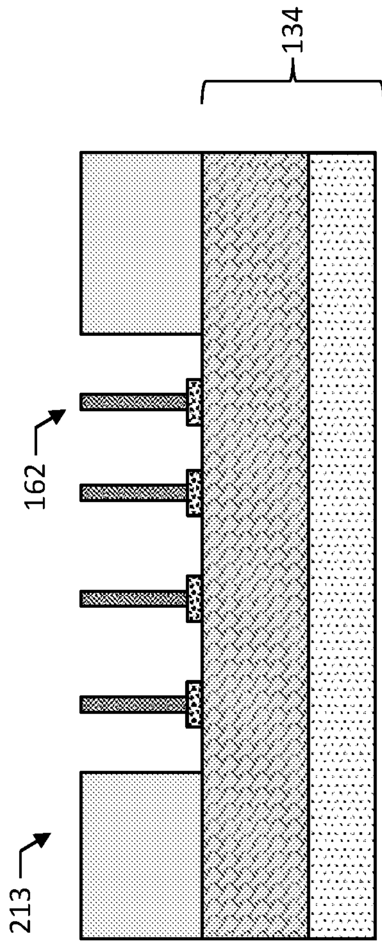


FIG. 5C

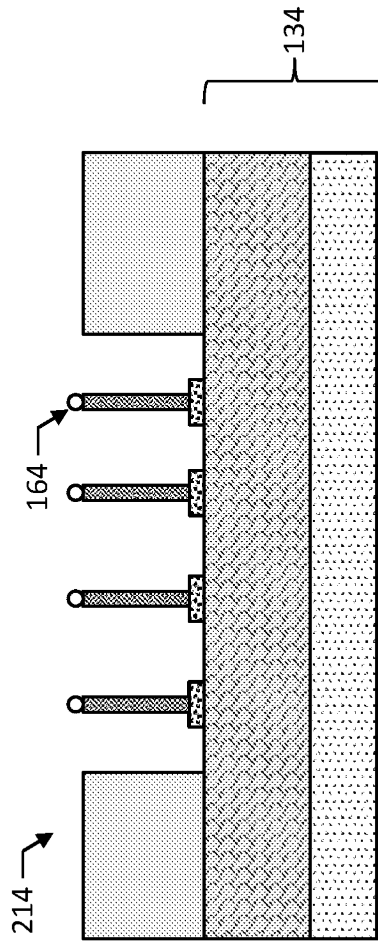
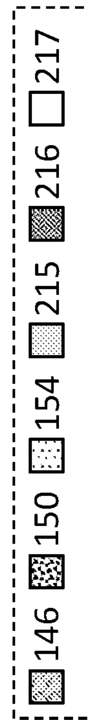


FIG. 5D



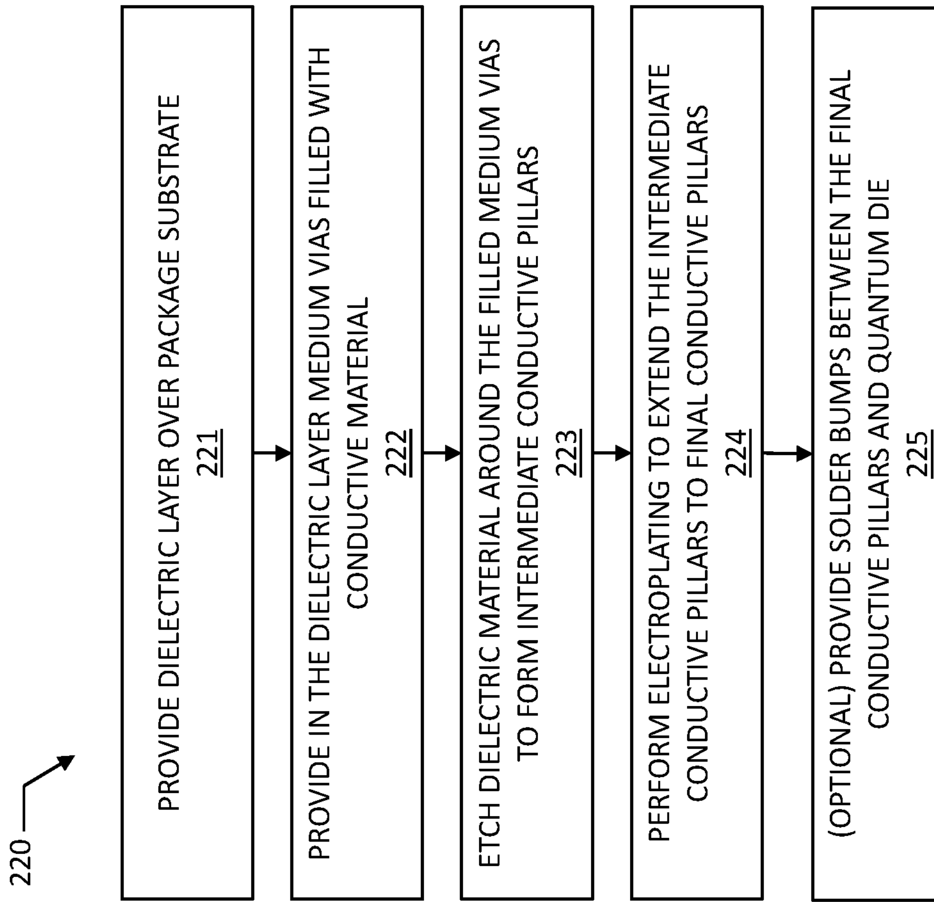


FIG. 6

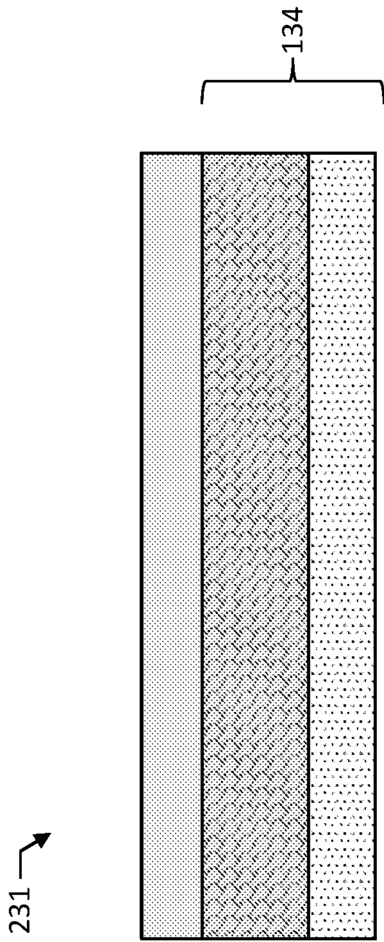


FIG. 7A

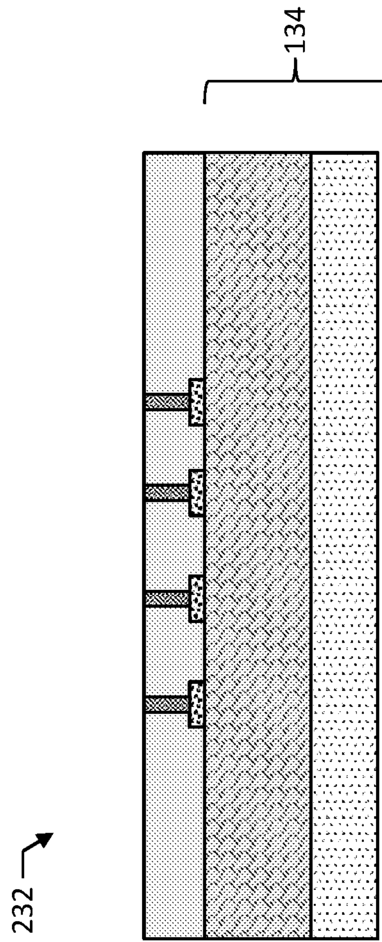
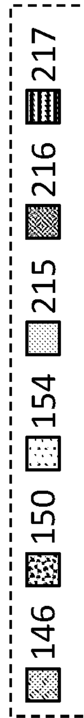


FIG. 7B



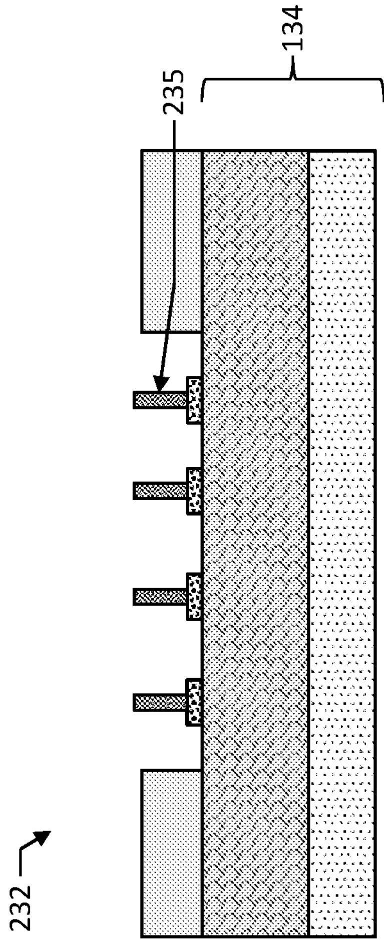


FIG. 7C

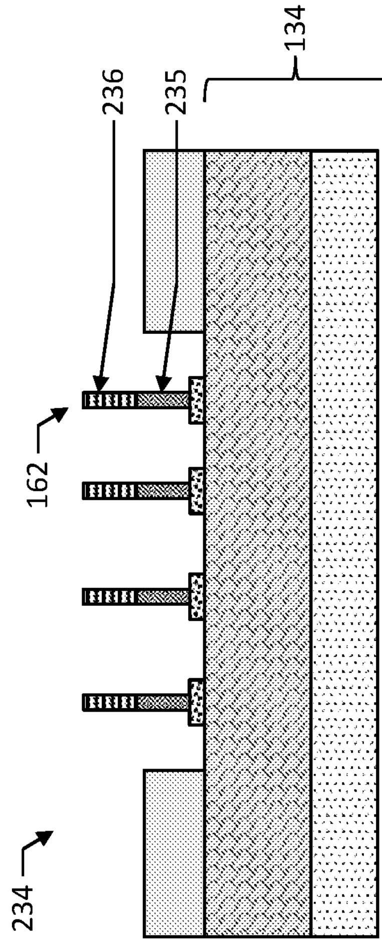
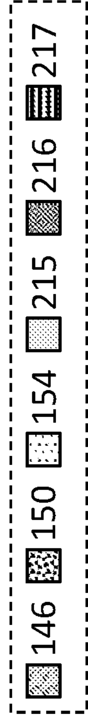


FIG. 7D



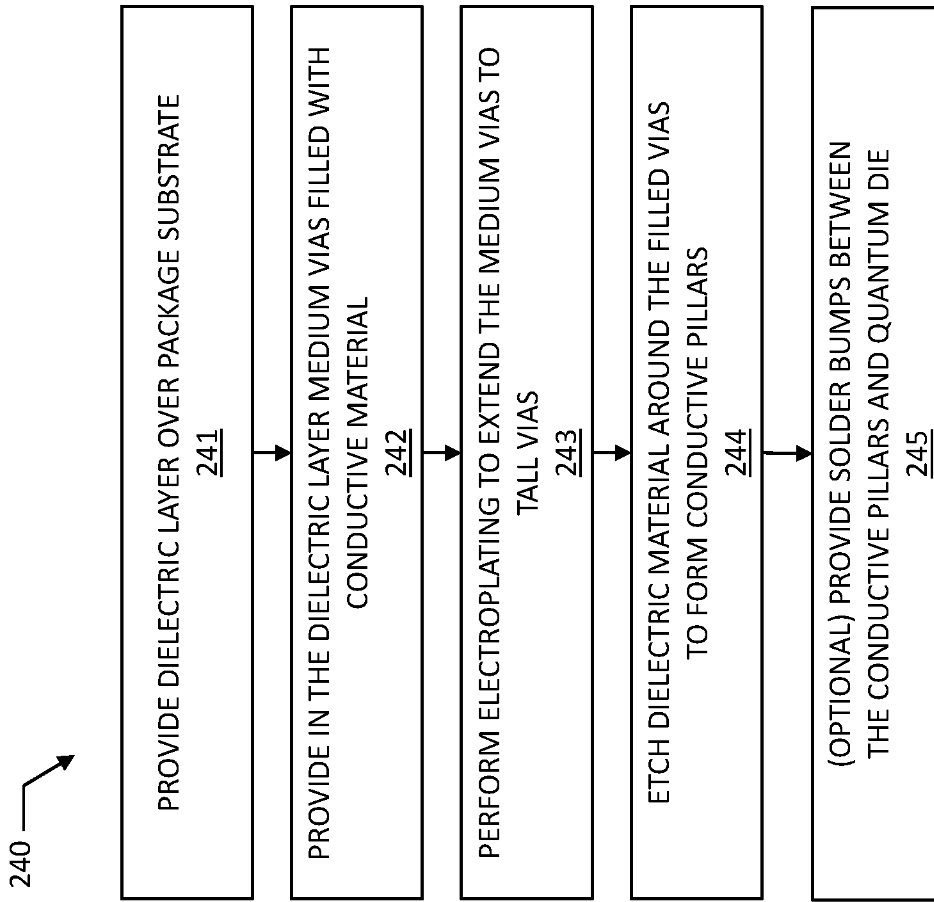


FIG. 8

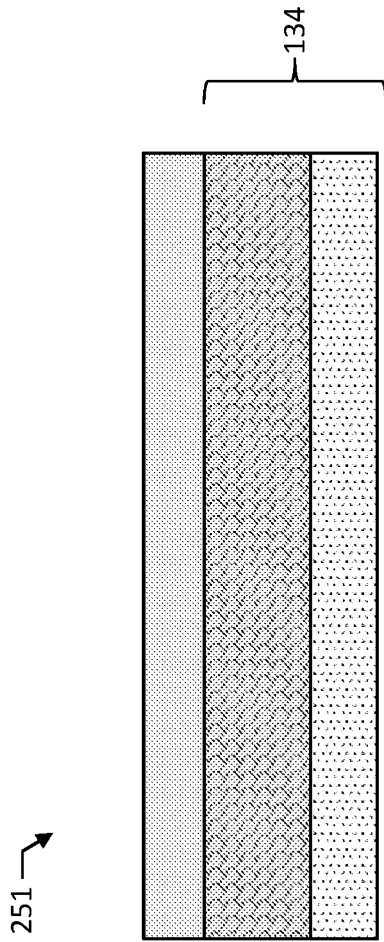


FIG. 9A

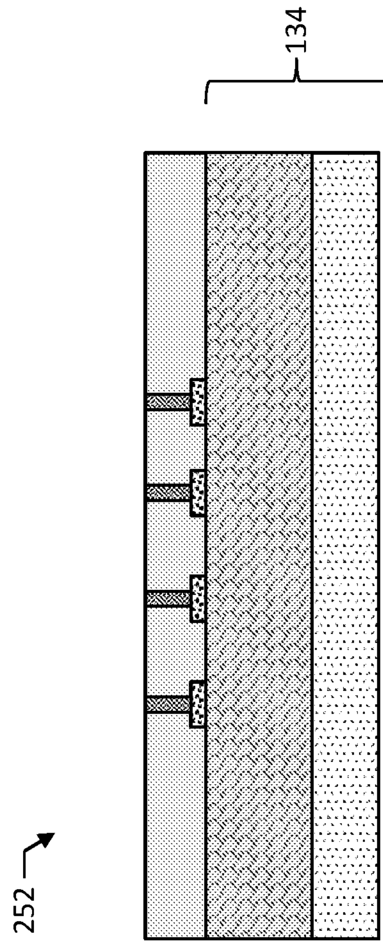
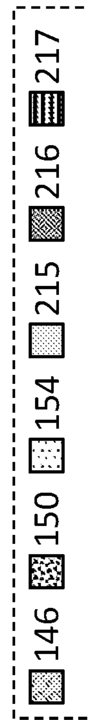


FIG. 9B



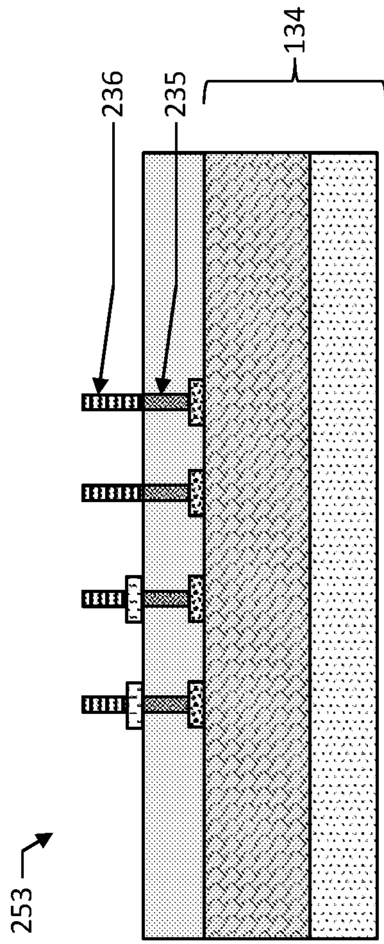


FIG. 9C

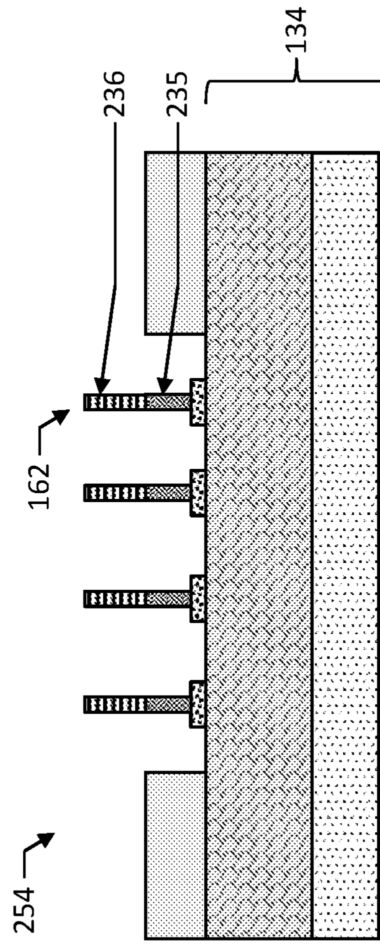
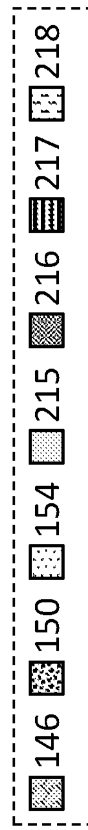


FIG. 9D



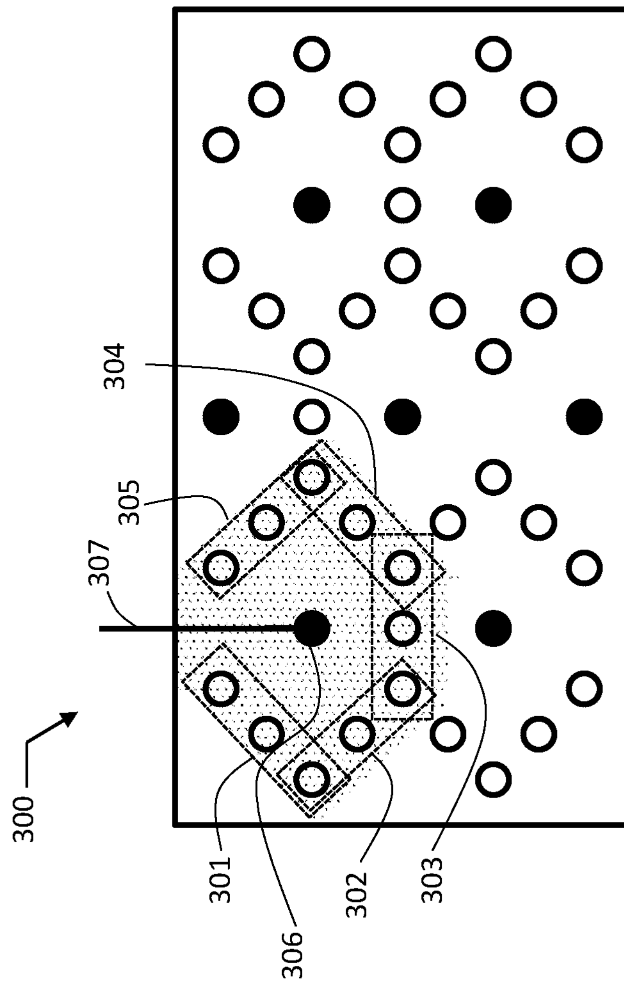


FIG. 10

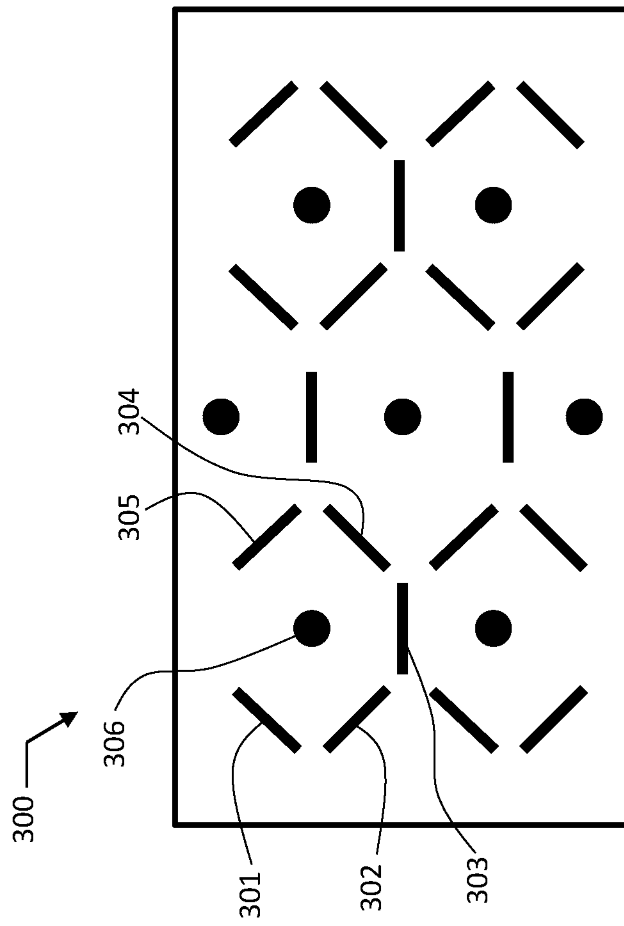


FIG. 11

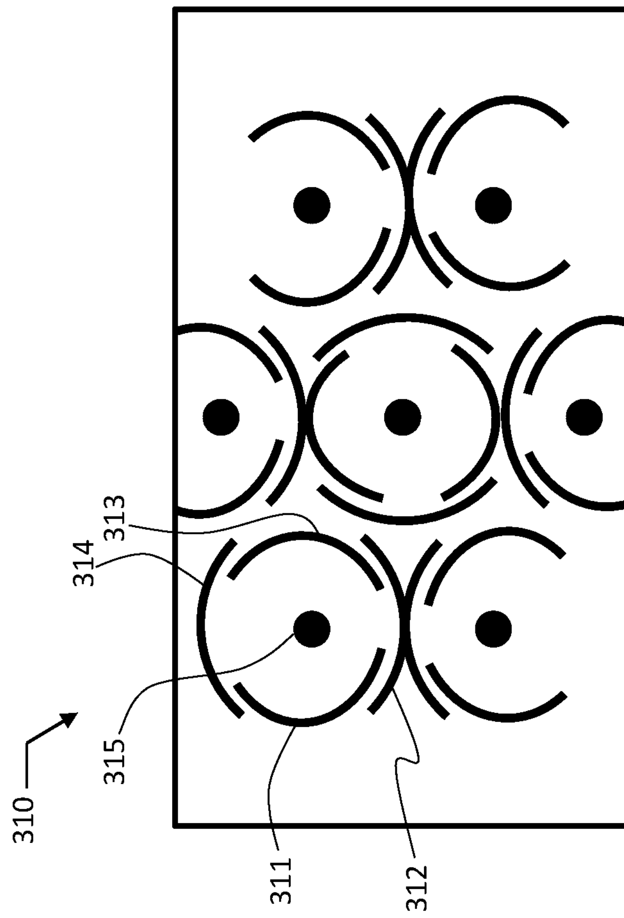


FIG. 12

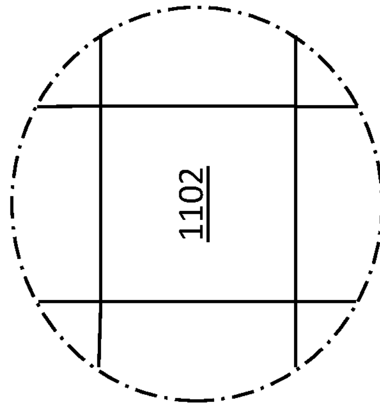


FIG. 13B

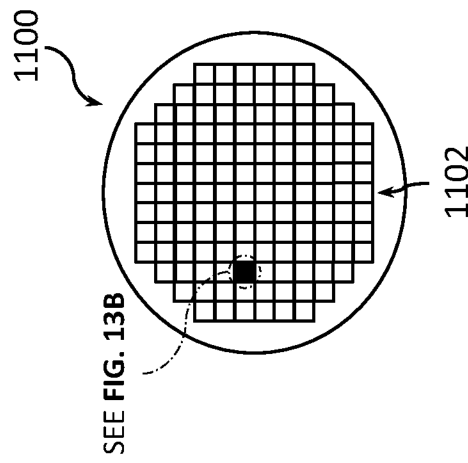


FIG. 13A

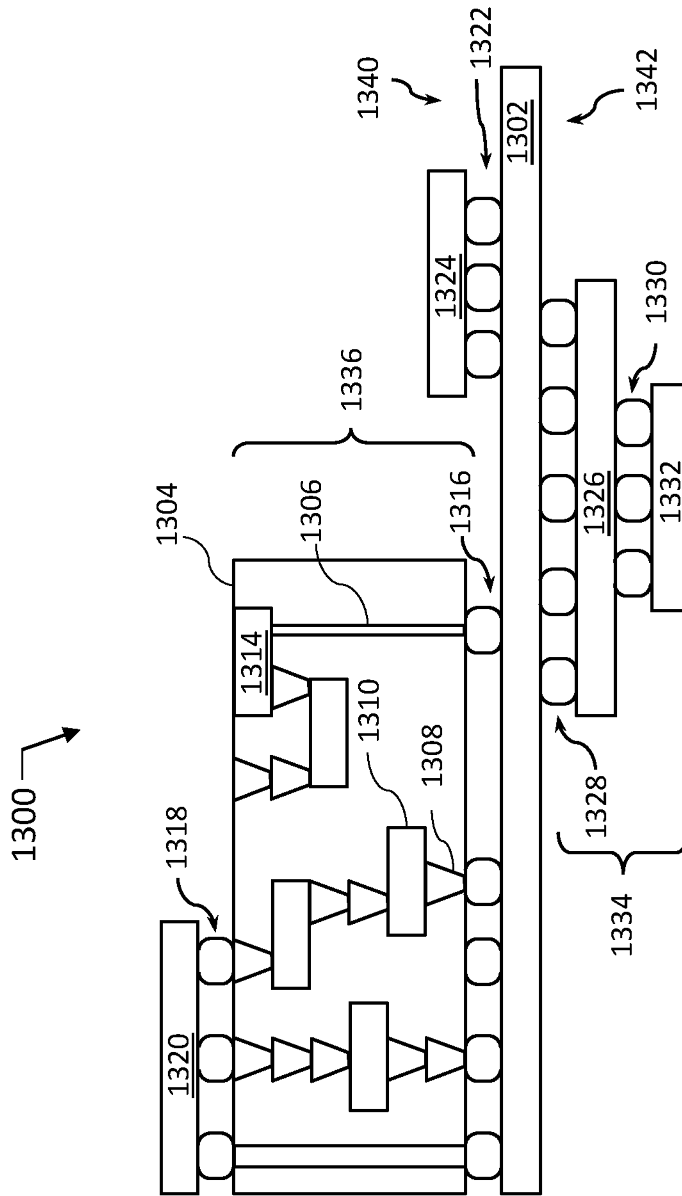


FIG. 14

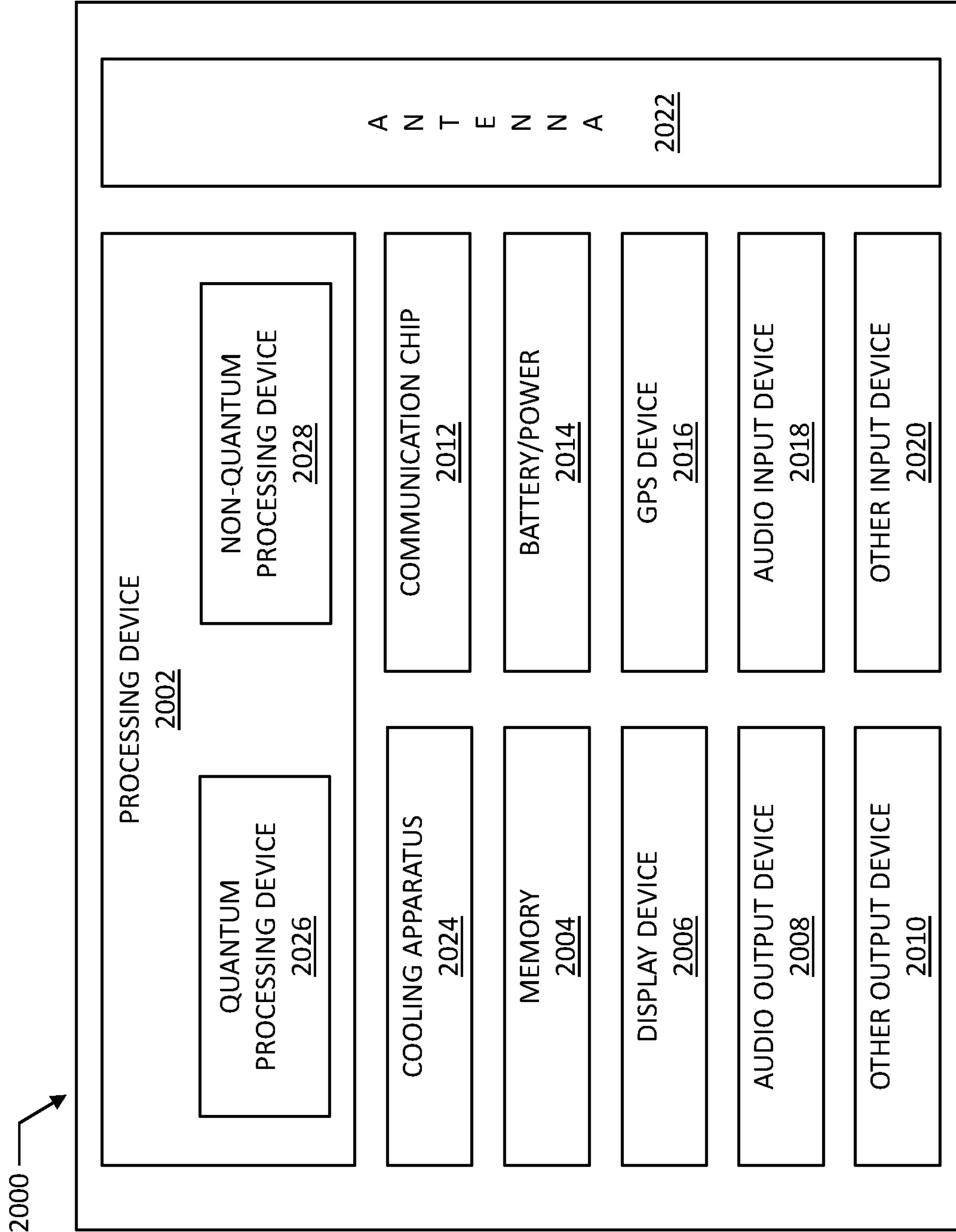


FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/037808

A. CLASSIFICATION OF SUBJECT MATTER

G06N 99/00(2010.01)i, B82Y 10/00(2011.01)n

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06N 99/00; H01L 23/00; H03K 19/195; H01L 21/50; H01L 29/06; H01L 23/498; H01L 31/109; H01L 21/48; B82Y 10/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: integrated, circuit, package, substrate, die, interconnect, pillar, height, width, ratio, quantum, component, resonator, and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2017-0141073 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 18 May 2017 See paragraphs [0021]-[0022], [0028]-[0031], [0040]-[0041], [0044]-[0045], [0047], [0061]; claim 1; and figures 1A, 2A, 5B-5D, 8.	15-24
Y		1-8,13-14,25
A		9-12
Y	US 2009-0206871 A1 (JAMES E. BAUMGARDNER et al.) 20 August 2009 See paragraph [0030]; and figure 1A.	1-8,13-14,25
A	US 2002-0030186 A1 (AKIHISA TOMITA) 14 March 2002 See paragraphs [0047]-[0060]; and figures 1-3.	1-25
A	US 2016-0343646 A1 (QUALCOMM INCORPORATED) 24 November 2016 See paragraphs [0036]-[0049]; and figures 3-6.	1-25
A	US 2015-0001705 A1 (MINKYUNG KANG et al.) 01 January 2015 See paragraphs [0031]-[0060]; and figures 1-3.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means
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"&" document member of the same patent family

Date of the actual completion of the international search
16 May 2018 (16.05.2018)

Date of mailing of the international search report
23 May 2018 (23.05.2018)

Name and mailing address of the ISA/KR
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BYUN, Sung Cheal
Telephone No. +82-42-481-8262

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