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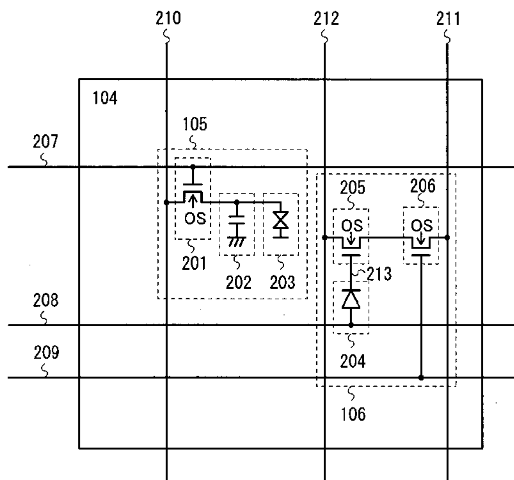
(54) **Title**: DISPLAY DEVICE



(57) **Abstract**: The display device has a display panel where a photosensor and a transistor including an oxide semiconductor layer are arranged. The display device detects a shadow of the object, which is projected on the display panel when the object approaches the display panel and blocks ambient light, with a photosensor, whereby a position or motion of the object is detected. Even when the object is not in contact with the display panel, the object can be detected.

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DESCRIPTION

DISPLAY DEVICE

5 TECHNICAL FIELD

[0001]

The technical field of the present invention relates to a display device and a driving method thereof.

10 BACKGROUND ART

[0002]

In recent years, a display panel provided with a touch sensor has attracted attention. Examples of the touch sensor includes a resistive touch sensor, a capacitive touch sensor, and an optical touch sensor which are different in operation principle.
15 An object (e.g., a pen or a finger) touches a display device, whereby data can be input to the display device.

[0003]

As an example of a device including such an optical touch sensor, a display device having an image capturing function, which is provided with a contact type area
20 sensor that captures an image, is given (e.g., see Patent Document 1).

[Reference]

[0004]

[Patent Document 1] Japanese Published Patent Application No. 2001-292276

25 DISCLOSURE OF INVENTION

[0005]

In the case of a display panel provided with the above touch sensor as an input device, the surface of the display panel continues to be touched by an object. Therefore, the display panel gets dirty easily and has a possibility that the display
30 quality is degraded. The display panel needs to have proper mechanical strength. Further, there is a problem in that the users of the display panel tend to be tired when the surface of the display panel is hard, for example.

[0006]

In view of the above problems, it is an objective to make it possible that a device detects a position and motion of an object even when the object is not in contact with a display panel.

5 [0007]

A circuit including a transistor is provided for a display panel having a touch sensor as an input device.

[0008]

When a transistor including single crystal silicon is used, the size of an area

10 sensor is limited by the size of a single crystal silicon substrate. In other words, formation of a large area sensor or a large area sensor also serving as a display device using a single crystal silicon substrate is costly and impractical.

[0009]

On the other hand, the size of a substrate can be easily increased when a thin

15 film transistor (TFT) including amorphous silicon is employed. However, field-effect mobility of an amorphous silicon thin film is low; thus, there is a limit on a circuit design; therefore, an area occupied by a circuit is increased.

[0010]

Further, thin film transistors including polycrystalline silicon are formed in

20 many cases by employing a method with which crystallization is performed by excimer laser annealing and therefore vary in their characteristics because of excimer laser annealing. Therefore, it is difficult to generate intensity distribution of detected light into electrical signals with high reproducibility with a photosensor using circuits including thin film transistors which vary in their characteristics.

25 [0011]

An object of an embodiment of the present invention is to provide a display panel including as an input device a touch sensor which can be mass-produced over a large substrate and has uniform and stable electric characteristics.

[0012]

30 Another object of an embodiment of the present invention is to provide a display device including a highly-functional touch sensor capable of fast response as an input device.

[0013]

A display device including a touch sensor as an input device is provided with a circuit having a transistor including an oxide semiconductor layer.

[0014]

5 However, a difference from the stoichiometric composition in the oxide semiconductor arises in a thin film formation process. For example, electric conductivity of the oxide semiconductor changes due to the excess or deficiency of oxygen. Further, hydrogen or moisture that enters the oxide semiconductor thin film during the formation of the thin film forms an oxygen (O)-hydrogen (H) bond and 10 serves as an electron donor, which is a factor of changing electric conductivity. Furthermore, since the O-H bond is a polar molecule, it serves as a factor of varying the characteristics of an active device such as a thin film transistor manufactured using an oxide semiconductor.

[0015]

15 In order to prevent variation in electric characteristics of the thin film transistor including an oxide semiconductor layer, which is disclosed in this specification, impurities such as hydrogen, moisture, a hydroxyl group, or a hydride (also referred to as a hydrogen compound) which cause the variation are intentionally removed from the oxide semiconductor layer. Additionally, the oxide semiconductor layer is highly 20 purified to become i-type (intrinsic) by supplying oxygen which is a major component of an oxide semiconductor, which is simultaneously reduced in a step of removing impurities.

[0016]

Therefore, it is preferable that the oxide semiconductor contains hydrogen and 25 carriers as little as possible. In the thin film transistor disclosed in this specification, a channel formation region is formed in the oxide semiconductor layer, in which hydrogen contained in the oxide semiconductor is set less than or equal to 5×10^{19} /cm^3, preferably, less than or equal to 5×10^{18} /cm^3, more preferably, less than or equal to 5×10^{17} /cm^3 or less than 5×10^{16} /cm^3; hydrogen contained in the oxide semiconductor is 30 removed as much as possible to be close to 0; and the carrier concentration is less than 5×10^{14} /cm^3, preferably, less than or equal to 5×10^{12} /cm^3.

[0017]

It is preferable that an off-state current be as small as possible in reverse characteristics of a thin film transistor. An off-state current (also referred to as a leakage current) is a current that flows between a source and a drain of a thin film
5 transistor in the case where a given gate voltage between –1 V to –10 V is applied. A current value per 1 μm in a channel width (w) of a thin film transistor including an oxide semiconductor, which is disclosed in this specification, is less than or equal to 100 aA/μm, preferably, less than or equal to 10 aA/μm, more preferably, less than or equal to 1 aA/μm. Further, since there is no pn junction and no hot carrier degradation,
10 electric characteristics of the thin film transistor is not adversely affected.

[0018]

The above concentration range of hydrogen can be obtained by secondary ion mass spectrometry (SIMS) or on the basis of data of SIMS. In addition, the carrier concentration can be measured by Hall effect measurement. As an example of an
15 equipment used for Hall effect measurement, the specific resistance/hole measuring system ResiTest 8310 (manufactured by TOYO Corporation) can be given. With the specific resistance/Hall measuring system ResiTest 8310, the direction and strength of a magnetic field are changed in a certain cycle and in synchronization therewith, only a Hall electromotive voltage caused in a sample is detected, so that AC (alternate current)
20 Hall measurement can be performed. Even in the case of a material with low mobility and high resistivity, a Hall electromotive voltage can be detected.

[0019]

As the oxide semiconductor layer used in this specification, any of a four-component metal oxide such as an In-Sn-Ga-Zn-O film, a three-component metal
25 oxide such as an In-Ga-Zn-O film, an In-Sn-Zn-O film, an In-Al-Zn-O film, a Sn-Ga-Zn-O film, an Al-Ga-Zn-O film, and a Sn-Al-Zn-O film, or a two-component metal oxide such as an In-Zn-O film, a Sn-Zn-O film, an Al-Zn-O film, a Zn-Mg-O film, a Sn-Mg-O film, and an In-Mg-O film, or a one-component metal oxide such as an In-O film, a Sn-O film, and a Zn-O film can be used. Further, SiO_2 may be contained in the
30 above oxide semiconductor layer.

[0020]

Note that as the oxide semiconductor layer, a thin film expressed by $InMO_3(ZnO)_m$ ($m > 0$) can be used. Here, M represents one or more metal elements selected from Ga, Al, Mn, and Co. For example, M can be Ga, Ga and Al, Ga and Mn, Ga and Co, or the like. An oxide semiconductor layer whose composition formula is represented by $InMO_3(ZnO)_m$ ($m > 0$), which includes Ga as M, is referred to as the In-Ga-Zn-O oxide semiconductor described above, and a thin film of the In-Ga-Zn-O oxide semiconductor is also referred to as an In-Ga-Zn-O-based non-single-crystal film.

[0021]

According to an embodiment, a display device has a display panel where a photosensor and a thin film transistor including an oxide semiconductor layer are arranged. The display device detects a shadow projected on the display panel when the object approaches the display panel and blocks ambient light. A position or motion of the shadow is detected, whereby a position or motion of the object is detected.

[0022]

According to another embodiment, a display device has a display panel where a photosensor and a thin film transistor including an oxide semiconductor layer are arranged. The display device detects light emitted from the display panel and reflected by an object with the photosensor when the object approaches the display panel. That is, when an image of a contactless object is shot by the photosensor, a position or motion of the object is detected.

[0023]

Thus, even in the case where an object is not in contact with a display panel, the object can be detected.

[0024]

Another embodiment is a display device having a display panel where pixels each including a photosensor and a thin film transistor including an oxide semiconductor layer are arranged in matrix; and an image processing portion. The display device has a function of detecting a contactless object. The photosensor is configured to detect a shadow of an object projected on the display panel. The image processing portion is configured to detect a position of the object on the basis of a position of the shadow of the object, and motion of the object on the basis of motion of the shadow.

[0025]

Another embodiment is a display device having a display panel where pixels each including a photosensor and a thin film transistor including an oxide semiconductor layer are arranged in matrix; and an image processing portion. The display device has a function of detecting a contactless object. The photosensor is configured to detect a shadow of an object projected on the display panel. The image processing portion is configured to detect a position of the object on the basis of a position of the shadow of the object, and motion of the object on the basis of motion of the shadow. The image processing portion is configured to recognize a region including the largest number of pixels detecting the shadow among a plurality of regions obtained by dividing the display panel, as positional data of the object.

[0026]

Another embodiment is a display device having a display panel where pixels each including a photosensor and a thin film transistor including an oxide semiconductor layer are arranged in matrix; and an image processing portion. The display device has a function of detecting a contactless object. The photosensor is configured to detect a shadow of an object projected on the display panel. The image processing portion is configured to detect a position of the object on the basis of a position of the shadow of the object, and motion of the object on the basis of motion of the shadow. The image processing portion is configured to recognize a region including the largest number of pixels detecting the shadow among a plurality of regions obtained by dividing the display panel, as positional data of the object. The image processing portion is configured to detect the motion of the object by comparing the successive positional data.

[0027]

Another embodiment is a display device having a display panel including a photodetection portion where pixels each include a first photosensor and a first thin film transistor including an oxide semiconductor layer and an area sensor where pixels each include a second photosensor and a second thin film transistor including an oxide semiconductor layer; and an image processing portion. The display device has a function of detecting a contactless object. The first photosensor is configured to detect a shadow of an object projected on the display panel. The image processing portion is

configured to detect a position of the object on the basis of a position of the shadow of the object, and motion of the object on the basis of motion of the shadow.

[0028]

Another embodiment is a display device having a display panel including a photodetection portion where pixels each include a first photosensor and a first thin film transistor including an oxide semiconductor layer and an area sensor where pixels each include a second photosensor and a second thin film transistor including an oxide semiconductor layer; and an image processing portion. The display device has a function of detecting a contactless object. The first photosensor is configured to detect a shadow of an object projected on the display panel. The image processing portion is configured to detect a position of the object on the basis of a position of the shadow of the object, and motion of the object on the basis of motion of the shadow. The image processing portion is configured to recognize a region including the largest number of pixels detecting the shadow among a plurality of regions obtained by dividing the display panel, as positional data of the object.

[0029]

Another embodiment is a display device having a display panel including a photodetection portion where pixels each include a first photosensor and a first thin film transistor including an oxide semiconductor layer and an area sensor where pixels each include a second photosensor and a second thin film transistor including an oxide semiconductor layer; and an image processing portion. The display device has a function of detecting a contactless object. The first photosensor is configured to detect a shadow of an object projected on the display panel. The image processing portion is configured to detect a position of the object on the basis of a position of the shadow of the object, and motion of the object on the basis of motion of the shadow. The image processing portion is configured to recognize a region including the largest number of pixels detecting the shadow among a plurality of regions obtained by dividing the display panel, as positional data of the object. The image processing portion is configured to detect the motion of the object by comparing the successive positional data.

[0030]

Another embodiment is a display device having a display panel including a

photodetection portion where pixels each include an infrared light sensor and a thin film transistor including an oxide semiconductor layer and an area sensor where pixels each include a visible light sensor. The photodetection portion is configured to detect light emitted from the display panel and reflected by an object when the object is not in
5 contact with the display panel. The area sensor is configured to detect light emitted from the display panel and reflected by the object when the object is in contact with the display panel.

[0031]

In the above structure, the number of the second photosensors is larger than
10 that of the first photosensors.

[0032]

In the above structure, the second photosensors are provided on the periphery of the first photosensor.

[0033]

15 When a contactless object can be detected, the frequency at which the object touches a display panel can be reduced and thus degradation in display quality can be prevented.

[0034]

With a thin film transistor including an oxide semiconductor layer, a display
20 device including a highly-functional touch panel capable of fast response as an input device can be provided.

BRIEF DESCRIPTION OF DRAWINGS

[0035]

25 FIG. 1 illustrates a structure of a display panel.

FIG. 2 illustrates a structure of a display panel.

FIG. 3 illustrates a structure of a display panel.

FIG. 4 is a timing chart.

FIG. 5 illustrates a structure of a display panel.

30 FIG. 6 is a cross-sectional view of a display panel.

FIG. 7 is a cross-sectional view of a display panel.

FIG. 8 illustrates a structure of a display panel.

FIGS. 9A to 9D each illustrate an example of an electronic device having a display panel.

FIG. 10 illustrates an image processing.

FIGS. 11A and 11B illustrate an image processing.

5 FIGS. 12A to 12E illustrate a thin film transistor and a method for manufacturing the thin film transistor.

FIGS. 13A to 13E illustrate a thin film transistor and a method for manufacturing the thin film transistor.

FIGS. 14A to 14D illustrate a thin film transistor and a method for 10 manufacturing the thin film transistor.

FIGS. 15A to 15D illustrate a thin film transistor and a method for manufacturing the thin film transistor.

FIG. 16 illustrates a thin film transistor.

FIG. 17 illustrates a thin film transistor.

15 FIG. 18 is a longitudinal cross-sectional view of an inverted staggered thin film transistor including an oxide semiconductor.

FIG. 19A is an energy band diagram (schematic diagram) of a cross section along A-A′ in FIG. 18, and FIG. 19B is an energy band diagram at the time when a voltage is applied.

20 FIG. 20A is an energy band diagram illustrating a state in which positive potential ($+V_G$) is applied to a gate (G1), and FIG. 20B is an energy band diagram illustrating a state in which negative potential ($-V_G$) is applied to a gate (G1).

FIG. 21 is an energy band diagram illustrating relationships between a vacuum level and a work function of a metal (ϕM) and between the vacuum level and electron 25 affinity (χ) of an oxide semiconductor.

FIG. 22 is a graph showing a relationship between field-effect mobility of a transistor and a frame frequency of image shooting, which is obtained by calculation.

BEST MODE FOR CARRYING OUT THE INVENTION

30 [0036]

Hereinafter, embodiments will be described in detail with reference to the

accompanying drawings. However, since embodiments described below can be embodied in many different modes, it is easily understood by those skilled in the art that the mode and the detail can be variously changed without departing from the scope of the present invention. Therefore, the disclosed invention should not be interpreted as 5 being limited to the following description of the embodiments. In the drawings for describing the embodiments, the same parts or parts having a similar function are denoted by the same reference numerals, and description of such parts is not repeated.

[0037]

(Embodiment 1)

10 In this embodiment, a display panel will be described with reference to FIG. 1, FIG. 2, FIG. 3, FIG. 4, and FIG. 5.

[0038]

A structure of the display panel will be described with reference to FIG. 1. A display panel 100 includes a pixel circuit 101, a display element control circuit 102, and 15 a photosensor control circuit 103. The pixel circuit 101 includes a plurality of pixels 104 arranged in a matrix of rows and columns. Each of the pixels 104 includes a display element 105 and a photosensor 106.

[0039]

Each of the display elements 105 includes a thin film transistor (TFT), a 20 storage capacitor, a liquid crystal element including a liquid crystal layer, and the like. The thin film transistor has a function of controlling injection or ejection of charge to/from the storage capacitor. The storage capacitor has a function of holding charge which corresponds to voltage applied to the liquid crystal layer. Taking advantage of the change in the direction of a polarization due to a voltage application to the liquid 25 crystal layer, tone of light passing through the liquid crystal layer is made (gray scale display is performed), so that image display is realized. Light that a light source (a backlight) emits from the rear side of a liquid crystal display device is used as the light passing through the liquid crystal layer.

[0040]

30 Note that the case where the display elements 105 include liquid crystal elements is described; however, other elements such as light-emitting elements may be included. The light-emitting element is an element in which the luminance is

controlled by current or voltage. Specifically, a light emitting diode, an EL element (organic EL element (organic light emitting diode (OLED) or an inorganic EL element), and the like are given.

[0041]

5 The photosensors 106 each include an element such as a photodiode, which has a function of generating an electrical signal when receiving light, and a thin film transistor. Note that as light which is received by the photosensors 106, ambient light is used in the case where image shooting data of a shadow of an object is detected, whereas reflected light obtained when light from a backlight is delivered to an object is 10 used in the case where image shooting data of the object itself is detected.

[0042]

The display element control circuit 102 controls the display elements 105 and includes a display element driver circuit 107 and a display element driver circuit 108. The display element driver circuit 107 inputs a signal to the display elements 105 15 through signal lines (also referred to as "source signal lines") such as video data signal lines. The display element driver circuit 108 inputs a signal to the display elements 105 through scan lines (also referred to as "gate signal lines"). For example, the display element driver circuit 108 for driving the scan lines has a function of selecting display elements 105 included in the pixels placed in a particular row. Further, the 20 display element driver circuit 107 for driving the signal lines has a function of giving a predetermined potential to the display elements 105 included in the pixels placed in the selected row. Note that in the display elements to which the display element driver circuit 108 for driving the scan lines gives a high potential, the thin film transistors are brought into conduction and charges given by the display element driver circuit 107 for 25 driving the signal lines are supplied to the display elements.

[0043]

The photosensor control circuit 103 controls the photosensor 106 and includes a photosensor readout circuit 109 connected to a photosensor output signal line and a photosensor reference signal line, and a photosensor driver circuit 110. The 30 photosensor driver circuit 110 has a function of performing reset operation and selecting operation on the photosensors 106 included in the pixels placed in a particular row, which are described below. Further, the photosensor readout circuit 109 has a function

of taking out output signals of the photosensors 106 included in the pixels in the selected row. Note that the photosensor readout circuit 109 may have a configuration in which an output, which is an analog signal, of the photosensor is extracted as an analog signal to the outside of the display panel by an OP amplifier; or a configuration in which the output is converted into a digital signal by an A/D converter circuit and then extracted to the outside of the display panel.

[0044]

The display panel 100 including a photosensor is provided with a circuit having a transistor including an oxide semiconductor layer.

[0045]

In order to prevent variation in electric characteristics of the thin film transistor including an oxide semiconductor layer, which is included in the display panel 100 including a photosensor, impurities such as hydrogen, moisture, a hydroxyl group, or a hydride (also referred to as a hydrogen compound) which cause the variation are intentionally removed from the oxide semiconductor layer. Additionally, the oxide semiconductor layer is highly purified to become i-type (intrinsic) by supplying oxygen which is a major component of an oxide semiconductor, which is simultaneously reduced in a step of removing impurities.

[0046]

Therefore, it is preferable that the oxide semiconductor contains hydrogen and carriers as little as possible. In the thin film transistor disclosed in this specification, a channel formation region is formed in the oxide semiconductor layer, in which hydrogen contained in the oxide semiconductor is set less than or equal to 5×10^{19} /cm^3, preferably, less than or equal to 5×10^{18} /cm^3, more preferably, less than or equal to 5×10^{17} /cm^3 or less than 5×10^{16} /cm^3; hydrogen contained in the oxide semiconductor is removed as much as possible to be close to 0; and the carrier concentration is less than 5×10^{14} /cm^3, preferably, less than or equal to 5×10^{12} /cm^3.

[0047]

It is preferable that an off-state current be as small as possible in reverse characteristics of a thin film transistor. An off-state current is a current that flows between a source and a drain of a thin film transistor in the case where a given gate

voltage between −1 V to −10 V is applied. A current value per 1 μm in a channel width (w) of a thin film transistor including an oxide semiconductor, which is disclosed in this specification, is less than or equal to 100 aA/μm, preferably, less than or equal to 10 aA/μm, more preferably, less than or equal to 1 aA/μm. Further, since there is no
5 pn junction and no hot carrier degradation, electric characteristics of the thin film transistor is not adversely affected.

[0048]

A circuit diagram of the pixel 104 will be described with reference to FIG. 2. The pixel 104 includes the display element 105 including a transistor 201, a storage
10 capacitor 202, and a liquid crystal element 203; and the photosensor 106 including a photodiode 204, a transistor 205, and a transistor 206. In FIG. 2, the transistor 201, the transistor 205, and the transistor 206 are each a thin film transistor including an oxide semiconductor layer.

[0049]

15 A gate of the transistor 201 is electrically connected to a gate signal line 207, one of a source and a drain of the transistor 201 is electrically connected to a video data signal line 210, and the other of the source and the drain of the transistor 201 is electrically connected to one electrode of the storage capacitor 202 and one electrode of the liquid crystal element 203. The other electrode of the storage capacitor 202 and the
20 other electrode of the liquid crystal element 203 are each held at a certain potential. The liquid crystal element 203 is an element including a pair of electrodes and a liquid crystal layer interposed between the pair of electrodes.

[0050]

When a potential at a high level "H" is applied to the gate signal line 207, the
25 transistor 201 applies the potential of the video data signal line 210 to the storage capacitor 202 and the liquid crystal element 203. The storage capacitor 202 holds the applied potential. The liquid crystal element 203 changes light transmittance in accordance with the applied potential.

[0051]

30 Since the off-state currents of the transistors 201, 205, and 206 which are each a thin film transistor including an oxide semiconductor layer are extremely small, a

storage capacitor can be extremely small or is not necessarily provided.

[0052]

One electrode of the photodiode 204 is electrically connected to a photodiode reset signal line 208, and the other electrode of the photodiode 204 is electrically connected to a gate of the transistor 205. One of a source and a drain of the transistor 205 is electrically connected to a photosensor reference signal line 212, and the other of the source and the drain of the transistor 205 is electrically connected to one of a source and a drain of the transistor 206. A gate of the transistor 206 is electrically connected to a gate signal line 209, and the other of the source and the drain of the transistor 206 is electrically connected to a photosensor output signal line 211.

[0053]

Next, a configuration of the photosensor readout circuit 109 will be described with reference to FIG. 3. In FIG. 3, a photosensor readout circuit 300 of one column of the pixels includes a transistor 301 and a storage capacitor 302. In addition, the photosensor output signal line 211 of the column of pixels and a precharge signal line 303 are provided.

[0054]

Note that in the circuit configurations in this specification, a thin film transistors including an oxide semiconductor layer are each denoted by a symbol "OS" so that they can be identified as a thin film transistors including an oxide semiconductor layer. In FIG. 2, the transistor 201, the transistor 205, and the transistor 206 are each a thin film transistor including an oxide semiconductor layer. In FIG. 3, the transistor 301 is a thin film transistor including an oxide semiconductor layer.

[0055]

In the circuit 300, the potential of the photosensor output signal line 211 is set to a reference potential before operation of the photosensor in the pixel. The reference potential set for the photosensor output signal line 211 may be a high potential or a low potential. In FIG. 3, by setting a potential of the precharge signal line 303 at a high level "H", the potential of the photosensor output signal line 211 can be set to a high potential which is a reference potential. Note that the storage capacitor 302 is not necessarily provided in the case where the parasitic capacitance of the photosensor output signal line 211 is large.

[0056]

Next, readout operation of the photosensor in the display panel is described with reference to a timing chart of FIG. 4. In FIG. 4, a signal 401, a signal 402, a signal 403, and a signal 404 respectively correspond to the potential of the photodiode reset signal line 208, the potential of the gate signal line 209 to which the gate of the transistor 206 is connected, the potential of the gate signal line 213 to which the gate of the transistor 205 is connected, and the potential of the photosensor output signal line 211 in FIG. 2. In addition, a signal 405 corresponds to the potential of the precharge signal line 303 in FIG. 3.

[0057]

In a time A, when the potential of the photodiode reset signal line 208 (the signal 401) is set at the potential "H", in other words, the potential of the photodiode reset signal line which is electrically connected to the photodiode is set so that a forward bias is applied to the photodiode (reset operation), the photodiode 204 is brought into conduction and the potential of the gate signal line 213 (the signal 403) to which the gate of the transistor 205 is connected is set at the potential "H". In addition, when the potential of the precharge signal line 303 (the signal 405) is set at the potential "H", the potential of the photosensor output signal line 211 (the signal 404) is precharged to the potential "H".

[0058]

In a time B, when the potential of the photodiode reset signal line 208 (the signal 401) is set at the potential "L" (accumulating operation), the potential of the gate signal line 213 to which the gate of the transistor 205 is connected (the signal 403) begins to be lowered due to an off current of the photodiode 204. The off current of the photodiode 204 increases when light is delivered; therefore, the potential of the gate signal line 213 to which the gate of the transistor 205 is connected (the signal 403) varies depending on the amount of delivered light. That is, a current between the source and the drain of the transistor 205 varies.

[0059]

In a time C, when the potential of the gate signal line 209 (the signal 402) is set at the potential "H" (selecting operation), the transistor 206 is brought into conduction and the photosensor reference signal line 212 and the photosensor output signal line 211

are brought into conduction through the transistor 205 and the transistor 206. Then, the potential of the photosensor output signal line 211 (the signal 404) begins to be lowered. Note that before the time C, the potential of the precharge signal line 303 (the signal 405) is set at the potential "L" and precharge of the photosensor output signal
5 line 211 is completed. Here, the rate at which the potential of the photosensor output signal line 211 (the signal 404) is lowered depends on the current between the source and the drain of the transistor 205. That is, the potential of the photosensor output signal line 211 (the signal 404) varies in accordance with the amount of light which is delivered to the photodiode 204.
10 [0060]

In a time D, when the potential of the gate signal line 209 (the signal 402) is set at the potential "L", the transistor 206 is turned off, whereby the potential of the photosensor output signal line 211 (the signal 404) is kept at a fixed value after the time D. Here, the value to be the fixed value varies in accordance with the amount of light
15 which is delivered to the photodiode 204. Therefore, the amount of light which is delivered to the photodiode 204 can be found by obtaining the potential of the photosensor output signal line 211.

[0061]

Based on the amount of light emitted to the photodiode 204 as described above,
20 it can be determined whether ambient light is incident on the photodiode 204 or a contactless object prevents ambient light from being incident on the photodiode 204, that is, the portion where ambient light is blocked is a shadow.

[0062]

The results of circuit calculation of a frequency of image shooting in the
25 photosensor 106 of FIG. 2 are shown in FIG. 22. FIG. 22 shows a relationship between field-effect mobility of the transistor 205 and the transistor 206 which are included in the photosensor 106 and a frame frequency of image shooting which is calculated from a reading speed.

[0063]

30 The circuit calculation was performed with the following conditions assumed. In a touch panel, which has a 20-inch FHD standard (1920 horizontal RGB pixels and 1080 vertical pixels), each pixel is provided with a photosensor, the parasitic

capacitance of the photosensor output signal line 211 is 20 pF (corresponds to the capacitor 302), the transistor 205 and the transistor 206 each have a channel length of 5 μm and a channel width of 16 μm, and the transistor 301 has a channel length of 5 μm and a channel width of 1000 μm. Note that a circuit simulator, Smart Spice
5 (manufactured by Silvaco Data Systems Inc.), is used for the calculation.

[0064]

The circuit calculation was performed with the following operations assumed. First, an initial state is to be a state immediately after the accumulating operation. Specifically , the potential of the gate signal line 213 is set at 8 V, the potential of the
10 gate signal line 209 is set at 0 V, the potential of the photosensor output signal line 211 is set at 8 V, the potential of the photosensor reference signal line 212 is set at 8 V, and the potential of the precharge signal line 303 is set at 0 V. After the potential of the precharge signal line 303 and the potential of the photosensor output signal line 211 are changed to 8 V and 0 V (precharged state) respectively, the potential of the precharge
15 signal line 303 and the potential of the gate signal line 209 are changed to 0 V and 8 V, respectively. In other words, the selecting operation is started. Note that the reference voltage is set at 0 V. After that, a final state is to be the time when the potential of the photosensor output signal line 211 is changed to 2 V, that is, the potential is changed by 2 V from the potential at the precharge operation. The time
20 from the initial state to the final state in the operations described above is to be time for image shooting per one row.

[0065]

The time needed for image shooting is to be 1080 times as much as the above time for image shooting per one row, and the inverse of the time for image shooting is to
25 be a frequency of the image shooting. As an example, the frequency of image shooting of 60 Hz means that the above time for image shooting per one row corresponds to the following equation: 1/60 [Hz] / 1080 [columns] = 15.43 [μs].

[0066]

According to the results in FIG. 22, it is found that the frequency of image
30 shooting is 70 Hz to 100 Hz in the case where the field-effect mobility of each of the transistor 205 and the transistor 206 is set at 10 cm^2/Vs to 20 cm^2/Vs on the assumption

that a transistor including an oxide semiconductor is used. On the other hand, in the case where the field-effect mobility of each of the transistor 205 and the transistor 206 is set at 0.5 cm^2/Vs on the assumption that a transistor including amorphous silicon is used, the frequency of image shooting is only about 5 Hz. In other words, a transistor
5 which is included in a photosensor is effectively formed with a transistor including an oxide semiconductor.

[0067]

FIG. 5 illustrates a display panel system 590 which detects motion of a contactless object, using a shadow of the object. Here, the display panel system 590
10 includes a display panel 100, a control circuit 591, an image processing circuit 592, a memory device 593 which stores image data. The control circuit 591 generates various timing signals for driving the display panel. The image processing circuit 592 performs arithmetic processing on the image data of the shadow of the contactless object, which is obtained by a photosensor, and detects motion of the shadow of the
15 object. Furthermore, the image processing circuit 592 stores image data needed in the subsequent image processing in the memory device 593, and reads the data stored in the memory device 593 and performs arithmetic processing thereon if needed.

[0068]

An example of a specific method of image processing performed by the image
20 processing circuit 592 will be described with reference to FIG. 10. In FIG. 10, a display region including 12 × 12 pixels is illustrated.

[0069]

The image processing is performed as follows: (1) a position of an object is extracted from the image data of the shadow of the object; (2) motion of the object is
25 detected from positional data of the object which are successively captured; (3) generation of input data in response to the motion of the object is performed; and the like.

[0070]

As for (1) extraction of a position of an object from the image data of the
30 shadow of the object, the display region is divided into four areas: an area 2001, an area 2002, an area 2003, and an area 2004, for example, as frames are marked with thick lines in FIG. 10. In each area, a ratio of portions recognized as a shadow of the object

to the area is calculated. More specifically, when the amount of light obtained by the photosensor in each pixel is lower than a given threshold value, the pixel detects a shadow of the object. Note that a pixel not detecting a shadow is denoted by a reference numeral 2005 and a pixel detecting a shadow is denoted by a reference 5 numeral 2006.

[0071]

Then, an area in which a ratio of the pixels over which the shadow is cast to all of the pixels is the highest of the areas 2001 to 2004 is extracted as a position of the object. In FIG. 10, the pixels detecting the shadow are marked with diagonal lines. 10 The ratio of the pixels detecting the shadow in each area is as follows: in the area 2001, the ratio is 25/36; the area 2002, 12/36; the area 2003, 3/36; and the area 2004, 6/36. The ratio of the pixels over which the shadow is cast is the highest in the area 2001; therefore, the area 2001 is extracted as a position of the object and the positional data thereof is obtained.

15 [0072]

Note that the display region is divided into more areas, whereby the position can be extracted more precisely.

[0073]

Next, (2) detection of motion of the object from positional data of the object 20 which are successively captured will be described more specifically: the positional data are successively obtained as described above, and then the positional data is compared with the positional data captured before and after the positional data is captured, whereby the motion of the object can be known. For example, when the last positional data is the right and the positional data of this time is the left, the object can be detected 25 to move from right to left. Moreover, in the case where the positional data is extracted more precisely, the more precise motion such as the motion speed in addition to the direction in which the object moves can be detected.

[0074]

As for (3) generation of input data in response to the motion of the object, it is 30 effective to preliminarily set the input data in flexible response to the motion of the object depending on the usage of the display panel. For example, the following application is possible: given that an object is a finger, when the finger moves from left

to right, a moving image is reproduced and when the finger moves from top to bottom, a moving image is stopped. Moreover, it is also effective to suppose a letter from an elaborate motion of a finger to determine it as input data.

[0075]

It is also effective that the sensitivity of the photosensor with respect to the amount of light is variable. In a structure in FIG. 2, for example, the potential applied to the photosensor (the potential of the photodiode reset signal line 208, the potential of the gate signal line 209, the potential of the photosensor reference signal line 212, or the potential of the precharge signal line 303) varies, so that the sensitivity to the amount of light is variable. Thus, when the sensitivity of the photosensor with respect to the amount of light is variable, the sensitivity can be set at an optimal value as appropriate depending on the environment (the brightness or the like) where the display panel is used and a shadow of a contactless object can easily be recognized. Moreover, the display panel can be used not only for detecting a shadow of a contactless object but also as a contact area sensor. That is to say, a function of detecting a contactless object and a function of detecting a touch object can be used as appropriate depending on the usage.

[0076]

With the above structure, a display panel capable of detecting even a contactless object and inputting data can be provided.

[0077]

Furthermore, the above image processing can be applied to the case of detecting light reflected by an object in addition to the case of detecting a shadow of the object. In the case of detecting reflection light, photosensors placed at a position toward which an object moves receive stronger light than those at the other positions. That is, an area, in the display region, which receives stronger light, is specified using the above image processing, whereby the position, the motion, or the shape of the object can be detected. In this case, the pixels which are marked with diagonal lines in FIG. 10 receive stronger light reflected by the object.

[0078]

Additionally, it is effective that a first photosensor which detects a contactless object and a second photosensor which detects a touch object are provided in the

display panel. The second photosensor is used as the contact area sensor. With such a structure, a display panel capable of detecting a contactless object and capable of detecting also a touch object can be provided. That is, two types of detection functions can be used as appropriate depending on the usage of the display panel.

5 [0079]

Pixels each including the first photosensor and pixels each including the second photosensor are arranged in matrix on the display panel. It is desirable that the number of second photosensors is larger than the number of first photosensors. The second photosensor serving as a contact area sensor is required to shoot a high resolution
10 image; therefore, a distance (pitch) between the second photosensors is short, whereby the resolution can be high. On the other hand, the first photosensor detecting a shadow only need to determine the position of the object; therefore, the first photosensor is not required to have as high resolution as the second photosensor used as a contact area sensor. That is, the distance between the arranged second photosensors may be shorter
15 than the distance between the arranged first photosensors.

[0080]

Note that pixels in each of which the first photosensor detecting a shadow is provided are pixels in each of which the second photosensor used as a contact area sensor is not provided. Therefore, photosensors serving as contact area sensors are
20 desirably provided in about one to three pixels around photosensor detecting a shadow so that a lost image in the pixels can be restored by image processing.

[0081]

FIG. 11A illustrates an example of pixels where the first photosensors detecting a shadow and the second photosensors used as a contact area sensor are arranged. In
25 FIGS. 11A and 11B, 12 × 12 pixels are used; however, the number of pixels is not limited to this.

[0082]

In FIG. 11A, the first photosensors are provided in pixels marked with diagonal lines, and the second photosensors are provided in the other pixels. The first
30 photosensors are arranged at intervals. For the above reason, the number of second photosensors is larger than that of first photosensors.

[0083]

Note that the first photosensors are not necessarily arranged at regular intervals as illustrated in FIG. 11A, and may be arranged at irregular intervals as illustrated in FIG. 11B. In the case where 640 × 480 pixels are used as a more practical example, when the pixels are divided into areas including hundred pixels of 10 × 10 pixels, a pixel of
5 the hundred pixels is provided with the first photosensor and the ninety-nine pixels are provided with the second photosensors, which is effective enough for the device to detect a shadow of the object and to serve as a contact area sensor. However, the structure is not limited to this. The ratio of the first photosensors to the second photosensors may be determined in accordance with the detection accuracy. The
10 number of the first photosensors and the number of the second photosensors can be equal to each other, for example.

[0084]

Note that, in the photosensor detecting a shadow and the photosensor used as a contact area sensor, it is effective to individually set a potential to be applied to each of
15 the photosensors (e.g., the potential of the photodiode reset signal line 208, the potential of the gate signal line 209, the potential of the photosensor reference signal line 212, or the potential of the precharge signal line 303 in FIG. 2 or FIG. 3). Moreover, it is effective that the sizes of photodiodes included in the photosensors or the circuit configurations of the photosensors vary from one photosensor to another.

20 [0085]

This embodiment can be implemented in appropriate combination with any of the other embodiments and examples.

[0086]

(Embodiment 2)

25 In this embodiment, a method for increasing detection accuracy of a photosensor in the case of using light reflected by an object will be described.

[0087]

For detection of a contactless object, slight light reflected by the object needs to be effectively detected. Specifically, the following method is given.

30 [0088]

A structure is employed in which a sensor which detects infrared light (an

infrared light sensor) is used as a photosensor and the infrared light sensor detects infrared light emitted from a touch panel and reflected by an object. The infrared light sensor can be formed, for example, by being provided with a stack of color filters of different colors (e.g., R (red) and B (blue), or R (red) and G (green)) on a photosensor
5 so that light (infrared light) other than visible light can be incident on the photosensor. By using color filters provided on a display panel for color display also as filters of the infrared light sensor, the number of steps can be reduced. Moreover, for example, a light source emitting infrared light in addition to visible light (white) is added to a backlight, whereby the touch panel can emit infrared light. As for infrared light, the
10 wavelength is longer and the amount of scattering is smaller than visible light; therefore, the detection accuracy can be easily increased. The structure of detecting infrared light is effective, particularly in the case where the object is a finger or a hand.

[0089]

When an infrared light sensor and a visible light sensor are formed using
15 different materials, the infrared light sensor may be formed using a material which absorbs light (infrared light) other than visible light. For example, a photosensor formed using InGaAs, PbS, PbSe, or the like absorbs infrared light efficiently.

[0090]

In the structure described in Embodiment 1 where the first photosensor
20 detecting a contactless object and the second photosensor detecting a touch object are provided in the display panel, an infrared light sensor is used for the first photosensor and a visible light sensor is used for the second photosensor. Accordingly, the accuracy of both a function of detecting a contactless object and a function as a contact area sensor can be improved. The first photosensors (the infrared light sensors) and
25 the second photosensors (the visible light sensors) can be arranged in a manner similar to that of Embodiment 1.

[0091]

Moreover, the image processing described in Embodiment 1 can be adopted.

[0092]

30 This embodiment can be implemented in appropriate combination with any of the other embodiments and examples.

[0093]

(Embodiment 3)

In this embodiment, a structure of a display device according to an embodiment of the present invention will be described with reference to FIG. 6.

[0094]

5 FIG. 6 illustrates an example of a cross-sectional view of the display device. In the display device illustrated in FIG. 6, a photodiode 502, a transistor 540, a transistor 503, and a liquid crystal element 505 are formed over a substrate 501 having an insulating surface (a TFT substrate).

[0095]

10 An oxide insulating layer 531, a protective insulating layer 532, an interlayer insulating layer 533, and an interlayer insulating layer 534 are provided over the transistor 503 and the transistor 540. The photodiode 502 is provided over the interlayer insulating layer 533. In the photodiode 502, a first semiconductor layer 506a, a second semiconductor layer 506b, and a third semiconductor layer 506c are 15 sacked in that order over the interlayer insulating layer 533 between an electrode layer 541 formed over the interlayer insulating layer 533 and an electrode layer 542 formed over the interlayer insulating layer 534.

[0096]

The electrode layer 541 is electrically connected to a conductive layer 543 20 which is formed in the interlayer insulating layer 534, and the electrode layer 542 is electrically connected to a gate electrode layer 545 through the electrode layer 541. The gate electrode layer 545 is electrically connected to a gate electrode layer of the transistor 540, and the photodiode 502 is electrically connected to the transistor 540. The transistor 540 corresponds to the transistor 205 in Embodiment 1.

25 [0097]

In order to prevent variation in electric characteristics of the transistor 503 and the transistor 540 each formed using an oxide semiconductor layer, which are included in a touch panel including a photosensor, impurities such as hydrogen, moisture, hydroxyl group, or a hydride (also referred to as a hydrogen compound) which cause the 30 variation are intentionally removed from the oxide semiconductor layer. Additionally, the oxide semiconductor layer is highly purified to become i-type (intrinsic) by supplying oxygen which is a major component of the oxide semiconductor layer, which

is simultaneously reduced in a step of removing impurities.

[0098]

Therefore, it is preferable that the oxide semiconductor layer contains hydrogen and carriers as little as possible. In the transistor 503 and the transistor 540, a channel formation region is formed in the oxide semiconductor layer, in which hydrogen contained therein is removed as much as possible to be close to 0 so that the hydrogen concentration is less than or equal to 5×10^{19} /cm^3, preferably, less than or equal to 5×10^{18} /cm^3, more preferably, less than or equal to 5×10^{17} /cm^3 or less than 5×10^{16} /cm^3, and the carrier concentration is less than 5×10^{14} /cm^3, preferably, less than or equal to 5×10^{12} /cm^3.

[0099]

It is preferable that an off-state current be as small as possible in reverse characteristics of the transistor 503 and the transistor 540. An off-state current is a current that flows between a source and a drain of a thin film transistor in the case where a gate voltage between –1 V to –10 V is applied. A current value per 1 μm in a channel width (w) of a thin film transistor formed using an oxide semiconductor, which is disclosed in this specification, is less than or equal to 100 aA/μm, preferably, less than or equal to 10 aA/μm, more preferably, less than or equal to 1 aA/μm. Further, since there is no pn junction and no hot carrier degradation, electric characteristics of the thin film transistor is not adversely affected.

[0100]

FIG. 18 is a longitudinal cross-sectional view of an inverted staggered thin film transistor formed using an oxide semiconductor. An oxide semiconductor layer (OS) is provided over a gate electrode (GE1) with a gate insulating film (GI) interposed therebetween, and a source electrode (S) and a drain electrode (D) are provided thereover.

[0101]

FIGS. 19A and 19B are energy band diagrams (schematic diagrams) of a cross section along A-A′ in FIG. 18. FIG. 19A illustrates the case where the potential applied to the source is equal to the potential applied to the drain (V_D = 0 V), and FIG. 19B illustrates the case where a positive potential with respect to the source is applied to the

drain ($V_D > 0$ V).

[0102]

FIGS. 20A and 20B are energy band diagrams (schematic diagrams) of a cross section along B-B′ in FIG. 18. FIG. 20A illustrates an on state in which a positive
5 potential ($+V_G$) is applied to a gate electrode (GE1) and carriers (electrons) flow between the source and the drain. FIG. 20B illustrates an off state in which a negative potential ($-V_G$) is applied to the gate (GE1) and minority carriers do not flow.

[0103]

FIG. 21 illustrates the relationships between the vacuum level and the work
10 function of a metal (ϕM) and between the vacuum level and the electron affinity (χ) of an oxide semiconductor.

[0104]

A conventional oxide semiconductor is typically an n-type semiconductor, and the Fermi level (E_F) is away from the intrinsic Fermi level (Ei) located in the middle of
15 a band gap and is located closer to the conduction band. Note that since hydrogen can serve as a donor, hydrogen is known as a factor to make the oxide semiconductor layer n-type.

[0105]

On the other hand, an oxide semiconductor according to the present invention
20 is an intrinsic (i-type) or a substantially intrinsic oxide semiconductor which is obtained by removing hydrogen that is an n-type impurity from an oxide semiconductor and highly purifying the oxide semiconductor such that an impurity is prevented from being contained therein as much as possible. In other words, a feature is that a highly purified i-type (intrinsic) semiconductor or a semiconductor close thereto is obtained by
25 removing an impurity such as hydrogen or water as much as possible. This enables the Fermi level (E_F) to be at the same level as the intrinsic Fermi level (Ei).

[0106]

The electron affinity (χ) of an oxide semiconductor is said to be 4.3 eV. The work function of titanium (Ti) included in the source electrode and the drain electrode is
30 substantially equal to the electron affinity (χ) of the oxide semiconductor. In that case, a Schottky barrier to electrons is not formed at an interface between the metal and the

oxide semiconductor.

[0107]

In other words, in the case where the work function of the metal (ϕM) and the electron affinity (χ) of the oxide semiconductor are equal to each other and the metal
5 and the oxide semiconductor are in contact with each other, an energy band diagram (a schematic diagram) as illustrated in FIG. 19A is obtained.

[0108]

In FIG. 19B, a black circle (•) represents an electron, and when a positive potential is applied to the drain, the electron is injected into the oxide semiconductor
10 layer over the barrier (h) and flows toward the drain. In that case, the height of the barrier (h) changes depends on the gate voltage and the drain voltage; in the case where a positive drain voltage is applied, the height of the barrier (h) is smaller than the height of the barrier in FIG. 19A where no voltage is applied, i.e., 1/2 of the band gap (Eg).

[0109]

15 At this time, the electron injected into the oxide semiconductor layer flows through the oxide semiconductor layer as illustrated in FIG. 20A. In addition, in FIG. 20B, when a negative potential is applied to the gate electrode (GE1), the value of current is as close to zero as possible because holes that are minority carriers do not substantially exist.

20 [0110]

For example, even a thin film transistor has a channel width W of 1×10^4 μm and a channel length of 3 μm, an off-state current is less than or equal to 10^{-13} A and a subthreshold swing (S value) is 0.1 V/dec. (the thickness of the gate insulating film: 100 nm).

25 [0111]

In this manner, when the oxide semiconductor layer is highly purified so that impurities are contained as little as possible, the operation of the thin film transistor can be favorable.

[0112]

30 Therefore, the above transistors 503 and 540 formed using the oxide semiconductor layer are thin film transistors having stable electric characteristics and

high reliability.

[0113]

As the oxide semiconductor layer included in each of the transistor 503 and the transistor 540, any of a four-component metal oxide such as an In-Sn-Ga-Zn-O film, a three-component metal oxide such as an In-Ga-Zn-O film, an In-Sn-Zn-O film, an In-Al-Zn-O film, a Sn-Ga-Zn-O film, an Al-Ga-Zn-O film, and a Sn-Al-Zn-O film, or a two-component metal oxide such as an In-Zn-O film, a Sn-Zn-O film, an Al-Zn-O film, a Zn-Mg-O film, a Sn-Mg-O film, an In-Mg-O film, an In-O film, a Sn-O film, and a Zn-O film can be used. Further, SiO_2 may be contained in the above oxide semiconductor layer.

[0114]

Note that as the oxide semiconductor layer, a thin film expressed by $InMO_3(ZnO)_m$ ($m > 0$) can be used. Here, M represents one or more metal elements selected from Ga, Al, Mn, and Co. For example, M can be Ga, Ga and Al, Ga and Mn, Ga and Co, or the like. An oxide semiconductor layer whose composition formula is represented by $InMO_3(ZnO)_m$ ($m > 0$), which includes Ga as M, is referred to as the In-Ga-Zn-O oxide semiconductor described above, and a thin film of the In-Ga-Zn-O oxide semiconductor is also referred to as an In-Ga-Zn-O-based non-single-crystal film.

[0115]

Here, a pin photodiode in which a semiconductor layer having p-type conductivity as the first semiconductor layer 506a, a high-resistance semiconductor layer (i-type semiconductor layer) as the second semiconductor layer 506b, and a semiconductor layer having n-type conductivity as the third semiconductor layer 506c are stacked is illustrated as an example.

[0116]

The first semiconductor layer 506a is a p-type semiconductor layer and can be formed using an amorphous silicon film containing an impurity element imparting p-type conductivity. The first semiconductor layer 506a is formed with a plasma CVD method with the use of a semiconductor source gas containing an impurity element belonging to Group 13 (such as boron (B)). As the semiconductor material gas, silane (SiH_4) may be used. Alternatively, Si_2H_6, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, SiF_4, or the like may be used. Further alternatively, an amorphous silicon film which does not contain an

impurity element may be formed, and then, an impurity element may be introduced to the amorphous silicon film with the use of a diffusion method or an ion injecting method. Heating or the like may be performed after introducing the impurity element with an ion injecting method or the like in order to diffuse the impurity element. In 5 this case, as a method of forming the amorphous silicon film, an LPCVD method, a chemical vapor deposition method, a sputtering method, or the like may be used. The first semiconductor layer 506a is preferably formed to have a thickness of greater than or equal to 10 nm and less than or equal to 50 nm.

[0117]

10 The second semiconductor layer 506b is an i-type semiconductor layer (intrinsic semiconductor layer) and is formed with an amorphous silicon film. As for formation of the second semiconductor layer 506b, an amorphous silicon film is formed with a plasma CVD method using a semiconductor material gas. As the semiconductor material gas, silane (SiH_4) may be used. Alternatively, Si_2H_6, SiH_2Cl_2, 15 $SiHCl_3$, $SiCl_4$, SiF_4, or the like may be used. The second semiconductor layer 506b may be alternatively formed with an LPCVD method, a chemical vapor deposition method, a sputtering method, or the like. The second semiconductor layer 506b is preferably formed to have a thickness of greater than or equal to 200 nm and less than or equal to 1000 nm.

20 [0118]

The third semiconductor layer 506c is an n-type semiconductor layer and is formed with an amorphous silicon film containing an impurity element imparting n-type conductivity. The third semiconductor layer 506c is formed with a plasma CVD method using a semiconductor material gas containing an impurity element belonging to 25 Group 15 (such as phosphorus (P)). As the semiconductor material gas, silane (SiH_4) may be used. Alternatively, Si_2H_6, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, SiF_4, or the like may be used. Further alternatively, an amorphous silicon film which does not contain an impurity element may be formed, and then, an impurity element may be introduced to the amorphous silicon film with the use of a diffusion method or an ion injecting 30 method. Heating or the like may be performed after the impurity element is introduced with an ion injecting method or the like in order to diffuse the impurity element. In this case, as a method of forming the amorphous silicon film, an LPCVD method, a

chemical vapor deposition method, a sputtering method, or the like may be used. The third semiconductor layer 506c is preferably formed to have a thickness of greater than or equal to 20 nm and less than or equal to 200 nm.

[0119]

5 The first semiconductor layer 506a, the second semiconductor layer 506b, and the third semiconductor layer 506c are not necessarily formed using an amorphous semiconductor, and they may be formed using a polycrystalline semiconductor or a microcrystalline semiconductor (a semi-amorphous semiconductor (SAS)).

[0120]

10 The microcrystalline semiconductor belongs to a metastable state of an intermediate between amorphous and single crystalline when Gibbs free energy is considered. That is, the microcrystalline semiconductor film is a semiconductor having a third state which is thermodynamically stable and has a short range order and lattice distortion. Columnar-like or needle-like crystals grow in a normal direction 15 with respect to a substrate surface. The Raman spectrum of microcrystalline silicon, which is a typical example of a microcrystalline semiconductor, is shifted to a small wavenumber region below 520 cm^{-1} which represents single-crystalline silicon. That is, the peak of the Raman spectrum of the microcrystalline silicon exists between 520 cm^{-1} which represents single crystal silicon and 480 cm^{-1} which represents amorphous 20 silicon. In addition, microcrystalline silicon contains hydrogen or halogen of at least 1 atomic% or more in order to terminate a dangling bond. Moreover, microcrystalline silicon may contain a rare gas element such as helium, argon, krypton, or neon to further promote lattice distortion, so that a microcrystalline semiconductor film with high thermodynamic stability can be obtained.

25 [0121]

The microcrystalline semiconductor film can be formed with a high-frequency plasma CVD method with a frequency of several tens of MHz to several hundreds of MHz or with a microwave plasma CVD method with a frequency of greater than or equal to 1 GHz. Typically, the microcrystalline semiconductor film can be formed 30 using a silicon hydride such as SiH_4, Si_2H_6, SiH_2Cl_2 or $SiHCl_3$, or a silicon halide such as $SiCl_4$ or SiF_4, which is diluted with hydrogen. With a dilution with one or a plural kinds of rare gas elements selected from helium, argon, krypton, or neon in addition to

silicon hydride and hydrogen, the microcrystalline semiconductor film can be formed. In that case, the flow ratio of hydrogen to the silicon hydride is 5:1 to 200:1, preferably, 50:1 to 150:1, more preferably, 100:1. Further, a hydrocarbon gas such as CH_4 or C_2H_6, a germanium gas such as GeH_4 or GeF_4, F_2, or the like may be mixed into the gas
5 containing silicon.

[0122]

In addition, since the mobility of holes generated by the photoelectric effect is lower than that of electrons, a pin photodiode has better characteristics when a surface on the p-type semiconductor layer side is used as a light-receiving plane. Here, an
10 example where light received by the photodiode 502 from a surface of the substrate 501, over which a pin photodiode is formed, is converted into electric signals will be described. Further, light from the semiconductor layer having a conductivity type opposite to that of the semiconductor layer on the light-receiving plane is disturbance light; therefore, the electrode layer is preferably formed using a light-blocking
15 conductive film. Note that a surface on the n-type semiconductor layer side can alternatively be used as the light-receiving plane.

[0123]

The liquid crystal element 505 includes a pixel electrode 507, liquid crystal 508, a counter electrode 509, an alignment film 511, and an alignment film 512. The pixel
20 electrode 507 is formed over the substrate 501, and the alignment film 511 is formed over the pixel electrode 507. The pixel electrode 507 is electrically connected to the transistor 503 through a conductive film 510. A substrate 513 (a counter substrate) is provided with the counter electrode 509, the alignment film 512 is formed on the counter electrode 509, and the liquid crystal 508 is interposed between the alignment
25 film 511 and the alignment film 512. The transistor 503 corresponds to the transistor 201 in Embodiment 1.

[0124]

A cell gap between the pixel electrode 507 and the counter electrode 509 can be controlled by using a spacer 516. In FIG. 6, the cell gap is controlled by using the
30 columnar spacer 516 selectively formed by photolithography. Alternatively, the cell gap can be controlled by dispersing spherical spacers between the pixel electrode 507 and the counter electrode 509.

[0125]

The liquid crystal 508 is surrounded by a sealing material between the substrate 501 and the substrate 513. The liquid crystal 508 may be injected with a dispenser method (droplet method) or a dipping method (pumping method).

5 [0126]

For the pixel electrode 507, a light-transmitting conductive material such as indium tin oxide (ITO), indium tin oxide containing silicon oxide (ITSO), organic indium, organic tin, indium zinc oxide (IZO) containing zinc oxide (ZnO), zinc oxide (ZnO), zinc oxide containing gallium (Ga), tin oxide (SnO_2), indium oxide containing
10 tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, or the like can be used. A conductive composition containing a conductive macromolecule (also referred to as a conductive polymer) can be used to form the pixel electrode 507. As the conductive macromolecule, a so-called π-electron conjugated conductive polymer can be used.
15 For example, polyaniline or a derivative thereof, polypyrrole or a derivative thereof, polythiophene or a derivative thereof, a copolymer of two or more kinds of them, and the like can be given.

[0127]

Since the transparent liquid crystal element 505 is given as an example in this
20 embodiment, the light-transmitting conductive material described above can be used also for the counter electrode 509 as in the case of the pixel electrode 507.

[0128]

An alignment film 511 is provided between the pixel electrode 507 and the liquid crystal 508, and an alignment film 512 is provided between the counter electrode
25 509 and the liquid crystal 508. The alignment film 511 and the alignment film 512 can be formed using an organic resin such as a polyimide or poly(vinyl alcohol). Alignment treatment such as rubbing is performed on their surfaces in order to align liquid crystal molecules in certain direction. Rubbing can be performed by rolling a roller wrapped with cloth of nylon or the like while applying pressure on the alignment
30 film so that the surface of the alignment film is rubbed in certain direction. Note that by using an inorganic material such as silicon oxide, the alignment film 511 and the alignment film 512 each having an alignment property can be directly formed with an

evaporation method without performing an alignment treatment.

[0129]

Further, a color filter 514 through which light in a particular wavelength range can pass is formed over the substrate 513 so as to overlap with the liquid crystal element 505. The color filter 514 can be selectively formed by photolithography after application of an organic resin such as an acrylic-based resin in which colorant is dispersed on the substrate 513. Alternatively, the color filter 514 can be selectively formed by etching after application of a polyimide-based resin in which colorant is dispersed on the substrate 513. Alternatively, the color filter 514 can be selectively formed with a droplet discharge method such as an ink-jet method.

[0130]

Furthermore, a shielding film 515 which can block light is formed over the substrate 513 so as to overlap with the photodiode 502. By providing the shielding film 515, light from a backlight that passes through the substrate 513 and enters the touch panel can be prevented from being directly delivered to the photodiode 502. Further, disclination due to disorder of alignment of the liquid crystal 508 among pixels can be prevented from being viewed. An organic resin containing black colorant such as carbon black or a low-valent titanium oxide can be used for the shielding film 515. Alternatively, a film formed using chromium can be used for the shielding film 515.

[0131]

Furthermore, a polarizing plate 517 is provided on a surface which is the opposite side of a surface of the substrate 501 over which the pixel electrode 507 is formed, and a polarizing plate 518 is provided on a surface which is the opposite side of a surface of the substrate 513 on which the counter electrode 509 is formed.

[0132]

With the use of an insulating material, the oxide insulating layer 531, the protective insulating layer 532, the interlayer insulating layer 533, and the interlayer insulating layer 534 can be formed, depending on the material, with a method such as a sputtering method, an SOG method, spin coating, dip coating, spray coating, or a droplet discharge method (e.g., an ink-jet method, screen printing, offset printing, or the like), or a tool (equipment) such as a doctor knife, a roll coater, a curtain coater, or a knife coater.

[0133]

As the oxide insulating layer 531, a single layer or a stacked layer of an oxide insulating layer such as a silicon oxide layer, a silicon oxynitride layer, an aluminum oxide layer, an aluminum oxynitride layer, or the like can be used.

5 [0134]

As an inorganic insulating material of the protective insulating layer 532, a single layer or a stacked layer of a nitride insulating layer such as a silicon nitride layer, a silicon nitride oxide layer, an aluminum nitride layer, an aluminum nitride oxide layer, or the like can be used. High-density plasma CVD with the use of microwaves (2.45

10 GHz) is preferably employed because formation of a dense and high-quality insulating layer having high withstand voltage is possible.

[0135]

For reduction of the surface roughness, an insulating layer functioning as a planarization insulating film is preferably used as the interlayer insulating layers 533

15 and 534. The interlayer insulating layers 533 and 534 can be formed using an organic insulating material having heat resistance such as a polyimide, an acrylic resin, a benzocyclobutene-based resin, a polyamide, or an epoxy resin. Other than such organic insulating materials, it is possible to use a single layer or stacked layers of a low-dielectric constant material (a low-k material), a siloxane-based resin,

20 phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), or the like.

[0136]

The liquid crystal element may be a TN (twisted nematic) mode liquid crystal element, a VA (vertical alignment) mode liquid crystal element, an OCB (optically compensated birefringence) mode liquid crystal element, an IPS (in-plane switching)

25 mode liquid crystal element, or the like. Alternatively, liquid crystal exhibiting a blue phase for which an alignment film is unnecessary may be used. The blue phase is one of liquid crystal phases and a phase which appears just before the transition from a cholesteric phase to an isotropic phase when the temperature of cholesteric liquid crystal is increased. A blue phase appears only within a narrow temperature range; therefore,

30 the liquid crystal 508 is formed using a liquid crystal composition containing a chiral agent at 5 wt.% or more in order to expand the temperature range. The liquid crystal composition including liquid crystal exhibiting a blue phase and a chiral agent has a

short response time of 1 millisecond or less and are optically isotropic; therefore, alignment treatment is unnecessary, and viewing angle dependence is small. In addition, since an alignment film does not need to be provided and rubbing treatment is unnecessary, electrostatic discharge damage caused by the rubbing treatment can be
5 prevented and defects and damage of the touch panel can be reduced in the manufacturing process. Thus, productivity of the touch panel can be increased.

[0137]

Note that although the liquid crystal element 505 in which the liquid crystal 508 is interposed between the pixel electrode 507 and the counter electrode 509 is
10 described as an example in this embodiment, the touch panel according to an embodiment of the present invention is not limited to this structure. A liquid crystal element in which a pair of electrodes is formed on the substrate 501 side like an IPS mode liquid crystal element may also be employed.

[0138]

15 Light from the backlight passes through the substrate 513 and the liquid crystal element 505 and is delivered to an object 521 on the substrate 501 side as shown by an arrow 520. Then, light reflected by the object 521 enters the photodiode 502 as shown by an arrow 522.

[0139]

20 When ambient light is detected, the display device receives ambient light from the substrate (TFT substrate) 501 side. The ambient light is blocked by the object 521 and thus, light to be incident on the photodiode 502 is blocked. That is, the photodiode 502 is to detect a shadow of the object.

[0140]

25 With the above structure, a display panel where data can be inputted by detection of motion of a contactless object can be provided.

[0141]

In addition, the display device of this embodiment can also detect an object even when the object is close to the display panel. The distance can be set to three
30 centimeters or shorter. The display device of this embodiment is more effective than a device provided with a CCD image sensor or the like.

[0142]

Further, in the display device of this embodiment, a light receiving surface of the photosensor (the photodiode 502) and a display surface of the display panel (on the substrate 501 side) face in the same direction. Therefore, an image of the object can be shot in the display panel. The display device of this embodiment is more effective
5 than a device provided with a CCD image sensor or the like.

[0143]

This embodiment can be implemented in appropriate combination with any of the other embodiments and examples.

[0144]

10 (Embodiment 4)

In this embodiment, another structure of a display panel according to an embodiment of the present invention will be described with reference to FIG. 7.

[0145]

FIG. 7 illustrates an example of a cross-sectional view of a display panel which
15 is different from that in Embodiment 3. The display panel illustrated in FIG. 7 shows an example where electric signals are obtained by converting light which enters the photodiode 502 through the counter substrate 513 opposed to the substrate 501, over which a pin photodiode is formed, after being reflected on the object 521 to be detected.

[0146]

20 Light from the backlight passes through the substrate 501 and the liquid crystal element 505 and is delivered to the object 521 on the substrate 513 side as shown by an arrow 560. Then, light reflected by the object 521 enters the photodiode 502 as shown by an arrow 562. Note that in this structure, the shielding film 515 is not provided in a region where the light shown by the arrow 562 passes therethrough. For example, an
25 opening may be formed in the shielding film 515 above the photodiode 502 so that light reflected by the object 521 can enter the photodiode 502.

[0147]

Since the field-effect mobility of holes generated by the photoelectric effect is lower than that of electrons, a pin photodiode has better characteristics when a surface
30 on the p-type semiconductor layer side is used as a light-receiving plane. Here, light which the photodiode 502 receives through the counter substrate 513 is converted into electric signals. Further, light from the semiconductor layer having a conductivity type

opposite to that of the semiconductor layer on the light-receiving plane is disturbance light; therefore, the electrode layer 541 is preferably formed using a light-blocking conductive film. Note that a surface on the n-type semiconductor layer side can alternatively be used as the light-receiving plane.

5 [0148]

Therefore, in the photodiode 502 of this embodiment, the third semiconductor layer 506c having n-type conductivity, the second semiconductor layer 506b which is a high-resistance semiconductor layer (i-type semiconductor layer), a first semiconductor layer 506a having p-type conductivity, and an electrode layer 542 are stacked in that 10 order over an electrode layer 541 connected to the gate electrode layer 545.

[0149]

A shielding film may be provided below the photodiode 502. The shielding film can prevent the light, from the backlight, which passes through the substrate (TFT substrate) 501 and enters the display panel from reaching the photodiode 502 directly; 15 thus, a display panel where a high resolution image can be shot can be provided. The shielding film can be formed using an organic resin containing a black pigment such as a carbon black or titanium lower oxide. Alternatively, a film of chromium can be used for the shielding film.

[0150]

20 When infrared light is detected using the photodiode 502, the color filter 514 which transmits infrared light may be provided over the photodiode 502. In that case, the color filter preferably has a stack of color filters of different colors.

[0151]

Moreover, when ambient light is detected, the display panel receives ambient 25 light from the substrate (counter substrate) 513 side. The ambient light is blocked by the object 521 and thus, light to be incident on the photodiode 502 is blocked. That is, the photodiode 502 is to detect a shadow of the object.

[0152]

The distance between the object and the display panel, and the directions of the 30 light receiving surface of the photosensor and the display surface of the display panel are similar to those in Embodiment 3. The light receiving surface of the photosensor faces in the same direction as the display surface of the display panel (toward the

counter substrate 513); thus, an image of the object can be shot in the display panel.

[0153]

This embodiment can be implemented in appropriate combination with any of the other embodiments and examples.

5 [0154]

(Embodiment 5)

In this embodiment, an example of a thin film transistor which can be applied to the display panel disclosed in this specification will be described. A thin film transistor 390 in this embodiment can be used as the thin film transistor formed using an

10 oxide semiconductor layer including a channel formation region in any of the above embodiments (e.g., the transistors 201, 205, 206, and 301 in Embodiment 1, and the transistors 503 and 540 in Embodiments 3 and 4). The same portions as those in the above embodiments and portions having functions similar to those of the portions in the above embodiments and steps similar to those in the above embodiments may be

15 handled as in the above embodiments, and repeated description is omitted. In addition, detailed description of the same portions is also omitted.

[0155]

An embodiment of a manufacturing method of the thin film transistor of this embodiment is described with reference to FIGS. 12A to 12E.

20 [0156]

FIGS. 12A to 12E illustrate an example of a cross-sectional structure of a thin film transistor. The thin film transistor 390 illustrated in FIGS. 12A to 12E is one of bottom gate thin film transistors and is also referred to as an inverted staggered thin film transistor.

25 [0157]

Although description is given using a single-gate thin film transistor as the thin film transistor 390, a multi-gate thin film transistor including a plurality of channel formation regions may be formed as needed.

[0158]

30 A process of manufacturing the thin film transistor 390 over a substrate 394 is described below with reference to FIGS. 12A to 12E.

[0159]

First, after a conductive film is formed over the substrate 394 having an insulating surface, a gate electrode layer 391 is formed in a first photolithography process. The gate electrode layer preferably has a tapered shape because coverage with a gate insulating layer stacked thereover can be improved. Note that a resist mask
5 may be formed by an ink-jet method. When the resist mask is formed by an ink-jet method, a photomask is not used; therefore, manufacturing costs can be reduced.

[0160]

There is no particular limitation on a substrate that can be used as the substrate 394 having an insulating surface as long as it has at least heat resistance to withstand
10 heat treatment performed later. A glass substrate formed using barium borosilicate glass, aluminoborosilicate glass, or the like can be used.

[0161]

When the temperature of the heat treatment performed later is high, a substrate having a strain point of 730 °C or higher is preferably used as the glass substrate. As a
15 material of the glass substrate, a glass material such as aluminosilicate glass, aluminoborosilicate glass, or barium borosilicate glass is used, for example. By containing a larger amount of barium oxide (BaO) than boron oxide, a glass substrate is heat-resistant and of more practical use. Therefore, a glass substrate containing a larger amount of BaO than B_2O_3 is preferably used.

20 [0162]

Note that, instead of the glass substrate described above, a substrate formed using an insulator such as a ceramic substrate, a quartz substrate, or a sapphire substrate may be used as the substrate 394. Alternatively, a crystallized glass substrate or the like may be used. Still alternatively, a plastic substrate or the like can be used as
25 appropriate.

[0163]

An insulating film serving as a base film may be provided between the substrate 394 and the gate electrode layer 391. The base film has a function of preventing diffusion of an impurity element from the substrate 394, and can be formed
30 with a single-layer structure or a layered structure using any of a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, and a silicon oxynitride film.

[0164]

The gate electrode layer 391 can be formed with a single-layer structure or a layered structure using any of metal materials such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, and scandium, and an alloy material including any of these materials as a main component.

5 [0165]

As a two-layer structure of the gate electrode layer 391, for example, a two-layer structure in which a molybdenum layer is stacked over an aluminum layer, a two-layer structure in which a molybdenum layer is stacked over a copper layer, a two-layer structure in which a titanium nitride layer or a tantalum nitride layer is 10 stacked over a copper layer, a two-layer structure in which a titanium nitride layer and a molybdenum layer are stacked, or a two-layer structure in which a tungsten nitride layer and a tungsten layer are stacked is preferable. As a three-layer structure, a stack of a tungsten layer or a tungsten nitride layer, an alloy layer of aluminum and silicon or an alloy layer of aluminum and titanium, and a titanium nitride layer or a titanium layer is 15 preferable. Note that the gate electrode layer may be formed using a light-transmitting conductive film. A light-transmitting conductive oxide can be given as an example of the light-transmitting conductive oxide film.

[0166]

Then, a gate insulating layer 397 is formed over the gate electrode layer 391.

20 [0167]

The gate insulating layer 397 can be formed with a single-layer structure or a layered structure using any of a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, an aluminum oxide layer, an aluminum nitride layer, an aluminum oxynitride layer, an aluminum nitride oxide layer, and a 25 hafnium oxide layer by a plasma CVD method, a sputtering method, or the like. In the case where a silicon oxide film is formed by a sputtering method, a silicon target or a quartz target is used as a target and oxygen or a mixed gas of oxygen and argon is used as a sputtering gas.

[0168]

30 Here, an oxide semiconductor that becomes intrinsic or substantially intrinsic by removal of impurities (a highly purified oxide semiconductor) is quite susceptible to the interface level or the interface charge; therefore, the interface with the gate

insulating layer is important. Thus, the gate insulating layer 397 that is to be in contact with a highly purified oxide semiconductor layer needs to have high quality.

[0169]

For example, a high-density plasma CVD method using microwaves (2.45 GHz) is preferably adopted because the formed insulating layer can be dense and have high withstand voltage and high quality. When a highly purified oxide semiconductor and a high-quality gate insulating layer are in contact with each other, the number of the interface levels can be reduced and interface characteristics can be favorable.

[0170]

It is needless to say that another film formation method such as a sputtering method or a plasma CVD method can be employed as long as a high-quality insulating layer can be formed as a gate insulating layer. Moreover, it is possible to use as the gate insulating layer an insulating layer whose quality and characteristics of an interface with an oxide semiconductor are improved with heat treatment performed after the formation of the insulating layer. In any case, an insulating layer that can reduce interface level density with an oxide semiconductor to form a favorable interface, as well as having favorable film quality as the gate insulating layer, is formed.

[0171]

The gate insulating layer 397 may have a structure where a nitride insulating layer and an oxide insulating layer are stacked over the gate electrode layer 391. For example, a silicon nitride layer (SiN_y ($y > 0$)) with a thickness of 50 nm to 200 nm inclusive is formed by a sputtering method as a first gate insulating layer and a silicon oxide layer (SiO_x ($x > 0$)) with a thickness of 5 nm to 300 nm inclusive is stacked as a second gate insulating layer over the first gate insulating layer. The thickness of the gate insulating layer may be set as appropriate depending on characteristics needed for a thin film transistor and may be approximately 350 nm to 400 nm.

[0172]

An oxide semiconductor layer 393 is formed over the gate insulating layer 397. Here, if an impurity is included in the oxide semiconductor layer 393, a bond between the impurity and a main component of the oxide semiconductor is cleaved by a stress such as high electric field or high temperature to result in a dangling bond, which causes

a shift of the threshold voltage (Vth).

[0173]

Therefore, the oxide semiconductor layer 393 and the gate insulating layer 397 which contacts with the oxide semiconductor layer 393 are formed so that impurities, 5 particularly hydrogen and water, are not included therein as little as possible, which allows formation of the thin layer transistor 390 with stable characteristics.

[0174]

In order that hydrogen, a hydroxyl group, and moisture might be contained in the gate insulating layer 397 and the oxide semiconductor layer 393 as little as possible, 10 it is preferable that the substrate 394 over which the gate electrode layer 391 is formed or the substrate 394 over which layers up to the gate insulating layer 397 are formed be preheated in a preheating chamber of a sputtering apparatus and the like as pretreatment for film formation so that impurities such as hydrogen and moisture adsorbed to the substrate 394 is eliminated. The temperature for the preheating is 100 °C to 400 °C 15 inclusive, preferably 150 °C to 300 °C inclusive. Note that a cryopump is preferable as an evacuation unit provided in the preheating chamber. Note that this preheating treatment may be omitted. Further, this preheating may be similarly performed on the substrate 394 over which layers up to a source electrode layer 395a and a drain electrode layer 395b have been formed, before formation of an oxide insulating layer 20 396.

[0175]

Then, the oxide semiconductor layer 393 is formed to a thickness of 2 nm to 200 nm inclusive over the gate insulating layer 397 (see FIG. 12A).

[0176]

25 Note that before the oxide semiconductor layer 393 is formed by a sputtering method, dust attached to a surface of the gate insulating layer 397 is preferably removed with reverse sputtering in which an argon gas is introduced and plasma is generated. The reverse sputtering refers to a method in which an RF power source is used for application of a voltage to the substrate side in an argon atmosphere so that plasma is 30 generated in the vicinity of the substrate to modify a surface of the substrate. Note that instead of an argon atmosphere, a nitrogen atmosphere, a helium atmosphere, an oxygen

atmosphere, or the like may be used.

[0177]

The oxide semiconductor layer 393 is formed by a sputtering method. The oxide semiconductor layer 393 is formed using an In-Ga-Zn-O-based oxide semiconductor layer, an In-Sn-Zn-O-based oxide semiconductor layer, an In-Al-Zn-O-based oxide semiconductor layer, a Sn-Ga-Zn-O-based oxide semiconductor layer, an Al-Ga-Zn-O-based oxide semiconductor layer, a Sn-Al-Zn-O-based oxide semiconductor layer, an In-Zn-O-based oxide semiconductor layer, a Sn-Zn-O-based oxide semiconductor layer, an Al-Zn-O-based oxide semiconductor layer, an In-O-based oxide semiconductor layer, a Sn-O-based oxide semiconductor layer, or a Zn-O-based oxide semiconductor layer. The oxide semiconductor layer 393 can be formed by a sputtering method in a rare gas (typically, argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere containing a rare gas (typically, argon) and oxygen. In the case of employing a sputtering method, a target containing SiO_2 at 2 wt% to 10 wt% inclusive may be used for film formation. In this embodiment, the oxide semiconductor layer 393 is formed by a sputtering method with the use of an In-Ga-Zn-O-based oxide semiconductor target.

[0178]

As a target for forming the oxide semiconductor layer 393 by a sputtering method, a metal oxide target containing zinc oxide as its main component can be used. As another example of a metal oxide target, an oxide semiconductor target containing In, Ga, and Zn (in a composition ratio, In_2O_3:Ga_2O_3:ZnO = 1:1:1 [molar ratio]) can be used. Alternatively, an oxide semiconductor target containing In, Ga, and Zn (the composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:2 or 1:1:4 [molar ratio]) may be used. The filling rate of an oxide semiconductor target is 90 % to 100 % inclusive, preferably 95 % to 99.9 % inclusive. A dense oxide semiconductor layer is formed using an oxide semiconductor target with a high filling rate.

[0179]

The substrate is held in a treatment chamber kept under reduced pressure, and the substrate is heated to a temperature of lower than 400 °C. Then, a sputtering gas from which hydrogen and moisture are removed is introduced into the treatment

chamber from which moisture is being removed, and the oxide semiconductor layer 393 is formed over the substrate 394 with the use of a metal oxide as a target. To remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably
5 used. Further, an evacuation unit may be a turbo molecular pump provided with a cold trap. In the deposition chamber which is evacuated with the cryopump, a hydrogen atom, a compound containing a hydrogen atom, such as water (H_2O), (more preferably, also a compound containing a carbon atom), and the like are removed, whereby the concentration of an impurity in the oxide semiconductor layer formed in the deposition
10 chamber can be reduced. By performing deposition by sputtering while removing moisture in the treatment chamber with the use of a cryopump, a substrate temperature in the formation of the oxide semiconductor layer 393 can be higher than or equal to room temperature and lower than 400 °C.

[0180]

15 An example of the deposition conditions are as follows: the distance between the substrate and the target is 100 mm, the pressure is 0.6 Pa, the DC power is 0.5 kW, and the atmosphere is an oxygen atmosphere (the flow rate of oxygen is 100 %). It is preferable that a pulsed DC power source be used because dust can be reduced and the film thickness can be uniform. The oxide semiconductor layer preferably has a
20 thickness of 5 nm to 30 nm inclusive. Note that the appropriate thickness depends on an oxide semiconductor material used and the thickness may be selected in accordance with a material.

[0181]

Examples of a sputtering method include an RF sputtering method in which a
25 high-frequency power source is used as a sputtering power source, a DC sputtering method, and a pulsed DC sputtering method in which a bias is applied in a pulsed manner. An RF sputtering method is mainly used in the case where an insulating film is formed, and a DC sputtering method is mainly used in the case where a metal film is formed.

30 [0182]

There is also a multi-source sputtering apparatus in which a plurality of targets

of different materials can be set. With the multi-source sputtering apparatus, films of different materials can be formed to be stacked in the same chamber, or plural kinds of materials can be discharged for film formation at the same time in the same chamber.

[0183]

5 In addition, there are a sputtering apparatus provided with a magnet system inside the chamber, which is for a magnetron sputtering method, and a sputtering apparatus which is used for an ECR sputtering method in which plasma produced with the use of microwaves is used without using glow discharge.

[0184]

10 Furthermore, as a deposition method using a sputtering method, there are also a reactive sputtering method in which a target substance and a sputtering gas component are chemically reacted with each other during deposition to form a thin compound film thereof, and a bias sputtering method in which voltage is also applied to a substrate during deposition.

15 [0185]

Then, in a second photolithography process, the oxide semiconductor layer is processed into an island-shaped oxide semiconductor layer 399 (see FIG. 12B). A resist mask for forming the island-shaped oxide semiconductor layer 399 may be formed by an ink-jet method. When the resist mask is formed by an ink-jet method, a
20 photomask is not used; therefore, manufacturing costs can be reduced.

[0186]

In forming the oxide semiconductor layer 399, a contact hole can be formed in the gate insulating layer 397.

[0187]

25 Note that the etching of the oxide semiconductor layer 393 may be dry etching, wet etching, or both dry etching and wet etching.

[0188]

As the etching gas for dry etching, a gas containing chlorine (chlorine-based gas such as chlorine (Cl_2), boron chloride (BCl_3), silicon chloride ($SiCl_4$), or carbon
30 tetrachloride (CCl_4)) is preferably used.

[0189]

Alternatively, a gas containing fluorine (fluorine-based gas such as carbon

tetrafluoride (CF_4), sulfur hexafluoride (SF_6), nitrogen trifluoride (NF_3), or trifluoromethane (CHF_3)); hydrogen bromide (HBr); oxygen (O_2); any of these gases to which a rare gas such as helium (He) or argon (Ar) is added; or the like can be used.

[0190]

5 As the dry etching method, a parallel plate RIE (reactive ion etching) method or an ICP (inductively coupled plasma) etching method can be used. In order to etch the film into a desired shape, the etching conditions (the amount of electric power applied to a coil-shaped electrode, the amount of electric power applied to an electrode on the substrate side, the temperature of the electrode on the substrate side, or the like)

10 are adjusted as appropriate.

[0191]

As an etchant used for wet etching, a mixed solution of phosphoric acid, acetic acid, and nitric acid, an ammonia hydrogen peroxide mixture (hydrogen peroxide (31 wt% in water): ammonia water of 28 wt%: water = 5:2:2), or the like can be used.

15 Alternatively, ITO07N (produced by KANTO CHEMICAL CO., INC.) may be used.

[0192]

The etchant used in the wet etching is removed by cleaning together with the material which is etched off. The waste liquid including the etchant and the material etched off may be purified and the material may be reused. When a material such as

20 indium included in the oxide semiconductor layer is collected from the waste liquid after the etching and reused, the resources can be efficiently used and the cost can be reduced.

[0193]

The etching conditions (such as an etchant, etching time, and temperature) are

25 appropriately adjusted depending on the material so that the oxide semiconductor film can be etched to have a desired shape.

[0194]

Note that it is preferable to perform reverse sputtering before formation of a conductive film in the following step so that a resist residue and the like attached to

30 surfaces of the oxide semiconductor layer 399 and the gate insulating layer 397 can be removed.

[0195]

Next, a conductive film is formed over the gate insulating layer 397 and the oxide semiconductor layer 399. The conductive film may be formed by a sputtering method or a vacuum evaporation method. As the material of the conductive film to be the source and drain electrode layers (including a wiring formed in the same layer as the
5 source and drain electrode layers), there are an element selected from Al, Cr, Cu, Ta, Ti, Mo, or W; an alloy including any of the above elements; an alloy containing a combination of any of these elements; and the like. Alternatively, a structure may be employed in which a high-melting-point metal layer of Cr, Ta, Ti, Mo, W, or the like is stacked over one of or both metal layers of Al, Cu, and the like. Still alternatively,
10 when an Al material to which an element preventing generation of hillocks and whiskers in an Al film, such as Si, Ti, Ta, W, Mo, Cr, Nd, Sc, or Y, is added is used, heat resistance can be increased.

[0196]

The conductive film may have a single-layer structure or a layered structure of
15 two or more layers. For example, a single-layer structure of an aluminum film including silicon, a two-layer structure in which a titanium film is stacked over an aluminum film, a three-layer structure in which a Ti film, an aluminum film, and a Ti film are stacked in the order presented, and the like can be given.

[0197]

20 Alternatively, the conductive film to be the source and drain electrode layers (including a wiring formed in the same layer as the source and drain electrode layers) may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), a mixed oxide of indium oxide and tin oxide (In_2O_3-SnO_2, abbreviated to ITO), a mixed oxide of indium oxide
25 and zinc oxide (In_2O_3-ZnO), or any of the metal oxides containing silicon or silicon oxide can be used.

[0198]

A third photolithography process is performed. A resist mask is formed over the conductive film and selective etching is performed, so that the source electrode layer
30 395a and the drain electrode layer 395b are formed. Then, the resist mask is removed (see FIG. 12C).

[0199]

Ultraviolet, a KrF laser beam, or an ArF laser beam is used for light exposure for forming the resist mask in the third photolithography process. A channel length L of the thin film transistor to be formed later depends on a width of an interval between a bottom portion of the source electrode layer 395a and a bottom portion of the drain electrode layer 395b which are adjacent to each other over the oxide semiconductor layer 399. Note that when light exposure is performed in the case where the channel length L is shorter than 25 nm, extreme ultraviolet with extremely short wavelengths of several nanometers to several tens of nanometers is used for light exposure for forming the resist mask in the third photolithography process. Light exposure with extreme ultraviolet leads to a high resolution and a large depth of field. Accordingly, the channel length L of the thin film transistor to be formed later can be set to 10 nm to 1000 nm inclusive. Thus, the operation speed of a circuit can be increased. Further, since an off current is significantly small in the thin film transistors of the present embodiment, low power consumption can be achieved.

[0200]

Note that materials and etching conditions are adjusted as appropriate so that the oxide semiconductor layer 399 is not completely removed when the conductive film is etched.

[0201]

In this embodiment, a Ti film is used as the conductive film, an In-Ga-Zn-O-based oxide semiconductor is used as the oxide semiconductor layer 399, and an ammonia hydrogen peroxide mixture (hydrogen peroxide (31 wt% in water): ammonia water of 28 wt%: water = 5:2:2) is used as an etchant.

[0202]

Note that in the third photolithography process, part of the oxide semiconductor layer 399 may be etched, whereby an oxide semiconductor layer having a groove (a depressed portion) may be formed. The resist mask used for forming the source electrode layer 395a and the drain electrode layer 395b may be formed by an ink-jet method. When the resist mask is formed by an ink-jet method, a photomask is not used; therefore, manufacturing costs can be reduced.

[0203]

To reduce the number of photomasks and steps in a photolithography step, etching may be performed with the use of a resist mask formed using a multi-tone mask which is a light-exposure mask through which light is transmitted so as to have a plurality of intensities. Since a resist mask formed using a multi-tone mask has a
5 plurality of thicknesses and can be further changed in shape by performing etching, the resist mask can be used in a plurality of etching steps to provide different patterns. Thus, a resist mask corresponding to at least two kinds of different patterns can be formed by using a multi-tone mask. Accordingly, the number of light-exposure masks can be reduced and the number of corresponding photolithography steps can be also
10 reduced, whereby simplification of a process can be realized.

[0204]

With plasma treatment with a gas such as N_2O, N_2, or Ar, water adsorbed to a surface of an exposed portion of the oxide semiconductor layer may be removed. Alternatively, plasma treatment may be performed using a mixed gas of oxygen and
15 argon.

[0205]

In the case of performing the plasma treatment, the oxide insulating layer 396 is sequentially formed without exposing the substrate 394 to the air (see FIG. 12D). Note that the oxide insulating layer 396 is in contact with part of the oxide
20 semiconductor layer 399 and serves as a protective insulating film. In this embodiment, the oxide insulating layer 396 is formed in contact with the oxide semiconductor layer 399 in a region where the oxide semiconductor layer 399 does not overlap with the source electrode layer 395a and the drain electrode layer 395b.

[0206]

25 In this embodiment, a silicon oxide layer having a defect is formed as the oxide insulating layer 396 with the use of a silicon target at a room temperature or a temperature lower than 100 °C under a sputtering gas atmosphere from which hydrogen and moisture are removed and which contains high-purity oxygen.

[0207]

30 For example, a silicon oxide film is formed by a pulsed DC sputtering method in which the purity of a sputtering gas is 6N, a boron-doped silicon target (the resistivity

is 0.01 Ω·cm) is used, the distance between the substrate and the target (T-S distance) is 89 mm, the pressure is 0.4 Pa, the DC power is 6 kW, and the atmosphere is an oxygen atmosphere (the oxygen flow rate is 100 %). The thickness of the silicon oxide film is 300 nm. Note that instead of a silicon target, quartz (preferably, synthetic quartz) can
5 be used as a target used when the silicon oxide film is formed. As a sputtering gas, oxygen or a mixed gas of oxygen and argon is used.

[0208]

In that case, the oxide insulating layer 396 is preferably formed after removing moisture in the treatment chamber. This is for preventing hydrogen, a hydroxyl group,
10 and moisture from being contained in the oxide semiconductor layer 399 and the oxide insulating layer 396.

[0209]

In order to remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium
15 sublimation pump is preferably used. Further, an evacuation unit may be a turbo molecular pump provided with a cold trap. In the deposition chamber which is evacuated with the cryopump, a hydrogen atom, a compound containing a hydrogen atom, such as water (H_2O), and the like are removed, whereby the concentration of an impurity in the oxide insulating layer 396 formed in the deposition chamber can be
20 reduced.

[0210]

Note that as the oxide insulating layer 396, a silicon oxynitride layer, an aluminum oxide layer, an aluminum oxynitride layer, or the like may be used instead of the silicon oxide layer.

25 [0211]

Further, heat treatment may be performed at 100 °C to 400 °C while the oxide insulating layer 396 and the oxide semiconductor layer 399 are in contact with each other. Since the oxide insulating layer 396 in this embodiment has many defects, with this heat treatment, an impurity such as hydrogen, moisture, a hydroxyl group, or a
30 hydride contained in the oxide semiconductor layer 399 can be diffused to the oxide insulating layer 396 so that the impurity in the oxide semiconductor layer 399 can be

further reduced.

[0212]

Through the above steps, the thin film transistor 390 including the oxide semiconductor layer 392 in which the concentration of hydrogen, moisture, a hydroxyl group, or a hydride is reduced can be formed (see FIG. 12E).

[0213]

Moisture in a reaction atmosphere is removed as described above in forming the oxide semiconductor layer, whereby the concentration of hydrogen and hydride in the oxide semiconductor layer can be reduced. Accordingly, the oxide semiconductor layer can be stable.

[0214]

A protective insulating layer may be provided over the oxide insulating layer. In this embodiment, a protective insulating layer 398 is formed over the oxide insulating layer 396. As the protective insulating layer 398, a silicon nitride film, a silicon nitride oxide film, an aluminum nitride film, an aluminum nitride oxide film, or the like is used.

[0215]

The substrate 394 over which layers up to the oxide insulating layer 396 have been formed is heated to a temperature of 100 °C to 400 °C, a sputtering gas from which hydrogen and moisture are removed and which contains high-purity nitrogen is introduced, and a silicon target is used, whereby a silicon nitride film is formed as the protective insulating layer 398. In this case, the protective insulating layer 398 is preferably formed after removing moisture in a treatment chamber, similarly to the oxide insulating layer 396.

[0216]

In the case where the protective insulating layer 398 is formed, the substrate 394 is heated to 100 °C to 400 °C in forming the protective insulating layer 398, whereby hydrogen or water contained in the oxide semiconductor layer 392 can be diffused to the oxide insulating layer 396. In that case, heat treatment is not necessarily performed after formation of the oxide insulating layer 396.

[0217]

In the case where the silicon oxide layer is formed as the oxide insulating layer 396 and the silicon nitride layer is stacked thereover as the protective insulating layer 398, the silicon oxide layer and the silicon nitride layer can be formed with the use of a common silicon target in the same treatment chamber. After a sputtering gas containing oxygen is introduced first, a silicon oxide layer is formed using a silicon target provided in the treatment chamber, and then, the sputtering gas is switched to nitrogen and the same silicon target is used to form a silicon nitride layer. Since the silicon oxide layer and the silicon nitride layer can be formed successively without exposing the oxide insulating layer 396 to the air, impurities such as hydrogen and moisture can be prevented from adsorbing onto a surface of the oxide insulating layer 396. After the protective insulating layer 398 is formed, heat treatment (at a temperature of 100 °C to 400 °C) for diffusing hydrogen or moisture contained in the oxide semiconductor layer to the oxide insulating layer may be performed.

[0218]

After the protective insulating layer is formed, heat treatment may be further performed at 100 °C to 200 °C inclusive for one hour to 30 hours inclusive in the air. This heat treatment may be performed at a fixed heating temperature. Alternatively, the following change in the heating temperature may be conducted plural times repeatedly: the heating temperature is increased from a room temperature to a temperature of 100 °C to 200 °C inclusive and then decreased to a room temperature. Further, this heat treatment may be performed under a reduced pressure. Under a reduced pressure, the heating time can be shortened. With this heat treatment, reliability of a display panel can be further improved.

[0219]

As mentioned above, moisture in a reaction atmosphere is removed in forming the oxide semiconductor layer to be a channel formation region over the gate insulating layer, whereby the concentration of hydrogen and hydride in the oxide semiconductor layer can be reduced.

[0220]

The above steps can be used for manufacture of backplanes (substrates over which thin film transistors are formed) of liquid crystal display panels,

electroluminescent display panels, display devices using electronic ink, or the like. Since the above steps can be performed at a temperature of 400 °C or lower, they can also be applied to manufacturing steps where a glass substrate with a thickness of 1 mm or smaller and a side of longer than 1 m is used. In addition, all of the above steps can 5 be performed at a treatment temperature of 400 °C or lower; therefore, display panels can be manufactured without consuming much energy.

[0221]

This embodiment can be implemented in appropriate combination with any of the other embodiments and examples.

10 [0222]

Thus, with a thin film transistor including an oxide semiconductor layer, a large touch panel having stable electric characteristics and high reliability can be provided.

[0223]

(Embodiment 6)

15 In this embodiment, another example of a thin film transistor which can be applied to the display panel disclosed in this specification will be described. A thin film transistor 310 in this embodiment can be used as the thin film transistor formed using an oxide semiconductor layer including a channel formation region in any of the above embodiments (e.g., the transistors 201, 205, 206, and 301 in Embodiment 1, and 20 the transistors 503 and 540 in Embodiments 3 and 4). The same portions as those in the above embodiments and portions having functions similar to those of the portions in the above embodiments and steps similar to those in the above embodiments may be handled as in the above embodiments, and repeated description is omitted. In addition, detailed description of the same portions is also omitted.

25 [0224]

An embodiment of a thin film transistor and a manufacturing method of the thin film transistor of this embodiment is described with reference to FIGS. 13A to 13E.

[0225]

FIGS. 13A to 13E illustrate an example of a cross-sectional structure of a thin 30 film transistor. The thin film transistor 310 illustrated in FIGS. 13A to 13E is one of bottom gate thin film transistors and is also referred to as an inverted staggered thin film

transistor.

[0226]

Although description is given using a single-gate thin film transistor as the thin film transistor 310, a multi-gate thin film transistor including a plurality of channel
5 formation regions may be formed as needed.

[0227]

A process of manufacturing the thin film transistor 310 over a substrate 305 is described below with reference to FIGS. 13A to 13E.

[0228]

10 First, after a conductive film is formed over the substrate 305 having an insulating surface, a gate electrode layer 311 is formed in a first photolithography process. Note that a resist mask may be formed by an ink-jet method. When the resist mask is formed by an ink-jet method, a photomask is not used; therefore, manufacturing costs can be reduced.

15 [0229]

There is no particular limitation on a substrate that can be used as the substrate 305 having an insulating surface as long as it has at least heat resistance enough to withstand heat treatment performed later. A glass substrate formed using barium borosilicate glass, aluminoborosilicate glass, or the like can be used.

20 [0230]

When the temperature of the heat treatment performed later is high, a substrate having a strain point of 730 °C or higher is preferably used as the glass substrate. As a material of the glass substrate, a glass material such as aluminosilicate glass, aluminoborosilicate glass, or barium borosilicate glass is used, for example. By
25 containing a larger amount of barium oxide (BaO) than boron oxide (B_2O_3), a glass substrate is heat-resistant and of more practical use. Therefore, a glass substrate containing a larger amount of BaO than B_2O_3 is preferably used.

[0231]

Note that, instead of the glass substrate described above, a substrate formed
30 using an insulator such as a ceramic substrate, a quartz substrate, or a sapphire substrate may be used as the substrate 305. Alternatively, a crystallized glass substrate or the like may be used.

[0232]

An insulating film serving as a base film may be provided between the substrate 305 and the gate electrode layer 311. The base film has a function of preventing diffusion of an impurity element from the substrate 305, and can be formed with a single-layer structure or a layered structure using any of a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, and a silicon oxynitride film.

[0233]

The gate electrode layer 311 can be formed with a single-layer structure or a layered structure using any of metal materials such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, and scandium, and an alloy material including any of these materials as a main component.

[0234]

As a two-layer structure of the gate electrode layer 311, for example, a two-layer structure in which a molybdenum layer is stacked over an aluminum layer, a two-layer structure in which a molybdenum layer is stacked over a copper layer, a two-layer structure in which a titanium nitride layer or a tantalum nitride layer is stacked over a copper layer, a two-layer structure in which a titanium nitride layer and a molybdenum layer are stacked, or a two-layer structure in which a tungsten nitride layer and a tungsten layer are stacked is preferable. As a three-layer structure, a stack of a tungsten layer or a tungsten nitride layer, an alloy layer of aluminum and silicon or an alloy layer of aluminum and titanium, and a titanium nitride layer or a titanium layer is preferable.

[0235]

Then, the gate insulating layer 307 is formed over the gate electrode layer 311.

[0236]

The gate insulating layer 307 can be formed with a single-layer structure or a layered structure using any of a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, and an aluminum oxide layer by a plasma CVD method, a sputtering method, or the like. For example, a silicon oxynitride layer may be formed by a plasma CVD method with SiH_4, oxygen, and nitrogen for a deposition gas. The thickness of the gate insulating layer 307 is 100 nm to 500 nm inclusive, and in the case where the gate insulating layer 307 has a layered structure, a

second gate insulating layer with a thickness of 5 nm to 300 nm inclusive is stacked over a first gate insulating layer with a thickness of 50 nm to 200 nm inclusive, for example.

[0237]

5 In this embodiment, a silicon oxynitride layer having a thickness of 100 nm is formed as the gate insulating layer 307 by a plasma CVD method.

[0238]

Then, an oxide semiconductor layer 330 is formed to a thickness of 2 nm to 200 nm inclusive over the gate insulating layer 307.

10 [0239]

Note that before the oxide semiconductor layer 330 is formed by a sputtering method, dust attached to a surface of the gate insulating layer 307 is preferably removed with reverse sputtering in which an argon gas is introduced and plasma is generated. Note that instead of an argon atmosphere, a nitrogen atmosphere, a helium atmosphere,
15 an oxygen atmosphere, or the like may be used.

[0240]

The oxide semiconductor layer 330 is formed using an In-Ga-Zn-O-based oxide semiconductor layer, an In-Sn-Zn-O-based oxide semiconductor layer, an In-Al-Zn-O-based oxide semiconductor layer, a Sn-Ga-Zn-O-based oxide
20 semiconductor layer, an Al-Ga-Zn-O-based oxide semiconductor layer, a Sn-Al-Zn-O-based oxide semiconductor layer, an In-Zn-O-based oxide semiconductor layer, a Sn-Zn-O-based oxide semiconductor layer, an Al-Zn-O-based oxide semiconductor layer, an In-O-based oxide semiconductor layer, a Sn-O-based oxide semiconductor layer, or a Zn-O-based oxide semiconductor layer. The oxide
25 semiconductor layer 330 can be formed by a sputtering method in a rare gas (typically, argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere containing a rare gas (typically, argon) and oxygen. In the case of employing a sputtering method, a target containing SiO_2 at 2 wt% to 10 wt% inclusive may be used for film formation. In this embodiment, the oxide semiconductor layer 330 is formed by a sputtering method with
30 the use of an In-Ga-Zn-O-based metal oxide target. FIG. 13A corresponds to a cross-sectional view at this stage.

[0241]

As a target for forming the oxide semiconductor layer 330 by a sputtering method, a metal oxide target containing zinc oxide as its main component can be used. As another example of a metal oxide target, an oxide semiconductor target containing In, Ga, and Zn (in a composition ratio, In_2O_3:Ga_2O_3:ZnO = 1:1:1 [molar ratio]) can be used. Alternatively, an oxide semiconductor target containing In, Ga, and Zn (the composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:2 or 1:1:4 [molar ratio]) may be used. The filling rate of an oxide semiconductor target is 90 % to 100 % inclusive, preferably 95 % to 99.9 %. A dense oxide semiconductor layer is formed using an oxide semiconductor target with a high filling rate.

[0242]

It is preferable to use a high-purity gas from which an impurity such as hydrogen, water, a substance having a hydroxyl group, or a hydride is removed to a concentration of several ppm or several ppb, as a sputtering gas when the oxide semiconductor layer 330 is formed.

[0243]

The substrate is held in a treatment chamber kept under reduced pressure, and the substrate temperature is set to 100 °C to 600 °C, preferably 200 °C to 400 °C. Film formation is performed while the substrate is heated, whereby the concentration of an impurity contained in the oxide semiconductor layer formed can be reduced. Further, damages due to sputtering can be reduced. Then, a sputtering gas from which hydrogen and moisture are removed is introduced into the treatment chamber from which moisture is being removed, and the oxide semiconductor layer 330 is formed over the substrate 305 with the use of a metal oxide as a target. To remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo molecular pump provided with a cold trap. In the deposition chamber which is evacuated with the cryopump, a hydrogen atom, a compound containing a hydrogen atom, such as water (H_2O), (more preferably, also a compound containing a carbon atom), and the like are removed, whereby the concentration of an impurity in the oxide semiconductor layer formed in the deposition chamber can be reduced.

[0244]

An example of the deposition conditions are as follows: the distance between the substrate and the target is 100 mm, the pressure is 0.6 Pa, the DC power is 0.5 kW, and the atmosphere is an oxygen atmosphere (the flow rate of oxygen is 100 %). It is
5 preferable that a pulsed DC power source be used because dust can be reduced and the film thickness can be uniform. The oxide semiconductor layer preferably has a thickness of 5 nm to 30 nm inclusive. Note that the appropriate thickness depends on an oxide semiconductor material used and the thickness may be selected in accordance with a material.

10 [0245]

Then, in a second photolithography process, the oxide semiconductor layer 330 is processed into an island-shaped oxide semiconductor layer. A resist mask for forming the island-shaped oxide semiconductor layer may be formed by an ink-jet method. When the resist mask is formed by an ink-jet method, a photomask is not
15 used; therefore, manufacturing costs can be reduced.

[0246]

Next, the oxide semiconductor layer is subjected to first heat treatment. With the first heat treatment, dehydration or dehydrogenation of the oxide semiconductor layer can be conducted. The temperature of the first heat treatment is higher than or
20 equal to 400 °C and lower than or equal to 750 °C, preferably higher than or equal to 400 °C and lower than the strain point of the substrate. Here, the substrate is introduced into an electric furnace which is one of heat treatment apparatuses, and heat treatment is performed on the oxide semiconductor layer in a nitrogen atmosphere at 450 °C for one hour; thus, an oxide semiconductor layer 331 is obtained (see FIG. 13B).

25 [0247]

The apparatus for the heat treatment is not limited to the electric furnace and may be the one provided with a device for heating an object to be processed, using heat conduction or heat radiation from a heating element such as a resistance heating element. For example, an RTA (rapid thermal anneal) apparatus such as a GRTA (gas rapid
30 thermal anneal) apparatus or an LRTA (lamp rapid thermal anneal) apparatus can be used. An LRTA apparatus is an apparatus for heating an object to be processed by

radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus for heat treatment using a high-temperature gas. As the gas, an inert gas which does not react
5 with an object to be processed in heat treatment, such as nitrogen or a rare gas such as argon is used.

[0248]

For example, as the first heat treatment, GRTA may be performed as follows. The substrate is transferred and put in an inert gas which has been heated to a high
10 temperature of 650 °C to 700 °C, heated for several minutes, and transferred and taken out of the inert gas which has been heated to a high temperature. GRTA enables high-temperature heat treatment in a short time.

[0249]

Note that in the first heat treatment, it is preferable that water, hydrogen, and
15 the like be not included in nitrogen or a rare gas such as helium, neon, or argon. Alternatively, it is preferable that nitrogen or a rare gas such as helium, neon, or argon introduced into an apparatus for the heat treatment have a purity of 6N (99.9999 %) or more, preferably, 7N (99.99999 %) or more (that is, an impurity concentration is set to 1 ppm or lower, preferably, 0.1 ppm or lower).

20 [0250]

Alternatively, the first heat treatment of the oxide semiconductor layer may be performed on the oxide semiconductor layer 330 which has not yet been processed into the island-shaped oxide semiconductor layer. In that case, after the first heat treatment, the substrate is taken out of the heating apparatus and a photolithography process is
25 performed.

[0251]

The heat treatment having an effect of dehydration or dehydrogenation on the oxide semiconductor layer may be performed at any of the following timings: after the oxide semiconductor layer is formed; after a source electrode layer and a drain electrode
30 layer are formed over the oxide semiconductor layer; and after a protective insulating film is formed over the source electrode layer and the drain electrode layer.

[0252]

In the case of forming a contact hole in the gate insulating layer 307, the step may be performed either before or after dehydration or dehydrogenation of the oxide semiconductor layer 330.

5 [0253]

Note that the etching of the oxide semiconductor layer is not limited to wet etching and may be dry etching.

[0254]

The etching conditions (such as an etchant, etching time, and temperature) are
10 appropriately adjusted depending on the material so that the oxide semiconductor film can be etched to have a desired shape.

[0255]

Next, a conductive film to be the source and drain electrode layers (including a wiring formed in the same layer as the source and drain electrode layers) is formed over
15 the gate insulating layer 307 and the oxide semiconductor layer 331. The conductive film may be formed by a sputtering method or a vacuum evaporation method. As the material of the conductive film to be the source and drain electrode layers (including the wiring formed in the same layer as the source and drain electrode layers), there are an element selected from Al, Cr, Cu, Ta, Ti, Mo, or W; an alloy including any of the above
20 elements; an alloy containing a combination of any of these elements; and the like. Alternatively, a structure may be employed in which a high-melting-point metal layer of Cr, Ta, Ti, Mo, W, or the like is stacked over one of or both metal layers of Al, Cu, and the like. Still alternatively, when an Al material to which an element preventing generation of hillocks and whiskers in an Al film, such as Si, Ti, Ta, W, Mo, Cr, Nd, Sc,
25 or Y, is added is used, heat resistance can be increased.

[0256]

The conductive film may have a single-layer structure or a layered structure of two or more layers. For example, a single-layer structure of an aluminum film including silicon, a two-layer structure in which a titanium film is stacked over an
30 aluminum film, a three-layer structure in which a Ti film, an aluminum film, and a Ti film are stacked in the order presented, and the like can be given.

[0257]

Alternatively, the conductive film to be the source and drain electrode layers (including a wiring formed in the same layer as the source and drain electrode layers) may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), a mixed oxide of indium
5 oxide and tin oxide (In_2O_3-SnO_2, abbreviated to ITO), a mixed oxide of indium oxide and zinc oxide (In_2O_3-ZnO), or any of the metal oxides containing silicon or silicon oxide can be used.

[0258]

If heat treatment is performed after formation of the conductive film, it is
10 preferable that the conductive film have heat resistance enough to withstand the heat treatment.

[0259]

A third photolithography process is performed. A resist mask is formed over the conductive film and selective etching is performed, so that a source electrode layer
15 315a and a drain electrode layer 315b are formed. Then, the resist mask is removed (see FIG. 13C).

[0260]

Ultraviolet, a KrF laser beam, or an ArF laser beam is used for light exposure for forming the resist mask in the third photolithography process. A channel length L
20 of the thin film transistor to be formed later depends on a width of an interval between a bottom portion of the source electrode layer 315a and a bottom portion of the drain electrode layer 315b which are adjacent to each other over the oxide semiconductor layer 331. Note that when light exposure is performed in the case where the channel length L is shorter than 25 nm, extreme ultraviolet with extremely short wavelengths of
25 several nanometers to several tens of nanometers is used for light exposure for forming the resist mask in the third photolithography process. Light exposure with extreme ultraviolet leads to a high resolution and a large depth of field. Accordingly, the channel length L of the thin film transistor to be formed later can be set to 10 nm to 1000 nm inclusive. Thus, the operation speed of a circuit can be increased. Further,
30 an off current is significantly small in the thin film transistors of the present embodiment, so that low power consumption can be achieved.

[0261]

Note that materials and etching conditions are adjusted as appropriate so that the oxide semiconductor layer 331 is not completely removed when the conductive film is etched.

[0262]

5 In this embodiment, a Ti film is used as the conductive film, an In-Ga-Zn-O-based oxide semiconductor is used as the oxide semiconductor layer 331, and an ammonia hydrogen peroxide mixture (hydrogen peroxide (31 wt% in water): ammonia water of 28 wt%: water = 5:2:2) is used as an etchant.

[0263]

10 Note that in the third photolithography process, part of the oxide semiconductor layer 331 may be etched, whereby an oxide semiconductor layer having a groove (a depressed portion) may be formed. The resist mask used for forming the source electrode layer 315a and the drain electrode layer 315b may be formed by an ink-jet method. When the resist mask is formed by an ink-jet method, a photomask is 15 not used; therefore, manufacturing costs can be reduced.

[0264]

Further, an oxide conductive layer may be formed between the oxide semiconductor layer 331 and the source and drain electrode layers 315a and 315b. The oxide conductive layer and the metal layer for forming the source and drain electrode 20 layers can be formed successively. The oxide conductive layer can function as a source region and a drain region.

[0265]

When the oxide conductive layer is provided as the source region and the drain region between the oxide semiconductor layer 331 and the source and drain electrode 25 layers 315a and 315b, the source region and the drain region can have lower resistance and the transistor can operate at high speed.

[0266]

To reduce the number of photomasks and steps in a photolithography step, etching may be performed with the use of a resist mask formed using a multi-tone mask 30 which is a light-exposure mask through which light is transmitted so as to have a plurality of intensities. Since a resist mask formed using a multi-tone mask has a

plurality of thicknesses and can be further changed in shape by performing etching, the resist mask can be used in a plurality of etching steps to provide different patterns. Thus, a resist mask corresponding to at least two kinds of different patterns can be formed by using a multi-tone mask. Accordingly, the number of light-exposure masks can be reduced and the number of corresponding photolithography steps can be also reduced, whereby simplification of a process can be realized.

[0267]

Next, plasma treatment with a gas such as N_2O, N_2, or Ar is performed. With this plasma treatment, water adsorbed to a surface of an exposed portion of the oxide semiconductor layer is removed. Alternatively, plasma treatment may be performed using a mixed gas of oxygen and argon.

[0268]

After the plasma treatment is performed, an oxide insulating layer 316 which serves as a protective insulating film and is in contact with part of the oxide semiconductor layer is formed without exposure of the oxide semiconductor layer to the air.

[0269]

The oxide insulating layer 316 can be formed to a thickness of longer than or equal to 1 nm by a sputtering method or the like as appropriate, which inhibits an impurity such as water or hydrogen from entering the oxide insulating layer 316. If hydrogen is contained in the oxide insulating layer 316, entry of the hydrogen to the oxide semiconductor layer or abstract of oxygen in the oxide semiconductor layer by the hydrogen might be caused, whereby a backchannel of the oxide semiconductor layer might decrease in resistance (to be n-type) and thus a parasitic channel might be formed. Therefore, it is important that a formation method in which hydrogen is not used is employed so that the oxide insulating layer 316 is formed containing as little hydrogen as possible.

[0270]

The oxide insulating layer 316 which is formed in contact with the oxide semiconductor layer is formed using an inorganic insulating film that does not contain impurities such as moisture, a hydrogen ion, and OH^- and blocks entry of such impurities from the outside, typically, a silicon oxide film, a silicon oxynitride film, an

aluminum oxide film, or an aluminum oxynitride film. In this embodiment, a silicon oxide film is formed to a thickness of 200 nm as the oxide insulating layer 316 by a sputtering method. The substrate temperature in film formation may be higher than or equal to room temperature and lower than or equal to 300 °C and in this embodiment, is 5 100 °C. The silicon oxide film can be formed by a sputtering method in a rare gas (typically, argon) atmosphere, an oxygen atmosphere, or an atmosphere containing a rare gas (typically, argon) and oxygen. Further, a silicon oxide target or a silicon target can be used as a target. For example, the silicon oxide film can be formed using a silicon target by a sputtering method in an atmosphere containing oxygen and nitrogen.

10 [0271]

In that case, the oxide insulating layer 316 is preferably formed removing moisture in the treatment chamber. This is for preventing hydrogen, a hydroxyl group, and moisture from being contained in the oxide semiconductor layer 331 and the oxide insulating layer 316.

15 [0272]

In order to remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo molecular pump provided with a cold trap. In the deposition chamber which is 20 evacuated with the cryopump, a hydrogen atom, a compound containing a hydrogen atom, such as water (H_2O), and the like are removed, whereby the concentration of an impurity in the oxide insulating layer 316 formed in the deposition chamber can be reduced.

[0273]

25 It is preferable to use a high-purity gas from which an impurity such as hydrogen, water, a hydroxyl group, or a hydride is removed to a concentration of several ppm or several ppb, as a sputtering gas when the oxide insulating layer 316 is formed.

[0274]

Next, second heat treatment (preferably 200 °C to 400 °C inclusive, for 30 example, from 250 °C to 350 °C inclusive) is performed in an inert gas atmosphere or an oxygen gas atmosphere. For example, the second heat treatment is performed in a

nitrogen atmosphere at 250 °C for one hour. In the second heat treatment, the oxide semiconductor layer is heated while part of the oxide semiconductor layer (a channel formation region) is in contact with the oxide insulating layer 316.

[0275]

5 Through the above steps, the initially formed oxide semiconductor layer is decreased in resistance by the first heat treatment for dehydration or dehydrogenation, and then part of the oxide semiconductor layer which is in contact with the oxide insulating layer 316 is selectively changed to be in an oxygen excess state by the second heat treatment. As a result, the channel formation region 313 which overlaps with the 10 gate electrode layer 311 becomes intrinsic, and a high-resistance source region 314a and a high-resistance drain region 314b which overlap with the source electrode layer 315a and the drain electrode layer 315b, respectively, are formed in a self-aligned manner. Thus, the thin film transistor 310 is formed (see FIG. 13D).

[0276]

15 When a silicon oxide layer having many defects is used as the oxide insulating layer 316, the heat treatment after formation of the silicon oxide layer has an effect in diffusing an impurity such as hydrogen, moisture, a hydroxyl group, or a hydride contained in the oxide semiconductor layer to the oxide insulating layer so that the impurity contained in the oxide semiconductor layer can be further reduced.

20 [0277]

Note that by forming the high-resistance drain region 314b (and the high-resistance source region 314a) in the oxide semiconductor layer overlapping with the drain electrode layer 315b (and the source electrode layer 315a), reliability of the thin film transistor can be improved. Specifically, by forming the high-resistance drain 25 region 314b, the structure can be obtained in which conductivities of the drain electrode layer 315b, the high-resistance drain region 314b, and the channel formation region 313 vary in that order. Therefore, in the case where the thin film transistor operates with the drain electrode layer 315b connected to a wiring for supplying a high power supply potential *VDD*, the high-resistance drain region serves as a buffer and a high electric 30 field is not applied locally even if a high electric field is applied between the gate electrode layer 311 and the drain electrode layer 315b; thus, the withstand voltage of the thin film transistor can be increased.

[0278]

The high-resistance source region 314a or the high-resistance drain region 314b in the oxide semiconductor layer 331 is formed in the entire thickness direction in the case where the thickness of the oxide semiconductor layer 331 is 15 nm or smaller. However, in the case where the thickness of the oxide semiconductor layer 331 is 30 nm or larger, they are formed only in part of the oxide semiconductor layer 331, that is, in a region, which is in contact with the source electrode layer 315a or the drain electrode layer 315b, and the vicinity thereof. Therefore, a region which is close to the gate insulating film 331 can be made to be i-type.

[0279]

A protective insulating layer 308 may be additionally formed over the oxide insulating layer 316. The protective insulating layer 308 is formed using an inorganic insulating film which does not contain impurities such as moisture, a hydrogen ion, and OH^- and blocks entry of these from the outside: for example, a silicon nitride film, an aluminum nitride film, a silicon nitride oxide film, an aluminum nitride oxide film, or the like. For example, a silicon nitride film is formed by an RF sputtering method. An RF sputtering method is preferable as a formation method of the protective insulating layer because of high productivity. In this embodiment, as the protective insulating layer, a protective insulating layer 306 is formed using a silicon nitride film (see FIG. 13E).

[0280]

The substrate 305 over which layers up to the oxide insulating layer 316 have been formed is heated to a temperature of 100 °C to 400 °C, a sputtering gas from which hydrogen and moisture are removed and which contains high-purity nitrogen is introduced, and a silicon target is used, whereby a silicon nitride layer is formed as the protective insulating layer 306. In this case, the protective insulating layer 306 is preferably formed after removing moisture in a treatment chamber, similarly to the oxide insulating layer 316.

[0281]

After the formation of the protective insulating layer 308, heat treatment may be performed at 100 °C to 200 °C inclusive for one hour to 30 hours inclusive in the air.

This heat treatment may be performed at a fixed temperature. Alternatively, the following change in the heating temperature may be conducted plural times repeatedly: the heating temperature is increased from a room temperature to a temperature of 100 °C to 200 °C inclusive and then decreased to a room temperature. Further, this heat treatment may be performed under a reduced pressure. Under a reduced pressure, the heating time can be shortened.

[0282]

Note that a planarization insulating layer for planarization may be provided over the protective insulating layer 306.

[0283]

This embodiment can be implemented in appropriate combination with any of the other embodiments and examples.

[0284]

Thus, with a thin film transistor including an oxide semiconductor layer, a large touch panel having stable electric characteristics and high reliability can be provided.

[0285]

(Embodiment 7)

In this embodiment, another example of a thin film transistor which can be applied to the display panel disclosed in this specification will be described. A thin film transistor 360 in this embodiment can be used as the thin film transistor formed using an oxide semiconductor layer including a channel formation region in any of the above embodiments (e.g., the transistors 201, 205, 206, and 301 in Embodiment 1, and the transistors 503 and 540 in Embodiments 3 and 4). The same portions as those in the above embodiments and portions having functions similar to those of the portions in the above embodiments and steps similar to those in the above embodiments may be handled as in the above embodiments, and repeated description is omitted. In addition, detailed description of the same portions is also omitted.

[0286]

An embodiment of a thin film transistor and a manufacturing method of the thin film transistor of this embodiment is described with reference to FIGS. 14A to 14D.

[0287]

FIGS. 14A to 14D illustrate an example of a cross-sectional structure of a thin

film transistor. The thin film transistor 360 illustrated in FIGS. 14A to 14D is one of bottom gate thin film transistors, which is called a channel protective thin film transistor (also referred to as a channel-stop thin film transistor), and is also referred to as an inverted staggered thin film transistor.

5 [0288]

Although description is given using a single-gate thin film transistor as the thin film transistor 360, a multi-gate thin film transistor including a plurality of channel formation regions may be formed as needed.

[0289]

10 A process of manufacturing the thin film transistor 360 over a substrate 320 is described below with reference to FIGS. 14A to 14D.

[0290]

First, after a conductive film is formed over the substrate 320 having an insulating surface, the gate electrode layer 361 is formed in a first photolithography 15 process. Note that a resist mask may be formed by an ink-jet method. When the resist mask is formed by an ink-jet method, a photomask is not used; therefore, manufacturing costs can be reduced.

[0291]

Further, the gate electrode layer 361 can be formed with a single-layer structure 20 or a layered structure using any of metal materials such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, and scandium, and an alloy material including any of these materials as a main component.

[0292]

Then, the gate insulating layer 322 is formed over the gate electrode layer 361.

25 [0293]

In this embodiment, a silicon oxynitride layer having a thickness of 100 nm is formed as the gate insulating layer 322 by a plasma CVD method.

[0294]

Then, an oxide semiconductor layer is formed to a thickness of 2 nm to 200 nm 30 inclusive over the gate insulating layer 322 and processed into an island-shaped oxide semiconductor layer in a second photolithography process. In this embodiment, the oxide semiconductor layer is formed by a sputtering method with the use of an

In-Ga-Zn-O-based metal oxide target.

[0295]

In that case, the oxide semiconductor layer is preferably formed removing moisture in the treatment chamber. This is for preventing hydrogen, a hydroxyl group, 5 and moisture from being contained in the oxide semiconductor layer.

[0296]

In order to remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo 10 molecular pump provided with a cold trap. In the deposition chamber which is evacuated with the cryopump, a hydrogen atom, a compound containing a hydrogen atom, such as water (H_2O), and the like are removed, whereby the concentration of an impurity in the oxide semiconductor layer formed in the deposition chamber can be reduced.

15 [0297]

It is preferable to use a high-purity gas from which an impurity such as hydrogen, water, a hydroxyl group, or a hydride is removed to a concentration of several ppm or several ppb, as a sputtering gas used when the oxide semiconductor layer is formed.

20 [0298]

Next, the oxide semiconductor layer is subjected to dehydration or dehydrogenation. The temperature of first heat treatment for dehydration or dehydrogenation is higher than or equal to 400 °C and lower than or equal to 750 °C, preferably higher than or equal to 400 °C and lower than the strain point of the substrate. 25 Here, the substrate is introduced into an electric furnace which is one of heat treatment apparatuses, heat treatment is performed on the oxide semiconductor layer in a nitrogen atmosphere at 450 °C for one hour, and then, the oxide semiconductor layer is not exposed to the air so that entry of water and hydrogen into the oxide semiconductor layer is prevented; thus, an oxide semiconductor layer 332 is obtained (see FIG. 14A).

30 [0299]

Next, plasma treatment with a gas such as N_2O, N_2, or Ar is performed. With

this plasma treatment, water adsorbed to a surface of an exposed portion of the oxide semiconductor layer is removed. Alternatively, plasma treatment may be performed using a mixed gas of oxygen and argon.

[0300]

5 Next, an oxide insulating layer is formed over the gate insulating layer 322 and the oxide semiconductor layer 332 and a third photolithography process is performed. A resist mask is formed and selective etching is performed, so that the oxide insulating layer 366 is formed. Then, the resist mask is removed.

[0301]

10 In this embodiment, a silicon oxide film is formed to a thickness of 200 nm as the oxide insulating layer 366 by a sputtering method. The substrate temperature in film formation may be higher than or equal to room temperature and lower than or equal to 300 °C and in this embodiment, is 100 °C. The silicon oxide film can be formed by a sputtering method in a rare gas (typically, argon) atmosphere, an oxygen atmosphere, 15 or an atmosphere containing a rare gas (typically, argon) and oxygen. Further, a silicon oxide target or a silicon target can be used as a target. For example, the silicon oxide film can be formed using a silicon target by a sputtering method in an atmosphere containing oxygen and nitrogen. The oxide insulating layer 366 which is formed in contact with the oxide semiconductor layer in a region having a lower resistance is 20 formed using an inorganic insulating film that does not contain impurities such as moisture, a hydrogen ion, and OH^- and blocks entry of such impurities from the outside, typically, a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, or an aluminum oxynitride film.

[0302]

25 In that case, the oxide insulating layer 366 is preferably formed removing moisture in the treatment chamber. This is for preventing hydrogen, a hydroxyl group, and moisture from being contained in the oxide semiconductor layer 332 and the oxide insulating layer 366.

[0303]

30 In order to remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium

sublimation pump is preferably used. Further, an evacuation unit may be a turbo molecular pump provided with a cold trap. In the deposition chamber which is evacuated with the cryopump, a hydrogen atom, a compound containing a hydrogen atom, such as water (H_2O), and the like are removed, whereby the concentration of an
5 impurity in the oxide insulating layer 366 formed in the deposition chamber can be reduced.

[0304]

It is preferable to use a high-purity gas from which an impurity such as hydrogen, water, a hydroxyl group, or a hydride is removed to a concentration of several
10 ppm or several ppb, as a sputtering gas used when the oxide insulating layer 366 is formed.

[0305]

Next, second heat treatment (preferably 200 °C to 400 °C inclusive, for example, from 250 °C to 350 °C inclusive) may be performed in an inert gas
15 atmosphere or an oxygen gas atmosphere. For example, the second heat treatment is performed in a nitrogen atmosphere at 250 °C for one hour. With the second heat treatment, heat is applied while part of the oxide semiconductor layer (a channel formation region) is in contact with the oxide insulating layer 366.

[0306]

20 In this embodiment, heat treatment is further performed on the oxide semiconductor layer 332 over which the oxide insulating layer 366 is provided and part of the oxide semiconductor layer 332 is exposed, in an inert gas atmosphere such as nitrogen or under reduced pressure. By performing heat treatment in an inert gas atmosphere such as nitrogen or under reduced pressure, the resistance of regions of the
25 oxide semiconductor layer 332, which are not covered with the oxide insulating layer 366 and are thus exposed, can be reduced. For example, heat treatment is performed in a nitrogen atmosphere at 250 °C for one hour.

[0307]

With the heat treatment for the oxide semiconductor layer 332 provided with
30 the oxide insulating layer 366 in a nitrogen atmosphere, the resistance of the exposed regions of the oxide semiconductor layer 332 is reduced. Thus, an oxide

semiconductor layer 362 including regions with different resistances (indicated as shaded regions and white regions in FIG. 14B) are formed.

[0308]

Next, after a conductive film is formed over the gate insulating layer 322, the oxide semiconductor layer 362, and the oxide insulating layer 366, and a fourth photolithography process is performed. A resist mask is formed and selective etching is performed, so that a source electrode layer 365a and a drain electrode layer 365b are formed. Then, the resist mask is removed (see FIG. 14C).

[0309]

As the material of the source electrode layer 365a and the drain electrode layer 365b, there are an element selected from Al, Cr, Cu, Ta, Ti, Mo, or W; an alloy including any of the above elements; an alloy film containing a combination of any of these elements; and the like. Alternatively, a structure may be employed in which a high-melting-point metal layer of Cr, Ta, Ti, Mo, W, or the like is stacked over one of or both metal layers of Al, Cu, and the like. Still alternatively, when an Al material to which an element preventing generation of hillocks and whiskers in an Al film, such as Si, Ti, Ta, W, Mo, Cr, Nd, Sc, or Y, is added is used, heat resistance can be increased.

[0310]

The source electrode layer 365a and the drain electrode layer 365b may each have a single-layer structure or a layered structure of two or more layers. For example, a single-layer structure of an aluminum film including silicon, a two-layer structure in which a titanium film is stacked over an aluminum film, a three-layer structure in which a Ti film, an aluminum film, and a Ti film are stacked in the order presented, and the like can be given.

[0311]

Alternatively, the source electrode layer 365a and the drain electrode layer 365b may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), an alloy of indium oxide and tin oxide (In_2O_3-SnO_2, abbreviated to ITO), an alloy of indium oxide and zinc oxide (In_2O_3-ZnO), or any of the metal oxide materials containing silicon or silicon oxide can be used.

[0312]

Through the above steps, the oxide semiconductor layer which has been formed is decreased in resistance by the heat treatment for dehydration or dehydrogenation, and then part of the oxide semiconductor layer is selectively changed to be in an oxygen excess state. As a result, the channel formation region 363 which
5 overlaps with the gate electrode layer 361 becomes intrinsic, and a high-resistance source region 364a and a high-resistance drain region 364b which overlap with the source electrode layer 365a and the drain electrode layer 365b, respectively, are formed in a self-aligned manner. Thus, the thin film transistor 360 is formed.

[0313]

10 Note that by forming the high-resistance drain region 364b (and the high-resistance source region 364a) in the oxide semiconductor layer overlapping with the drain electrode layer 365b (and the source electrode layer 365a), reliability of the thin film transistor can be improved. Specifically, by forming the high-resistance drain region 364b, the structure can be obtained in which conductivities of the drain electrode
15 layer 365b, the high-resistance drain region 364b, and the channel formation region 363 vary. Therefore, in the case where the thin film transistor operates with the drain electrode layer 365b connected to a wiring for supplying a high power supply potential *VDD*, the high-resistance drain region serves as a buffer and a high electric field is not applied locally even if a high electric field is applied between the gate electrode layer
20 361 and the drain electrode layer 365b; thus, the withstand voltage of the thin film transistor can be increased.

[0314]

A protective insulating layer 323 is formed over the source electrode layer 365a, the drain electrode layer 365b, and the oxide insulating layer 366. In this embodiment,
25 the protective insulating layer 323 is formed using a silicon nitride film (see FIG. 14D).

[0315]

Note that an oxide insulating layer may be further formed over the source electrode layer 365a, the drain electrode layer 365b, and the oxide insulating layer 366, and the protective insulating layer 323 may be stacked over the oxide insulating layer.

30 [0316]

This embodiment can be implemented in appropriate combination with any of the other embodiments and examples.

[0317]

Thus, with a thin film transistor including an oxide semiconductor layer, a large touch panel having stable electric characteristics and high reliability can be provided.

[0318]

5 (Embodiment 8)

In this embodiment, another example of a thin film transistor which can be applied to the display panel disclosed in this specification will be described. A thin film transistor 350 in this embodiment can be used as the thin film transistor formed using an oxide semiconductor layer including a channel formation region in any of the 10 above embodiments (e.g., the transistors 201, 205, 206, and 301 in Embodiment 1, and the transistors 503 and 540 in Embodiments 3 and 4). The same portions as those in the above embodiments and portions having functions similar to those of the portions in the above embodiments and steps similar to those in the above embodiments may be handled as in the above embodiments, and repeated description is omitted. In addition, 15 detailed description of the same portions is also omitted.

[0319]

An embodiment of a thin film transistor and a manufacturing method of the thin film transistor of this embodiment is described with reference to FIGS. 15A to 15D.

[0320]

20 Although description is given using a single-gate thin film transistor as a thin film transistor 350, a multi-gate thin film transistor including a plurality of channel formation regions may be formed as needed.

[0321]

A process of manufacturing the thin film transistor 350 over a substrate 340 is 25 described below with reference to FIGS. 15A to 15D.

[0322]

First, after a conductive film is formed over the substrate 340 having an insulating surface, a gate electrode layer 351 is formed in a first photolithography process. In this embodiment, a tungsten film is formed as the gate electrode layer 351 30 to a thickness of 150 nm.

[0323]

Then, a gate insulating layer 342 is formed over the gate electrode layer 351.

In this embodiment, a silicon oxynitride layer is formed as the gate insulating layer 342 to a thickness of 100 nm by a plasma CVD method.

[0324]

Next, after a conductive film is formed over the gate insulating layer 342, and a second photolithography process is performed. A resist mask is formed and selective etching is performed, so that a source electrode layer 355a and a drain electrode layer 355b are formed. Then, the resist mask is removed (see FIG. 15A).

[0325]

Then, an oxide semiconductor layer 345 is formed (see FIG. 15B). In this embodiment, the oxide semiconductor layer 345 is formed by a sputtering method with the use of an In-Ga-Zn-O-based metal oxide target. The oxide semiconductor layer 345 is processed into an island-shaped oxide semiconductor layer in a third photolithography process.

[0326]

In that case, the oxide semiconductor layer 345 is preferably formed removing moisture in the treatment chamber. This is for preventing hydrogen, a hydroxyl group, and moisture from being contained in the oxide semiconductor layer 345.

[0327]

In order to remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo molecular pump provided with a cold trap. In the deposition chamber which is evacuated with the cryopump, a hydrogen atom, a compound containing a hydrogen atom, such as water (H_2O), and the like are removed, whereby the concentration of an impurity in the oxide semiconductor layer 345 formed in the deposition chamber can be reduced.

[0328]

It is preferable to use a high-purity gas from which an impurity such as hydrogen, water, a hydroxyl group, or a hydride is removed to a concentration of several ppm or several ppb, as a sputtering gas used when the oxide semiconductor layer 345 is formed.

[0329]

Next, the oxide semiconductor layer is subjected to dehydration or dehydrogenation. The temperature of first heat treatment for dehydration or dehydrogenation is higher than or equal to 400 °C and lower than or equal to 750 °C, preferably higher than or equal to 400 °C and lower than the strain point of the substrate.
5 Here, the substrate is introduced into an electric furnace which is one of heat treatment apparatuses, heat treatment is performed on the oxide semiconductor layer in a nitrogen atmosphere at 450 °C for one hour, and then, the oxide semiconductor layer is not exposed to the air so that entry of water and hydrogen into the oxide semiconductor layer is prevented; thus, an oxide semiconductor layer 346 is obtained (see FIG. 15C).
10 [0330]

As the first heat treatment, GRTA may be performed as follows. The substrate is transferred and put in an inert gas which has been heated to a high temperature of 650 °C to 700 °C, heated for several minutes, and transferred and taken out of the inert gas which has been heated to a high temperature. GRTA enables
15 high-temperature heat treatment in a short time.

[0331]

Then, an oxide insulating layer 356 which serves as a protective insulating film and is in contact with the oxide semiconductor layer 346 is formed.

[0332]

20 The oxide insulating layer 356 can be formed to a thickness of larger than or equal to 1 nm by a sputtering method or the like as appropriate, which is a method with which an impurity such as water or hydrogen does not enter the oxide insulating layer 356. When hydrogen is contained in the oxide insulating layer 356, entry of the hydrogen to the oxide semiconductor layer or extraction of oxygen in the oxide
25 semiconductor layer by the hydrogen is caused, whereby a back channel of the oxide semiconductor layer comes to have a lower resistance (to be n-type) and thus a parasitic channel might be formed. Therefore, it is important that a formation method in which hydrogen is not used is employed so that the oxide insulating layer 356 is formed containing as little hydrogen as possible.

30 [0333]

In this embodiment, a silicon oxide film is formed to a thickness of 200 nm as

the oxide insulating layer 356 by a sputtering method. The substrate temperature in film formation may be higher than or equal to room temperature and lower than or equal to 300 °C and in this embodiment, is 100 °C. The silicon oxide film can be formed by a sputtering method in a rare gas (typically, argon) atmosphere, an oxygen atmosphere,
5 or an atmosphere containing a rare gas (typically, argon) and oxygen. Further, a silicon oxide target or a silicon target can be used as a target. For example, the silicon oxide film can be formed using a silicon target by a sputtering method in an atmosphere containing oxygen and nitrogen. The oxide insulating layer 356 which is formed in contact with the oxide semiconductor layer in a region having a lower resistance is
10 formed using an inorganic insulating film that does not contain impurities such as moisture, a hydrogen ion, and OH^- and blocks entry of such impurities from the outside, typically, a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, or an aluminum oxynitride film.

[0334]

15 In that case, the oxide insulating layer 356 is preferably formed removing moisture in the treatment chamber. This is for preventing hydrogen, a hydroxyl group, and moisture from being contained in the oxide semiconductor layer 352 and the oxide insulating layer 356.

[0335]

20 In order to remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo molecular pump provided with a cold trap. In the deposition chamber which is evacuated with the cryopump, a hydrogen atom, a compound containing a hydrogen
25 atom, such as water (H_2O), and the like are removed, whereby the concentration of an impurity in the oxide insulating layer 356 formed in the deposition chamber can be reduced.

[0336]

It is preferable to use a high-purity gas from which an impurity such as
30 hydrogen, water, a hydroxyl group, or a hydride is removed to a concentration of several ppm or several ppb, as a sputtering gas used when the oxide insulating layer 356 is

formed.

[0337]

Next, second heat treatment (preferably 200 °C to 400 °C inclusive, for example, from 250 °C to 350 °C inclusive) is performed in an inert gas atmosphere or 5 an oxygen gas atmosphere. For example, the second heat treatment is performed in a nitrogen atmosphere at 250 °C for one hour. With the second heat treatment, heat is applied while part of the oxide semiconductor layer (a channel formation region) is in contact with the oxide insulating layer 356.

[0338]

10 Through the above steps, the formed oxide semiconductor layer is decreased in resistance by the heat treatment for dehydration or dehydrogenation, and then part of the oxide semiconductor layer is selectively changed to be in an oxygen excess state. As a result, the i-type oxide semiconductor layer 352 is formed. Through the above steps, the thin film transistor 350 is formed.

15 [0339]

A protective insulating layer may be additionally formed over the oxide insulating layer 356. For example, a silicon nitride film is formed by an RF sputtering method. In this embodiment, as the protective insulating layer, a protective insulating layer 343 is formed using a silicon nitride film (see FIG. 15D).

20 [0340]

Note that a planarization insulating layer for planarization may be provided over the protective insulating layer 343.

[0341]

This embodiment can be implemented in appropriate combination with any of 25 the other embodiments and examples.

[0342]

Thus, with a thin film transistor including an oxide semiconductor layer, a large touch panel having stable electric characteristics and high reliability can be provided.

[0343]

30 (Embodiment 9)

In this embodiment, another example of a thin film transistor which can be

applied to the display panel disclosed in this specification will be described. A thin film transistor 380 in this embodiment can be used as the thin film transistor formed using an oxide semiconductor layer including a channel formation region in any of the above embodiments (e.g., the transistors 201, 205, 206, and 301 in Embodiment 1, and
5 the transistors 503 and 540 in Embodiments 3 and 4).

[0344]

In this embodiment, an example which is partly different from Embodiment 6 in the manufacturing process of a thin film transistor will be described with reference to FIG. 16. Since FIG. 16 is the same as FIGS. 13A to 13E except for part of the steps,
10 common reference numerals are used for the same portions, and detailed description of the same portions is omitted.

[0345]

According to Embodiment 6, a gate electrode layer 381 is formed over a substrate 370, and a first gate insulating layer 372a and a second gate insulating layer
15 372b are stacked thereover. In this embodiment, a gate insulating layer has a two layer structure in which a nitride insulating layer and an oxide insulating layer are used as the first gate insulating layer 372a and the second gate insulating layer 372b, respectively.

[0346]

As the oxide insulating layer, a silicon oxide layer, a silicon oxynitride layer, an
20 aluminum oxide layer, an aluminum oxynitride layer, a hafnium oxide layer, or the like may be used. As the nitride insulating layer, a silicon nitride layer, a silicon nitride oxide layer, an aluminum nitride layer, an aluminum nitride oxide layer, or the like may be used.

[0347]

25 In this embodiment, the gate insulating layer may have a structure where a silicon nitride layer and a silicon oxide layer are stacked over the gate electrode layer 381. A silicon nitride layer (SiN_y ($y > 0$)) with a thickness of 50 nm to 200 nm inclusive (50 nm in this embodiment) is formed by a sputtering method as a first gate insulating layer 372a and a silicon oxide layer (SiO_x ($x > 0$)) with a thickness of 5 nm to
30 300 nm inclusive (100 nm in this embodiment) is stacked as a second gate insulating layer 372b over the first gate insulating layer 372a; thus, the gate insulating layer with a

thickness of 150 nm is formed.

[0348]

Next, the oxide semiconductor layer is formed and then processed into an island-shaped oxide semiconductor layer in a photolithography process. In this 5 embodiment, the oxide semiconductor layer is formed by a sputtering method with the use of an In-Ga-Zn-O-based metal oxide target.

[0349]

In that case, the oxide semiconductor layer is preferably formed removing moisture in the treatment chamber. This is for preventing hydrogen, a hydroxyl group, 10 and moisture from being contained in the oxide semiconductor layer.

[0350]

In order to remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo 15 molecular pump provided with a cold trap. In the deposition chamber which is evacuated with the cryopump, a hydrogen atom, a compound containing a hydrogen atom, such as water (H_2O), and the like are removed, whereby the concentration of an impurity in the oxide semiconductor layer formed in the deposition chamber can be reduced.

20 [0351]

It is preferable to use a high-purity gas from which an impurity such as hydrogen, water, a hydroxyl group, or a hydride is removed to a concentration of several ppm or several ppb, as a sputtering gas used when the oxide semiconductor layer is formed.

25 [0352]

Next, the oxide semiconductor layer is subjected to dehydration or dehydrogenation. The temperature of first heat treatment for dehydration or dehydrogenation is higher than or equal to 400 °C and lower than or equal to 750 °C, preferably higher than or equal to 425 °C. Note that in the case of the temperature that 30 is 425 °C or more, the heat treatment time may be one hour or less, whereas in the case of the temperature less than 425 °C, the heat treatment time is longer than one hour.

Here, the substrate is introduced into an electric furnace which is one of heat treatment apparatuses, heat treatment is performed on the oxide semiconductor layer in a nitrogen atmosphere, and then, the oxide semiconductor layer is not exposed to the air so that entry of water and hydrogen into the oxide semiconductor layer is prevented. Thus, the oxide semiconductor layer is obtained. After that, a high-purity oxygen gas, a high-purity N_2O gas, or an ultra-dry air (with a dew point of –40 °C or less, preferably –60 °C or less) is introduced into the same furnace and cooling is performed. It is preferable that water, hydrogen, and the like be not contained in the oxygen gas or the N_2O gas. Alternatively, the purity of the oxygen gas or the N_2O gas which is introduced into the heat treatment apparatus is preferably 6N (99.9999 %) or more, more preferably 7N (99.99999 %) or more (i.e., the impurity concentration of the oxygen gas or the N_2O gas is preferably 1 ppm or lower, more preferably 0.1 ppm or lower).

[0353]

Note that the heat treatment apparatus is not limited to the electric furnace, and for example, may be an RTA (rapid thermal annealing) apparatus such as a GRTA (gas rapid thermal annealing) apparatus or an LRTA (lamp rapid thermal annealing) apparatus. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (electromagnetic waves) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. An LRTA apparatus may be provided with not only a lamp but also a device for heating an object to be processed by heat conduction or heat radiation from a heater such as a resistance heater. GRTA is a method for performing heat treatment using a high-temperature gas. As the gas, an inert gas which does not react with an object to be processed with heat treatment, such as nitrogen or a rare gas such as argon is used. Alternatively, the heat treatment may be performed at 600 °C to 750 °C for several minutes by an RTA method.

[0354]

Moreover, after the first heat treatment for dehydration or dehydrogenation, heat treatment may be performed at from 200 °C to 400 °C, preferably from 200 °C to 300 °C, in an oxygen gas atmosphere or a N_2O gas atmosphere.

[0355]

The first heat treatment of the oxide semiconductor layer may be performed before processing the oxide semiconductor layer into the island-like oxide semiconductor layer. In that case, after the first heat treatment, the substrate is taken
5 out of the heating apparatus and a photolithography step is performed.

[0356]

Through the above process, an entire region of the oxide semiconductor layer is made to be in an oxygen excess state; thus, the oxide semiconductor layer has higher resistance, that is, the oxide semiconductor layer becomes i-type. Accordingly, an
10 oxide semiconductor layer 382 whose entire region is i-type is formed.

[0357]

Next, a conductive film is formed over the oxide semiconductor layer 382, and a photolithography process is performed. A resist mask is formed over the conductive film and the conductive film is etched selectively, whereby a source electrode layer
15 385a and a drain electrode layer 385b are formed. Then, an oxide insulating layer 386 is formed over the second gate insulating layer 372b, the oxide semiconductor layer 382, the source electrode layer 385a, and the drain electrode layer 385b by a sputtering method.

[0358]

20 In that case, the oxide insulating layer 386 is preferably formed removing moisture in the treatment chamber. This is for preventing hydrogen, a hydroxyl group, and moisture from being contained in the oxide semiconductor layer 382 and the oxide insulating layer 386.

[0359]

25 In order to remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo molecular pump provided with a cold trap. In the deposition chamber which is evacuated with the cryopump, a hydrogen atom, a compound containing a hydrogen
30 atom, such as water (H_2O), and the like are removed, whereby the concentration of an impurity in the oxide insulating layer 386 formed in the deposition chamber can be reduced.

[0360]

It is preferable to use a high-purity gas from which an impurity such as hydrogen, water, a hydroxyl group, or a hydride is removed to a concentration of several ppm or several ppb, as a sputtering gas used when the oxide insulating layer 386 is formed.

[0361]

Through the above steps, a thin film transistor 380 can be formed.

[0362]

Next, in order to reduce variation in electric characteristics of the thin film transistors, heat treatment (preferably at 150 °C or higher and lower than 350 °C) may be performed in an inert gas atmosphere such as a nitrogen gas atmosphere. For example, the heat treatment is performed in a nitrogen atmosphere at 250 °C for one hour.

[0363]

A protective insulating layer 373 is formed over the oxide insulating layer 386. In this embodiment, the protective insulating layer 373 is formed to a thickness of 100 nm with the use of a silicon nitride film by a sputtering method.

[0364]

The protective insulating layer 373 and the first gate insulating layer 372a each formed using a nitride insulating layer do not contain impurities such as moisture, hydrogen, a hydride, and hydroxide and has an effect of blocking entry of these from the outside.

[0365]

Therefore, in a manufacturing process after formation of the protective insulating layer 373, entry of an impurity such as moisture from the outside can be prevented. Further, even after a device is completed as a semiconductor device having a display panel, such as a liquid crystal display device, entry of an impurity such as moisture from the outside can be prevented in the long term; therefore, long-term reliability of the device can be achieved.

[0366]

Further, part of the second gate insulating layer 372b between the first gate

insulating layer 372a and the protective insulating layer 373 formed using a nitride insulating layer may be removed so that the protective insulating layer 373 and the first gate insulating layer 372a are in contact with each other.

[0367]

5 Accordingly, impurities such as moisture, hydrogen, a hydride, and hydroxide in the oxide semiconductor layer are reduced as much as possible and entry of such impurities is prevented, so that the concentration of impurities in the oxide semiconductor layer can be maintained to be low.

[0368]

10 Note that a planarization insulating layer for planarization may be provided over the protective insulating layer 373.

[0369]

This embodiment can be implemented in appropriate combination with any of the other embodiments and examples.

15 [0370]

Thus, with a thin film transistor including an oxide semiconductor layer, a large display device having stable electric characteristics and high reliability can be provided.

[0371]

(Embodiment 10)

20 In this embodiment, another example of a thin film transistor which can be applied to a display panel, which is disclosed in this specification, will be described. A thin film transistor described in this embodiment can be applied to the thin film transistor in any of Embodiments 1 to 9.

[0372]

25 In this embodiment, an example of using a conductive material having a light-transmitting property for a gate electrode layer, a source electrode layer, and a drain electrode layer will be described. Therefore, part of this embodiment can be performed in a manner similar to that of the above embodiments, and repetitive description of the same portions as or portions having functions similar to those in the 30 above embodiments and steps for manufacturing such portions will be omitted. In addition, detailed description of the same portions is not repeated.

[0373]

For example, materials of the gate electrode layer, the source electrode layer, and the drain electrode layer can be a conductive material that transmits visible light, and any of the following metal oxides can be applied for example: an In-Sn-O-based metal oxide, an In-Sn-Zn-O-based metal oxide; an In-Al-Zn-O-based metal oxide; a Sn-Ga-Zn-O-based metal oxide; an Al-Ga-Zn-O-based metal oxide; a Sn-Al-Zn-O-based metal oxide; an In-Zn-O-based metal oxide; a Sn-Zn-O-based metal oxide; an Al-Zn-O-based metal oxide; an In-O-based metal oxide; a Sn-O-based metal oxide; and a Zn-O-based metal oxide. The thickness thereof can be set in the range of greater than or equal to 50 nm and less than or equal to 300 nm, as appropriate. As a film formation method of the metal oxide used for the gate electrode layer, the source electrode layer, and the drain electrode layer, a sputtering method, a vacuum evaporation method (an electron beam evaporation method or the like), an arc discharge ion plating method, or a spray method is used. When a sputtering method is employed, film formation may be performed using a target including SiO_2 at a concentration of greater than or equal to 2 wt% and less than or equal to 10 wt%.

[0374]

Note that the unit of the percentage of components in the conductive film that transmits visible light is atomic percent, and the percentage of components is evaluated by analysis using an electron probe X-ray microanalyzer (EPMA).

[0375]

In a pixel provided with a thin film transistor, when a pixel electrode layer, another electrode layer (such as a capacitor electrode layer), or another wiring layer (such as a capacitor wiring layer) is formed using the conductive film that transmits visible light, a display device having high aperture ratio can be realized. Needless to say, it is preferable that a gate insulating layer, an oxide insulating layer, a protective insulating layer, and a planarization insulating layer in the pixel be also each formed using a film that transmits visible light.

[0376]

In this specification, a film that transmits visible light means a film having such a thickness as to have transmittance of visible light between 75 % and 100 %. In the case where the film has conductivity, the film is also referred to as a transparent

conductive film. Further, a conductive film which is semi-transmissive with respect to visible light may be used for metal oxide applied to the gate electrode layer, the source electrode layer, the drain electrode layer, the pixel electrode layer, another electrode layer, or another wiring layer. The conductive film which is semi-transmissive with respect to visible light indicates a film having transmittance of visible light between 50 % and 75 %.

[0377]

When a thin film transistor has a light-transmitting property, the aperture ratio can be increased because light is transmitted even when the thin film transistor is provided so as to overlap with a display region or a photosensor and thus display or detection of light is not interfered. In addition, by using a film having a light-transmitting property for components of a thin film transistor, a high aperture ratio can be achieved even when one pixel is divided into a plurality of sub-pixels in order to realize a wide viewing angle. That is, a high aperture ratio can be maintained even when a group of high-density thin film transistors is provided, so that a sufficient area of a display region can be secured. For example, in the case where one pixel includes two to four sub-pixels, an aperture ratio can be improved because the thin film transistor has a light-transmitting property. Further, when a storage capacitor is formed using the same steps and the same materials as the component of the thin film transistor, the storage capacitor can also have a light-transmitting property; therefore, the aperture ratio can be further increased.

[0378]

This embodiment can be implemented in appropriate combination with any of the other embodiments and examples.

[0379]

(Embodiment 11)

In this embodiment, an example of a thin film transistor which can be applied to the display panel disclosed in this specification will be described. A thin film transistor 650 in this embodiment can be used as the thin film transistor formed using an oxide semiconductor layer including a channel formation region in any of the above embodiments (e.g., the transistors 201, 205, 206, and 301 in Embodiment 1, and the transistors 503 and 540 in Embodiments 3 and 4).

[0380]

In this embodiment, an example in which an oxide semiconductor layer is surrounded by a nitride insulating film when seen in a cross section thereof will be shown with reference to FIG. 17. Since FIG. 17 is the same as FIGS. 12A to 12E except that there is differences in the top surface shape and the position of the end portion of an oxide insulating layer and in the structure of a gate insulating layer, common reference numerals are used for the same portions, and detailed description of the same portions is omitted.

[0381]

The thin film transistor 650 illustrated in FIG. 17 is a bottom gate thin film transistor, and includes, over a substrate 394 having an insulating surface, a gate electrode layer 391, a gate insulating layer 652a which is formed using a nitride insulating layer, a gate insulating layer 652b which is formed using an oxide insulating layer, an oxide semiconductor layer 392, a source electrode layer 395a, and a drain electrode layer 395b. Further, an oxide insulating layer 656 which covers the thin film transistor 650 and is stacked over the oxide semiconductor layer 392 is provided. Further, a protective insulating layer 653 which is formed using a nitride insulating layer is provided over the oxide insulating layer 656. The protective insulating layer 653 is in contact with the gate insulating layer 652a which is formed using a nitride insulating layer.

[0382]

In the thin film transistor 650 in this embodiment, the gate insulating layer has a stacked structure in which the nitride insulating layer and the oxide insulating layer are stacked over the gate electrode layer. Further, before the protective insulating layer 653 which is formed using a nitride insulating layer is formed, the oxide insulating layer 656 and the gate insulating layer 652b are selectively removed to expose the gate insulating layer 652a which is formed using a nitride insulating layer.

[0383]

At least the top surfaces of the oxide insulating layer 656 and the gate insulating layer 652b are larger than the top surface of the oxide semiconductor layer 392, and the top surface shapes of the oxide insulating layer 656 and the gate insulating layer 652b preferably covers the thin film transistor 650.

[0384]

Further, the protective insulating layer 653 which is formed using a nitride insulating layer covers the top surface of the oxide insulating layer 656 and the side surfaces of the oxide insulating layer 656 and the gate insulating layer 652b, and is in contact with the gate insulating layer 652a which is formed using a nitride insulating layer.

[0385]

For the protective insulating layer 653 and the gate insulating layer 652a which are each formed using a nitride insulating layer, an inorganic insulating film which does not contain impurities such as moisture, a hydrogen ion, and OH^- and blocks entry of the impurities from the outside is used: for example, a silicon nitride film, a silicon oxynitride film, an aluminum nitride film, or an aluminum oxynitride film obtained with a sputtering method or a plasma CVD method is used.

[0386]

In this embodiment, as the protective insulating layer 653 which is formed using a nitride insulating layer, a silicon nitride layer having a thickness of 100 nm is provided with an RF sputtering method so as to cover the bottom surface, the top surface, and the side surface of the oxide semiconductor layer 392.

[0387]

With the structure illustrated in FIG. 17, an impurity such as hydrogen, moisture, a hydroxyl group, or a hydride in the oxide semiconductor layer is reduced due to the gate insulating layer 652b and the oxide insulating layer 656 which are provided to surround and be in contact with the oxide semiconductor layer, and entry of moisture from the outside in a manufacturing process after formation of the protective insulating layer 653 can be prevented because the oxide semiconductor layer is surrounded by the gate insulating layer 652a and the protective insulating layer 653 which are each formed using a nitride insulating layer. Further, even after a device is completed as a display panel, such as a display device, entry of an impurity such as moisture from the outside can be prevented in the long term; therefore, long-term reliability of the device can be achieved.

[0388]

In this embodiment, one thin film transistor is covered with a nitride insulating

layer; however, an embodiment of the present invention is not limited to this structure. Alternatively, a plurality of thin film transistors may be covered with a nitride insulating layer, or a plurality of thin film transistors in a pixel portion may be collectively covered with a nitride insulating layer. A region where the protective insulating layer 653 and
5 the gate insulating layer 652a are in contact with each other may be formed so that at least the pixel portion of the active matrix substrate is surrounded.

[0389]

This embodiment can be implemented in appropriate combination with any of the other embodiments and examples.

10 [Example 1]

[0390]

In this example, arrangement of a panel and light sources in a display panel according to an embodiment of the present invention will be described. FIG. 8 illustrates an example of a perspective view of a structure of a display panel according
15 to an embodiment of the present invention. The display panel illustrated in FIG. 8 is provided with a panel 1601 where pixels each including a liquid crystal element, a photodiode, a thin film transistor, and the like are formed between a pair of substrates; a first diffusing plate 1602; a prism sheet 1603; a second diffusing plate 1604; a light guide plate 1605; a reflection plate 1606; a backlight 1608 including a plurality of light
20 sources 1607; and a circuit substrate 1609.

[0391]

The panel 1601, the first diffusing plate 1602, the prism sheet 1603, the second diffusing plate 1604, the light guide plate 1605, and the reflection plate 1606 are stacked in this order. The light sources 1607 are provided in an end portion of the light guide
25 plate 1605. Light from the light sources 1607 is diffused inside the light guide plate 1605, and passes through the first diffusing plate 1602, the prism sheet 1603, and the second diffusing plate 1604. Thus, the panel 1601 is uniformly irradiated with light from the counter substrate side (one side of the liquid crystal panel 1601, on which the light guide plate 1605 and the like are provided).

30 [0392]

Although the first diffusing plate 1602 and the second diffusing plate 1604 are used in this embodiment, the number of diffusing plates is not limited thereto. The

number of diffusing plates may be one, or may be three or more. The diffusing plate is acceptable as long as it is provided between the light guide plate 1605 and the panel 1601. Therefore, a diffusing plate may be provided only between the panel 1601 and the prism sheet 1603, or may be provided only between the light guide plate 1605 and
5 the prism sheet 1603.

[0393]

Further, the cross section of the prism sheet 1603 is not limited to a sawtooth shape illustrated in FIG. 8. The prism sheet 1603 may have a shape with which light from the light guide plate 1605 can be concentrated on the panel 1601 side.

10 [0394]

The circuit substrate 1609 is provided with a circuit which generates various kinds of signals inputted to the panel 1601, a circuit which processes the signals, a circuit which processes various signals outputted from the panel 1601, or the like. In FIG. 8, the circuit substrate 1609 and the panel 1601 are connected to each other via a
15 flexible printed circuit (FPC) 1611. Note that the circuit may be connected to the panel 1601 with a chip on glass (COG) method, or part of the circuit may be connected to the FPC 1611 with a chip on film (COF) method.

[0395]

FIG. 8 shows an example in which the circuit substrate 1609 is provided with
20 control circuits which control driving of the light sources 1607, where the control circuits and the light sources 1607 are connected via the FPC 1610. However, the above control circuits may be formed in the panel 1601; in this case, the panel 1601 and the light sources 1607 are connected via an FPC or the like.

[0396]

25 Although FIG. 8 shows an example of an edge-light type light source in which the light sources 1607 are disposed in an end portion of the panel 1601, a touch panel according to an embodiment of the present invention may be a direct-below type that includes the light sources 1607 disposed directly below the panel 1601.

[0397]

30 When a finger 1612, which is an object, gets close to the panel 1601 from the TFT substrate side (the side over the panel 1601, which is opposite to the backlight 1608), light from the backlight 1608 passes through the panel 1601, and part of the light

is reflected by the finger 1612 and enters the panel 1601 again. Image data of the finger 1612, which is the object, can be obtained by obtaining image data with the photosensors 106 in the pixels 104.

[0398]

5 This embodiment can be implemented in appropriate combination with any of the other embodiments and the other example.

[Example 2]

[0399]

The display panel according to an embodiment of the present invention can 10 input data by detecting motion of a contactless object. Therefore, an electronic device having the display panel according to an embodiment of the present invention can be equipped with a more highly functional application due to the display panel added as a component. The display panel according to an embodiment of the present invention can be included in display devices, laptop personal computers, and image reproducing 15 devices provided with recording media (typically devices which reproduce the content of recording media such as DVDs (digital versatile discs) and include displays for displaying the reproduced images). In addition to the above examples, as an electronic device which can include the display panel according to an embodiment of the present invention, mobile phones, portable game consoles, portable information terminals, 20 e-book readers, video cameras, digital still cameras, goggle-type displays (head mounted displays), navigation systems, audio reproducing devices (e.g., car audio components and digital audio players), copiers, facsimiles, printers, multifunction printers, automated teller machines (ATM), vending machines, and the like can be given. Specific examples of these electronic devices are illustrated in FIGS. 9A to 9D.

25 [0400]

FIG. 9A illustrates a display device that includes a housing 5001, a display portion 5002, a support 5003, and the like. The display panel according to an embodiment of the present invention can be used for the display portion 5002. The display panel according to an embodiment of the present invention used for the display 30 portion 5002 makes it possible to provide a display device which is capable of capturing image shooting data with high resolution and is equipped with more highly functional applications. Note that a display device includes all display devices for displaying

information, such as display devices for personal computers, for receiving television broadcasts, and for displaying advertisements.

[0401]

FIG. 9B illustrates a portable information terminal that includes a housing 5101, 5 a display portion 5102, a switch 5103, operation keys 5104, an infrared port 5105, and the like. The display panel according to an embodiment of the present invention can be used for the display portion 5102. The display panel according to an embodiment of the present invention used for the display portion 5102 makes it possible to provide a portable information terminal which is capable of capturing image shooting data with 10 high resolution and is equipped with more highly functional applications.

[0402]

FIG. 9C illustrates an automated teller machine that includes a housing 5201, a display portion 5202, a coin slot 5203, a paper money slot 5204, a card slot 5205, a passbook slot 5206, and the like. The display panel according to an embodiment of the 15 present invention can be used for the display portion 5202. The display panel according to an embodiment of the present invention used for the display portion 5202 makes it possible to provide an automated teller machine which is capable of capturing image shooting data with high resolution and is equipped with more highly functional applications. An automated teller machine using the display panel according to an 20 embodiment of the present invention can read, with higher precision, biological information to be used for biometric authentication, such as a fingerprint, a face, a hand print, a palm print, a hand vein pattern, or an iris. Therefore, a false non-match rate which is caused by false recognition of a person to be identified as a different person and a false acceptance rate which is caused by false recognition of a different person as 25 a person to be identified can be suppressed.

[0403]

FIG. 9D illustrates a portable game console that includes a housing 5301, a housing 5302, a display portion 5303, a display portion 5304, a microphone 5305, a speaker 5306, an operation key 5307, a stylus 5308, and the like. The display panel 30 according to an embodiment of the present invention can be used for the display portion 5303 or the display portion 5304. The display panel according to an embodiment of the present invention used for the display portion 5303 or the display portion 5304

makes it possible to provide a portable game console which is capable of capturing image shooting data with high resolution and is equipped with more highly functional applications. Note that although the portable game console illustrated in FIG. 9D includes two display portions, the display portions 5303 and 5304, the number of
5 display portions included in the portable game console is not limited thereto.

[0404]

This embodiment can be implemented in appropriate combination with any of the other embodiments and the other example.

10 This application is based on Japanese Patent Application serial no. 2009-255452 filed with Japan Patent Office on November 6, 2009, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A display device comprising:

a display panel including pixels arranged in matrix; and

an image processing portion operationally connected to the display panel,

5 wherein each of the pixels includes a photosensor and a transistor including an oxide semiconductor layer,

wherein the photosensor is configured to detect a shadow of an object projected on the display panel, and

wherein the image processing portion is configured to detect a position of the

10 object using data of the shadow of the object, which is obtained by the photosensor.

2. The display device according to claim 1,

wherein the image processing portion is configured to detect motion of the object by comparing successive data of the position of the object.

15

3. The display device according to claim 1,

wherein each of the pixels further includes a display element.

4. A display device comprising:

20 a display panel including pixels arranged in matrix; and

an image processing portion operationally connected to the display panel,

wherein each of the pixels includes a photosensor and a transistor including an oxide semiconductor layer,

wherein the photosensor is configured to detect a shadow of an object projected

25 on the display panel,

wherein the image processing portion is configured to detect a position of the object using data of the shadow of the object, which is obtained by the photosensor, and

wherein the image processing portion is configured to recognize a region including the largest number of pixels detecting the shadow among a plurality of

30 regions obtained by dividing the display panel, as positional data of the object.

5. The display device according to claim 4,

wherein the image processing portion is configured to detect motion of the object by comparing successive positional data of the object.

6. The display device according to claim 4,

5 wherein each of the pixels further includes a display element.

7. A display device comprising:

a display panel including pixels arranged in matrix, the pixels including first pixels and second pixels; and

10 an image processing portion operationally connected to the display panel,

wherein each of the first pixels includes a first photosensor and a first transistor including an oxide semiconductor layer,

wherein each of the second pixels includes a second photosensor and a second transistor including an oxide semiconductor layer,

15 wherein the first photosensor is configured to detect a shadow of an object projected on the display panel,

wherein the second photosensor is configured to detect a presence of the object which is in contact with the display panel, and

wherein the image processing portion is configured to detect a position of the

20 object using data of the shadow of the object, which is obtained by the first photosensor.

8. The display device according to claim 7,

wherein the image processing portion is configured to detect motion of the object by comparing successive data of the position of the object.

25

9. The display device according to claim 7,

wherein the number of the second photosensors is larger than that of the first photosensors.

30 10. The display device according to claim 7,

wherein the second pixels are provided on a periphery of each of the first pixels.

11. A display device comprising:

a display panel including pixels arranged in matrix, the pixels including first pixels and second pixels; and

5 an image processing portion operationally connected to the display panel,

wherein each of the first pixels includes a first photosensor and a first transistor including an oxide semiconductor layer,

wherein each of the second pixels includes a second photosensor and a second transistor including an oxide semiconductor layer,

10 wherein the first photosensor is configured to detect a shadow of an object projected on the display panel,

wherein the second photosensor is configured to detect a presence of the object which is in contact with the display panel,

wherein the image processing portion is configured to detect a position of the 15 object using data of the shadow of the object, which is obtained by the first photosensor, and

wherein the image processing portion is configured to recognize a region including the largest number of pixels detecting the shadow among a plurality of regions obtained by dividing the display panel, as positional data of the object.

20

12. The display device according to claim 11,

wherein the image processing portion is configured to detect motion of the object by comparing successive positional data of the object.

25 13. The display device according to claim 11,

wherein the number of the second photosensors is larger than that of the first photosensors.

14. The display device according to claim 11,

30 wherein the second pixels are provided on a periphery of each of the first pixels.

15. A display device comprising a display panel including pixels arranged in matrix, the pixels including first pixels and second pixels,

wherein each of the first pixels includes an infrared light sensor and a first transistor including an oxide semiconductor layer,

5 wherein each of the second pixels includes a visible light sensor and a second transistor including an oxide semiconductor layer,

wherein the infrared light sensor is configured to detect light emitted from the display panel and reflected by an object when the object is not in contact with the display panel, and

10 wherein the visible light sensor is configured to detect light emitted from the display panel and reflected by the object when the object is in contact with the display panel.

16. The display device according to claim 15,

15 wherein the number of the second pixels are larger than that of the first pixels.

17. The display device according to claim 15,

wherein the second pixels are provided on a periphery of each of the first pixels.

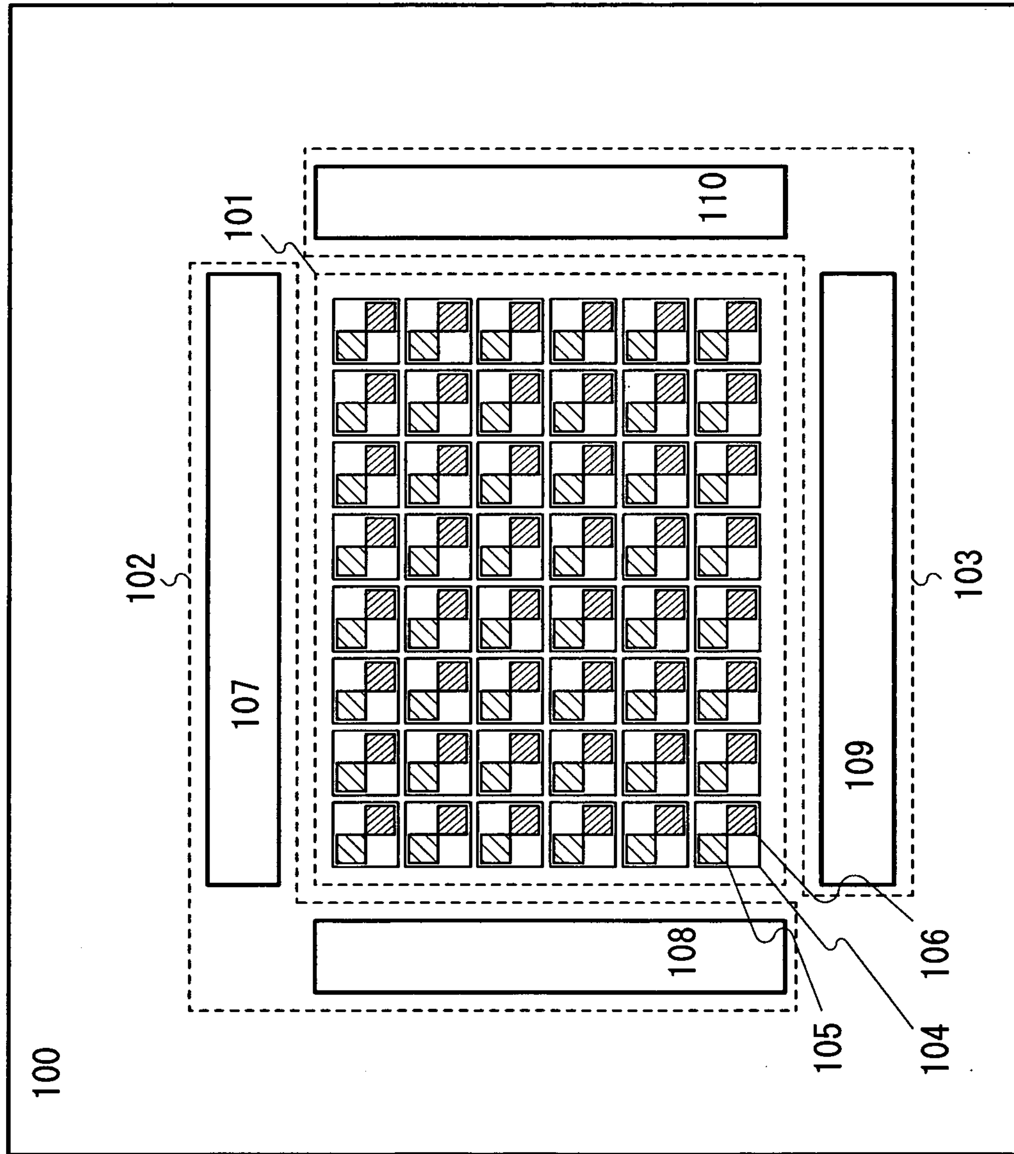


FIG. 1

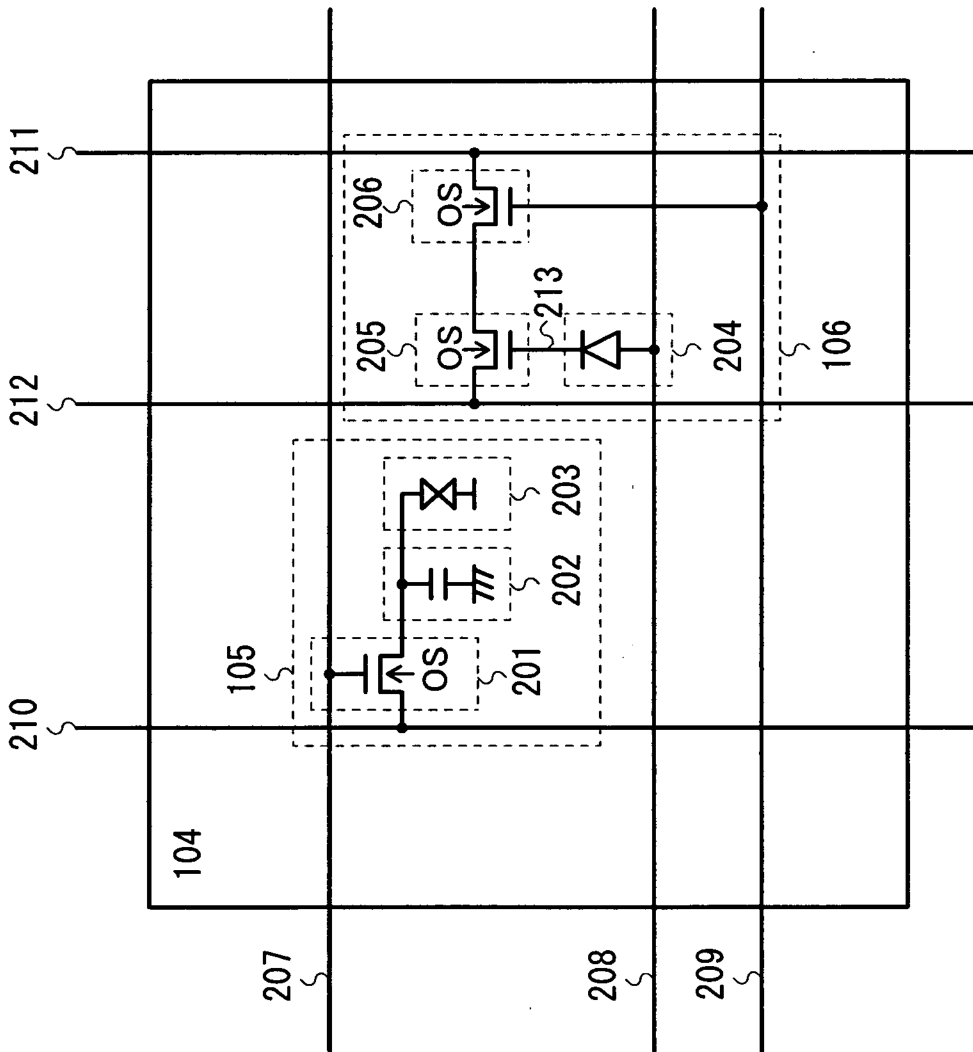


FIG. 2

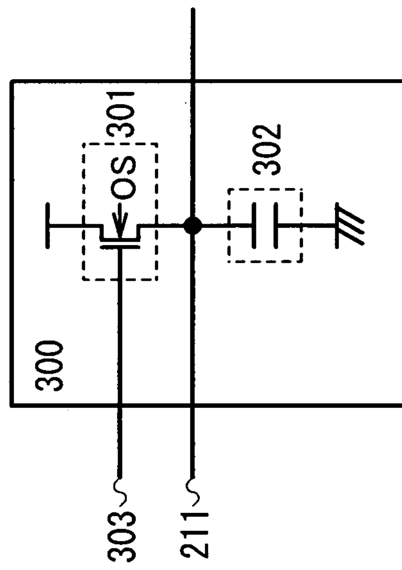


FIG. 3

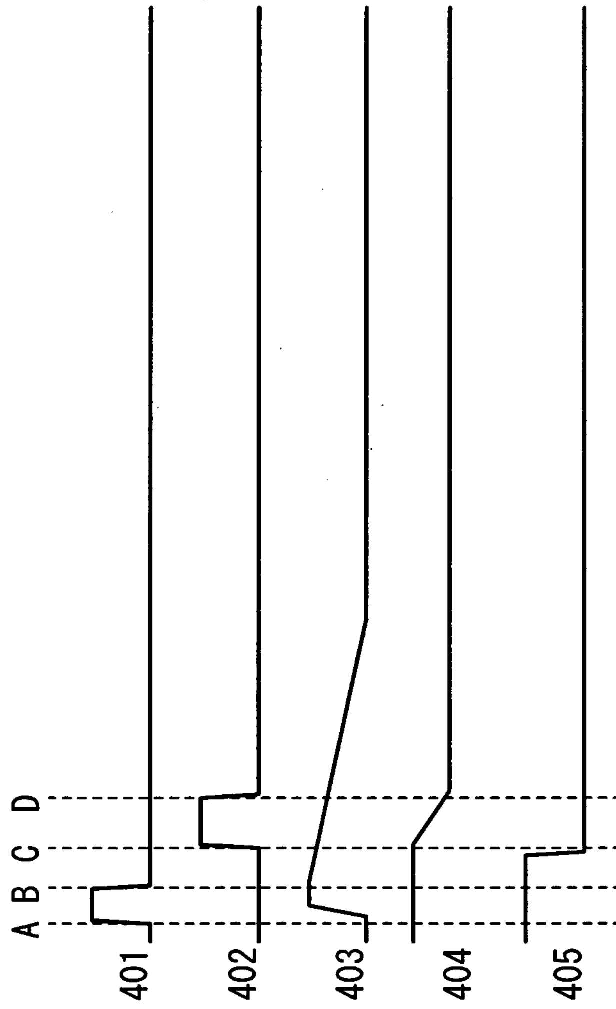


FIG. 4

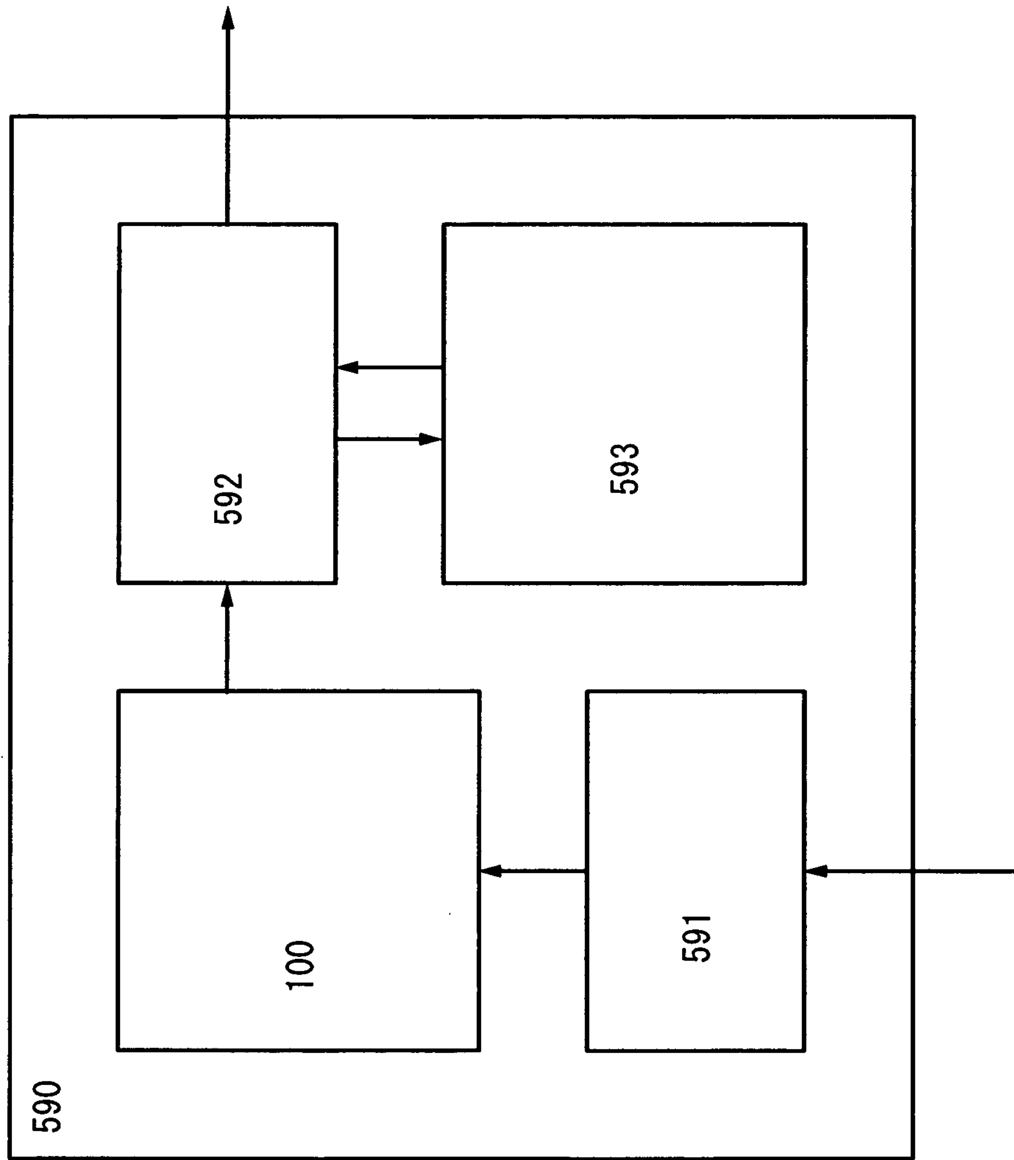


FIG. 5

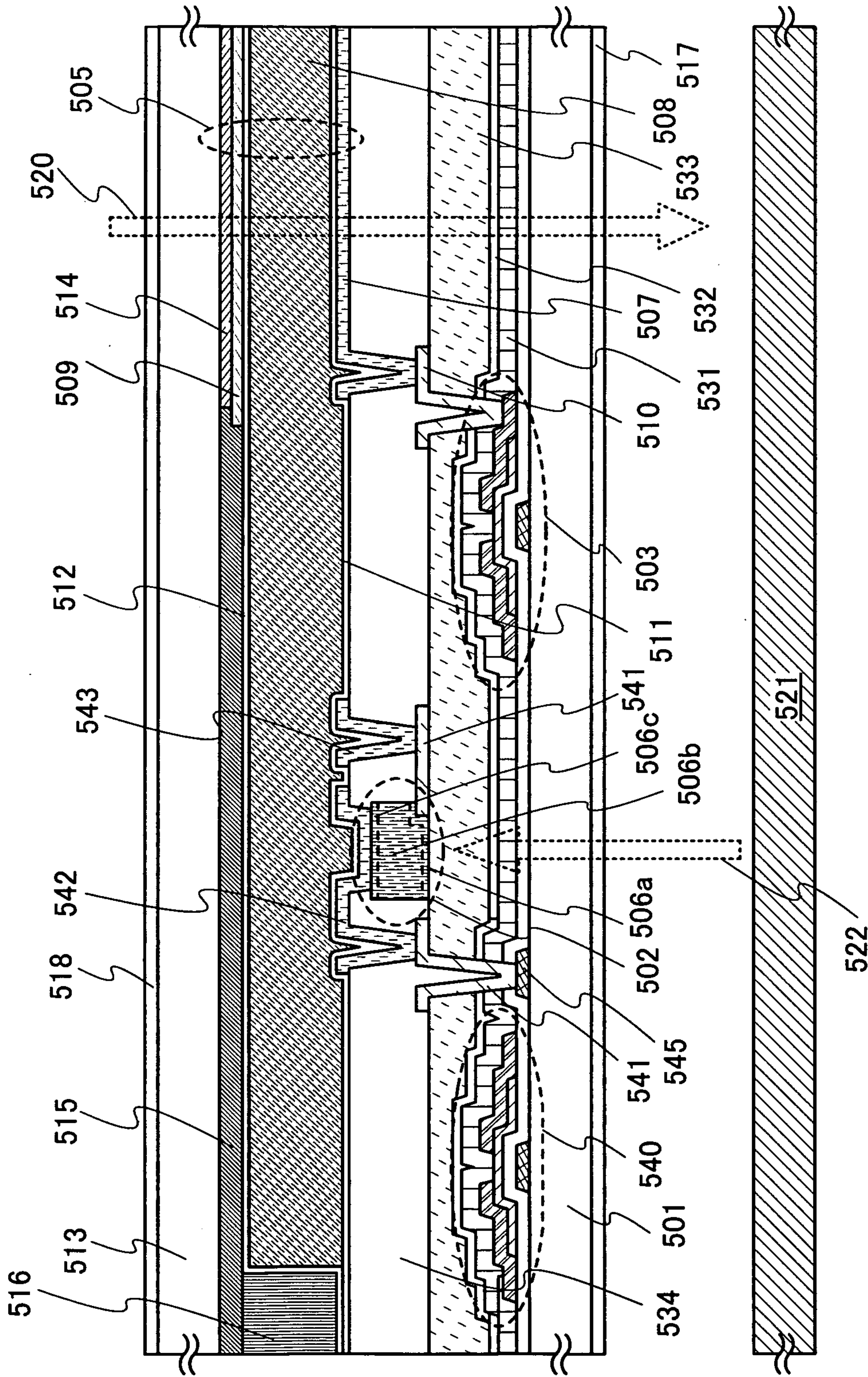


FIG. 6

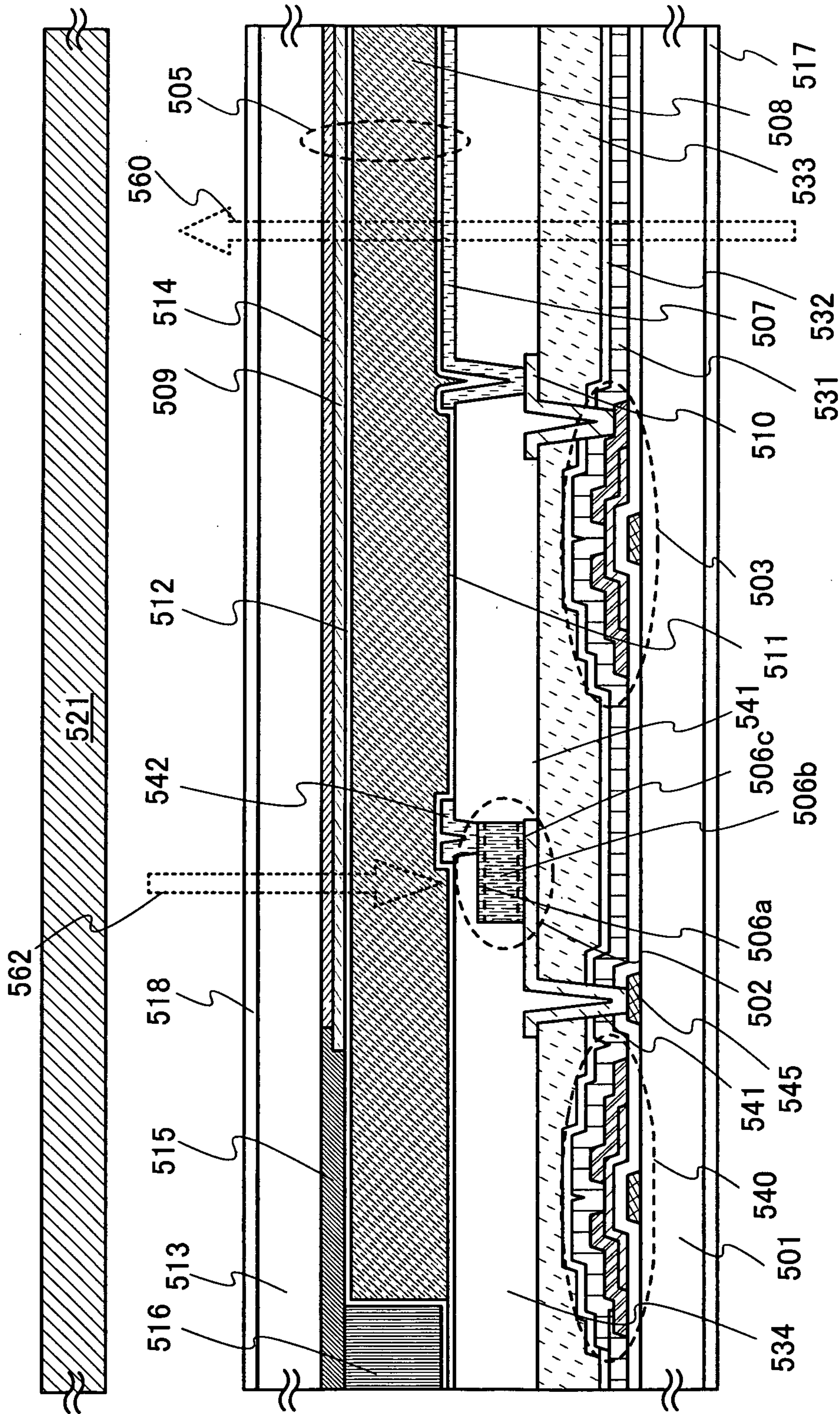


FIG. 7

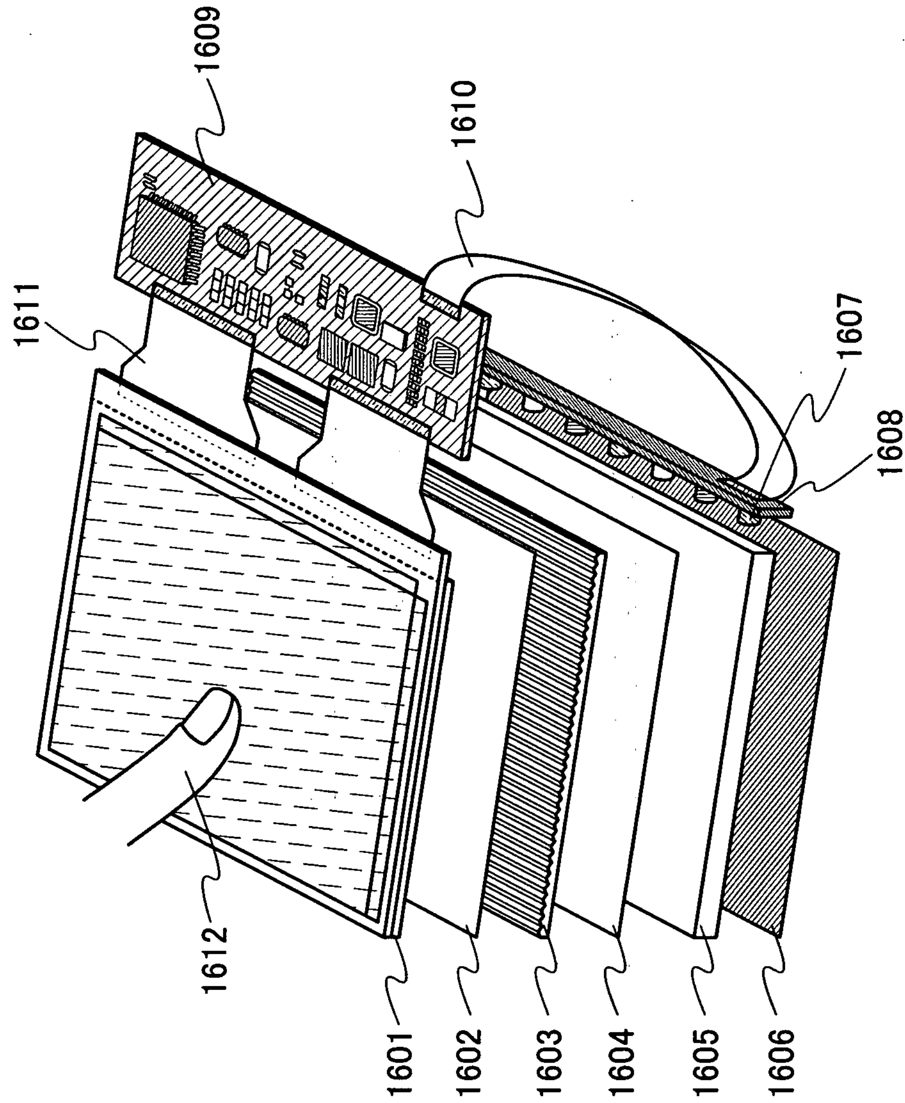


FIG. 8

FIG. 9A

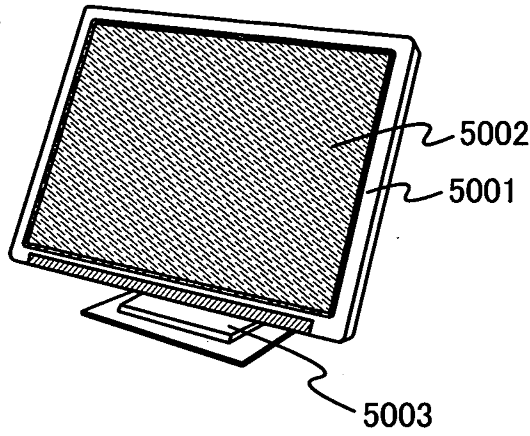


FIG. 9B

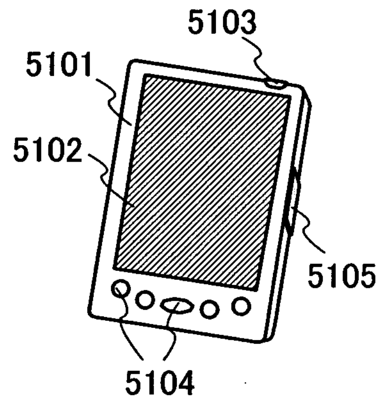


FIG. 9C

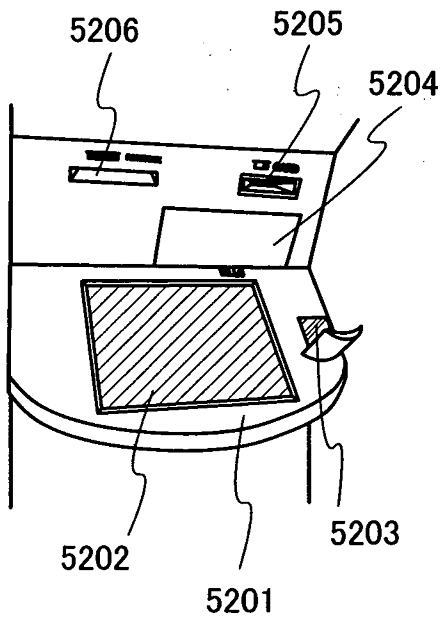


FIG. 9D

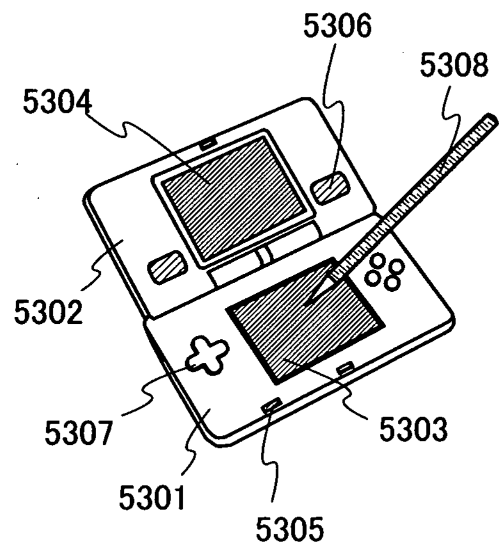


FIG. 10

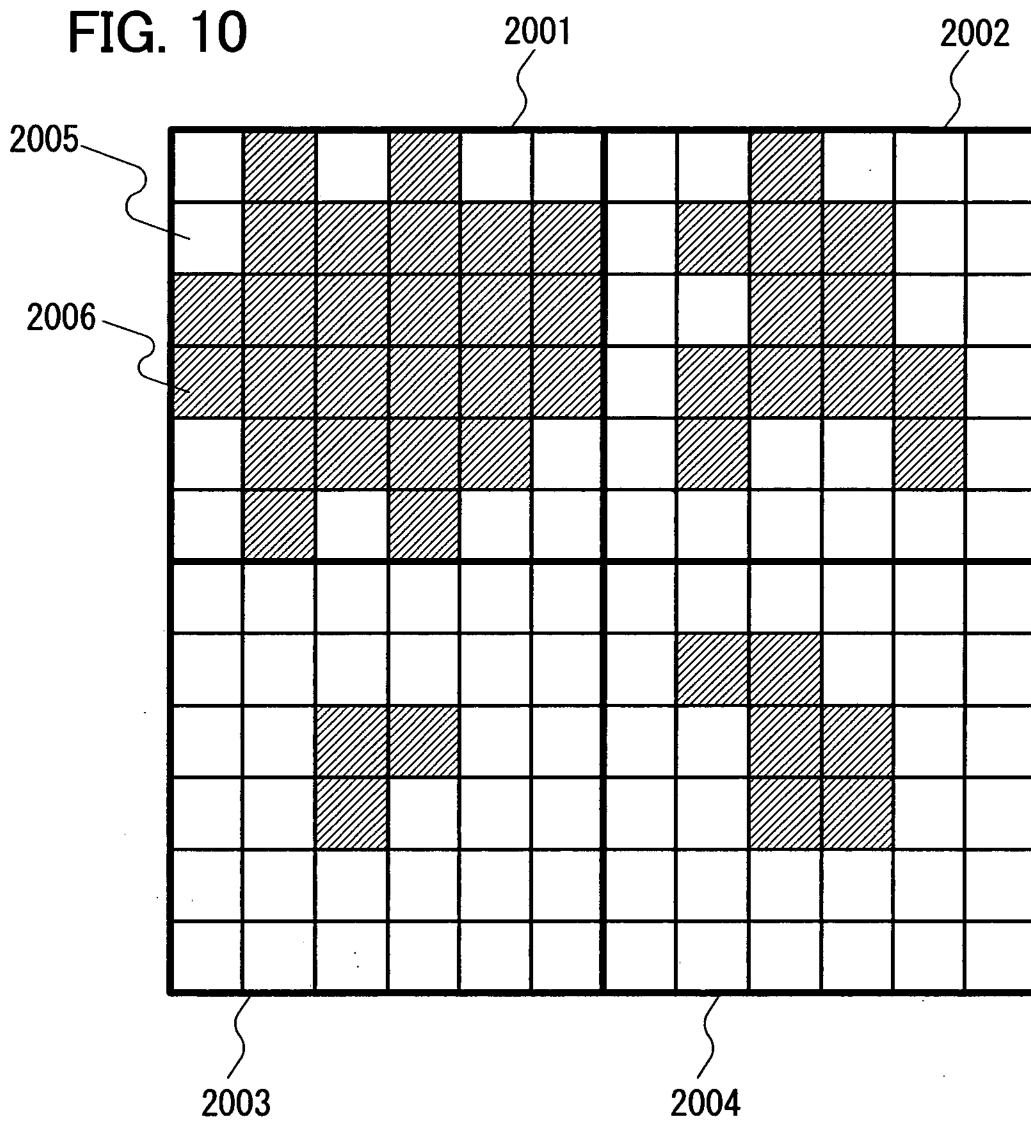


FIG. 11A

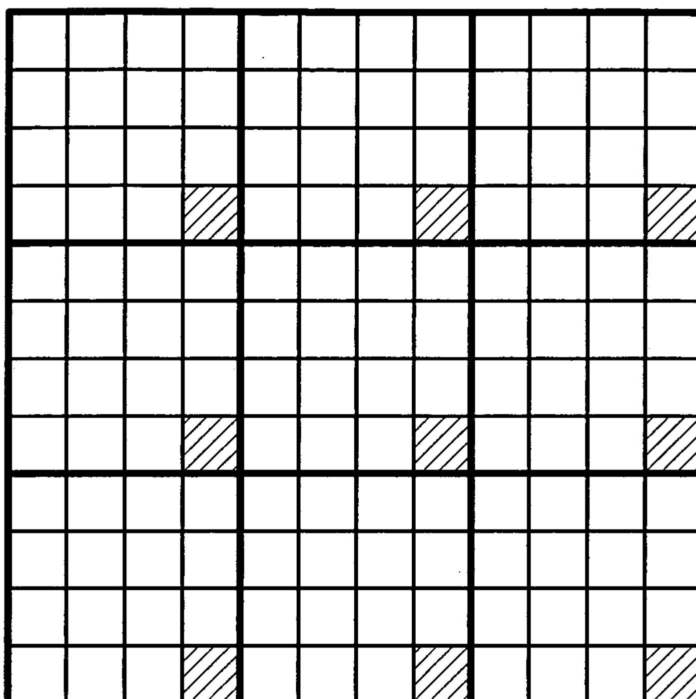


FIG. 11B

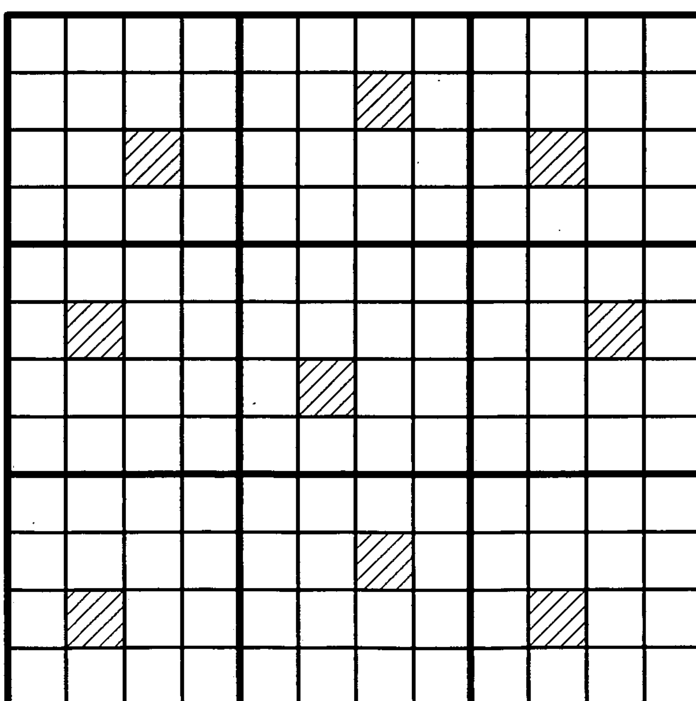


FIG. 12A

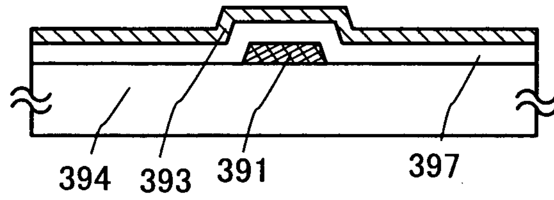


FIG. 12B

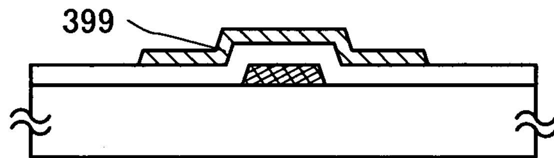


FIG. 12C

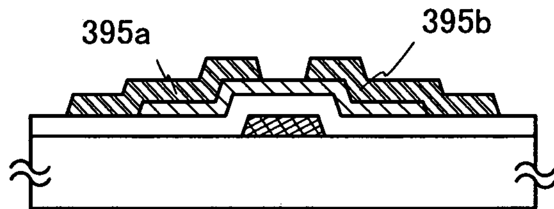


FIG. 12D

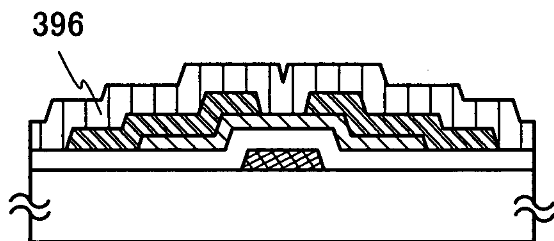


FIG. 12E

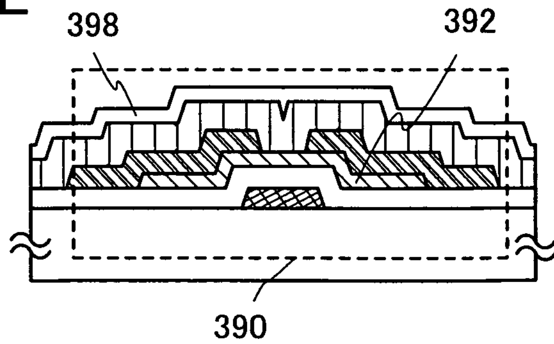


FIG. 13A

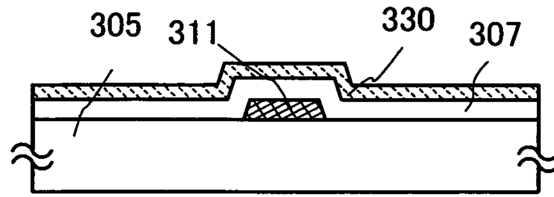


FIG. 13B

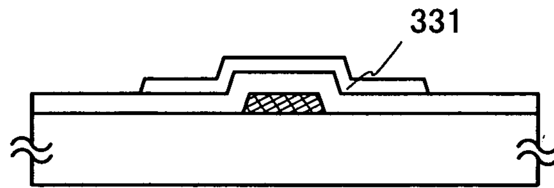


FIG. 13C

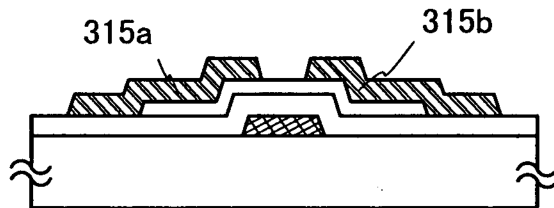


FIG. 13D

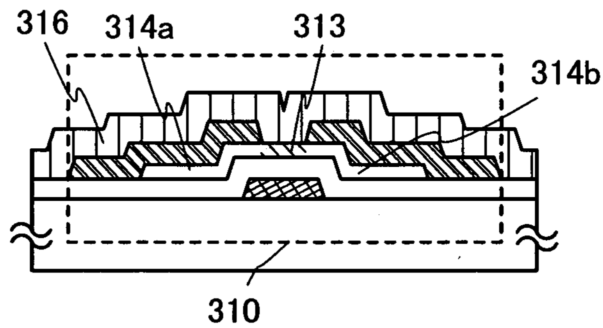


FIG. 13E

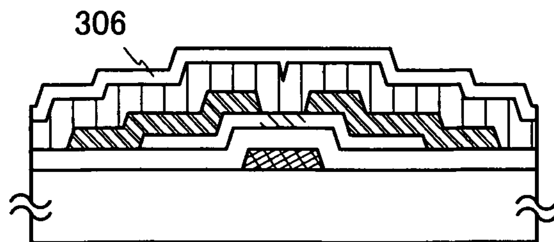


FIG. 14A

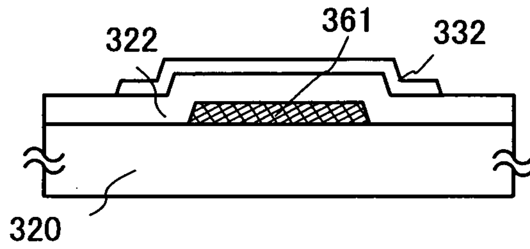


FIG. 14B

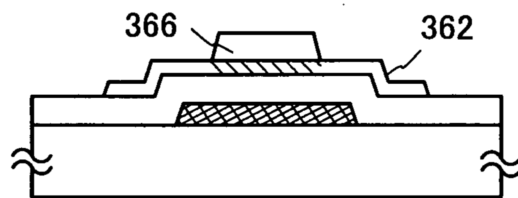


FIG. 14C

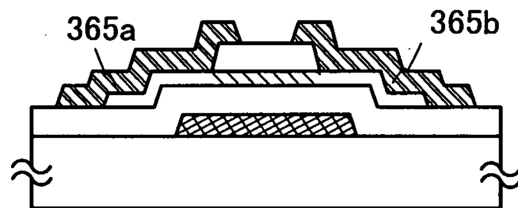


FIG. 14D

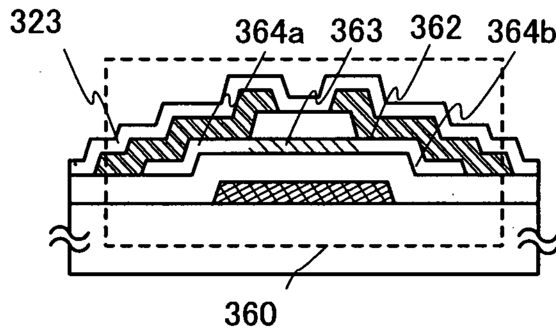


FIG. 15A

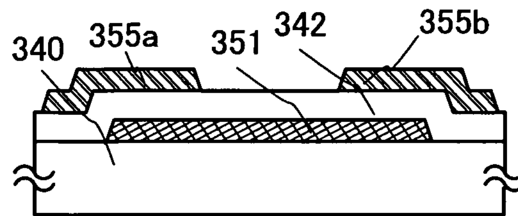


FIG. 15B

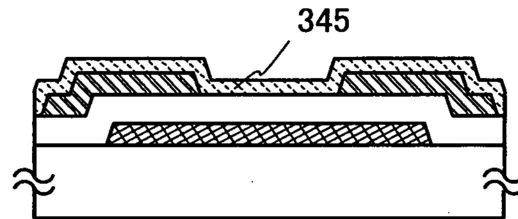


FIG. 15C

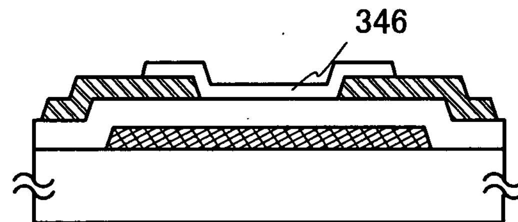


FIG. 15D

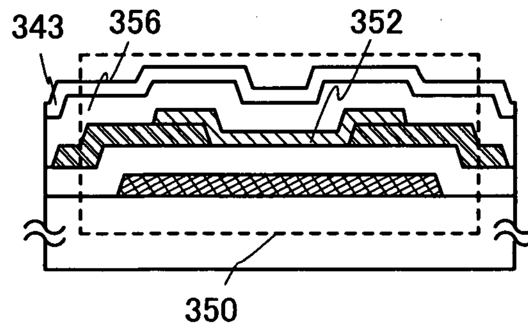


FIG. 16

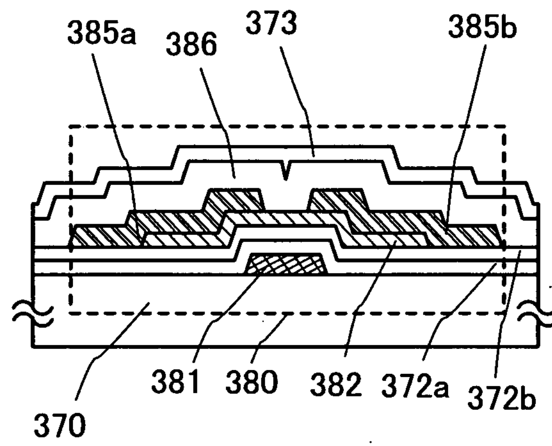


FIG. 17

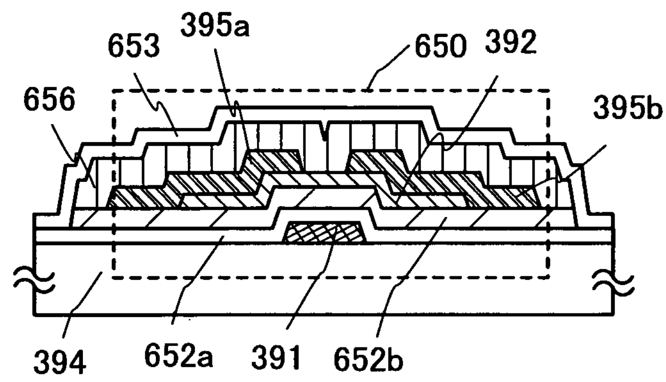


FIG. 18

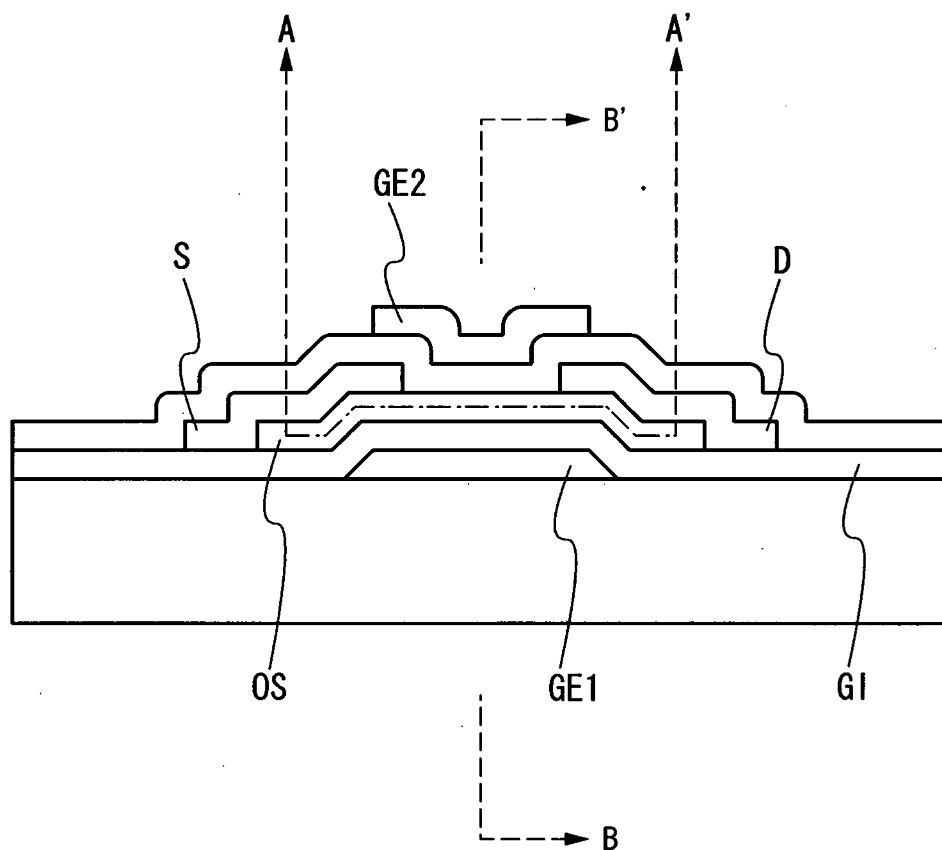


FIG. 19A

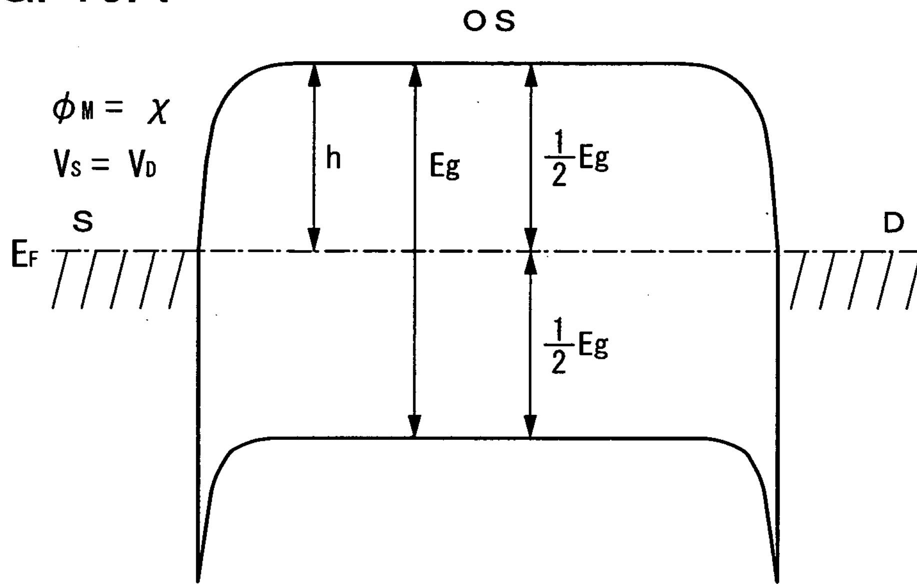


FIG. 19B

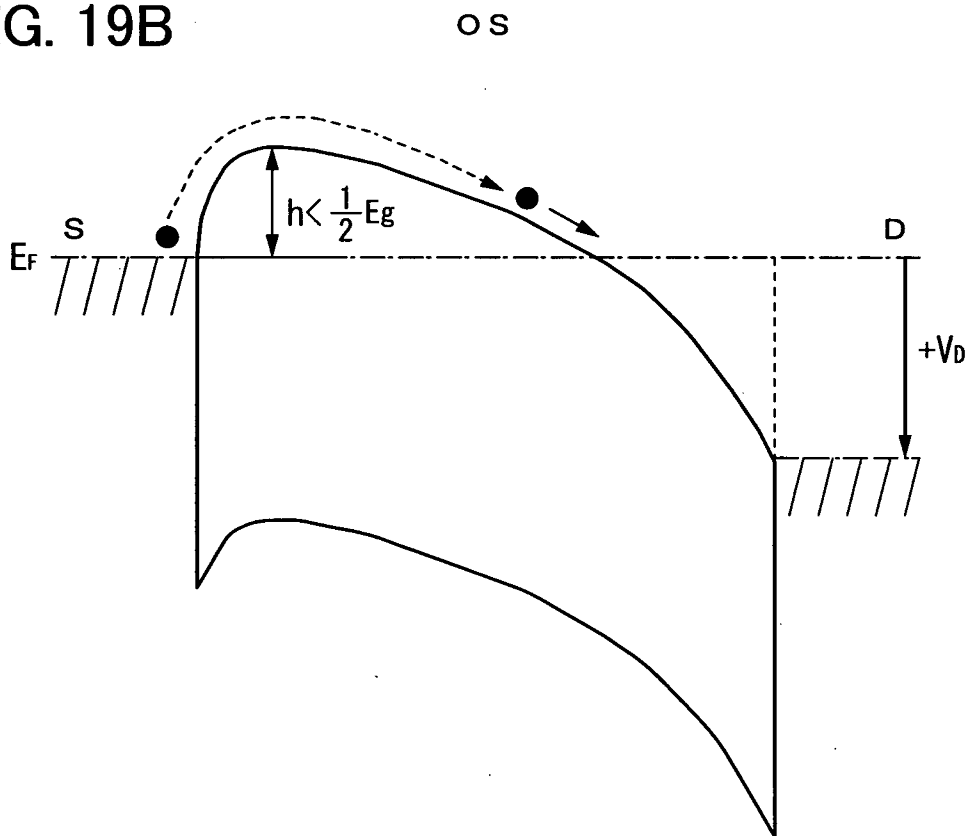


FIG. 20A

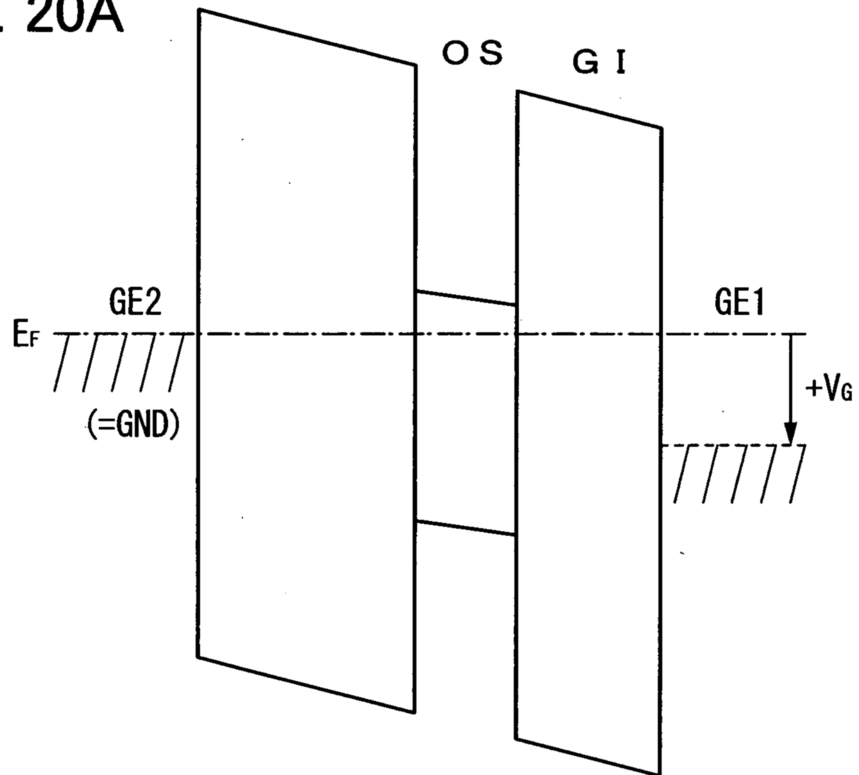


FIG. 20B

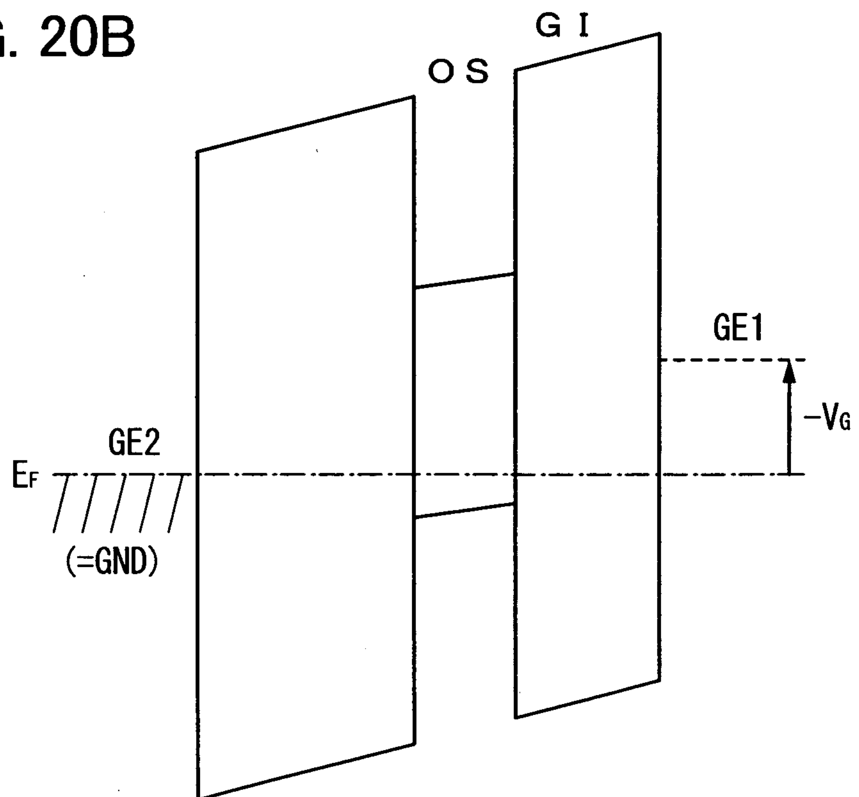


FIG. 21

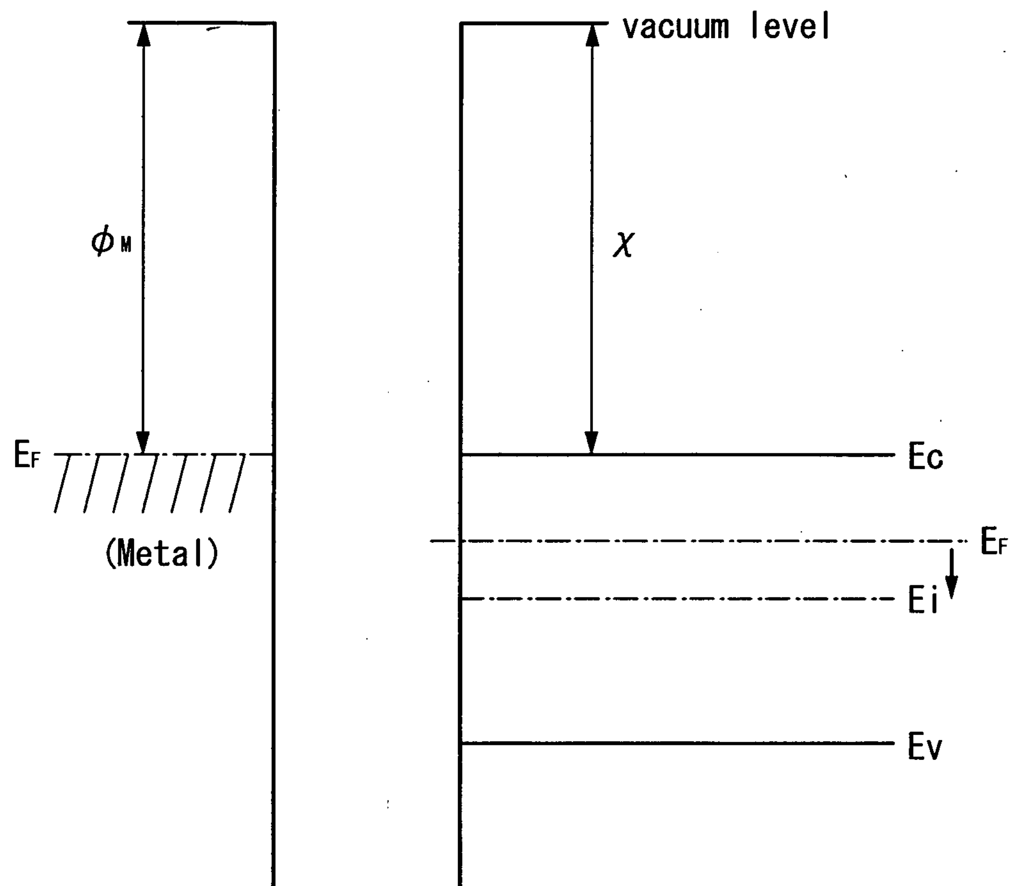
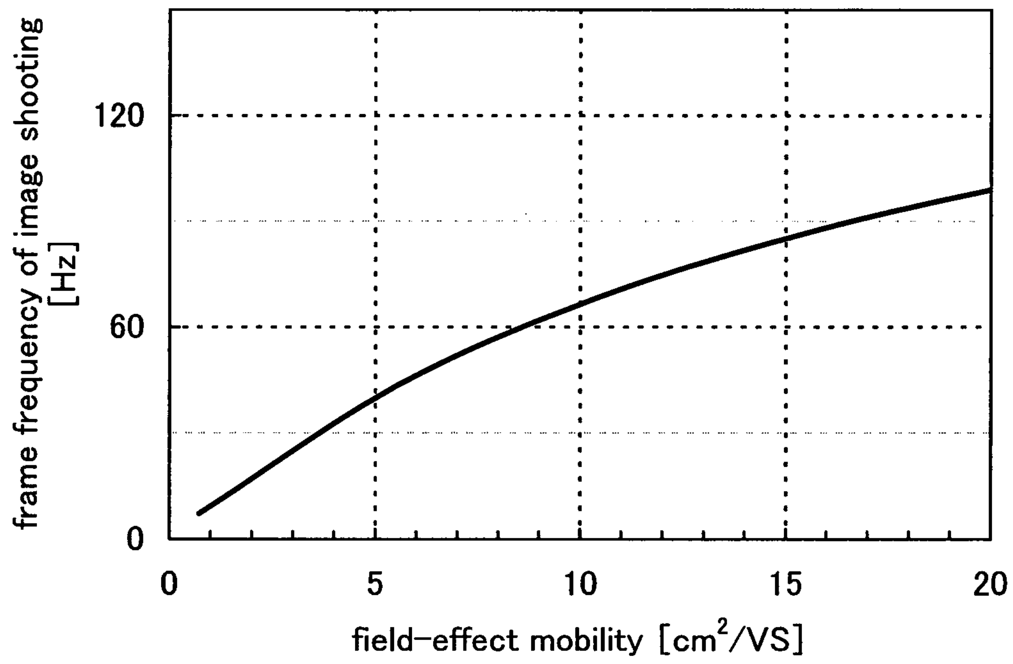


FIG. 22



EXPLANATION OF REFERENCE

100: display panel, 101: pixel circuit, 102: display element control circuit, 103: photosensor control circuit, 104: pixel, 105: display element, 106: photosensor, 107: display element driver circuit, 108: display element driver circuit, 109: circuit, 110: photosensor driver circuit, 201: transistor, 202: storage capacitor, 203: liquid crystal element, 204: photodiode, 205: transistor, 206: transistor, 207: gate signal line, 208: photodiode reset signal line, 209: gate signal line, 210: video data signal line, 211: photosensor output signal line, 212: photosensor reference signal line, 213: gate signal line, 300: circuit, 301: transistor, 302: storage capacitor, 303: precharge signal line, 305: substrate, 306: protective insulating layer, 307: gate insulating layer, 310: thin film transistor, 311: gate electrode layer, 313: channel formation region, 314a: high-resistance source region, 314b: high-resistance drain region, 315a: source electrode layer, 315b: drain electrode layer, 316: oxide insulating layer, 320: substrate, 322: gate insulating layer, 323: protective insulating layer, 330: oxide semiconductor layer, 331: oxide semiconductor layer, 332: oxide semiconductor layer, 340: substrate, 342: gate insulating layer, 343: protective insulating layer, 345: oxide semiconductor layer, 346: oxide semiconductor layer, 350: thin film transistor, 351: gate electrode layer, 352: oxide semiconductor layer, 355a: source electrode layer, 355b: drain electrode layer, 356: oxide insulating layer, 360: thin film transistor, 361: gate electrode layer, 362: oxide semiconductor layer, 363: channel formation region, 364a: high-resistance source region, 364b: high-resistance drain region, 365a: source electrode layer, 365b: drain electrode layer, 366: oxide insulating layer, 370: substrate, 372a: gate insulating layer, 372b: gate insulating layer, 373: protective insulating layer, 380: thin film transistor, 381: gate electrode layer, 382: oxide semiconductor layer, 385a: source electrode layer, 385b: drain electrode layer,

386: oxide insulating layer, 390: thin film transistor, 391: gate electrode layer, 392: oxide semiconductor layer, 393: oxide semiconductor layer, 394: substrate, 395a: source electrode layer, 395b: drain electrode layer, 396: oxide insulating layer, 397: gate insulating layer, 398: protective insulating layer, 399: oxide semiconductor layer, 401: signal, 402: signal, 403: signal, 404: signal, 405: signal, 501: substrate, 502: photodiode, 503: transistor, 505: liquid crystal element, 506a: semiconductor layer, 506b: semiconductor layer, 506c: semiconductor layer, 507: pixel electrode, 508: liquid crystal, 509: counter electrode, 510: conductive film, 511: alignment film, 512: alignment film, 513: substrate, 514: color filter, 515: shielding film, 516: spacer, 517: polarizing plate, 518: polarizing plate, 520: arrow, 521: object, 522: arrow, 531: oxide insulating layer, 532: protective insulating layer, 533: interlayer insulating layer, 534: interlayer insulating layer, 540: transistor, 541: electrode layer, 542: electrode layer, 543: conductive layer, 545: gate electrode layer, 590: display panel system, 591: control circuit, 592: image processing circuit, 593: memory device, 650: thin film transistor, 652a: gate insulating layer, 652b: gate insulating layer, 653: protective insulating layer, 656: oxide insulating layer, 1601: panel, 1602: diffusing plate, 1603: prism sheet, 1604: diffusing plate, 1605: light guide plate, 1606: reflection plate, 1607: light source, 1608: backlight, 1609: circuit substrate, 1610: FPC, 1611: FPC, 1612: finger, 2001: area, 2002: area, 2003: area, 2004: area, 2005: pixel, 2006: pixel, 5001: housing, 5002: display portion, 5003: supporting base, 5101: housing, 5102: display portion, 5103: switch, 5104: operation key, 5105: infrared rays port, 5201: housing, 5202: display portion, 5203: coin slot, 5204: bill slot, 5205: card slot, 5206: bankbook slot, 5301: housing, 5302: housing, 5303: display portion, 5304: display portion, 5305: microphone, 5306: speaker, 5307: operation key, and 5308: stylus.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2010/068649

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. G06F3/041(2006.01)i, G02F1/133(2006.01)i, G02F1/1333(2006.01)i, H01L27/146(2006.01)i, H01L29/786(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. G06F3/041, G02F1/133, G02F1/1333, H01L27/146, H01L29/786

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	JP 2007-102154 A (Toshiba Matsushita Display Technology) 2007.04.19, whole document & US 2006/0262055 A1	1-6 7-14
Y A	JP 2009-146100 A (SONY CORPORATION) 2009.07.02, whole document (No Family)	1-6,15-17 7-14
Y A	JP 2009-224479 A (FUJI PHOTO FILM CO., LTD.) 2009.10.01, whole document (No Family)	1-6,15-17 7-14
Y	JP 2005-275644 A (Sharp Kabushiki Kaisha) 2005.10.06, whole document (No Family)	15-17

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27.01.2011	08.02.2011

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