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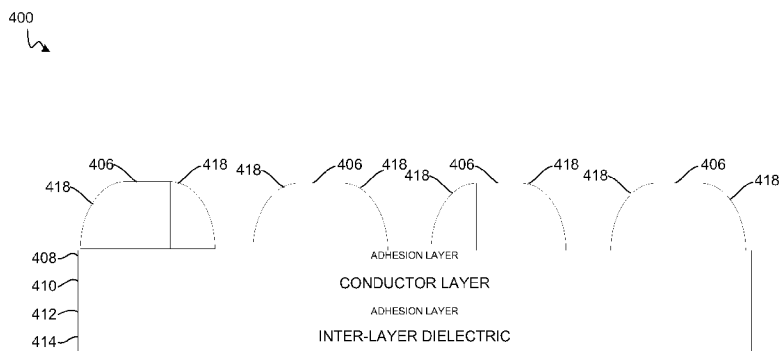


FIG. 4E

(57) Abstract: The present invention provides apparatus, methods, and systems for fabricating memory lines and structures using double sidewall patterning for four times half pitch relief patterning. The invention includes forming features from a first template layer disposed above a substrate, forming half-pitch sidewall spacers adjacent the features, forming smaller features in a second template layer by using the half-pitch sidewall spacers as a hardmask, forming quarter-pitch sidewall spacers adjacent the smaller features, and forming conductor features from a conductor layer by using the quarter-pitch sidewall spacers as a hardmask. Numerous additional aspects are disclosed.



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C. DOCUMENTS CONSIDERED TO BE RELEVANT				
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.		
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Y	US 2009/202952 A1 (ABRAHAM DAVID W [US] ET AL) 13 August 2009 (2009-08-13) abstract; claims; figures 1-3 paragraph [0005] paragraph [0013] - paragraph [0021] -----	1-14		
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<table style="width: 100%; border: none;"> <tr> <td style="width: 50%; border: none;"><input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C.</td> <td style="width: 50%; border: none;"><input checked="" type="checkbox"/> See patent family annex.</td> </tr> </table>			<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C.	<input checked="" type="checkbox"/> See patent family annex.
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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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