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Current Status and Opportunities of Organic Thin-Film Transistor Technologies

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(Invited Paper)

Abstract— **Attributed to its advantages of super mechanical flexibility, very low-temperature processing, and compatibility with low cost and high throughput manufacturing, organic thin-film transistor (OTFT) technology is able to bring electrical, mechanical, and industrial benefits to a wide range of new applications by activating nonflat surfaces with flexible displays, sensors, and other electronic functions. Despite both strong application demand and these significant technological advances, there is still a gap to be filled for OTFT technology to be widely commercially adopted. This paper provides a comprehensive review of the current status of OTFT technologies ranging from material, device, process, and integration, to design and system applications, and clarifies the real challenges behind to be addressed.**

Index Terms— **Displays, flexible electronics, hybrid integration, organic thin-film transistor (OTFT), printed electronics, sensors.**

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I. INTRODUCTION

THE thin-film transistor (TFT) is a key element for realizing functional large area electronics systems including displays and sensors, by providing capabilities of matrix addressing, current driving, and signal processing [1], [2]. For many years, large area manufacturing of hydrogenated amorphous silicon (a-Si) TFT has been well established in the industry for flat-panel liquid crystal displays (LCDs) and imagers [3]. To overcome the poor mobility and bias stress instabilities of a-Si TFTs, low-temperature polycrystalline (LTPS) TFTs with much higher mobility and very stable electrical properties were developed, and have been successfully applied to commercial high-end LCD displays and organic light emitting diode (OLED) displays. However, the LTPS TFT requires additional high-cost laser crystallization and doping processes, and suffers poor spatial uniformity of the electrical properties [4]. Manufacturing of LTPS TFTs is difficult to be scaled up to large area (e.g., > Gen 6), which limits its low cost and large area applications. Since 2004, amorphous metal oxide semiconductor (AOS)-based TFTs have attracted wide attention for their advantages of high mobility, steep subthreshold and ultralow leakage current, with low cost and large area manufacturability attributes similar to a-Si TFT [5], [6]. With these attractive features, the AOS TFT has been quickly adopted to display manufacturing for commercial high-resolution low-power LCD panels and large size OLED panels. Moreover, with its low-temperature processing, the AOS TFT is also regarded a very promising solution for constructing high-performance large area flexible electronics [7], [8].

Compared to inorganic counterparts, organic TFTs (OTFTs) hold several unique advantages for low cost and ultraflexible electronics applications. First, the stack of organic semiconductor (OSC) and polymer gate dielectric with low temperature and fast annealing processes is compatible with low-cost high-throughput printing-based manufacturing [9], and also provides excellent intrinsic mechanical flexibility [10], [11] or even stretchability [12], [13] for truly flexible and stretchable electronics. Second, OSCs have great potential for continuous performance improvement and functionalization through molecule structure tailoring [14], [15] and physical blending [16], which opens a model of boosting the product performance or creating product differentiation by changing the active materials instead of the manufacturing facilities. Last but not least, with OSCs of different functionalities and also versatile device

structures available for making OTFTs, different functions can be easily integrated with very similar processes on the same plastic substrate to create shatterproof flexible integrated systems in compact form factors with nearly no increase in thickness and weight.

In summary, the OTFT technology is able to bring electrical, mechanical, and industrial benefits to many applications by activating nonflat surfaces with flexible displays, sensors, and other electronic functions. The promising applications of OTFTs thus cross many markets including consumer electronics (e.g., wearables and smart home), automotive, security (e.g., flexible fingerprint sensors for mobile, smart cards, and beyond), and medical industry (e.g., low-cost unbreakable X-ray imagers). As predicted by IDTechEx, the overall market for flexible electronics is forecast to reach nearly U.S. $70Bn by 2026. Due to their inherent amplification functions, good biocompatibility, high mechanical flexibility, and ease of miniaturization/integration, OTFTs have also emerged as a versatile platform for physical, chemical, and biological sensing applications [17]–[19]. Motivated by these, in last decades, significant efforts have been devoted to research and development of OTFT technologies, including materials, processes, devices, circuit integration, and applications, resulting in massive progresses [20]. The reported mobility values of OTFTs are much higher than a-Si TFTs, and even comparable with AOS and LTPS TFTs [21], [22]. Several material companies, including Merck, BASF, Polyera, NeuDrive, and Smartkem, can supply a commercial grade stack of OSC, dielectric, and interfacial materials for OTFTs. Lots of interesting advances in device engineering, circuit integration and applications of OTFTs have also been reported by different research groups and companies [23]–[28].

However, despite both strong application demand and these technological advances, there is still a gap to be filled for the OTFT technology to be commercially adopted. This paper will provide a comprehensive review of the current status of OTFT technologies ranging from material, device, process, integration to design and system applications, and clarify the real challenges behind to be addressed to enable the whole community to work together to find the solutions.

II. REVIEW OF CURRENT STATUS

There have been several good review articles on OTFTs published before, which are mainly from perspectives of fundamental material research and understanding related carrier transport and modulation physics [20], [29]–[38]. This part provides a comprehensive review of the current status of OTFT technologies ranging from material, device, process, integration to design, and system applications.

A. Materials

1) Organic Semiconductors: OSC is vital to OTFT, since it accommodates charge carrier to transport inside and thus mainly determines device performance. They can be synthesized with various functional groups to attain specific electrical and/or chemical properties. Consequently, a large number of OSCs have been developed [35], [36], as summarized in Fig. 1. OSCs can be processed by either physical vapor
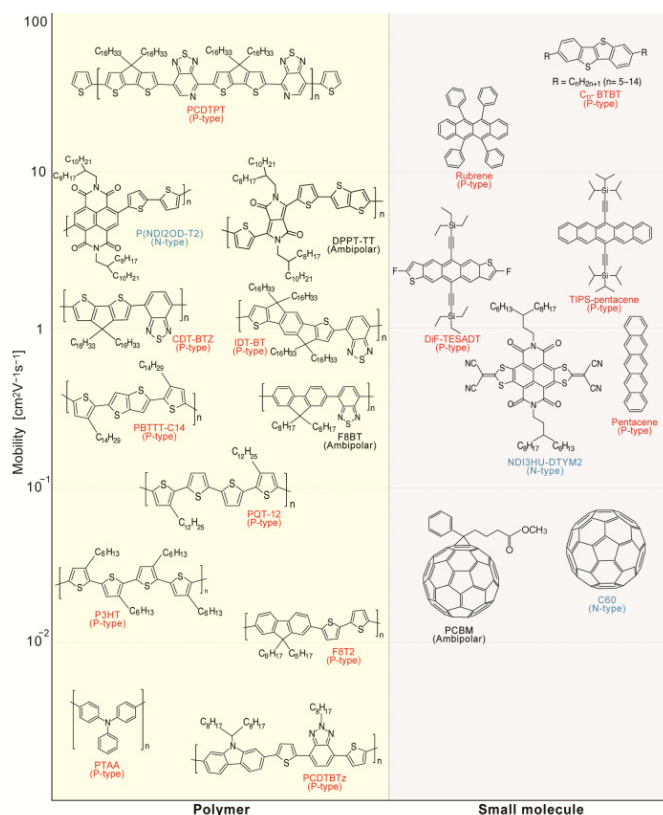

Fig. 1. Summary of typical OSCs for OTFT applications arranged with respect to the carrier mobility, where the OSCs are classified as polymer and small molecule. Also, their typical transport type is indicated below the abbreviation. It must be noted that those reported very high mobility values are shown to be significantly overestimated because the mobility extraction is based on the ideal FET model while neglecting the deviation of the electrical behavior of the fabricated OTFTs from that of an ideal FET [54].

deposition or solution-based processes. Whilst lots of academic research work used thermal evaporation to understand the fundamentals of charge transport and device physics, test the materials, or demonstrate the application ideas, industrial focus was on solution processing to provide low cost and scalable manufacturing options [9]. In general, the majority of OSCs are p-type semiconductors for both small molecules and polymers as seen in Fig. 1. One reason is that the electron-injection barrier is much higher than that of hole injection because the work function of accessible materials for electrode use is high and the OSC band gap is usually large [37], [38]. Another reason is that electron transport is prone to charge trapping.

In the 1990s, the highest performing soluble OSC materials were conjugated polymers, based on region-regular poly (3-hexylthiophene-2,5-diyl) (P3HT) (μ = 0.01–0.1 $\mathrm{cm^2V^{-1}s^{-1}}$) [39], whereas lower mobility but more environmentally stable polytriarylamines (PTAA) (μ = 0.001 $\mathrm{cm^2V^{-1}s^{-1}}$) was developed from chemistries originating in the organic photoconductor industry [40]. Other polymer-based OSCs, such as region-regular polyquaterthiophenes (PQTs) [41], poly(2,5-bis(3-alkylthiophen-2-yl)thieno(3,2-b)thiophene) (PBTTT) [42], and poly(9,9-din-octylfluorene-alt-benzothiadiazole) (F8BT) [43],

have extensively been studied for OTFTs. However, the general issue with polymer OSC was the low mobility, which was difficult to exceed 1 cm^{2}V^{-1}s^{-1}. Lately, donor–acceptor (D–A) copolymers, such as cyclopentadi-thiophene-benzothiadiazole [44], and indacenodithiophene-co-benzothiadiazole (IDT-BT) [45], broke such a convention and exhibited remarkably high mobility more than 1 cm^{2}V^{-1}s^{-1}. It was found that the charge transport in this family of polymeric OSCs (e.g., in IDT-BT) is no longer limited by $\pi-\pi$ stacking among molecular chains that often necessitates tight molecular packing motif and thus sacrifices the benefits of quasi-amorphous polymer. Rather, the aggregates formed by disordered subdomains interconnecting to enable macroscopic charge transport in electronic devices once the molecular weight is high enough, and the charge transport observed is approaching disorder-free levels [46].

The other type of soluble OSCs is based on small molecules, enabling the benefit of higher mobilities than polymeric OSCs. Typical materials include triisopropyl-silylethynyl pentacene (TIPS-pentacene) [47], 2,8-difluoro-5,11-bis (triethylsilylethynyl) anthradithiophene (diF-TESADT) [48], 2,7-dioctyl [1], benzothieno[3,2-b] [1], benzothiophene (C8-BTBT), and the relevant derivatives (Cn-BTBT) [21], [49], [50]. Though high mobility and band-like charge transport can be obtained [51], the polycrystalline or single-crystal small-molecule OSCs are sensitive to microstructural defects created by impurities and mechanical strain, and hence, they are not well suited for manufacturing large-area flexible electronics with ease of processing and good uniformity. To solve this issue, a blend of small molecule acene semiconductor such as TIPS pentacene and diF-TES-ADT with low-permittivity (low-k) polymeric binders was developed to improve crystallization control for higher carrier mobility and better uniformity [16], [52]. Interestingly, a blend of small molecule OSCs with high-k binder formulation has also demonstrated excellent uniformity of high mobility ($\mu > 4$ cm^{2}V^{-1}s^{-1}, $\pm 5\%$), and very importantly at a relatively short channel length of 10 μm [53]. Recently, extraordinarily high mobility values of several tens of cm^{2}V^{-1}s^{-1} have been reported for p-type OSCs, for both polymer and small molecules, as seen in Fig. 1, indicating the great potential for performance improvement with OSCs through chemical structure design and process optimization [21], [22]. However, these high-mobility values are shown to be significantly overestimated because the mobility extraction is based on the ideal field effect transistor (FET) model while neglecting the deviation of the electrical behavior of the fabricated OTFTs from that of an ideal FET [54].

To achieve complementary type circuits with large noise immunity and low static leakage current, the development of n-type OSC with performance comparable to p-type materials has been the main research focus [55]–[57]. For n-type OSCs, typical examples are fullerene (C$_{60}$) [58] and its sister C$_{70}$ [59], as well as the newly developed poly {{[N,N0-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2, 6-diyl]-alt-5,50-(2,20-bithiophene)}(P(NDI2OD-T2), also N2200) [60]. The highest electron mobility observed so far

TABLE I
SUMMARY OF TYPICAL POLYMER GATE DIELECTRICS
UTILIZED FOR OTFTs

Dielectric	Dielectric constant	Reference
CYTOP	2.1	[40]
Polystyrene	2.6	[68]
BCB	2.65	[69]
Polyimide	3.4	[70]
PVC	3.4	[71]
PMMA	3.5	[40]
SU8	3.9	[72]
PVP	4.5	[73]
PVA	7.8 - 10	[74]
CYEL	12	[75]
PVDF-TrFE	-	[76]
PVDF-TrFE-CTFE	>60	[78]

was about 1.2 cm^{2}V^{-1}s^{-1} in small-molecule NDI3HU-DTYM2 [61] and 6.4 cm^{2}V^{-1}s^{-1} in polymeric N2200 processed by bar coating [62].

2) Gate Dielectrics: Gate dielectric is another vital component in OTFTs since it serves as a barrier between the charge carriers transporting at the semiconductor-dielectric interface and those in the gate, and hence, it significantly affects OTFT performance. Gate dielectric determines the areal dielectric capacitance ($C_i = k\varepsilon_0/t_i$) and accordingly the areal charge density in the channel (Q_i), where k is the dielectric constant relative to that of vacuum (ε_0) and t_i is the dielectric thickness. A large C_i is desired for reducing the operating voltage, enhancing the transconductance and minimizing the short-channel effects with scaled devices [63]. It can be obtained by either decreasing t_i or is increasing k. For the former, however, the gate leakage should not be increased and for the later the device performance cannot be sacrificed.

In [31] and [64], many OTFT research activities used commercially available thermal oxidized SiO$_2$ as the gate dielectric, with a self-assembled monolayer (SAM) treatment to suppress the influence of hydroxyl groups on OSC molecular packing and carrier transport. Several high-k inorganic dielectrics were also employed [64], [65]. However, from an industry perspective, to achieve a commercially competitive OTFT technology, solution processable polymer dielectrics are preferable, because of their potential for low-cost manufacturing and excellent mechanical flexibility, though some vacuum deposited organic dielectrics have also been studied to provide high-insulation properties [66], [67]. Various solution processable polymer dielectrics (e.g., CYTOP [40], polystyrene [68], BCB [69], polyimide (PI) [70], PVC [71], poly (methyl methacrylate) (PMMA) [40], SU8 [72], polyvinylphenol (PVP) [73], and poly(vinyl alcohol) (PVA) [74]) have thus been extensively studied as summarized in Table I. However, most polymeric dielectrics have relatively low k. As a result, with a thick dielectric layer required to eliminate gate leakage and be compatible for large area solution-based processing, the reported OTFTs often require an operation voltage of a few tens of volts or even above 100 V.

High-k dielectrics could help to achieve low operation voltage with a thicker layer. However, there are very

few choices of suitable polymer dielectrics with high enough k values. Cyanoethylpullulan (CYEPL) [75], ferroelectric polymer poly (vinylidenefluoride-trifluoroethylene) [P(VDF-TrFE)] [76], and relaxor ferroelectric polymer poly(vinylidene fluoridetrifluoroethylene-chlorofloroethylene) [P(VDF-TrFE-CFE)] [77], [78] have been studied for low-voltage OTFTs. P(VDF-TrFE-CFE) was reported to have a k value above 60 [78]. When the high-k gate dielectric layer is directly interfacing the OSC channel, the energetic disorder caused by the dipoles in high-k dielectric would tend to trap carriers from gate bias induced conduction channel. The resulted localization of charge carriers could cause not only mobility degradation [40], but also increased hysteresis and device instabilities [79]. It was shown that, by inserting a thin, low-k dielectric layer between the high-k one and the OSC channel, the dipole field can be effectively screened for improved device performance [79]. In [80], it was found that, during spin coating of a blend of high molecule-weight PMMA with P(VDF-TrFE), the high molecule-weight PMMA tended to aggregate at the bottom of the deposited film, thus forming the low-k/high-k bi-layer gate dielectric structure for OTFTs in a simpler way.

A type of solid polymer electrolytes, so-called ion gels, has also been studied as a gate dielectric for low-voltage OTFTs [81], [82]. The ion gel was obtained by blending ionic liquids with a gelating triblock copolymer to form a physically cross-linked network and features very large specific capacitance exceeding 1 μF/cm^2 with thickness of about 1 μm, so that it can help to substantially reduce the operation voltage and simultaneously achieve very high driving currents. Despite that, the long polarization time of the ion gel dielectric may slow down the device operating speed, and the presence of ions in the solid electrolyte can cause electrochemical doping of the channel, thus inducing reliability issues.

Furthermore, in the fabrication of OTFTs devices, the deposition of two or more layers sequentially by solution processes could cause dissolution or swelling of the underlayer. Cross-linking of the polymer dielectrics by photograph- or thermal reactions has been studied to enhance solvent resistance, and also improve the electrical robustness [83]–[87].

3) Other Materials: With significant advances in fundamental material development, the industry can now supply volumes of OSC and gate dielectric materials for substantial pilot scale manufacturing processes of low-temperature flexible display backplanes with the device performance greater than a-Si TFTs. These materials have either been commercially available materials, which have been evaluated for compatibility or, in some cases, new materials have been synthesized with tailored properties. In addition to OSC and gate dielectric materials, other materials for substrate buffer layers, electrode treatment and passivation layers are also of importance. In the multilayer integration structure, materials at different layers have to be well matched with solubility difference or be cross-linkable. The OSC/dielectric interface is a critical one for efficient charge transport, as is the back-channel of the OSC layer. Therefore, in a top gate device, it is necessary to control the buffer layer [88], while in a bottom gate device, selecting a suitable passivation layer is critical [89]. Additionally, metallic
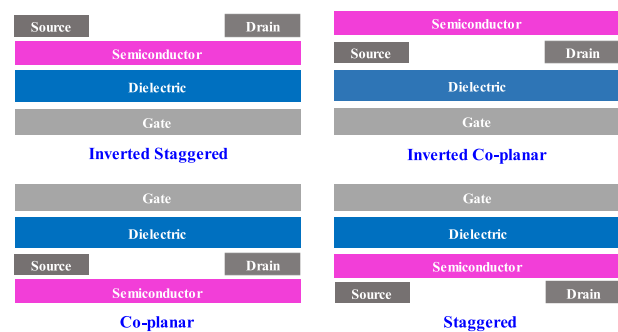

Fig. 2. Illustration of the four device structures used for OTFTs.

source/drain (S/D) electrodes often require SAM treatment to improve charge injection into the OSC layer [31]. The S/D electrodes used in manufacturing as opposed to research have to be compatible with the industry available processes and at an acceptable cost. Alternatives to gold (Au) are vital to the success of the industry, with silver (Ag) [74], indium tin oxide (ITO) [90], molybdenum (Mo) [91], and copper (Cu) [92] being amongst the list of some that have been investigated for this purpose. Therefore, the industry needs to work on developing a full package of materials alongside the OSCs to provide a total material solution for OTFT manufacturing.

B. Device Structure

As shown in Fig. 2, OTFTs can be implemented in four different structures depending on the relative locations of the electrodes. For most of basic research, the inverted staggered structure is used with highly doped silicon as the gate and thermally oxidized silicon oxide as the gate dielectric based on commercial silicon wafers for process simplicity [31]. Many reported high-mobility OTFTs were also fabricated in this way [15], [21], [22]. The coplanar structure was also recently realized to obtain excellent field effect transistor characteristics for ambipolar polymer OSCs by selective contact doping using p-type dopants [93]. However, these top-contact structures are difficult for OTFT circuit integration over large area because of the process difficulty of making S/D metal electrodes on top of the OSC layer with precise patterning. For bottom contact structures (inverted coplanar and staggered), the metal contacts are formed before deposition of the OSC layer, and can thus be finely patterned by industry compatible photolithography processes. Surface modifications of metal contacts with thiol SAMs can be used for obtaining low resistive and preferably ohmic metal/semiconductor contacts as well as good-quality semiconductor films on top of the S/D electrodes for higher performance and better uniformity of electrical characteristics [94]. With these considerations, they are also the choices in OTFT manufacturing trials in industry [95], [96]. Compared to the inverted coplanar structure, the staggered structure has a lower contact resistance for a larger effective area for carriers' injection at the source electrode. The contact resistance in the staggered structure OTFT was also found to be less dependent on the contact barrier than that in the inverted coplanar one, attributed to gate field enhanced charge injection [97].

Contact effects are usually present in OTFTs and they manifest by a reduction of effective mobility and transconductance. For this reason, scaling of channel lengths may be problematic, as the limiting effect of the contact becomes more pronounced. However, deliberately introducing a contact energy barrier may have beneficial effects despite the decrease in current and speed. A new structure named source-gated transistor (SGT) [98] is formed when a barrier (e.g., Schottky) at the source is used to restrict the current. Under normal operation, at low drain bias, the source barrier is reverse biased and the semiconductor is depleted of carriers across its whole thickness, leading to saturation of output current at comparatively low drain voltage. This allows energy-efficient operation while maintaining high intrinsic gain, from lower drain voltages than conventional FETs, and current is modulated in the first order by the gate electric field's effect on the effective source barrier height [99]. When this structure is applied for OSCs, the induced high drain electrical field in the device may result in enhanced carrier mobility and operating speed [100]. As a result of the current control method, drain current is virtually independent of source–drain separation, which increases performance uniformity in high-throughput technologies with low-resolution patterning. Importantly, the SGT structure was normally realized in inverted staggered structure, and would also possible to be made in staggered structure. Therefore, SGT and the conventional FET can be made on the same substrate, by varying the contact properties through choice of a different electrode metal or contact treatment, enabling the exploitation of both types of devices in the same circuits.

C. Process and Integration

The most ideal approach for OTFT integration is full additive printing for "manufacturing-on-demand" at a fraction of the cost and footprint. However, due to difficulties in technology scaling for fine structures and complicated multilayer integration, it is unrealistic today to use all additive printing processes for high-end applications, such as displays and imagers, which have strict requirements on performance, integration density and reliability. In LCDs, e-paper displays and X-imagers, OTFTs simply function as switches, while in OLED displays, OTFTs need to work as switches and current drivers and the pixel structure is much more complicated. Thus, it is clear in the short term, OTFT-based flexible electronics must be manufactured using more conventional processes—by repurposing existing manufacturing equipment to minimize barriers to entry and get products to market that validate the 'product performance' and applications and prove business cases for the value that OTFT can bring to applications. In the meantime, lots of research is undergoing on addressing issues on all printing processes, for many very cost sensitive applications with less requirements on the integration density and reliability.

1) Processes Compatible With Established Industry Facilities: The display industry currently manufactures over 150 million square meters of display backplanes per year on glass, which is supported by mature industry players ranging from materials suppliers to equipment vendors. In the near
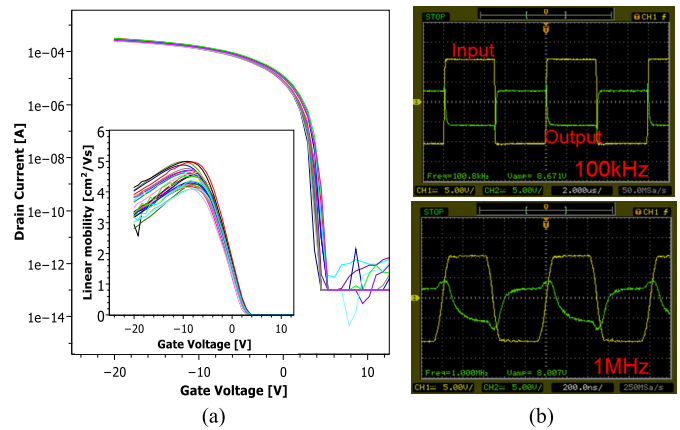

Fig. 3. (a) Transfer curves for OTFTs made using FlexOS OSC in staggered Corbino structure with a channel length of 7 μm ($V_{DS} = -2$ V), and the measured linear mobility average was 4.4 cm^2/V s for 30 devices with standard deviation of 7% as shown in the inset. (b) Transient characterization of nand3 logic gate made with the OTFT at 100 kHz and 1 MHz driven from a function generator and with power supply voltage of -20 V.

future OTFT can access some of this capacity for production of plastic-based displays and other applications provided that the materials are compatible with established toolsets. A nonexhaustive list of reported examples of OTFT processes demonstrated at pilot manufacturing scale include (substrate size in brackets): FlexEnable in the U.K. (14 in square), Sony in Japan (6 in round), LG Display in South Korea (370 mm × 470 mm), Samsung (300 mm × 400 mm), Polyera in Taiwan (200 mm^2) and CPI in the U.K. (200 mm). The Plastic Logic manufacturing facility in Germany (Gen 3.5, 650 mm × 780 mm) based on the FlexEnable process is currently the only example of a full manufacturing line for OTFTs. The processes currently employed in the display industry and also used in OTFT manufacture include sputtering, photolithography, wet etching, dry etching, spin coating and slot die coating. Materials used for the OSC layer are perhaps the most sensitive and exposure to oxidizing chemicals such as nitric acid and aggressive organic solvents such as photoresist stripper should be avoided throughout the process. Sputtering and dry etching have also been reported to have impacts on the OTFT characteristics of certain materials [101]–[103]. Some degree of protection is thus often required by dielectric, metal or other photoresist layers throughout the processes so that aggressive chemicals and processes can be used. With the high-resolution patterning, good overlay accuracy, and low defect density common to display manufacturing, OTFT can achieve high performance with good uniformity in prototype devices, examples being rollable OLED displays [104], production quality electrophoretic products [105], and high-frequency (1 MHz) logic, as shown in Fig. 3.

2) Full Printing Processes: Besides being developed for various flexible backplanes for e-paper, LCDs, OLED displays, and imagers, OTFTs can find strong opportunities in the short/medium term for mass produced disposable electronic systems so-called "smart labels" or "smart tags," which are indeed not economically viable to be realized by the established silicon technology.
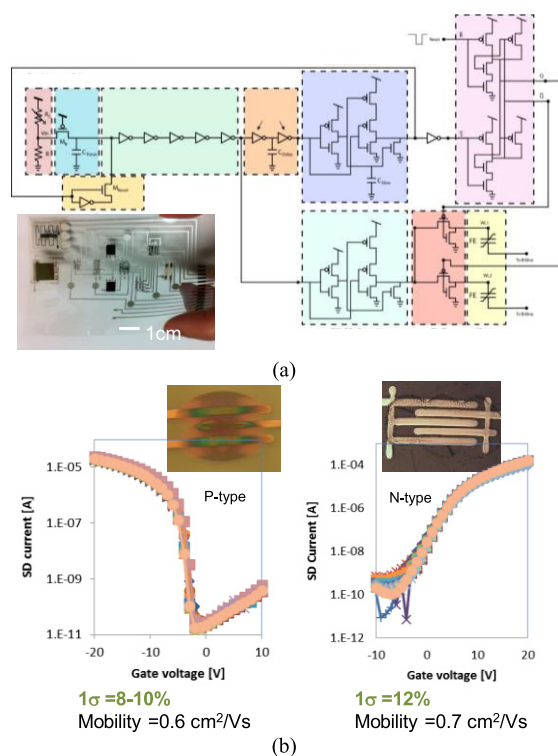
(a)

(b)

Fig. 4. (a) Printed time-temperature dose tag showing the different subcircuits and a photograph of the tag. Reprint with permission from [107]. (b) For this tag, the transfer characteristics for 30 typical OTFTs using p-type semiconductor or n-type semiconductor. The photographs show the semiconductors printed over interdigitated electrodes.

The simplest applications are based on the all organic stand-alone system. For example, a low scale of integration logic block was connected to a suitable sensor, i.e., a toggle button and/or a simple fuse, to detect the opening of a package, and can drive a simple display showing the status of such package [106]. Such simple, stand-alone, yet effective tag, could be attached to the package in the same way a normal graphical label is, sharing a very similar geometrical form factor and mechanical properties, provided that a suitable interconnection to the sensor is guaranteed. Such possibility must, however, be sustained by the development of high-throughput, yet reliable printing processes, capable of keeping the overall tag cost extremely low. As shown in Fig. 4(a), a time-temperature dose tag was fabricated on flexible plastic foil and comprised a thermistor divider, complementary organic circuits, and two nonvolatile memory cells [107], after achieving having reasonable device uniformity of both p- and n-type OTFTs with additive printing processes [Fig. 4(b)]. If integrated with an appropriate power supply, the tag could operate as a stand-alone system, with nonvolatile memory for later readout for a wide range of potential applications in food and medicine spoilage. It is a promising step toward economical printed OTFT stand-alone sensor systems.

For the commercially available batteries used as the power supply for these stand-alone systems, the output voltage level of around 1.5–4 V is often insufficient to surpass the threshold voltage for many printed OTFTs that have been demonstrated so far. In order to operate the system, either the supply voltage must be increased or the operation voltage of OTFTs should

be reduced. The supply voltage can be boosted by connecting batteries in series or by adding a voltage multiplier [108] or charge pump circuit [109], which, however, increases the system complexity and cost. Low-voltage operable and stable OTFT is thus very important for this system, but it is challenging to be achieved by only enlarging the gate dielectric capacitance with ultrathin or high-k gate dielectric layer, especially when the devices need to be manufactured by all additive printing processes to make a commercially viable technology. Recently, several studies have shown that it is feasible to reduce the subgap density of states (DOS) at the channel through solution processed OSCs for realizing low-voltage OTFTs with small gate dielectric capacitance [74], [110]. Therefore, a relatively thick low-k polymer dielectric can be applied, which can help to achieve excellent stability and also has wide material choices [71], [72], [83], [86], [87]. Such a low-voltage OTFT can be fabricated by inkjet printing all layers including electrodes, gate dielectric, OSC, and encapsulation layers, proving the most economic manufacturing approach [111].

For more envisioned applications, which need to have wireless connections with users, the stand-alone system is not applicable. In such systems, a series of functions, including accurate and complex signal processing, power management and communication are required to be performed in a severely power constrained system. These functions are very challenging to be realized with printed OTFTs today. A hybrid technology is thus necessary to combine the OTFT with low-voltage silicon chips [112]. In such a system as illustrated in Fig. 5, a transducer circuit is implemented using printed OTFTs to convert the sensed signal to a standard voltage output. Various functional sensing materials can also be integrated through the printed OTFT technology. A common read-out and signal processing hardware or specific silicon chip consisting of analog-to-digital converter, processor, wireless interface for data output (e.g., near-field communication, Bluetooth, …) can thus be implemented for these different sensors. With a fixed silicon chip design and additive printing of the OTFT-based front end for the custom design, this hybrid integration would provide a low cost and versatile solution to "smart tag" systems. For this integration, with the fully-printable low voltage and stable OTFT, sensor tags were made to be operated in a low-voltage (3.3 V) battery powered electronic system for long term and repeatable ammonia and pH sensing, respectively [24], [71].

Compared to the hybrid solution with a silicon chip, a "chip-less" design would be desired to provide a lower cost solution for wireless sensor tags by seamlessly integrating all the required electronics, sensing and antenna driving functionalities [113], [114]. For that, high speed printed OTFTs to afford signal modulation frequency of at least tens of megahertz are needed to construct the wireless communication interfaces. The transition frequency or cutoff frequency f_T is widely adopted for the evaluation of the operation speed of a single transistor [115]–[118]. Two methods were generally adopted for measuring f_T: a direct evaluation of the transconductance and gate capacitance via the measurement of small current signals flowing into the device electrodes [116], [117] or
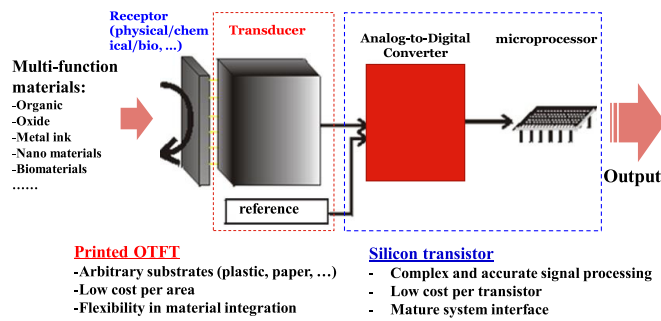
Fig. 5.   Illustration of a hybrid integration approach combining the advantages of both the printed OTFT and the silicon technology.
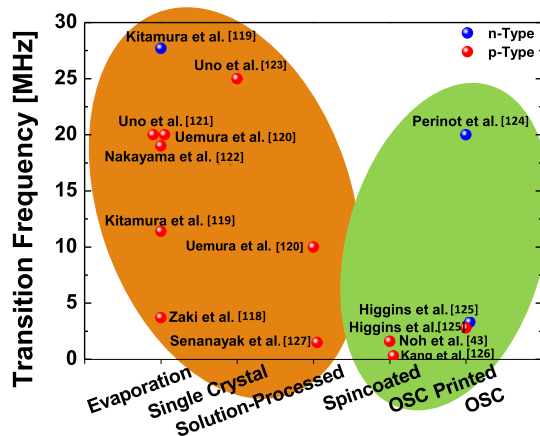

Fig. 6.   Overall comparative plot of the best f_T results for OTFTs, which f_T was explicitly measured and reported in the literature. The works are classified with respect to the fabrication methods adopted for the patterning of the electrodes and for the deposition of the semiconductor.

the evaluation of the two-port-network h_{21} hybrid parameter [118]. Enhancing f_T of OTFTs requires the adoption of OSC materials guaranteeing high effective mobility and architectures with scaled channel lengths and reduction of parasitic capacitances posing constraints on the patterning technology that has to be maintained compatible with cost-effective large-area processes. Fig. 6 summarizes the measured f_T of OTFTs from selected works achieving the best results, which are classified with respect to the fabrication methods adopted for the patterning of the electrodes and for the deposition of the OSC layer [43], [118]–[127]. The record f_T reported to date reaches the value of 27.7 MHz for a device based on C_{60} with a channel length of 2 μm defined by photolithography [119]. Recently, OTFTs with f_T of 20 MHz were fabricated by means only of scalable coating techniques and laser-based direct-writing methods with a completely mask-less procedure [124]. A much higher throughput approach was demonstrated by Kang *et al.* [126], who used highly scaled gravure printing to fabricate OTFTs with a fast printing speed of 1 m/s, despite a lower $f_T = 0.3$ MHz. It is important to highlight that those high f_T values were generally achieved with operation voltages of several tens of volts. Indeed, to comply with the requirement of low-voltage operation which is necessary for applications in the fields of wearable and portable devices, it is desirable to achieve high-frequency operation for a supply voltage lower than such a value. The works where
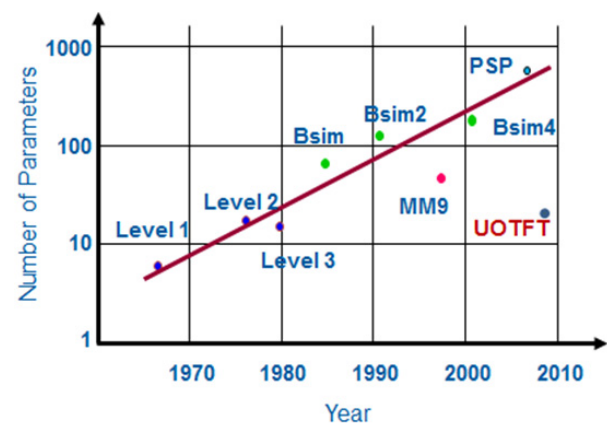

Fig. 7.   Comparison of the number of parameters in the developed UOTFT model in commercial circuit simulator SmartSPICE with the models for silicon FETs.

high-frequency operation is combined with low-voltage operation are a minority. The representative work by Zaki *et al.* [118] obtained $f_t = 3.7$ MHz for a bias voltage as low as 3 V.

D. Device Modeling and Circuit Design

Accurate compact models are basis for efficient circuit design to move the OTFT technology from devices to circuits and systems. In the past, corresponding development of physics-based compact models has been under continuous progress, after many fundamental aspects of OTFTs were revealed [128], [129]. Models to be able to capture non-ideal realistic device behaviors, including gate bias (V_{GS}) dependent mobility [130], [131], nonexponential dependence of subthreshold current on V_{GS} [132], [133], and contact resistance effects [134], have been developed. Smooth linear-to-saturation transition and subthreshold to above-threshold transition were further worked out to connect these discrete models for unified compact models, which cover all regimes of OTFT operations and are able to be implemented into circuit simulators to reach an effective convergence [130], [135]. For the large variations in OTFT materials and structures, further modeling efforts have been devoted to the capability of rearrangement and flexibility for capturing the essence in the behaviors of various OTFTs in a consistent and relatively simple way, and allowing for easier implementation, modifications, and parameter extraction [128], [136]. These developed models can be conveniently implemented into commercial circuit simulator for circuit simulation using Verilog-A, which, however, is slower and less efficient than a well-developed SPICE model [137]. Currently, the only OTFT SPICE model available in commercial circuit simulator is the universal OTFT (UOTFT) model in SmartSPICE, which combines the robust concepts of universal charge-based FET modeling with OTFT specific charge, mobility and contact resistance bias, and temperature dependence [138]. The parameters in the UOTFT are significantly less than that in those advanced models for modern silicon FETs, as shown in Fig. 7.

To design and construct complex circuits and systems, the complementary type is a preferred choice for its low static power, rail-to-rail operation, and large noise margin [139].
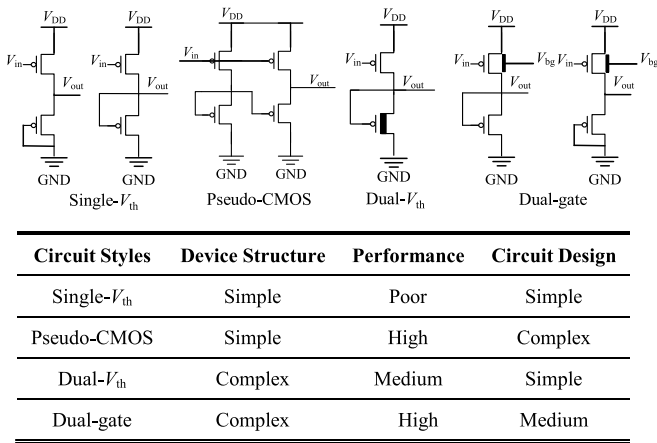
Fig. 8. Comparisons of different unipolar circuit styles for OTFTs.

Circuit Styles	Device Structure	Performance	Circuit Design
Single-V_{th}	Simple	Poor	Simple
Pseudo-CMOS	Simple	High	Complex
Dual-V_{th}	Complex	Medium	Simple
Dual-gate	Complex	High	Medium

However, it is difficult to find n- and p-type semiconductor materials with equivalent performance and compatible processes that would allow easy fabrication of high-performance complementary circuits. For print processing, complementary design is easy to realize since the two semiconductors are additively patterned in just two steps. For photolithographic processing, at least three more masking steps are required to pattern two semiconductors due to the subtractive process. Therefore, the unipolar designs have been widely adopted for OTFT logic circuits. Although having the advantage of simplicity, the common unipolar logic circuit design could hardly provide sufficient noise margins to accommodate normal OTFT parameter variations for building complex circuits. To improve the robustness to parametric variability, advanced device or circuit architectures such as pseudo CMOS [140], dual-V_{th} TFT logic [141], and dual-gate structure [142] were proposed. Therefore, considering the tradeoff among performance, process simplicity and design complexity as shown in Fig. 8, it would be helpful to predict the yield and the performance in the early device development or circuit design stage to select the most cost-effective solution for realizing the required functional circuit of good manufacturability [143], [144].

E. EDA Tools and Design Kits

Electronic design automation (EDA) tools have been a key factor for the success of the microelectronic industry since they allowed building complex (nonregular) integrated circuits with an increasing number of transistors (according the Moore's Law) in a reduce amount of time. EDA tools strongly developed the concept of technology-independent circuit design that is later mapped into technology dependent cells and structures (based on transistor models and design rules), that were described in the technology or process design kit [technology design kit or process design kit (PDK)] available for every stable technological process. This leads to the concept of fab-only and fabless semiconductor industry. Fab-only consists of companies that does not produce semiconductor products or chips being commercialized (i.e., TSMC or UMC) while fab-less companies are concentrated in application-oriented technology-independent that do not own fabrication processes (i.e., Qualcomm or ARM both around the mobile industry).
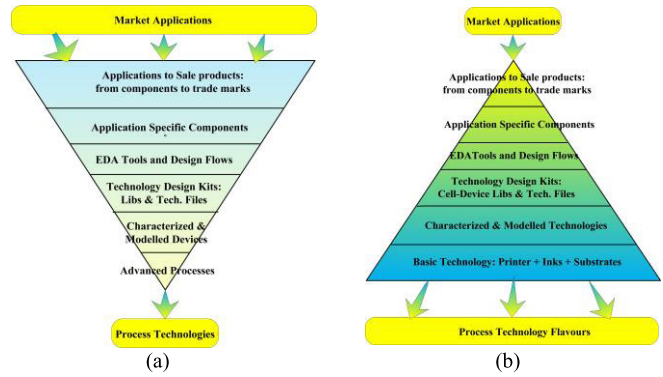

Fig. 9. (a) View of the current silicon microelectronics industry where many fabless industries develop a wide range of products implemented in a reduced set of fab facilities thanks to its highly segmented horizontal business model. (b) View of the current flexible electronics industry with a reduced set of products that have a wide range of technologies available for its implementation in a closed vertical business model.

As shown in previous sections, design of future flexible systems based on OTFTs will include heterogeneous integration of different technologies (flexible + silicon, flexible + flexible, flexible + functionalization). Moreover, there is also an increase of homogeneous integration systems (displays + logic + actuators, sensors + processing + antenna) in a given technology and substrate. Both approaches require the implementation of complex integrated functionalities that required mixing different design disciplines and methods. Currently, there is not any single EDA tool capable of coping all those aspects that require not only the corresponding device modeling but also mixed-mode simulators, variability analysis and detailed layout extraction tools.

Big players in the EDA industry such as Synopsys, Cadence, or Mentor Graphics can cover almost all design aspects. Their tools allow very high design productivity at the cost of expensive licenses. Part of this design productivity comes from the fact that any given circuit or structure can be easily and quickly redesigned for a different technology or process variation thus strongly reducing circuit any redesign effort. Technology dependent tools are ready to use and the methods to add the information related to any OTFT or general TFT technologies are specified around the PDK concept [145]. However, those big players are not yet paying attention to specific tools for OTFT- or TFT-based systems. The main reason is that the process technology has a very wide range of choices, while existing valued market applications is much less compared to that of the silicon microelectronics industry as illustrated in Fig. 9.

Other EDA tools used for OTFT circuit design are as follows.

1) Other low-cost PC-based EDA tools (i.e., Tanner or PhoenixBV).
2) Tools coming from the display industry (i.e., Silvaco) that include a strong link with device level simulation.
3) The large set of tools coming from the printed circuit board industry that is weekly connected with simulation but allow checking geometrical and electrical design rules before sending the circuit for fabrication, and are much cheaper.
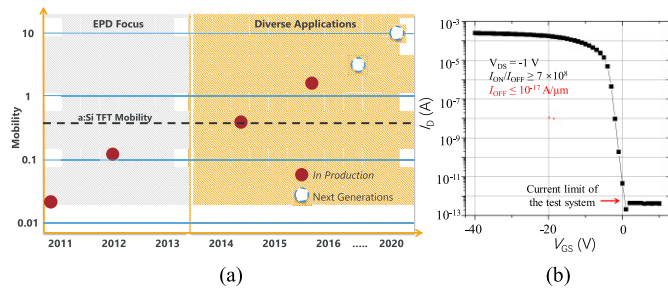
(a)   (b)

Fig. 10. (a) Performance roadmap in terms of mobility for the OTFT technology in FlexEnable. (b) Measured transfer performance of the current OTFT fabricated in FlexEnable with a channel length of 5 μm and a channel width of 50 000 μm.

4) Open-source or free tools (i.e., Glade, Klayout, Alliance).
5) There are still a high number of designs that are just being designed with graphic editors.

EDA tools are usually related with design methodologies that have been traditionally classified as device-based (or full-custom) and cell-based (or semicustom). Current OTFT circuits require low design effort compared with silicon ones [146]. Most of the implemented designs are still device based [23], [147], [148] so that designers and up by drawing the final circuit layouts. Nonetheless, there are several circuits that are already been built using cell-based design techniques that include some degree of automation in the placement and routing, such as standard-cells or gate-arrays [149]–[151].

A novel circuit design initiative is devoted to let designers use the capabilities of digital printing on top of TFTs built with other technologies for building circuits to improve their functional or performance characteristics by adding identification codes, calibration circuits, programmable memory or *ad hoc* arithmetic circuits. Examples are: 1) user-customizable logic paper with sea-of-transmission-gates of organic CMOS and inkjet printed interconnects [151]; 2) programmable logic circuits (PAL) for functional integrated smart plastic systems [106]; 3) print-programmable read-only memory [152]; and 4) inkjet-configurable gate arrays with high-resolution OTFTs and inkjet printed interconnecting dots [153].

F. Applications and Status of Industrialization

The OTFT backplane technology developed by FlexEnable (previously Plastic Logic) is the first and possibly only OTFT technology used in products today. The products are e-paper displays manufactured by Plastic Logic Germany (e.g., popSLATE, an iPhone cover containing a OTFT-driven flexible e-paper display). Within the past two years, the OTFT performance has risen to be above that of a-Si TFT for all key electrical parameters including mobility, stability and uniformity, opening up possibilities for a wide range of new applications. As shown in Fig. 10(a), the mobility of the OTFT is now about 1.5 cm^{2}V^{-1}s^{-1} at a channel length less than 5 μm. A separate but often less-discussed electrical benefit of OTFT is leakage current. Compared with a-Si TFTs, the OTFT can easily have leakage currents two or even three orders lower. Fig. 10(b) is the measured transfer curve of

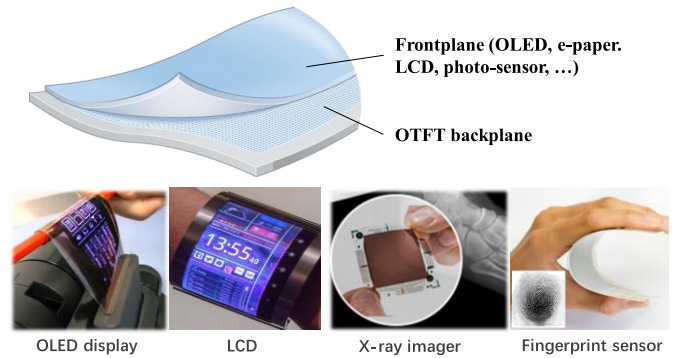OLED display   LCD   X-ray imager   Fingerprint sensor

Fig. 11. Illustration of the integration structure and the photographs of the developed flexible system applications based on the OTFT backplane technology from FlexEnable.

an OTFT with a channel width of 50 000 μm in order to measure the leakage. It can be seen that even with such a large channel width, leakage is still lower than the noise in the test system—indicating very low true leakage current less than 10^{-17} A/μm for the device. This very low leakage brings benefits to displays in allowing low-frame rate driving (power saving), and also to sensors, enabling greater sensitivity, which for applications like X-ray sensors means the use of lower doses. Besides the e-paper displays, a series of more advanced display and sensor applications have been demonstrated with this OTFT technology, as shown in Fig. 11.

In addition to array backplanes, simple OTFT circuitry is promising for bio-sensor applications. Most of the OTFT-based biosensors, including organic FETs and organic electrochemical transistors, are potentiometric transducers [19]. A little change in the effective gate voltage will lead to a pronounced channel current response. Therefore, due to their inherent amplification functions, good biocompatibility, high mechanical flexibility, and ease of miniaturization/integration, OTFTs have emerged as a versatile platform for biological applications. Recently, different types of biosensors, including enzyme [154], deoxyribonucleic acid [155], cells [156], neuron [157], and bacteria and protein sensors [158], [159], have been successfully developed based on the interactions between biological analytes and organic channel or gate electrode of an OTFT modified with specific biomolecules and functional materials. Although OTFT-based biosensors have not yet been commercialized, some devices including enzyme sensors may find big market in the future. For examples, glucose sensor is a very important healthcare product since the population of diabetes mellitus in the world increases every year. The prevalence of diabetes for all age groups worldwide was estimated to be 2.8% in 2000 and 4.4% in 2030 [160]. Currently, the operation of all of the blood glucose meters in the market is based on finger stick assays, which is painful and can cause stress to the patient. Therefore, developing noninvasive glucose meter with high accuracy becomes the trend of blood glucose determination. OTFT-based enzyme biosensors can be used for noninvasive glucose detection by measuring the glucose level in body fluid, which may have a huge market in the future [161]. Other enzyme biosensors, like uric acid and cholesterol sensors, are also very useful in healthcare products. Nevertheless, the commercialization of OTFT-based

biosensors relies on the development of fabrication techniques for mass production and the synthesis of biocompatible and stable OSCs specifically for biological applications.

III. CHALLENGES AND OUTLOOK

The above review shows massive progresses on all aspects of the OTFT technologies. However, to become a widely adopted technology for the envisioned applications, there are still lots of challenges ahead to be addressed. This part will try to clarify these key challenges.

First, in terms of materials, there is still lack of material stacks to be used for producing high performance, stable and uniform OTFTs in large area compatible processes. The current OTFT community is perhaps too focused on charge mobility of materials as a figure of merit. The processes and device structures used for testing the material performance are not for scalable manufacturing. A greater emphasis should be placed on other attributes such as uniformity, stability, manufacturability and short channel device performance. In addition, as highlighted by a recent paper, mobility estimation from nonideal FET current–voltage characteristics typical for OTFTs has been shown to produce values that are incorrect by an order of magnitude or more [54]. When the high performance does not translate into the expected performance in the types of devices used in manufacturing, then this reduces confidence of the technology as a whole. Possibly the figures of merit for materials and devices should be defined by the electronic design community since they are the ones who will produce designs in the technology that meets the specifications of end users. Moreover, many physical and chemical interactions between the OSC layer and other dielectric, metal and interfacial layer materials in the device stack are not only important for initial device performance but are critical for control of the device stability under electrical stress [162]. In addition to performance, material stacks also need to be developed for processing OTFTs to be able to meet the strict reliability test requirements, which are defined by applications. Deep understanding of the instability issues of OTFTs and finding the solutions to develop stable and reliable OTFTs is thus of great importance [163].

The challenge with device uniformity has been the other main hurdle to practical large-scale OTFT circuits [25], [28], [107], [164]–[166]. In the comparison between all printed OTFTs [107] and the vacuum processed ones of finely patterned electrodes [25], similar level of performance variations can be observed, indicating that the main source of variations in OTFT devices mainly comes from the OSC film. The large device performance variations lead to decreased circuit noise margin and thus poor yield. Therefore, to improve circuit yield, the device uniformity need to be improved by either molecule level design to reduce material disorder [46], [167] or developing processing techniques for better crystallization control of the OSC film [168].

Second, there is no standard material stacks, device /integration architectures, and manufacturing processes for the whole community to work with. Diversity of materials choices, device structures, and processes are advantages of OTFTs to provide a versatile technology platform. However, it also brings challenges to the whole community to work together to address the common technology issues and build an industry chain toward commercialization like that in silicon semiconductor industry. For different types of applications, the processing approaches would vary to have the optimal balance between the performance and the cost. For example, for high-resolution flexible display or imagers application, standard manufacturing and device integration architecture can be constructed based on the well-established processes in the display industry, including sputtering, photolithography, wet/dry etching, spin coating and slot-die coating. The large material research community can thus have clear objectives of matching the device integration and manufacturing processes, while achieving required performance. While the ongoing material and process research is valuable in tackling current and future device performance obstacles, the development of robust design tools require stable materials and processes. The development of industry standard OTFT compact models, and associated process/technology design tools is essential to lower the entry barrier for product designers. The design community will continuously add functionality and IP value which in turn leads to greater technology dissemination and adoption. Owning a strong design community will be able to speed up product development cycles, maximize the performance capability of the technology, and exploit the new applications based on the technology. Prerequisite to this is the development of manufacturing design rule manuals and standardized process design kits. Inbuilt in this are many challenges related to compact model parameter extraction templates, meaningful layout, design rule check tools and a seamless design automation flow.

An important advantage of OTFTs is that they can be manufactured by printing, eventually allowing a highly customized fabrication of organic and hybrid integrated circuits, especially when digital printing techniques are adopted, ultimately handing an on-demand electronics. This concept which has been developed at research level in the last one or two decades needs to face a reality where such tools that would allow this shift of paradigm in electronics fabrication, are not yet developed outside the laboratories. Therefore, printing OTFTs allowing design and custom fabrication of circuits needs more work on standardization of materials, components and processes, design tools and accessible fabrication tools.

The separation between fabs and fabless industries is popular for other mass market domains apart from the semiconductor industry (i.e., the traditional printing industry) but it is not for niche oriented domains (i.e., displays or micro electromechanical system). The integration of circuit with OTFTs seems to show that there will be room for mass production for a wide range of applications, as illustrated in Fig. 12. If this happens, fabs will open their technologies to the application-oriented industries by providing PDKs (geometric and simulation information) and clear cost models. Opening access to technologies will for sure boost and enlarge the applications since it will lower the entry barriers for those industries. Different initiatives have already set the basis for building this path [169], [170] and have demonstrated the feasibility of using this model to build complex systems.
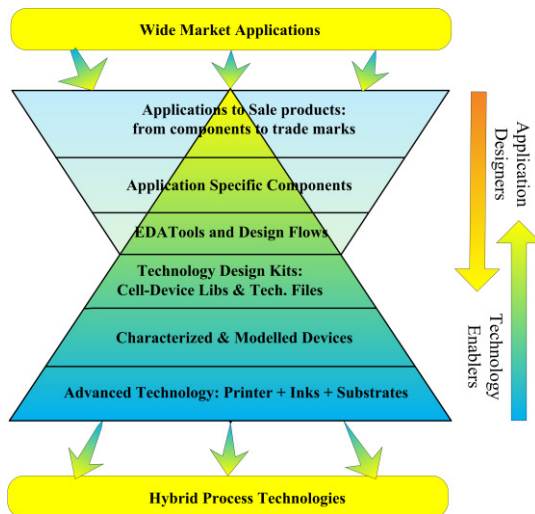
Fig. 12. Future view of the OTFT-based large area electronics industry with a wide set of products for different applications that profit from a wide range of hybrid technologies available for its implementation in an open horizontal business model through the integration of their PDKs into the EDA tools.

Third, tradeoffs between performance and large area low cost processing need to be much better balanced. Strong opportunities can be opened for OTFTs with a suitable combination of mass-scale processes and suitable performances. Clearly, these two goals require tradeoffs, since large-area manufacturing poses constraints for example on critical features, thus ultimately limiting performances. A clear challenge, therefore, is to develop methodologies characterized by a high patterning resolution, down to the micrometer size, while maintaining scalability, compatibility with cheap plastic foils and a reasonable throughput. Aggressive downscaling of features size to a sub-micrometer level may not be required, as back on the envelop estimations return tens of megahertz operation of OTFT with micrometer scale channels and mobility in the 1–5 $cm^2V^{-1}s^{-1}$ if capacitive parasitism is kept under control. Overall, the challenge in this respect can be pinned down to the control of the device footprint and capacitive parasitism, possibly benefiting from approaches previously adopted in established technologies, such as self-alignment, while maintaining a suitably high yield.

Another tradeoff is between reducing the operation voltage and having device structures compatible with large area solution-based processing. Most of those envisioned applications of OTFTs are portable or wearable, requiring the devices to be integrated in severely power-constraint electronic systems with battery or ac. field. This poses a stringent requirement on the operation voltage of the OTFT circuitry, which in principle should be scaled down to 3 V, or even below. However, for OTFTs over large area substrates, especially based on solution processed multilayer integration, the gate insulator layer needs to be thick enough (at least a few hundred nanometers) for the concern of device reliability and yield. Therefore, lots of work on using high-*k* gate dielectric material or even solid electrolytes to realize low voltage with a thick dielectric layer [81], [84]. The issue for high-*k* gate dielectric layer is that high-*k* dielectric materials could be unfavorable for carrier transport due to the broadening of the trap
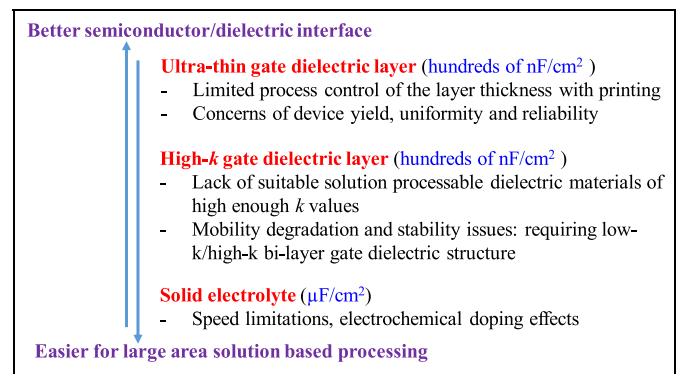

Fig. 13. Illustration of between and having device structures compatible with large area solution-based processing by using different gate dielectric technologies for reducing the operation voltage.

DOS at the semiconductor/dielectric interface by the formed dipole disorder [40]. The solid electrolyte can even induce electrochemical doping of the channel due to the presence of ions affect, causing reliability issues and slow operation speed [85]. As summarized in Fig. 13, for the conventional way of enlarging the gate dielectric capacitance to reduce the operation voltage, there is tradeoff between processability and performance requirements. A promising solution is to reduce the subgap DOS at the channel through solution processed OSCs, and thus, very small gate dielectric capacitance can be used to realize low operation voltage [77], [112]. This approach provides the possibility of using a wide range of low-*k* polymer dielectric materials in a relatively thick layer to achieve stable low-voltage OTFTs [69], [74], [75], [88].

Last but not least, focused applications needs to be clearly defined. The technology platform in FlexEnable (previously Plastic Logic) has demonstrated that there are no fundamental problems with the OTFT technology for commercialization. It is also shown that OTFT has huge market potential, and can completely change our view of where and how electronics is used in our daily lives. However, confidence in the OTFT technology might be increased if a greater number of fab or pilot lines existed with a predictable yield and uniformity. On the other hand, however, investments would not be put on constructing new fab or pilot lines or even upgrading existing fabs for OTFT manufacturing if no clear applications were seen.

Therefore, with a near-overwhelming list of applications (both existing and new markets), OTFT technology companies need, therefore, to focus on the right applications. Building partnerships with other parts of the supply chain is critical to building an ecosystem for the OTFT technology, and allows technology companies to focus on their respective areas of expertise.

IV. CONCLUSION

The review of research and development progresses in all aspects ranging from fundamental material and device research to manufacturing trials in last decades shows that solid basis has been formed for the OTFT technology to become commercially successful. However, to eventually become a widely

adopted technology for the envisioned applications, there are still lots of challenges ahead to be addressed. The first one is to develop OTFT material stacks capable of producing high performance, stable, and uniform OTFTs in large area compatible processes.

The second challenge would be how to define standard material stacks, device/integration architectures, and manufacturing processes to allow the whole community to work on the common issues, and also reduce the entry barrier for the design community. How to balance the device performance and the large low-cost manufacturability is also important to meet the application requirement. Finally, with a near-overwhelming list of applications (both existing and new markets), focused applications need to be clarified, from which different requirement on the device performance, uniformity, and manufacturing scale of OTFTs can then be defined. To address these challenges, the whole community needs clear application and technology roadmaps and also standards in terms of materials, device/integration structures, and processes to work together.

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