A Neural Probe with up to 966 Electrodes and up to 384 Configurable Channels in 0.13µm SOI CMOS

Carolina Mora Lopez, *Member, IEEE*, Jan Putzeys, Bogdan Cristian Raducanu, *Graduate Student Member, IEEE*, Marco Ballini, *Member, IEEE*, Shiwei Wang, Alexandru Andrei, Veronique Rochus, Roeland Vandebriel, Simone Severi, Chris Van Hoof, *Member, IEEE*, Silke Musa, Nick Van Helleputte, *Member, IEEE*, Refet Firat Yazicioglu, *Member, IEEE*, and Srinjoy Mitra, *Member, IEEE*

***Abstract*—*In vivo* recording of neural action-potential and local-field-potential signals requires the use of high-resolution penetrating probes. Several international initiatives to better understand the brain are driving technology efforts towards maximizing the number of recording sites while minimizing the neural probe dimensions. We designed and fabricated (0.13-µm SOI Al CMOS) a 384-channel configurable neural probe for large-scale *in vivo* recording of neural signals. Up to 966 selectable active electrodes were integrated along an implantable shank (70 µm wide, 10 mm long, 20 µm thick), achieving a crosstalk of -64.4 dB. The probe base (5×9 mm^2) implements dual-band recording and a 171.6 Mbps digital interface. Measurement results show a total input-referred noise of 6.4 µV$_{rms}$ and a total power consumption of 49.1 µW/channel.**

***Index Terms*—Active electrode, active probe, biopotential, implantable device, low-noise amplifier, multi-electrode array, neural amplifier, neural probe, neural recording.**

I. Introduction

Large-scale *in vivo* recording of neuron populations has emerged as a key approach towards understanding how neural networks in the brain work [1]. Microfabricated silicon neural probes have established as the dominant technology in this field and have achieved ever increasing densities and numbers of simultaneous recording electrodes while reducing the probe-shank dimensions for minimal tissue damage [2]–[10]. A high electrode density is crucial in order to increase the spatial resolution and thus the accuracy of identifying individual neurons from large populations [11]. A large number of simultaneously-recorded electrodes, on the other hand, increases tissue coverage and allows recording from many neurons spanning multiple brain regions, thus providing insight into specific behaviors and self-organized processes encoded by neuron ensembles [12].

Increasing the density and number of electrodes can be achieved by reducing the electrode area and pitch. This will, however, increase the electrode impedance and interconnect wire density thus deteriorating the signal crosstalk and increasing the sensitivity to electromagnetic interferences. To address these drawbacks, the active electrode concept was proposed in [7], where *in situ* buffering circuits (pixel amplifiers) were integrated beneath each electrode to locally transform the high electrode impedance and be able to drive the high interconnect density. This approach has enabled an almost threefold increase of the electrode number per cross-sectional area in [7] compared to prior non-active silicon probes [2]–[6], [8], [9].

The number of simultaneous recording electrodes is primarily limited by the number of parallel readout channels available and the maximum number of interconnect wires between the probe shank and the probe base. The number of interconnect wires is strictly limited by the shank width which determines the invasiveness of the probe. By using time-division multiplexing integrated in the shank, as many as 1440 parallel readout channels have recently been demonstrated [10]. However, the need for complex pixel circuits in this design resulted in a reduced noise performance and larger pixel area.

Implantable neural probes are targeted to record neural signals with amplitudes in the order of few µV to several mV and frequency spans from dc to a few kHz. Two different kinds of signals can be identified in a frequency band of 10 kHz: the local-field potentials (LFPs) in the low frequency range (< 1 kHz) and the action potentials (APs) in the high frequency range (~0.3-10 kHz). Neural signals present a *~1/f* frequency dependency [13], which means that the signals above 10 kHz are highly attenuated. Since the LFP signals can have much

Manuscript received August 16th, 2016; revised xxx xx, 2016. Financial support for this research undertaken at imec was provided by the Howard Hughes Medical Institute, the Allen Institute of Brain Science and the University College London with funding from the Gatsby Charitable Foundation and the Wellcome Trust.

C. M. Lopez, J. Putzeys, B. C. Raducanu, M. Ballini, S. Wang, A. Andrei, V. Rochus, R. Vandebriel, S. Severi, C. Van Hoof, N. Van Helleputte and S. Musa are with imec, Leuven, Belgium (e-mail: moralope@imec.be).

B. C. Raducanu and C. Van Hoof are also with the Electrical Engineering Department-ESAT, KU Leuven, Leuven, Belgium.

R. F. Yazicioglu was with imec, Leuven, Belgium. He is now with GlaxoSmithKline, Stevenage, UK.

S. Mitra was with imec, Leuven, Belgium. He is now with the School of Engineering, University of Glasgow, Glasgow, UK.

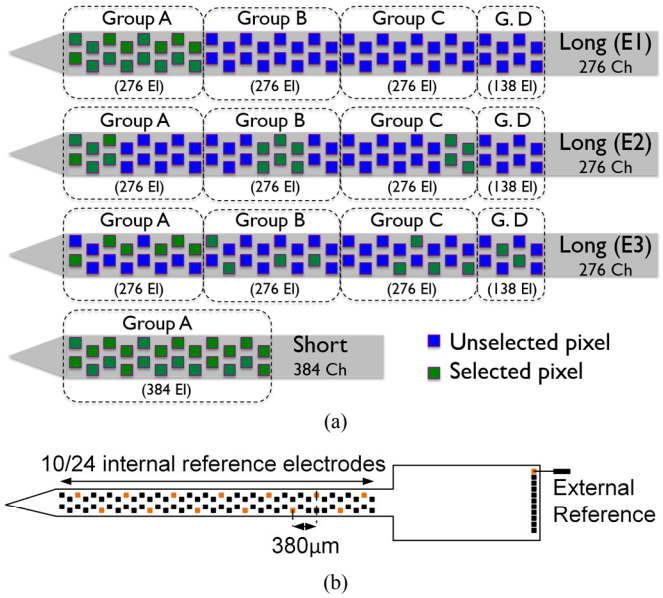


Fig. 1. Neural probe functionality. (a) Pixel selectivity examples for the long-shank probe: all consecutive electrodes in a group (E1), subgroups of consecutive electrodes at different depths (E2) and nearly randomly distributed electrodes (E3). All electrodes in the short-shank probe can be simultaneously read out. (b) Reference electrode selectivity concept.

larger amplitudes (i.e. up to 2 orders of magnitude) than the AP signals, it is important to provide appropriate low-noise amplification and sufficient dynamic range to accurately record both signals. Current state-of-the-art neural-recording chips focus on a single signal band [14], provide band separation [7], [15], [16] or record the full band with [17]–[19] or without [20] adjustable filter settings.

This paper presents an extended description of our previous work [21], in which we present an active neural probe with 384 configurable channels for high-density recordings in acute and chronic rodent studies. Up to 966 selectable, neuron-sized electrodes (12×12 µm^2) were densely packed along a narrow (70 µm) and thin (20 µm) implantable shank using integrated CMOS. This probe achieves the highest electrode density reported so far with more than twice as many electrodes per cross-sectional area compared to the state-of-the-art [7], [10]. The probe allows simultaneous recording from up to 384 electrodes, which is a more than sevenfold increase compared to [7]. A maximum of 384 dedicated interconnect wires are routed between the shank and the base, thus also reaching the highest interconnect density reported for silicon neural probes.

This paper is organized as follows. In Section II we describe the concept of the active neural probe and in Section III we explain the proposed architecture and the design of the main circuit blocks. The device fabrication process is outlined in Section IV. Section V provides high-level details of the headstage and system design. The measurement results obtained from both electrical performance characterization and saline experiments are presented in Section VI. Finally, Section VII states the conclusions of this paper.

II. Neural Probe Concept

The active neural probe consists of an implantable shank and a non-implantable base, both integrated in the same silicon substrate. Two different shank architectures were developed: a short 5-mm shank with 384 active electrodes (covering 3.84 mm) for mouse experiments, and a long 10-mm shank with 966 selectable active electrodes (covering 9.66 mm) for rat experiments. In both architectures, the electrode arrays are arranged in 2 columns with a tetrode-like layout. While in the short version all the electrodes can be recorded at once, a local switch matrix in the long shank provides flexibility to select up to 276 electrodes for simultaneous recording. This reduced number of simultaneously-recorded electrodes is due to layout limitations in the shank and it is discussed in Section IIIA. The electrode selectivity is described further in Section IIA. The active electrodes in this design provide low output impedance and therefore low pixel-to-pixel crosstalk [7]. Pseudo-differential amplification is achieved by using a similar reference pixel.

The probe base (5×9 mm^2), which has the same design in both architectures, contains an array of 384 recording channels to perform analog pre-processing and digitization of the neural signals. The unused 108 channels in the long-shank probe are left disconnected and can be powered off if it is desirable to save power. The reference signal of each channel can be selected independently from 11 available options as described in Section IIB. A digital interface enables the configuration and calibration of the probe, as well as the transmission of the digitized neural data.

A. Pixel Selectivity

The electrodes in the long-shank probe can be selected in groups or spread along the shank in a pseudo-random manner, as represented seen in Fig. 1a. The 966 pixels (i.e. *in situ* amplifiers under each electrode) in the shank can be virtually divided in 3 groups of 276 pixels each (i.e. groups A-C) and one half-group of 138 pixels (i.e. group D), which all share the 276 recording channels. Therefore, each channel could be connected to 3 or 4 pixels, but only one pixel can be connected at a time. The short-shank probe, however, includes only one group of 384 pixels and does not require selectivity.

In the example E1, 276 consecutive pixels are all selected from a same group, covering a length of 2.76 mm. This can be useful in experiments that need simultaneous recordings from a large single brain area. The example E2 shows how subgroups of adjacent pixels could be selected from three different groups, thus enabling the recording from different brain areas simultaneously. In this case, the pixel subgroups must have different positions in the array so that they are connected to different channels. The last example (E3) shows a pseudo-random selection of pixels, all connected to different channels.

B. Reference Selection

The reference signal of each channel can be selected independently from 10 (short shank) or 7 (long shank) of the internal electrodes or an external electrode. As represented in Fig. 1b, the electrodes that can be selected as an internal reference are distributed uniformly every 380 µm in both shank architectures. Therefore, 10 of the 384 recording electrodes in

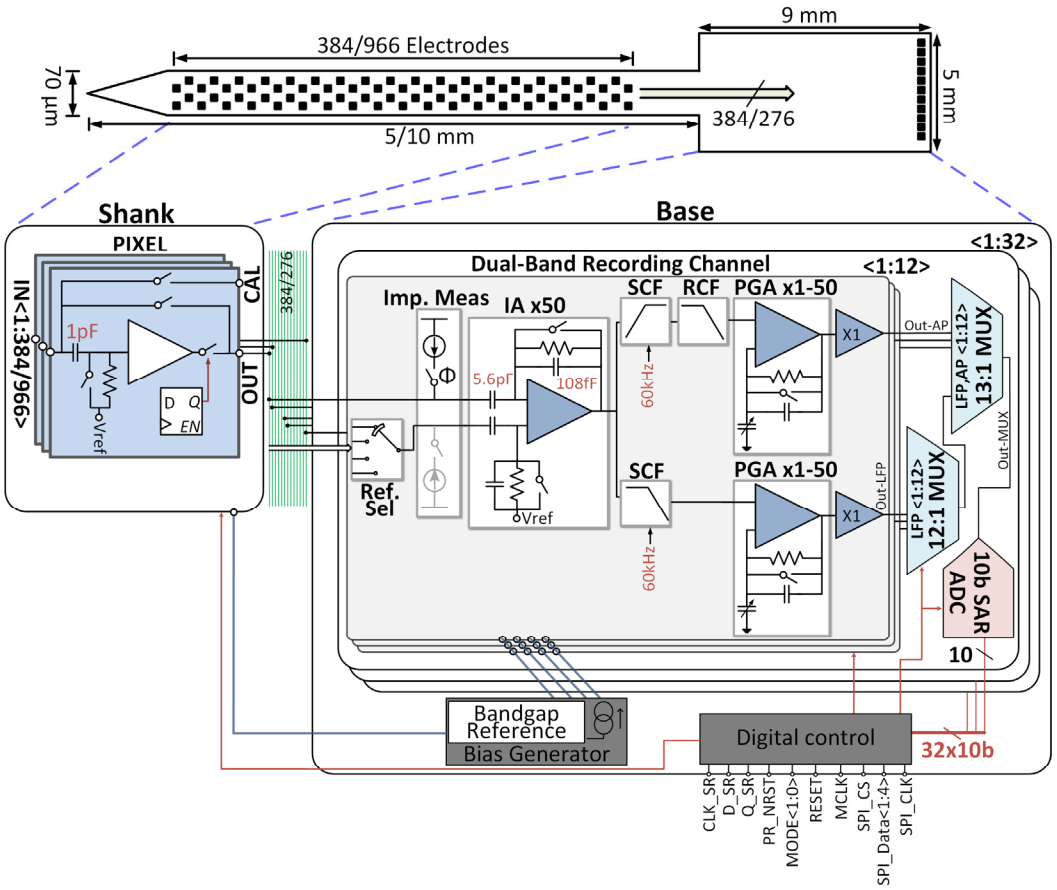


Fig. 2. High-level system architecture of the proposed active neural probe (pixel schematic corresponds to the long-shank version). The channel implements a band splitting technique to record both AP and LFP signals with independently programmable gains.

the short shank can be used as internal references, while 24 of the 966 (i.e. 7 in each group and 3 in the last half-group) selectable recording electrodes in the long shank can be used as internal references. The selectivity of the internal references works in the same way as the selectivity of the recording electrodes. However, in this case, multiple internal references could be selected simultaneously to form a distributed reference electrode. The flexibility of each channel to select independently its reference signal may help improving the common-mode rejection (CMR) of the pseudo-differential input stage. This is because the nearest reference can always be selected for every recording electrode.

An external electrode can be connected to one of the probe input pads. The signal provided by this electrode is also buffered with a reference pixel located at the beginning of the shank (i.e. probe neck) so that it can match better the recording pixel and, therefore, improve the CMR.

III. Chip Architecture

Fig. 2 shows the circuit architecture of the neural probe. The implantable shank consists of an array of 384 or 966 active pixels, for the short and long probes, respectively, connecting to the surface electrodes. An additional pixel is used to buffer the external reference electrode. The 384 channels in the base allow dual-band recording by splitting and amplifying the AP (0.3/0.5/1-10 kHz) and LFP (0.5-1000 Hz) bands with channel-independent programmable gains (50-2500 V/V), thus making optimal use of the analog-to-digital converter (ADC) dynamic range. Each channel also includes a 1-kHz square-wave current generator for simultaneous impedance measurement of all the selected electrodes. Both bands in a group of 12 channels are combined by using two time-division multiplexers (MUXs) that sample the AP and LFP signals at 30 kS/s and 2.5 kS/s, respectively, thus optimizing the output data rate. A 10-bit successive approximation register (SAR) ADC follows the MUX. A digital control block transmits the data from the 32 ADCs through four serial peripheral interface (SPI) data lines at a combined rate of 171.6 Mbps. The main constraints that governed our design decisions are explained below, together with a detailed description of some of the main circuit blocks.

A. Layout Constraints

The probe dimensions were decided based on two main restrictions: i) the target application and system requirements, and ii) the processing limitations. For the target application, two different shank lengths were chosen so that the impact of the length on both rat and mouse experiments could be studied. The width of the shank was chosen to minimize the tissue damage during implantation, while still being able to accommodate the desired number of signals lines (i.e. number of simultaneous recording channels). Also, the width of the probe base was limited to minimize the dimensions of this non-implantable rigid silicon piece. Due to the lithographic limitation on reticle

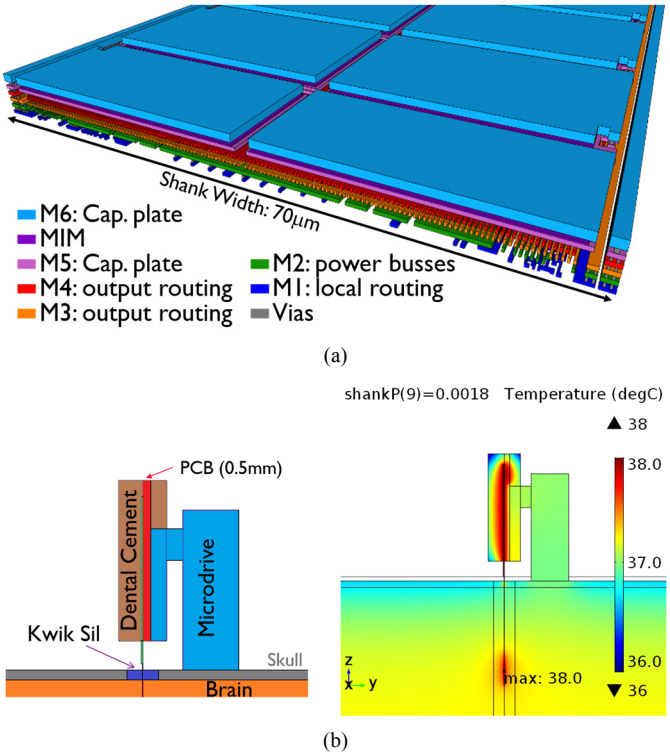


Fig. 3. Design constraints. (a) Layout constraints in the long-shank due to the limited width and number of metal layers. (b) Schematic of the 3D FEM model used for thermal simulations (left) and simulation results showing the heat distribution in the probe shank and base (right).

size (~ 22 mm × 22 mm), there was a trade-off between the maximum length of the shank (i.e. a larger sensing area) and the length of the base (i.e. higher number of recording channels). A maximum shank length of 10 mm was considered adequate for rat experiments. The rest of the reticle length is used to fit the tapered probe neck (1 mm) and the base (9 mm).

To simplify the packaging effort and minimize the dimension of the probe-holding printed-circuit board (PCB), the number of I/O pads were minimized and placed only on one side of the probe base. This last restriction sets a very important layout constrain in this design. The need to distribute power and control signals from the pads to the opposite-side of the base and to the tip of shank requires metal wires that can be up to 20 mm long. This could cause severe voltage drops in the power/ground busses which had to be carefully considered during floorplan and design.

Other important constraints that governed the design and the layout of the pixel are: the limited shank width, the pixel area (i.e. electrode pitch) and number of simultaneously-recorded electrodes. Therefore, as shown in Fig. 3a, a tradeoff between local routing, power distribution and number of signal wires had to be made in this design. In the chosen 6-metal process (M1-M6), the local routing of the long-shank pixel was completed with only one metal layer (M1), all the power/reference distribution was restricted to only M2, the routing of the pixel outputs was done in two layers (M3 and M4) and, finally, the metal-insulator-metal (MIM) capacitors occupied the two top layers (M5-M6). Due to the limited shank width, only 276 signal lines could be accommodated in the two metal layers for the long-shank probe. In the short-shank probe, however, the pixel did not require the selection circuits and this space was used to accommodate additional signal lines in M1 and M2, reaching a total of 384.

B. Power Constraints

The power constraints in this design were set by the limited brain tissue heating (< 1°C) allowed in this application [22]. In order to prevent excessive heating beyond these limits, we performed thermal finite element method (FEM) simulations using Comsol Multiphysics® software to determine the upper limits of power dissipation for the probe base. These simulations follow a similar approach as the one presented in [22]. For our work, we considered the worst-case scenario where all the power dissipation in the shank is concentrated in one pixel group (i.e. 276 consecutive pixels selected). To make the simulations realistic, we included several means of heat sink: the brain, some dental cement covering the probe base outside the brain, a holding PCB with metal planes and a microdrive. A schematic of the 3D FEM model is shown in Fig. 3b (left).

For the FEM simulations, the power dissipation of the whole shank was fixed to the power required to achieve the desired noise performance in the pixel amplifiers. Based on our noise simulations, this power was 6.6 µW/pixel, corresponding to a whole-shank power dissipation of 1.8 mW for the 276 pixels in a group. After setting the power dissipation in the shank, the goal of the FEM simulations was to find the maximum power dissipation allowed in the probe base before the brain tissue heating increases beyond the safe limits. The simulation results in Fig. 3b (right) show that, for this shank power consumption, it is possible to maintain the tissue heating below 1°C if the power dissipation in the base is kept below 20 mW. This limit was used to set the power specs of the different building blocks in the probe base, including the digital control. Since it is difficult to validate these simulation results with actual thermal measurements in a realistic setup and with the required sensitivity, we are currently investigating the integration of thermal sensors for a future shank design.

C. Pixel and Shank Design

Since the pixel is the input stage of the analog front-end and is located in the shank, it was designed under stringent area, power and noise constraints. As seen in Fig. 2, the pixel contains an AC-coupled source-follower, which uses a pseudo-resistor to set the dc input voltage and define a very-low-frequency high-pass corner. The pixel input can also be accessed to apply a common calibration signal or to measure the electrode impedance. A local shift register (SR) controls the pixel selectivity and connects to the adjacent pixels to form a single SR chain in the shank.

Unlike [7], the pixel is implemented as a source follower to further reduce the output impedance and crosstalk. This also reduces ambient light-sensitivity effects observed in the previous common-source architecture. Metal shielding of sensitive components and guard rings around the pixels were also implemented to further reduce the light effects. The entire

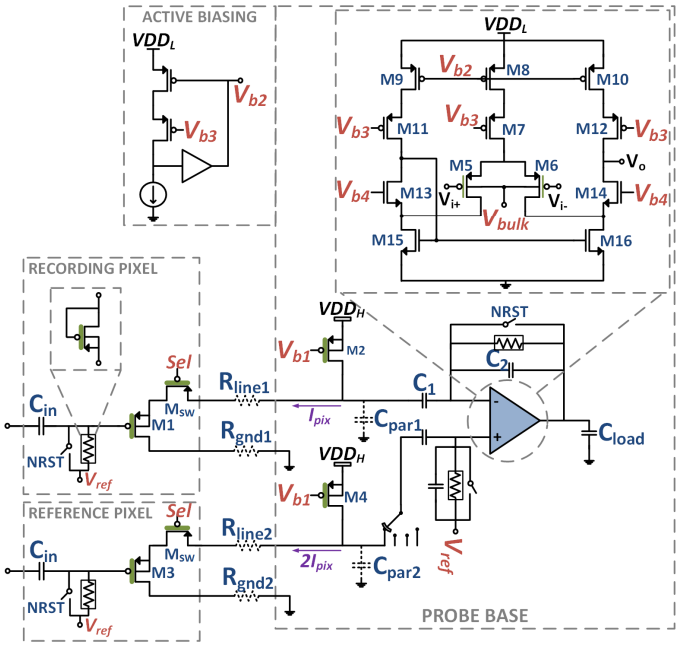


Fig. 4. Detailed circuit schematics of the recording and reference pixels in pseudo-differential configuration and the IA. The M_1-M_6 devices and the pseudo-resistors are implemented with thick-oxide transistors.

recording pixel occupies an area of 20 × 30 µm^2.

The schematic of the pixel and the subsequent instrumentation amplifier (IA) are shown in Fig. 4. The bias transistors of the source followers ($M_{2/4}$ = 30µm/30µm) were placed in the probe base to reduce the pixel area and power dissipation (i.e. only a fraction of the supply voltage drops across $M_{1/3}$ = 120µm/0.65µm, leading to a power reduction of 30%). This also allows to use a single switch (M_{SW} = 24.2µm /0.3µm) for both selecting or powering down the pixel. Since the bias current also flows through this output switch, its flicker noise contribution could become significant compared to the low targeted noise. To mitigate this effect, the size of M_{SW} was maximized within the area constraints.

Due to the high gate leakage of the standard transistors in this technology, the input and bias transistors of the source follower are implemented with thick-oxide transistors. This eliminates gate shot-noise components and minimizes the current flowing through the pseudo-resistor, thus keeping the input-node voltage and the high-pass-corner frequency stable. The pixel is supplied with 1.8 V (VDD_H) to accommodate the higher headroom voltages required for the thick-oxide transistors.

The limited width of the power and ground busses running along the shank resulted in unwanted power-supply voltage drops and ground shifts towards the tip of the shank, affecting the biasing of the source followers. These unknown supply voltage drops can be as large as 100 mV (depending on the pixel position within the shank) and were taken into account during corner simulations. Based on simulations, the supply and bias (V_{ref}) voltages were carefully chosen to ensure proper biasing of the thick-oxide transistors along the whole shank and over process, voltage and temperature corners, while limiting the power consumption and the noise. Dynamic supply-voltage drops, which can occur during the simultaneous digital activity of the pixels (i.e. SR chain programming), were greatly reduced by using MOS decoupling capacitors to fill the empty areas of the pixel and also in the shank tip. Monte-Carlo simulations were also performed to make sure that the remaining supply voltage shifts were not causing timing violation in the SR chain.

An additional pixel is added at the beginning of the shank to buffer the external reference electrode signal. This pixel or one of the predefined recording pixels can be selected to act as a reference in the pseudo-differential configuration. Depending on the selected recording and reference electrodes, the two pseudo-differential signal paths can have unequal resistive and capacitive (e.g. one reference pixels can be connected to several channels) loads. The noise degradation caused by this mismatch was mitigated by increasing the reference pixel bandwidth (i.e. doubling its bias current), thus achieving sufficient common-mode noise suppression. This optimization was done by simulating a worst-case scenario in which one reference pixel is connected to all the 384 channels. The CMR also depends on the reference pixel choice due to the load mismatch and the possible power-supply voltage mismatch caused by the voltage drops along the shank. The best CMR is achieved when both the recording and the reference pixels are closely located.

D. Recording Channel Design

The channel architecture consists of (see Fig. 2): a square-wave current generator that can be used for electrode-impedance measurements, an IA with a fixed gain of 50 V/V, two analog filters to separate APs and LFPs into two different channel paths, two programmable-gain amplifiers (PGAs) providing gains in the range 1-50 V/V and two output buffers to drive the subsequent analog multiplexer and ADC. The two AP and LFP channel paths are amplified with band- and channel-independent gain settings. The recording channel achieves an input-referred noise of 5.5 μV_{rms} and 8 μV_{rms} in the AP (0.3 - 10 kHz) and LFP (0.5 - 1000 Hz) bands, respectively, and has a total power consumption of 23.4 µW.

- *Instrumentation Amplifier*

The IA, which is shown in Fig. 4, is implemented as a folded-cascode operational transconductance amplifier (OTA) with capacitive feedback (C_1/C_2 = 50). Pseudo-resistors are used to set the dc voltage at the inputs of the OTA and to implement, together with the feedback capacitor, a high-pass filter with a corner frequency lower than 1 Hz. Since the preceding stage does not provide gain, the noise of this block must be minimized. The IA consumes 18.6 µW and dominates the total power consumption of the channel.

To mitigate the gate-leakage issues at the input nodes, the input transistors of the OTA ($M_{5\text{-}6}$) as well as the pseudo-resistors are implemented with thick-oxide transistors, while the other transistors in the OTA ($M_{7\text{-}16}$) are implemented with standard devices. Different to the pixel, the IA and the rest of the channel are supplied with a low voltage (VDD_L = 1.2 V) to maintain the total power consumption within the budget. To enable the combination and correct biasing of both high-V_t thick-oxide transistors and standard transistors, we used forward body biasing in the input transistors (V_{bulk} = 0.6 V) to lower their V_t while ensuring low junction-diode forward

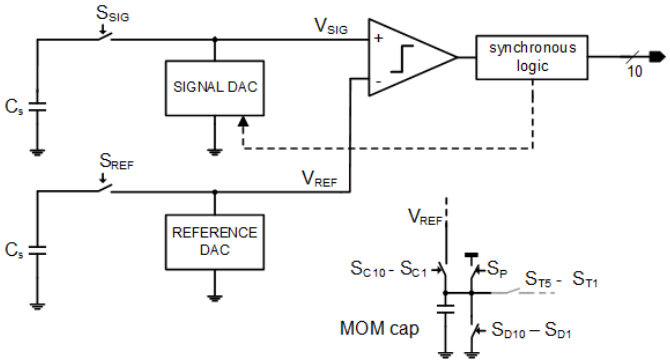


Fig. 5. Simplified schematic of the charge-sharing 10-b SAR ADC and details of a DAC unit (bottom right).

current. With this technique, it is possible to keep all the transistors in saturation over the process corners without degrading the IA performance. A potential disadvantage of this technique is that the junction-diode forward current and the threshold voltage of the input pair are dependent on the input common-mode signal. However, this does not represent an issue for the expected ac input common-mode signal at this stage (i.e. max. 10 mV).

Since all the 384 IAs share a common voltage biasing circuit, even small individual gate leakages add up to a considerable amount of current that is sufficient to pull up the bias voltage significantly. Active biasing was applied to the large current-source devices ($M_{8\text{-}10}$) to mitigate this effect by increasing the driving capability of the bias source. This technique was also used for biasing all the other amplifiers in the channel.

- *Analog Filters*

A switched-capacitor (SC) architecture was chosen for the band-splitting filters inside the channels (SCF blocks in Fig. 2) to provide low channel-to-channel variation of the corner frequencies. The band-limited IA (i.e. bandwidth is ~15 kHz) performs the antialiasing function for the SC filters running at 60 kHz. Since the neural signals present at frequencies >10 kHz are very small due to their *1/f* nature, no significant signal aliasing is caused by the SC filters. The effect of noise aliasing, verified in both simulations and testing, is also negligible.

A first-order passive high-pass SC filter with a programmable corner frequency of 300, 500 or 1000 Hz is used for the AP signal path. This filter is followed by a buffered first-order low-pass RC filter (RCF block in Fig. 2) with a cutoff frequency of 10 kHz which is employed as an anti-aliasing filter before the channel multiplexing. The LFP signal path uses a first-order passive low-pass SC filter with a cutoff frequency of 1 kHz.

- *Programmable Gain Amplifier*

The PGA is a non-inverting closed-loop amplifier with capacitive feedback. In order to set the dc voltage of the negative OTA's input node, a pseudo-resistor is used in the feedback loop. This amplifier is designed to have rail-to-rail input and output swing, low distortion and an appropriate gain range to provide additional amplification after the IA. Therefore, a complementary folded-cascode architecture with a second stage was chosen for the OTA. A programmable capacitor array with 8 settings enables the gain programmability (i.e. 1, 2.5, 5, 10, 20, 30, 40 and 50 V/V). This programmability is independent for each channel and signal band, and requires 6 bits per channel (for two PGAs). The power consumption of this block is 0.5 µW.

- *Output Buffer*

The channel output buffer provides rail-to-rail input and output swing, low distortion and good driving capability to drive the subsequent MUX and ADC at the required settling time. A class AB amplifier offers the best compromise between current capability and distortion. In this design, the Hogervorst architecture [23] has been used, which consist of a rail-to-rail input stage, a summing circuit and a rail-to-rail class-AB output stage. The amplifier is compensated by including cascode stages in a Miller loop. This block consumes a quiescent power of 1.3 µW and provides a maximum current capability of 1 mA.

E. ADC Design

SAR ADCs are one of the preferred choices for bio-potential recording applications due to their suitable resolution and frequency ranges, and their low power dissipation [14], [17], [18]. In this design, the AP and LFP signals of 12 channels are multiplexed to one 10-bit SAR ADC running at a sampling rate of 390 kHz. Since we are splitting the AP and LFP signals into two different channels that can be amplified with different gains, the dynamic range requirements for the ADC can be relaxed, leading to power and area savings. Therefore, a resolution of 10 bits is sufficient to digitize both neural signals in this architecture. The design of the digital-to-analog converter (DAC) is fundamental to a SAR ADC and generally determines the overall area and power requirement. Hence, a metal-oxide-metal (MOM) capacitor based, charge-sharing DAC [24] is chosen due to its low-power and low-area properties. The chip contains 32 ADCs distributed along the base, which draw significant switching current from the power supply. In this synchronous SAR architecture, the switching of all the comparators happens at the same time, without causing crosstalk among the ADCs. This might introduce a constant error over all comparators which can be canceled out later. The charge-sharing architecture ensures that all the charge required for the DAC is drawn at the beginning of the conversion cycle, and only discharges take place during the SAR algorithm. Since the DACs are completely disconnected from *VDD* during a conversion cycle, this choice mitigates the effect of any possible supply loading during synchronous comparison.

This architecture (Fig. 5) does not require a dedicated reference voltage, and the reference DACs of two consecutive ADCs share their charges (one pre-charged to *VDD* and the other discharged to *GND*) at the beginning of the conversion cycle. Similarly, the sampling capacitor (C_S) is added in parallel with the signal-DAC, whose units are pre-charged to *VDD* (switch S_P) and signal-dependently discharged (S_{D10}-S_{D1}).

A MOM capacitor of 256 fF is used for the most-significant-bit (MSB) of the DAC, and the size of the four subsequent capacitors decreases geometrically (e.g. 128 fF, 64 fF, etc.).

However, for the last 5 bits, the size of the capacitor is kept constant (16 fF) while the pre-charge voltage is decreased (e.g. *VDD*/4, *VDD*/8, etc.) by sharing the charge through switches S_{T5}-S_{T1}. This prevents the unit capacitor for this 10-bit ADC from becoming too small (i.e. 0.5 fF) and sensitive to parasitic effects that may degrade the performance.

In order to ensure that all the ADCs have a uniform transfer function across the chip, the architecture includes a few control bits that can be used to fine-tune the slope and offset of each ADC separately. The ADC transfer curve can be checked during the calibration phase and the tuning settings can be locally stored for future operation.

F. Digital Control

The digital-control block provides control of the SC filter, MUX and ADC operations, enables the programming of the internal SR chains in both the shank and base, and implements a SPI interface to serialize and transmit the parallel output data of the 32 ADCs. Other functionality includes the control of the square-wave current sources for impedance measurement and the control of the probe test modes.

An input master clock with a frequency of 93.6 MHz is used to derive all the required internal clocks. This clock is generated by an external oscillator located in the system headstage (see Section V). The master SPI interface provides an output clock at 46.8 MHz for synchronization with an external slave device and four data lines where the output data of the 32 ADCs are serialized with a combined effective data rate of 171.6 Mbps. The SPI output data is divided in 110-bit frames, and a frame counter is provided for external synchronization. The SR programming also employs a serial protocol with a clock rate of 500 kHz.

IV. Device Fabrication

The probes were fabricated using a 6-metal-layer 0.13-µm SOI Aluminum CMOS technology and a 200-mm fab-compatible post-CMOS process. Fig. 6 shows the chip photographs with details of the base and shank circuit blocks. Fig. 7a shows a singulated final probe with highlights of the shank tip (Fig. 7b) and rounded neck (Fig. 7c). The shank is 10-mm long and 70-µm wide. A reliable shank thickness of 21.8 ± 0.3 µm (Fig. 7d) and low bending of < 100 µm were achieved by combining Si_3N_4 stress compensation with wafer backside thinning and deep Si etching. The deep Si etch process was optimized to achieve very smooth shank etch walls. The tip has a length of 300 µm and a sharp opening angle of 13.3°, a geometry targeting low tissue damage [25]. The probe base area and thickness are 5 × 9 mm^2 and 420 µm (Fig. 7c), respectively. The thick base provides stability during automated probe assembly.

A scalable and CMOS-compatible process was developed to achieve the low-impedance and biocompatible [26] TiN electrodes (Fig. 7e). The 12 × 12 µm^2 electrodes are arranged in a tetrode-like configuration with center-to-center distances of 32 µm, 25.5 µm and 20 µm to neighboring sites, as shown in Fig. 7b. The grid-like configuration of the electrode vias (Fig. 7e) connecting the TiN electrodes with the underlying

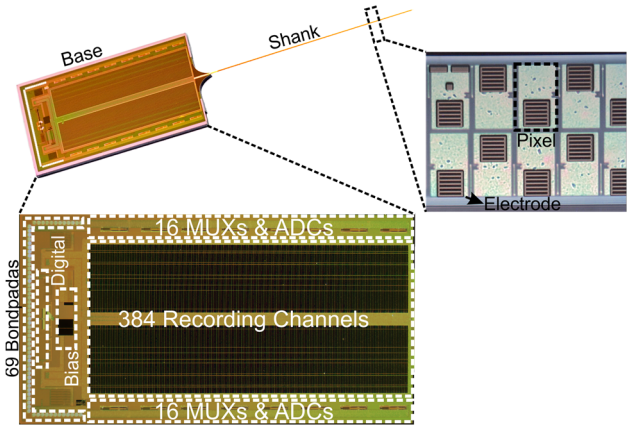


Fig. 6. Die photo of the active neural probe. The dimensions of the long shank are 70 µm × 10 mm, with a thickness of 20 µm. The probe base occupies a total area of 5 × 9 mm^2, with a thickness of 420 µm.

electronics increases the effective electrode area and lowers the contact resistance by enhancing the TiN deposition conformity over the via sidewalls. The vias are parallel to the shank axis across the whole array. The average electrode impedance at 1 kHz measured with dedicated test electrode arrays in phosphate-buffered saline (PBS) of pH 7.4 was 154 ± 9 kΩ (n = 1265) immediately after immersion and 166 ± 11 kΩ after 8 weeks soaking in saline.

After post-CMOS processing, the final probes are wire-bonded onto custom flexible PCBs (Fig. 8). Only 52 of the 69 bondpads are required during normal operation, while the remaining 17 are used for verification purposes and are not wire-bonded. The probe base was covered by a metal-coated Si spacer that acts as a light-shield and reference surface during implantation. The bond-wires are finally sealed in a black bio-compatible epoxy (Master Bond EP42HT-2MED).

V. Headstage and System Design

Due to the size and power dissipation requirements of the probe, certain functionality is pushed towards a small-size PCB called a headstage (Fig. 8a). The probe, along with an electrically-erasable programmable ROM (EEPROM) memory, is wire-bonded on a flexible PCB with rigid ends, which attaches to the headstage using a zero insertion force (ZIF) connector (Fig. 8b). The small headstage (20 × 16 mm^2, 1.1 g) connects to a back-end field-programmable gate array (FPGA) board through a 5m, flexible, dual micro-coax cable. The micro-coax cable is used for power delivery to the headstage and for data communication. The cable is selected for maximum flexibility and low weight (3.5g/m), to minimize the strain in freely moving animal experiments.

The data communication is ensured through a dedicated gigabit multimedia serial-link serializer chip (MAX9271) located in the headstage and its corresponding de-serializer (MAX9272A) located at the back-end PCB. The serializer provides a high-bandwidth unidirectional connection used for streaming the neural data, as well as a low-bandwidth bidirectional link used for controlling and programming the neural probe. The headstage contains a small FPGA which can

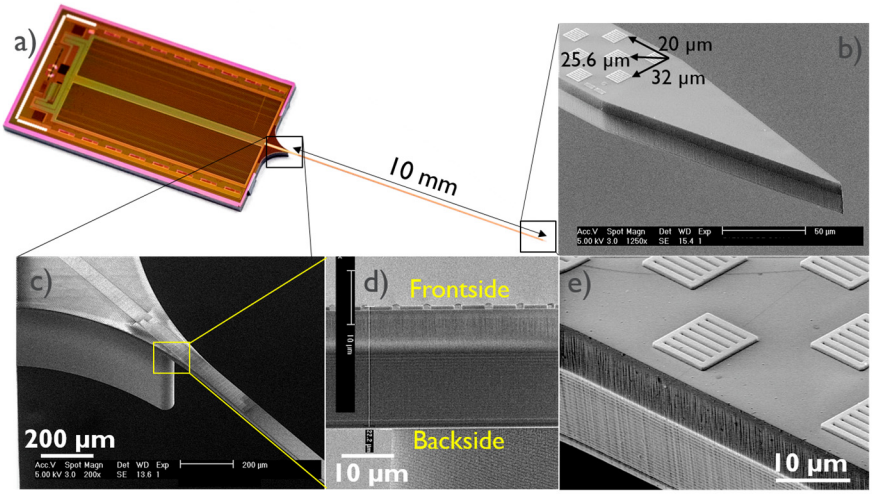
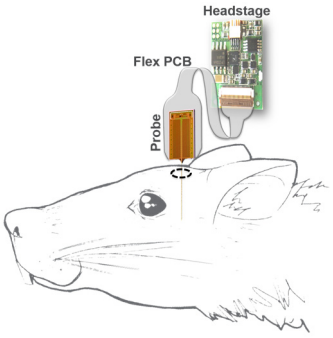
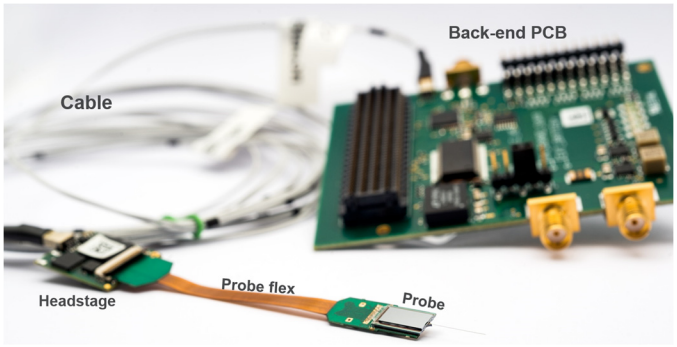


Fig. 7. Details of the probe fabrication. (a) Singulated neural probe device after post-CMOS processing. (b) Details of the shank tip and electrode arrangement. (c) Details of the probe neck and thick base. (d) Details of the uniform shank thickness. (e) Details of the TiN electrodes and via grids.



(a)



(b)

Fig. 8. System design. (a) Schematic drawing of the implanted probe connected to a headstage PCB. (b) Picture the complete recording system.

configure the neural probe. It also generates the required clocks and analog-calibration signals through a dual DAC. Furthermore, it provides access to the dedicated EEPROM containing the calibration parameters unique to each probe. Multiple low-noise, low-drop-out regulators located on the headstage are used to generate the required power supplies for the headstage and the probe.

The back-end part of the system is comprised of an off-the-shelf FPGA development board (Xilinx KC705, not shown) with a mezzanine PCB attachment containing the de-serializer chip (Fig. 8b). A Gigabit Ethernet connection is used between the system and a PC to stream the data and control the probe. The onboard FPGA provides data buffering and preprocessing, as well as sufficient resources for closed-loop neuroscience experiments.

VI. Experimental Results

A. Performance Measurements

After post-CMOS fabrication, the performance of the neural probes has been measured using a custom test PCB for bench tests. The circuits were battery-powered and shielded with a Faraday cage during experiments at room temperature (~22°C). A HP3562A dynamic analyzer was used to measure the channel input-referred voltage noise spectrum and transfer functions. The other parameters were measured through the digital interface using a National Instruments PXI 6544 data acquisition card to interface with the PC.

Table I compares the measured performance of our probe with the state-of-the-art. When first reported [21], this work achieved the highest number of electrodes in a single shank (966), the lowest cross-sectional-area coefficient (CSAC = 1.45 µm^2, corresponding to the shank cross-sectional area divided by the number of electrodes in the shank) [7], and the highest number of recording channels (384) integrated in the same probe substrate. The number of electrodes and channels have been recently surpassed by the work of Raducanu *et. al.* [10]. However, this probe continues to have the lowest CSAC, which indicates a potentially lower invasiveness with respect to the number of sites available for recording.

The long-shank crosstalk at 1 kHz was measured with a dedicated test structure in which 179 pixels were used as aggressors to one grounded victim pixel. The measured shank crosstalk is -64.4 dB (i.e. 0.06%), which is ~20 dB lower compared to [7] thanks to the lower output impedance of the pixels. The channel-to-channel crosstalk in the base of the long-

TABLE I
MEASURED PERFORMANCE CHARACTERISTICS AND COMPARISON TO PRIOR ART

Parameter	*Measured Values*									
	[8]	*[9]*	*[18]*	*[3]*	*[5]*	*[4]*	*[7]*	*[10]*	*This work*	
Probe Shank										
No./Type Electrodes	334 Passive	200 Passive	--	8 Passive	64 Passive	257 Passive	455 Active	1356 Active	**384 Active**	**966 Active**
Electrode Area [μm^2]	707	81	--	100	108	1963	78.6/491	400	**144**	**144**
Electrode Pitch [μm]	30	11	--	100	24	60	35	22.5	**20**	**20**
CSAC [μm^2]	11.98	3.75	--	127.5	30.55		10.99	3.7	**3.65**	**1.45**
Total Power/El [μW]	--	--	--	--	--	--	3.6	3	**4.7**	**4.7**
Crosstalk [dB]	--	--	--	--	-84	--	-44.8	-63	**--**	**-64.4**
Probe Base (Recording System)										
No./Type Channels	16	1000*	100	8 Integrated	64 Hybrid	128** Hybrid	52 Integrated	678 Integrated	**384 Integrated**	**276 Integrated**
Gain	--	--	400/600	1000	194	70.8	30-4000	50-2500	**50-2500**	
HP Corner [Hz]	--	--	0.25	300	1.3	1	0.5/200/ 300/500	0.5/300/ 500/1000	**0.5/300/ 500/1000**	
LP Corner [kHz]	--	--	2.5-10	10	6.4	10	0.2/6	0.3/0.5/ 1/8	**1/10**	
THD	--	--	0.53% @ $1mV_{pp}$	--	--	--	1% @ $18mV_{pp}$	--	**0.4% @ $10mV_{pp}$**	
CMRR/PSRR [dB]	--	--	73/80	--	83/84	--	60/76	--	**>60/>70**	
ADC Resolution [b]	--	--	9	5	--	--	10	10	**10**	
Sampling Rate (kS/s)	--	--	200 (10 Ch)	160 (8 Ch)	--	--	120 (4 Ch)	400 (20 Ch)	**390 (13 Ch)**	
Full probe										
Supply Voltage [V]	--	--	0.45	3	3	--	1.8	1.2/1.8	**1.2/1.8**	
Total Power/Ch [μW]	--	--	0.94***	94.5	351.6	39.1	27.84	45	**49.06**	
Total Area/Ch [mm^2]	--	--	0.25	0.625	0.45	--	0.19	0.12	**0.12**	
Input Noise (μV)	--	--	3.2 (1Hz-10kHz)	8.9 (300Hz-10kHz)	2 (1Hz-6.5kHz)	3.7 (1Hz-10kHz)	3.2 (300Hz-6kHz)	12.4 (300Hz-7.5kHz)	**6.36 (300Hz-10kHz)**	

* In a 5-shank arrangement
** In a 16-shank arrangement
*** IO digital power not included in this number.

shank probe was also measured for a worst-case scenario in which 275 channels acted as aggressors to one victim grounded channel. The measurement results show a base crosstalk of -37.4 dB.

The total power consumption of the long-shank probe is 18.84 mW (i.e 1.31 mW consumed at the shank and 17.53 mW at the base), which was measured during recording operation with the SPI lines connected to a load of ~4 pF and with all the 384 channels powered on (even when only 276 are actually connected to the pixels). From this power, 6.12 mW are consumed by the digital-control block to transfer 171.6 Mbps of data at 1.8 V. According to the FEM simulation results described in Section IIIB, the power consumption of the probe is expected to be within the safety limits (i.e. lower than 20 mW).

Fig. 9 shows the channel input-referred noise and transfer functions for different programmable gains and bandwidths (i.e. AP and LFP bands). They were measured with a spectrum analyzer from the channel analog output. Additionally, the gain, filter cutoff frequencies and the input-referred noise of all the channels (excluding the 7 channels connected to the internal reference electrodes) were measured in saline for the complete recording chain in a long-shank probe. For this, the data was collected through the digital SPI interface using the system described in Section V and analyzed in software with custom Matlab® scripts. The minimum gain setting of the AP band was measured by applying a sinusoidal signal of 1.8 kHz frequency to the saline solution. The calculated gain was 40.50 ± 0.33 (n = 269) and the histogram is shown in Fig. 10a. The high-pass cutoff frequencies of the AP (300-Hz setting) and LFP bands were measured by applying a square-wave voltage of 10 mV_{pp} amplitude and 0.2 Hz frequency to the saline solution. The high-pass corner frequency is then calculated from the decay time of the transient response. The high-pass filter corners were 313.0 ± 4.3 Hz and 0.32 ± 0.01 Hz (n = 269) for the AP and LFP bands, respectively. The histograms can be seen in Fig. 10b and Fig. 10c. It should be noted that the LFP high-pass filter is implemented with pseudo-resistors, thus it is very dependent on process and temperature variations. Nevertheless, this cutoff frequency shows low variation within a single device and remains below 1 Hz, which is important to avoid attenuation of the lower frequencies of interest in the LFP band. The input-referred noise of the complete recording chain, measured for all the electrode-channel combinations (n = 942) and using an external reference electrode, is 6.36 ± 0.80 and 10.32 ± 1.89 μV_{rms}, integrated in the AP (0.3-10 kHz) and LFP (0.5-1000 Hz) bands, respectively. This includes the electrochemical electrode noise as well. The AP-band noise histogram is shown in Fig.

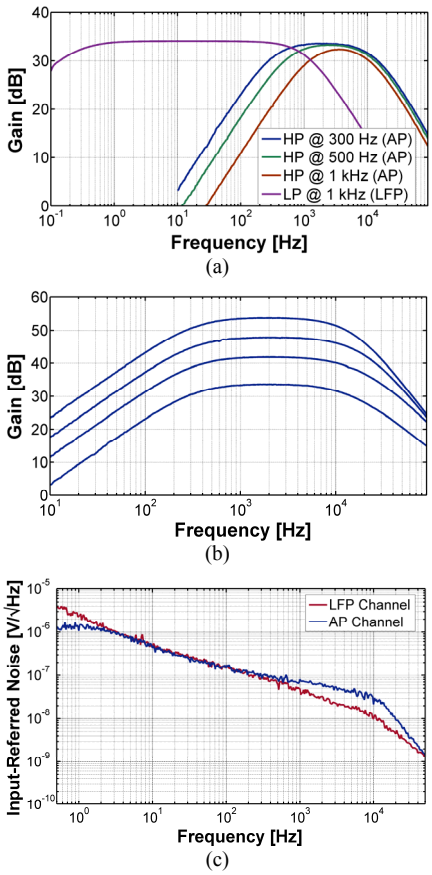


Fig. 9. Channel characteristics. (a) Measured closed-loop transfer function of one recording channel for different programmable bandwidths and (b) gains. (c) Input-referred noise for both the AP (0.3 kHz filter setting) and LFP frequency ranges.

10d. It can be seen that 94.8% of the pixel-channel combinations have an integrated noise below 7.5 μV_{rms}. All the histograms shown in Fig. 10 demonstrate a low channel-to-channel variability of the most important performance parameters.

The PSRR of the complete recording chain at 50 Hz, measured in saline with an external reference electrode, is measured to be >70 dB. The full-chain CMRR at 50 Hz is also measured in saline in two conditions: i) a worst-case configuration in which one pixel in the shank tip is recorded using an external reference electrode (i.e. the recording and reference pixels are very far from each other and the electrode impedances are not matched) and ii) a best-case configuration in which one pixel is recorded using an internal reference pixel next to it (i.e. the recording and reference pixels are closely located and the electrode impedances are matched). The worst-case CMRR in the first condition is measured as 40 dB, while the best-case CMRR in the second condition is measured as 48 dB. The measured CMRR of the recording channel alone is >60 dB, which shows that the full-chain CMRR is dominated by the mismatch of the pseudo-differential input stage and is highly dependent on the choice of the reference electrode. However, the worst-case CMRR achieved for the external-electrode configuration is comparable to the one achieved in passive probes under the same conditions (e.g. the CMRR of a passive

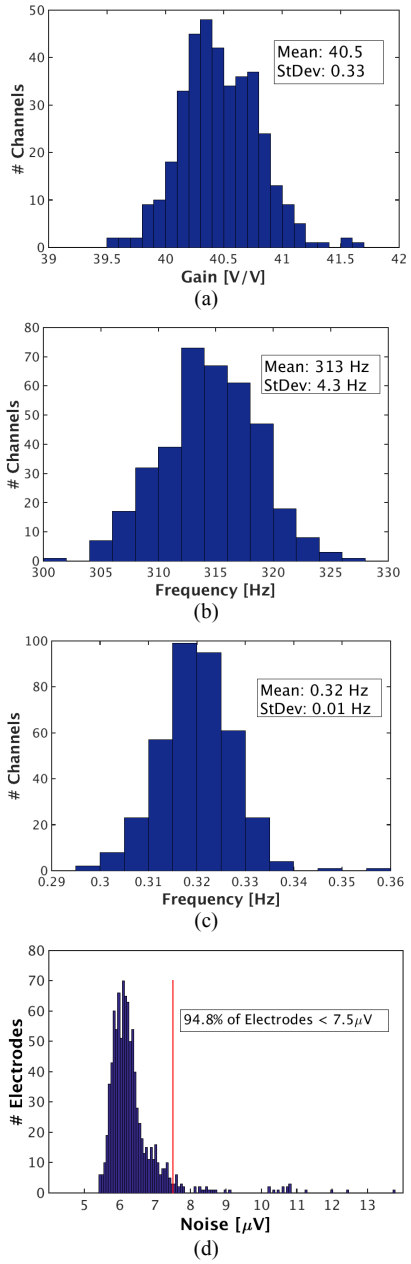


Fig. 10. Histograms of some of the measured performance parameters in one long-shank probe. (a) Minimum AP-band gain histogram (n = 269). (b) AP-band high-pass filter cutoff frequency histogram (n = 269). (c) LFP-band high-pass filter cutoff frequency histogram (n = 269). (d) AP-band integrated input-referred noise histogram (n = 942).

probe with 150-kΩ recording electrodes measured with a 13-MΩ input-impedance amplifier [27] using a 50-Ω external reference electrode can be calculated as ~39 dB, when only the input voltage divider caused by the two unmatched electrodes is taken into account). The signal distortion of the complete recording chain stays below 0.4% total harmonic distortion (THD) for input amplitudes below 10 mV in all the electrode-channel combinations of one device.

The signal-to-noise-and-distortion ratio (SNDR) of the 10-bit SAR ADC standalone is measured as 50.87 dB at a 1-kHz input frequency, corresponding to an effective number of bits (ENOB) of 8.16 b. The total dynamic power consumption of the ADC is 11.6 µW, when operating at 390 kS/s (i.e. sampling 13

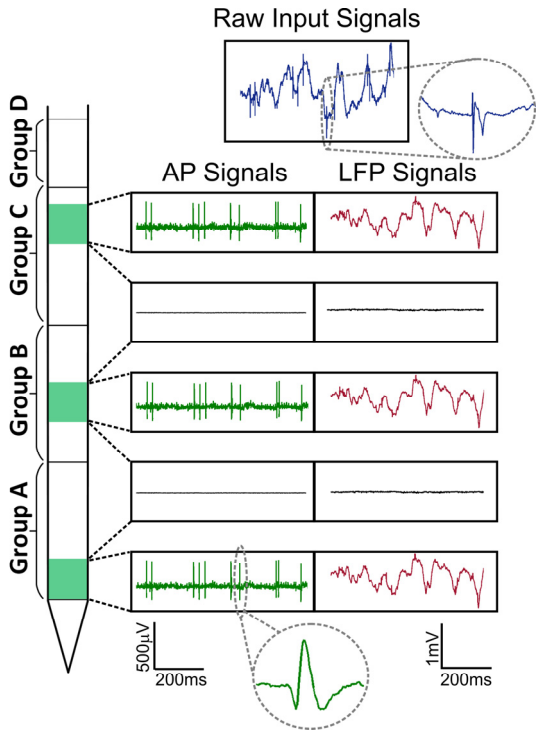


Fig. 11. Saline measurement results: recording from a set of pre-recorded neural data in saline. Three different sub-regions along the shank were selected. Successful separation of both AP and LFP signals is achieved. No crosstalk is observed in the unconnected channels.

channels at 30 kS/s). The figure of merit (FOM) is then calculated as 108.4 fJ/conversion-step. The maximum differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC, measured using conventional histogram testing, are -0.4/+0.4 LSB and -1.3/+0.9 LSB, respectively.

B. Saline Measurements

To further validate the functionality of the neural probe and complete system, we performed measurement in saline (PBS) by applying a set of pre-recorded neural data containing AP and LFP information. Measurements were done using a gain of 1000 for the AP band and a gain of 50 for the LFP band. The high-pass filter setting in the AP band was set to 300 Hz. In this experiment, the signals were applied to the saline solution through a National Instruments PXI 4461 dynamic signal analyzer and 3 distributed pixel subgroups were selected in the shank: pixels 1-80, 369-448 and 737-816. The rest of the pixels remained disconnected from the channels. The circuits were battery-powered and shielded with a Faraday cage during experiments. An external Ag/AgCl electrode was used as a reference for all the channels.

The output signals from the 384 parallel recording channels were acquired using the system described in Section V and stored in real time by a custom Labview software. Fig. 11 shows a 0.75-s extract of the recording, which demonstrates successful recording and separation of the AP and LFP signals at different shank depths. The signals are shown as input-referred, i.e. divided by the band gain. No signal was present in the unconnected channels, showing that the pixel-to-pixel and channel-to-channel crosstalk is minimum.

Extended *in vivo* characterization of these neural probes has been sucessfully performed with several devices, demonstrating their functionality and performance when being used in the target application. Some examples of datasets acquired during such *in vivo* experiments and their experimental descriptions are available on the Web [28], [29]. A complete analysis of the *in vivo* characterization will be reported in a separate publication.

CONCLUSIONS

In conclusion, we report on a CMOS neural probe, which integrates *in situ* buffering under each electrode and implements a high-density electrode array with reduced crosstalk, low noise, and small shank dimensions. The whole recording chain achieves an input-referred noise of 6.36 μV_{rms} in the AP band, a total power consumption of 49.06 µW/channel and a CSAC of 1.45 μm^2 for the long-shank probe. A very low channel-to-channel variability has been demonstrated for the most important performance parameters, and the probe functionality has been verified with successful saline recordings of pre-recorded neural data. The presented high-density probe will enable large-scale recording of neural activity, thus exceeding the capabilities of existing technologies.

ACKNOWLEDGEMENTS

The authors thank Kasra Garakoui for his help in ADC measurements.

REFERENCES

[1] G. Buzsáki *et al.*, “Tools for probing local circuits: High-density silicon probes combined with optogenetics,” *Neuron*, vol. 86, no. 1. pp. 92–105, 2015.

[2] T. J. Blanche, M. A. Spacek, J. F. Hetke, and N. V Swindale, “Polytrodes: high-density silicon electrode arrays for large-scale multiunit recording.,” *J Neurophysiol*, vol. 93, no. 5, pp. 2987–3000, May 2005.

[3] R. H. Olsson and K. D. Wise, “A three-dimensional neural recording microsystem with implantable data compression circuitry,” *Solid-State Circuits, IEEE J.*, vol. 40, no. 12, pp. 2796–2804, 2005.

[4] T. Torfs *et al.*, “Two-Dimensional Multi-Channel Neural Probes With Electronic Depth Control,” *Biomed. Circuits Syst. IEEE Trans.*, vol. 5, no. 5, pp. 403–412, 2011.

[5] J. Du, T. J. Blanche, R. R. Harrison, H. A. Lester, and S. C. Masmanidis, “Multiplexed, high density electrophysiology with nanofabricated neural probes.,” *PLoS One*, vol. 6, no. 10, p. e26204, 2011.

[6] K. Seidl, M. Schwaerzle, I. Ulbert, H. P. Neves, O. Paul, and P. Ruther, “CMOS-based high-density silicon microprobe arrays for electronic depth control in intracortical neural recording-characterization and application,” *J. Microelectromechanical Syst.*, vol. 21, no. 6, pp. 1426–1435, 2012.

[7] C. M. Lopez *et al.*, “An Implantable 455-Active-Electrode 52-Channel CMOS Neural Probe,” *Solid-State Circuits, IEEE J.*, vol. 49, no. 1, pp. 248–261, Jan. 2014.

[8] A. S. Herbawi *et al.*, “CMOS-based neural probe with enhanced electronic depth control,” *2015 Transducers - 2015 18th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*. pp. 1723–1726, 2015.

[9] J. Scholvin *et al.*, “Close-packed silicon microelectrodes for scalable spatially oversampled neural recording,” *IEEE Trans. Biomed. Eng.*, vol. 63, no. 1, pp. 120–130, 2016.

[10] B. C. Raducanu *et al.*, “Time multiplexed active neural probe with 678 parallel recording sites,” in *2016 46th European Solid-State Device Research Conference (ESSDERC)*, 2016, pp. 385–388.

[11] G. Buzsaki, “Large-scale recording of neuronal ensembles.,” *Nat Neurosci*, vol. 7, no. 5, pp. 446–451, May 2004.

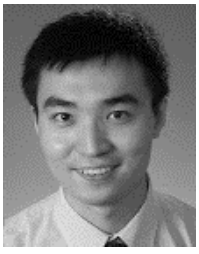
[12] B. L. McNaughton, J. O'Keefe, and C. A. Barnes, "The stereotrode: A new technique for simultaneous isolation of several single units in the central nervous system from multiple unit records," *J. Neurosci. Methods*, vol. 8, no. 4, pp. 391–397, 1983.
[13] C. Bédard, H. Kröger, and A. Destexhe, "Does the 1/f frequency scaling of brain signals reflect self-organized critical states?," *Phys. Rev. Lett.*, vol. 97, no. 11, 2006.
[14] B. Gosselin *et al.*, "A Mixed-Signal Multichip Neural Recording Interface With Bandwidth Reduction," vol. 3, no. 3, pp. 129–141, 2009.
[15] R. Muller, S. Gambini, and J. M. Rabaey, "A 0.013mm^2 5µW DC-coupled neural signal acquisition IC with 0.5V supply," *Solid-State Circuits, IEEE Journal of*, vol. 47, no. 1. pp. 232–243, 2012.
[16] W. Biederman *et al.*, "A Fully-Integrated, Miniaturized (0.125 mm^2) 10.5 µW Wireless Neural Sensor," *Solid-State Circuits, IEEE Journal of*, vol. 48, no. 4. pp. 960–970, 2013.
[17] H. Gao *et al.*, "HermesE: A 96-Channel Full Data Rate Direct Neural Interface in 0.13 µm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 47, no. 4. pp. 1043–1055, 2012.
[18] D. Han, Y. Zheng, R. Rajkumar, G. S. Dawe, and M. Je, "A 0.45 V 100-Channel Neural-Recording IC With Sub- µW/Channel Consumption in 0.18 µm CMOS.," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 6, pp. 735–46, 2013.
[19] W. Biederman *et al.*, "A 4.78 mm^2 Fully-Integrated Neuromodulation SoC Combining 64 Acquisition Channels with Digital Compression and Simultaneous Dual Stimulation," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 1038–1047, 2015.
[20] M. Yin, D. A. Borton, J. Aceros, W. R. Patterson, and A. V. Nurmikko, "A 100-channel hermetically sealed implantable device for chronic wireless neurosensing applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 2, pp. 115–128, 2013.
[21] C. M. Lopez *et al.*, "A 966-electrode neural probe with 384 configurable channels in 0.13µm SOI CMOS," in *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, 2016, vol. 59, pp. 392–393.
[22] S. Kim, P. Tathireddy, R. A. Normann, and F. Solzbacher, "Thermal impact of an active 3-D microelectrode array implanted in the brain.," *IEEE Trans Neural Syst Rehabil Eng*, vol. 15, no. 4, pp. 493–501, Dec. 2007.
[23] R. Hogervorst, J. P. Tero, and J. H. Huijsing, "A Compact Power-Efficient 3 V CMOS Rail-to-Rail Input/Output Operational Amplifier for VLSI Cell Libraries," *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1505–1513, 1994.
[24] J. Craninckx and G. Van Der Plas, "A 65fJ/conversion-step 0-to-50MS/s 0-to-0.7mW 9b charge-sharing SAR ADC in 90nm digital CMOS," in *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, 2007.
[25] A. Andrei, M. Welkenhuysen, B. Nuttin, and W. Eberle, "A response surface model predicting the in vivo insertion behavior of micromachined neural implants.," *J. Neural Eng.*, vol. 9, no. 1, p. 16005, 2011.
[26] M. Schaldach and A. Bolz, "Longterm Stability of TiN," in *Bioceramics and the Human Body*, A. Ravaglioli and A. Krajewski, Eds. Dordrecht: Springer Netherlands, 1992, pp. 326–333.
[27] Intan Technologies LLC, "RHD2000 Series Digital Electrophysiology Interface Chips." Datasheet, Intan Technologies LLC, 2013.
[28] Nick Steinmetz, "Dataset: recording with a Neuropixels Phase3 electrode array," *CortexLab at UCL*. [Online]. Available: http://data.cortexlab.net/singlePhase3/. [Accessed: 11-Nov-2016].
[29] N. Steinmetz, "Dataset: simultaneous recording with two Neuropixels Phase3 electrode arrays," *CortexLab at UCL*. [Online]. Available: http://data.cortexlab.net/dualPhase3/. [Accessed: 11-Nov-2016].

Carolina Mora Lopez received her Ph.D. degree in Electrical Engineering in 2012 from the KU Leuven, Belgium, in collaboration with imec, Belgium. She is currently working at imec as a researcher in the Biomedical Circuits team, designing and testing microelectronic interfaces for neural-sensing applications. Her research interests include analog and mixed-signal circuit design for sensor, bioelectronics and neural interfaces.

Jan Putzeys started his career at imec in 2000 as a characterization engineer on cryogenic CMOS readout circuits for space applications. He has been developing dedicated test setups for low noise, low power readout electronics, cryogenic circuits and pulsed I-V measurements. He has designed readout systems for CCD and CMOS imagers, mainly for medical applications. Currently he's mainly involved in system design for neural readout ICs, with a focus on low power consumption and miniaturization.

Bogdan C. Raducanu was born in Romania in 1987. He has received his B.E. in Electronics and Telecommunications and M.E. in Bioinformatics and Complex Systems from the Politehnica University of Bucharest (PUB), Bucharest, Romania, in 2010 and 2012, respectively. He has been with Infineon Technologies in 2009-2012 and is currently pursuing his Ph.D. in biomedical circuits with imec and KU Leuven.

Marco Ballini received his Ph.D. degree in electrical engineering from ETH Zurich, Switzerland, in 2013. The focus of his Ph.D. work was on the design of CMOS-based microelectrode arrays. He is currently working at imec, Leuven, Belgium, as Analog IC Designer in the Biomedical Circuits team. His research interests include low-power analog and mixed-signal circuits for sensors, bioelectronics and neural interfaces.



Shiwei Wang (M'13) received the B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2010, and the Ph.D degree from the University of Edinburgh, Edinburgh, U.K., in 2014.

Following the Ph.D, he has been with Chinese Academy of Sciences, Shenzhen, China, working on ASIC designs for cochlea/retinal implants. In 2015 he joined the Biomedical Circuits team at imec, Leuven, Belgium, where he is currently working on ASIC designs for neural interfaces and other biomedical applications.

Alexandru Andrei received his Ph.D. on semiconductor microsystems from INSA Lyon in 2005. After working two years on piezoelectric MEMS at FEMTO-ST in Besancon, he joined the Life Science Technologies team of imec, Belgium, in 2008. Ever since he worked on the design and manufacture of implantable microsystems. His research activity focuses into translating new device concepts into Si prototypes by creating an executable and manufacturable process flow based on a combination of innovative steps as well as existing process technologies.

Véronique Rochus (born 1978) received her M.S. degree in Physics Engineering from University of Liège in 2001 and a D.E.A. on "Nanostructures et Microsystèmes pour l'électronique et les communications" at the University of Paris-Sud in 2002. She received her Ph.D. in Applied Science from University of Liège in 2006 and then worked on MEMS modelling as postdoctoral researcher financed by Belgian National Fund for Scientific Research until 2010. During that period she performed postdoc stays at TU Delft as well as at Kyoto University. Afterwards she joined the imec in 2010 where she is now senior Microsystems Design Engineer and where he actively contributes to the research in the field of Microsystem design and modeling.

Roeland Vandebriel received his bachelor degree in Electronical Engineering in 1999 from the KHLIM in Diepenbeek, Belgium. He started his carrier at Xircom as hardware design engineer. Since 2001 he joint imec and build up a very broad experience in multiple disciplines. He was involved in several projects related to: building the Picard platform for rapid prototyping systems, digital signal processing for wireless systems, digital data processing, controllers for imager sensors and digital enabling systems for analog R&D.

Simone Severi received the M.S. degree in microelectronic engineering from the University of Bologna, Italy, in 2001 and the Ph.D. degree from the KU Leuven in 2006. During his Ph.D he worked on ultimate device scaling, innovative channel engineering and processing for future CMOS devices technologies. Since 2007, he joined imec Leuven working on Microsystems for mass data storage devices, on poly-SiGe surface micromachining technology and CMOS integrated biosensors. Since 2009 he became team leader of the specialty component group at imec, with specific focus on MEMS and Bio-Photonics sensors.

Chris Van Hoof received the Ph.D. degree in electrical engineering from the University of Leuven, Belgium, in 1992. He is Director of Wearable Healthcare at imec and is also imec Fellow. He has a track record of over 20 years of initiating, executing, and leading national and international contract R&D at imec. His work resulted in three startups (two in the healthcare domain) and he has delivered sensor flight hardware to two cornerstone European Space Agency missions. After receiving his Ph.D. from the University of Leuven in 1992 in collaboration with imec, he has held positions at imec as manager and director in diverse technical fields (sensors and imagers, MEMS and autonomous microsystems, wireless sensors, and body-area networks, wearable health). He has published over 600 papers in journals and conference proceedings and given over 60 invited talks. He is also full professor at the University of Leuven (KU Leuven).

Silke Musa received her MS degree in Applied Natural Science from the University of Freiberg, Germany, in 2006 and her Ph.D. in Physics from the University in Leuven, Belgium, in 2011. From 2012 to 2013 she was Team Leader of In Vivo Technologies at imec, and in 2013 she became Project Leader at imec. Since April 2016 she is Program Manager of the Smart Neuroprostheses/Neurotransducer Program at imec. She is author of 16 articles and three inventions. Her research interests include implantable devices, biosensors, microfabrication, electrode materials for recording & stimulation of cells, electrochemistry, and embedded systems.

Nick Van Helleputte received the MS degree in electrical engineering in 2004 from the KU Leuven, Belgium. He received his Ph.D. degree from the same institute in 2009 (MICAS research group). His Ph.D. research focused on low-power ultra-wide-band analog front-end receivers for ranging applications. He joined imec in 2009 as an Analog R&D Design Engineer. He is currently team leader of the biomedical circuits and systems team. His research focus is on ultra-low-power circuits for biomedical applications. He has been involved in analog and mixed-signal ASIC design for wearable and implantable healthcare applications. Nick is an IEEE member and served on the technical program committee of VLSI circuits symposium.

Refet Firat Yazicioglu has received the Ph.D. degree in Electronics Engineering from KU Leuven in 2008 in collaboration with imec, Belgium. He worked at imec, Belgium as R&D Team Leader and Principal Scientist, where he was leading the "Biomedical Integrated Circuits" team focusing on Analog and Mixed Signal Integrated Circuit design for wearable and

implantable biomedical applications. He is now working at GSK as head of Neuromodulation Devices.

During his career, Dr. Yazicioglu has (co)authored over 70 publications, 3 book chapters, and a book on ultra-low-power circuit and system design for biomedical applications, and authored several patents in this field. He has developed several generations of integrated circuits for wearable and implantable healthcare applications.

Srinjoy Mitra received his bachelor degree from Calcutta, India, and the M.Tech. degree from the Indian Institute of Technology, Bombay, India, in 2003. After briefly working in microelectronic industry, he completed his Ph.D. from the Institute of Neuroinformatics (UNI), ETH Zurich, Switzerland, in 2008. Between 2008 and 2010 he worked as a Postdoctoral Researcher at Johns Hopkins University, Baltimore, MD, USA. He then joined the medical electronics team at imec, Belgium, and worked there as a Senior Scientist until early 2016. At imec he had taken up lead roles in various industrial and public funded projects primarily related to biopotential recording. For the last few years Dr. Mitra led multiple projects on neural implants for central and peripheral nervous system. He has recently joined the University of Glasgow, Glasgow, U.K., as a Lecturer in the Biomedical Engineering Division. His primary research interest is in designing novel mixed signal CMOS circuits for advancement in medical and neural electronics.